LINEAR OPTOCOUPLER TAKES ON 7500 V

AN EARLY LOOK AT THE ISSCC

FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE

ELECTRONIC DESIGN

A PENTON PUBLICATION U.S. $5.00

JANUARY 10, 1991

TECHNOLOGY FORECAST:

TOMORROW'S RENAISSANCE DESIGN TEAM

•NEW SECTION: DESIGNING FOR PC SYSTEMS

QUICKLOOK PAGE 149

Knock-your-socks-off PLD software on a shoestring budget.

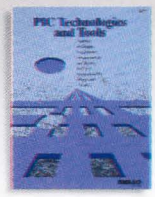
Who says you can't afford the world's best PLD development tools? Data I/O®'s industry-standard design software and programming solutions are more powerful—and more affordable—than ever before. So now the best tools on the market are also the best value.

NEW ABEL™-4 marks a major milestone in PLD software. The leader in device support, ABEL-4 automatically identifies which PLDs match your design needs with new SmartPart™ intelligent device selection. New optional device fitters automatically assign pins and configure macrocells for complex device architectures. And an all-new user interface speeds the entire PLD design process.

A major new version of the leading schematic capture software, **NEW FutureNet®-5**, redefines "ease-of-use" with pop-up menus, extensive dialog boxes and a fast symbol browsing feature.

To make designing for testability practical, choose **NEW PLDgrade.™** This inexpensive fault grading software helps you optimize your design for testability before production.

And the affordable **NEW 2900 Programming System** brings the cost of high-performance programming down to earth. Its innovative technology makes programming any PLD—even surface-mount devices—fast and easy.



CALL TODAY for your FREE tutorial on designing with PLDs—a $12.95 value.

1-800-247-5700

The Personal Silicon Experts

DATA I/O Corporation

Data I/O Corporation 10525 Willows Road N.E., P.O. Box 97046, Redmond, WA 98073-9746, U.S.A. (206) 881-6444/1-800-247-5700
Data I/O Canada 6725 Airport Road, Suite 302, Mississauga, Ontario L4V 1V2 (416) 678-0761
Data I/O Europe World Trade Center, Strawinskylaan 633, 1077 XX Amsterdam, The Netherlands + 31 (0)20-6622866/Telex 16616 DATIO NL
Data I/O Instrumatic Electronic Systems Vertriebs GmbH Lochhamer Schlag 5A, 8032 Graefelfing, W. Germany, + 49 (0)89-858580
Data I/O Japan Sumitomoseimei Higashishinbashi Bldg., 8F, 2-1-7, Higashi-Shinbashi, Minato-Ku, Tokyo 105, Japan
(03) 432-6991/Telex 2522685 DATAIO J

Finally, FDDI worthy of the name.

It's one thing to set the standard for an entire industry, as HP helped to do with FDDI. But it's quite another to follow it up with products that set the standard for performance and quality. Of course, that's just the HP way.

Case in point, our new integrated FDDI transceiver with integral MIC receptacle makes the most of its HP heritage. Engineered to meet and beat FDDI standards, this single-piece solution provides consistent performance over a wide range of operating temperatures and voltages. The bottom line is a 14.5dB power budget that exceeds the 11dB FDDI PMD standard, resulting in a comfortable 3.5dB design margin.

Attributes that stem directly from HP's role as a vertically integrated supplier. Which means we have direct control over all the active elements of our FDDI designs, ensuring you a consistently high quality product – and a constant high volume supply.

What's more, our new FDDI transceiver is just one part of a growing family of 1300nm products. Like our individual transmitter/receiver pair – for FDDI and general-purpose applications – that offer data speeds up to 200MBd. With more new and innovative products on the way.

So, if you're in the process of building a name in fiber optic networks, remember this – there's only one supplier of FDDI products worthy of the HP name. For more information, call HP today at **1-800-752-0900, ext. 1960**. We'll make it worthy of your time.

There is a better way.

HEWLETT PACKARD

CG08001

CIRCLE 100

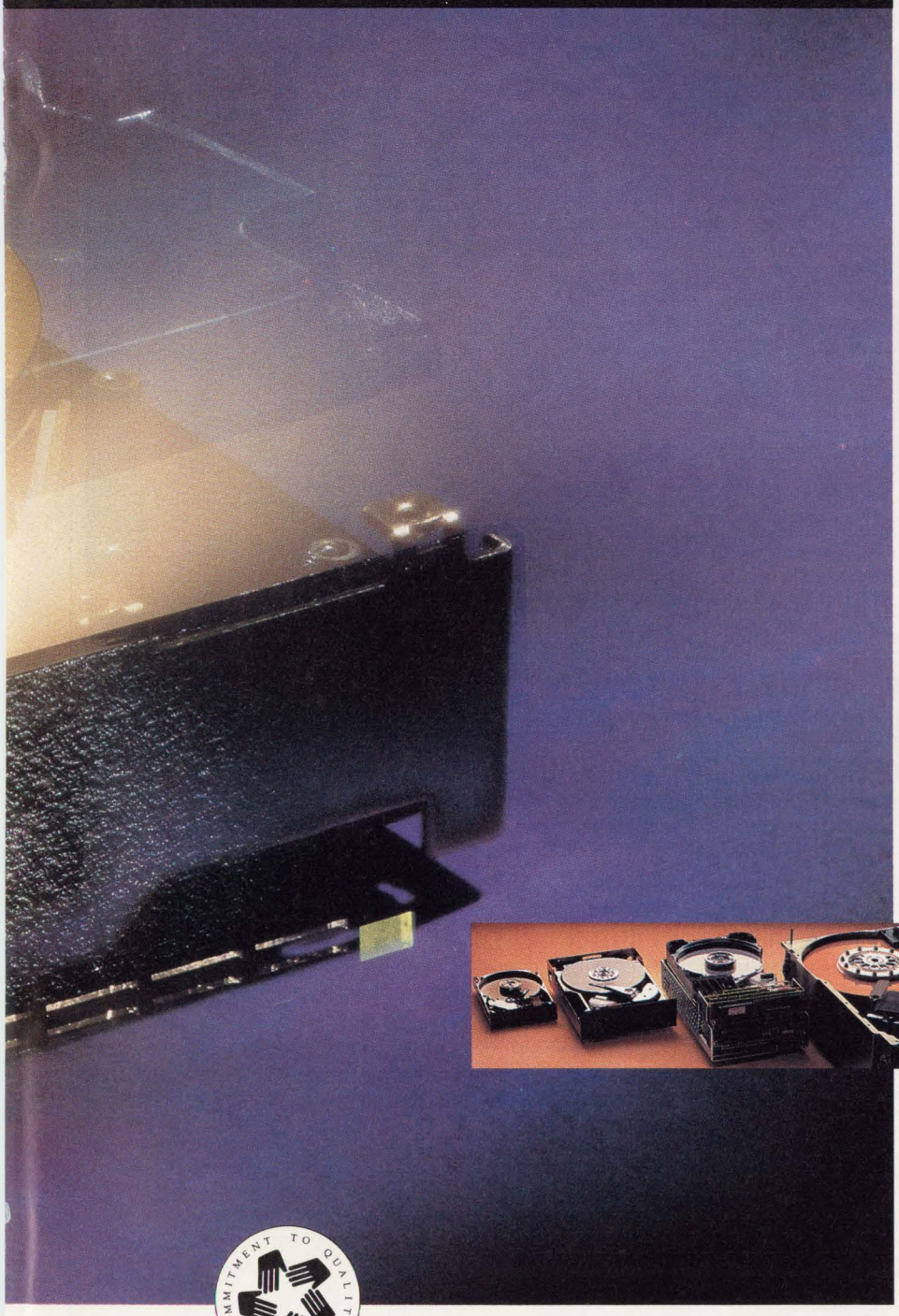
Outside, all disc drives look t
It's really what's inside that co

he same. unts.

Apart from our nameplate, a Seagate disc drive looks much like any other when viewed from the outside. But it's the tangible and intangible elements we put inside that make a Seagate drive really shine.

If you could see inside you'd find the best components available. Many of them—such as discs, motors, semiconductors and thin-film heads—we design and build ourselves, allowing us to control their quality, cost and availability. Most of what we don't manufacture is obtained from a select group of vendors who must meet our strict Supplier Certification Program criteria. This guarantees consistently high quality and continual conformance to our customers' requirements.

H N O L O G Y



Technology is another key Seagate ingredient. As the holder of over 200 disc drive patents, we constantly develop state-of-the-art technologies to enhance the value of our products to our customers. For example, Zone Bit Recording™ increases the amount of information that can be stored on a disc. But besides increasing the drive's capacity and throughput, ZBR™ technology can reduce the required number of heads and discs, thereby reducing costs, increasing performance and making the drive significantly more reliable.

The third major factor that sets Seagate drives apart is our commitment. You see it in the inspired dedication of our employees: like our engineers, who apply the latest technology advances to our current models. In our assemblers and technicians, who are committed to producing defect-free products. And in our sales, customer service and technical support groups, who continually go the extra mile to ensure complete customer satisfaction.

But most of all, Seagate drives are built upon experience: the market insight and technical knowhow that can only come from selling more than 25 million drives since the industry's inception. It's the kind of experience you won't find at any other disc drive company.

To be sure you're getting Seagate quality and technology inside where it counts, make sure there's a Seagate nameplate on the outside. For more information, contact Seagate at 800-468-DISC, or 408-438-6550.

A COMMITMENT TO QUALITY Seagate

Seagate

The first name in disc drives

CIRCLE 211

JANUARY 10, 1991 VOL. 39, NO. 1

ELECTRONIC DESIGN

COMING NEXT ISSUE
- First details on a new method of analog-signal storage
- PIPS—A special section on power, interconnections, passive components, and switches and relays; includes a design article, manufacturer listings, and latest products
- A user's guide to power-conversion modules
- What's new in computer boards at Buscon West
- Protecting expensive hybrid power op amps
- New filtering scheme cuts switcher's noise to linear supply levels
- Plus regular features:
Pease Porridge
Ideas for Design
Technology Advances

Certificate of Merit
Winner, 1988
Jesse H. Neal Editorial
Achievement Awards

Cover: Joe Drivas

ELECTRONIC DESIGN (USPS 172-080; ISSN 0013-4872) is published semi monthly by Penton Publishing Inc., 1100 Superior Ave., Cleveland, OH 44114-2543. Paid rates for a one year subscription are as follows: $75 U.S., $140 Canada, $230 International. Second-class postage paid at Cleveland, OH, and additional mailing offices. Editorial and advertising addresses: ELECTRONIC DESIGN, 611 Route #46 West, Hasbrouck Heights, NJ 07604. Telephone (201) 393-6060. Facsimile (201) 393-0204.

For subscriber change of address and subscription inquiries, call (216) 696-7000.

POSTMASTER: Please send change of address to ELECTRONIC DESIGN, Penton Publishing Inc., 1100 Superior Ave., Cleveland, OH 44114-2543.

IN 1990, WE'RE FINA JOE, BOB, BEN AND FRAN

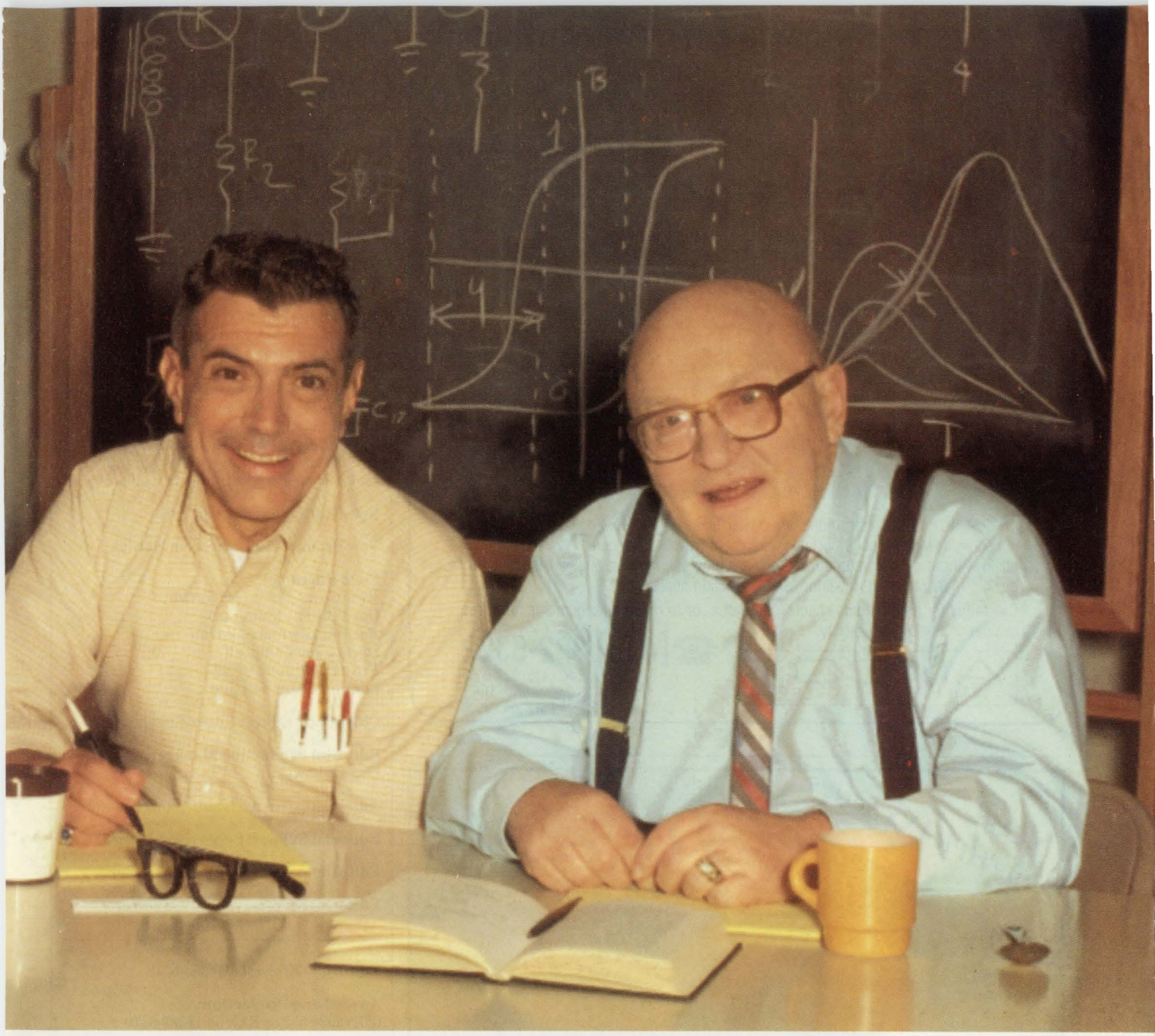
Nowadays it's called "Concurrent Engineering". Back then it was simply the way the job got done. A small group of people in constant communication. From flowchart changes to thermal problems. From concept to manufacturing.

Did it work? You bet. It gave us things we now use every day. Like television. Radio. And computers.

But time passed, the technology got more complex, and the people became departments. "Over the wall" engineering carried the day. Unfortunately, a lot was lost in the process. Projects began to control people, instead of people controlling projects.

Now there's a way to regain the human dimension that makes concurrent engineering such a powerful competitive weapon. It's called the Concurrent Design Environment.™

No matter how many engineers, no matter how complex the technology, no matter how many design disciplines involved, the Concurrent



LLY BACK TO WHAT K WERE DOING IN 1963.

Design Environment binds your engineering force into a highly interactive team. Its Falcon Framework™ combines state of the art design tools with unprecedented engineering management capacity. For virtually all electronics technologies and engineering disciplines. With tools from any source, including third party and in-house.

So let us show you how to turn back the clock by moving your engineering forward. For a free videotape about the Concurrent Design Environment, call **1-800-547-7390.**

Mentor Graphics®

Changing The Way The World Designs. Together.

Editor-in-Chief: Stephen E. Scrupski

Executive Editor: Roger Allan

Managing Editor: Bob Milne

Senior Editors: Frank Goodenough, Milt Leonard, John Novellino

Technology Editors:
Analog & Power: Frank Goodenough
Communications & Industrial: Milt Leonard (San Jose)
Components & Packaging: David Maliniak
Computer-Aided Engineering: Lisa Maliniak
Computer Systems: Richard Nass
Semiconductors: Dave Bursky (San Jose)
Test & Measurement: John Novellino

News Editor: Sherrie Van Tyle

New Products Editor: Susan Nordyk

Field Bureaus:
West Coast Executive Editor: Dave Bursky (San Jose)
Boston: Lawrence Curran
Dallas: Jon Campbell
Frankfurt: John Gosch
London: Peter Fletcher

Chief Copy Editor: Roger Engelke, Jr.

Editorial Production Manager: Lisa Iarkowski

Administrative Assistant: Janis Kunkel

Editorial Support Supervisor: Mary James

Editorial Assistant: Ann Kunzweiler

Editorial Secretary: Bradie Guerrero

Editorial Offices: (201) 393-6272

Advertising Production: (201) 393-6093 or FAX (201) 393-0410

Production Manager: Michael McCabe
Production Assistants: Donna Marie Bright, Doris Carter, Eileen Slavinsky

Circulation Manager: Robert Clark

Promotion Manager: Clifford Meth

Reprints: Helen Ryan (201) 423-3600

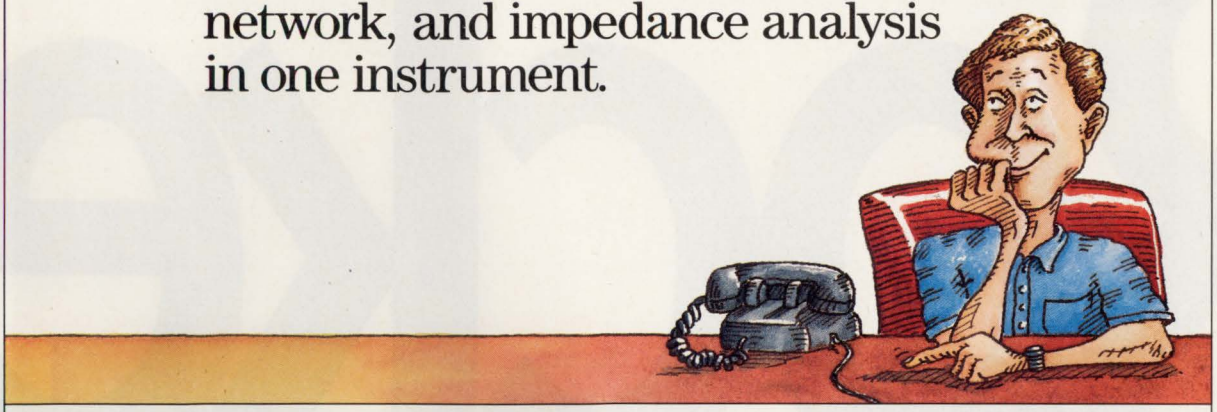
Group Art Director: Peter K. Jeziorski

Computer Systems Administrator: Anne Gilio Turtoro

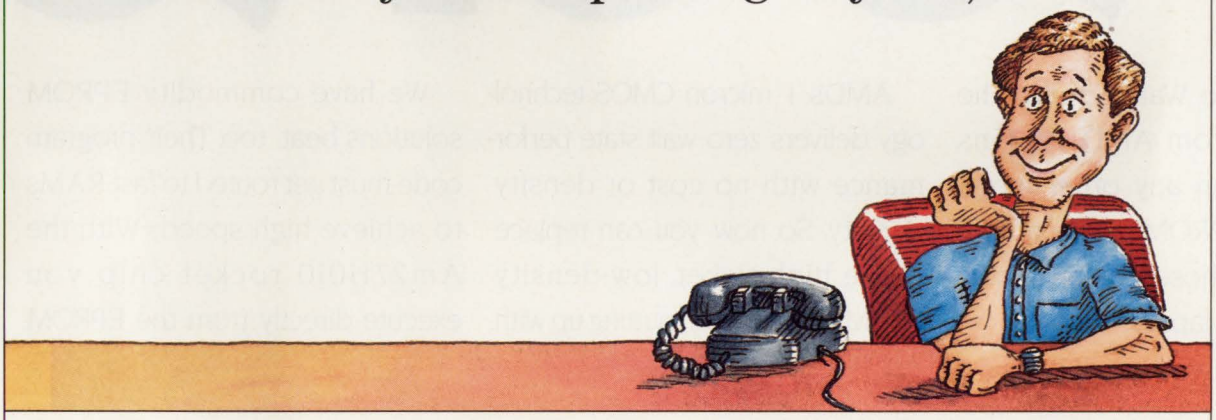
Published by Penton Publishing
Vice President-Editorial: Perry Pascarella
Group Editorial Director: Leland Teschler

Publisher: Paul C. Mazzacano

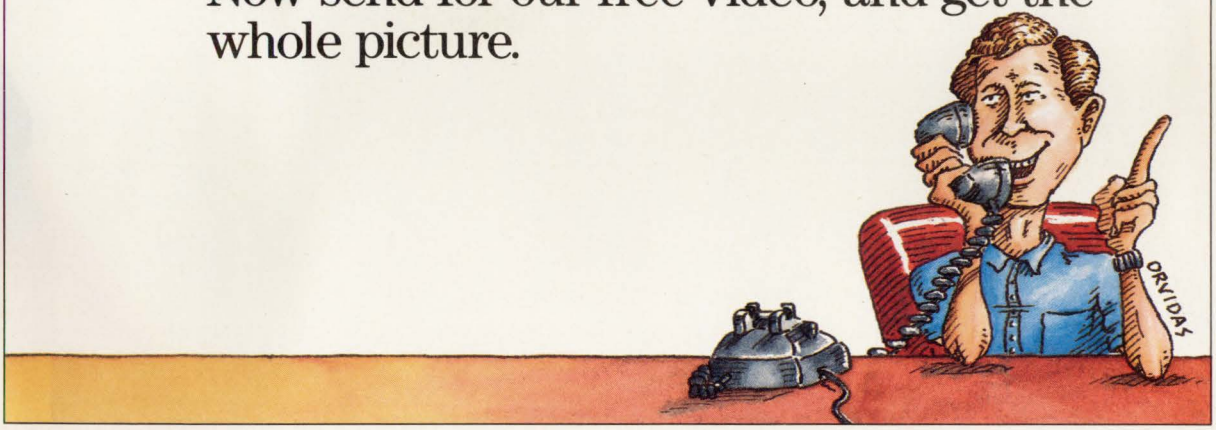
Picture yourself with 500 MHz spectrum, network, and impedance analysis in one instrument.



Picture yourself spending only $25,000.*



Now send for our free video, and get the whole picture.



If your audio, baseband, HF, VHF, and IF designs require spectrum, vector network or impedance analysis, watch this.

Our HP 4195A 500 MHz Network/Spectrum analyzer video shows you how to get the measurement capability you need along with the convenience and flexibility that you want. All in one instrument, for $25,000.*

You'll see how the HP 4195A handles a wide range of applications with balanced specs. Like spectrum analysis performance of −135 dBm sensitivity, 3 Hz to 300 kHz RBW. And > 100 dB vector network analysis dynamic range with ±0.05 dB/±0.3 degree accuracy.

So get the picture. Call **1-800-752-0900**. Ask for **Ext. 1148** and receive your free video. It's a picture you'll want to be a part of.

*U.S. list base price.

There is a better way.

HEWLETT PACKARD

CIRCLE 164

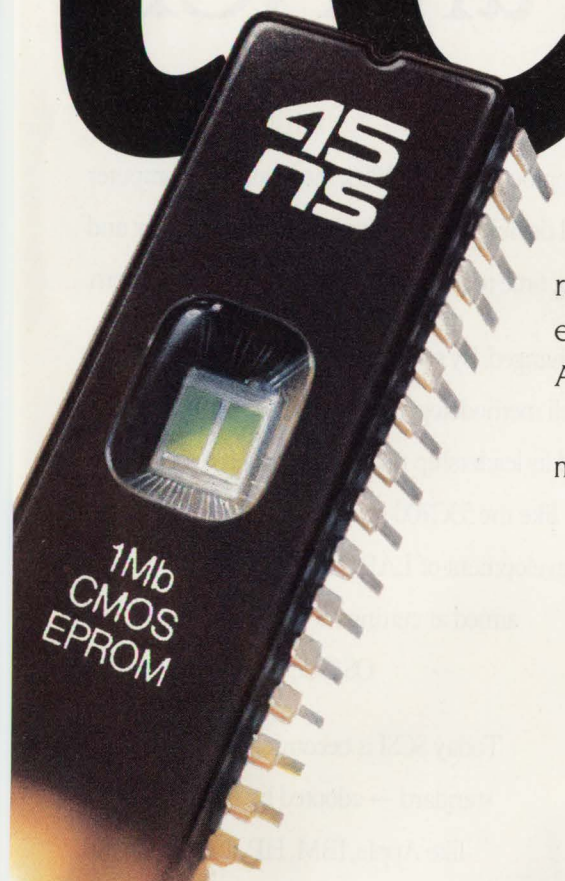
Rocke

Welcome to Warp Speed: The Am27H010 from AMD. At 45ns, it's faster than any other megabit CMOS EPROM. Fast enough to eliminate those irritating short term memory lapses.

AMD's 1 micron CMOS technology delivers zero wait state performance with no cost or density penalty. So now you can replace those high-ticket, low-density PROMs you've been putting up with.

We have commodity EPROM solutions beat, too. Their program code must get routed to fast RAMs to achieve high speed. With the Am27H010 rocket chip you execute directly from the EPROM.

t.chip.



And no one can give you the range of densities—and the fastest part at every density—like AMD can.

Fact is, we make and sell more megabit EPROMs than anyone.

The Am27H010 is ready in volume and priced right.

So call 800-222-9323 and get the parts worth not waiting for.

Advanced Micro Devices

901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088

CIRCLE 81

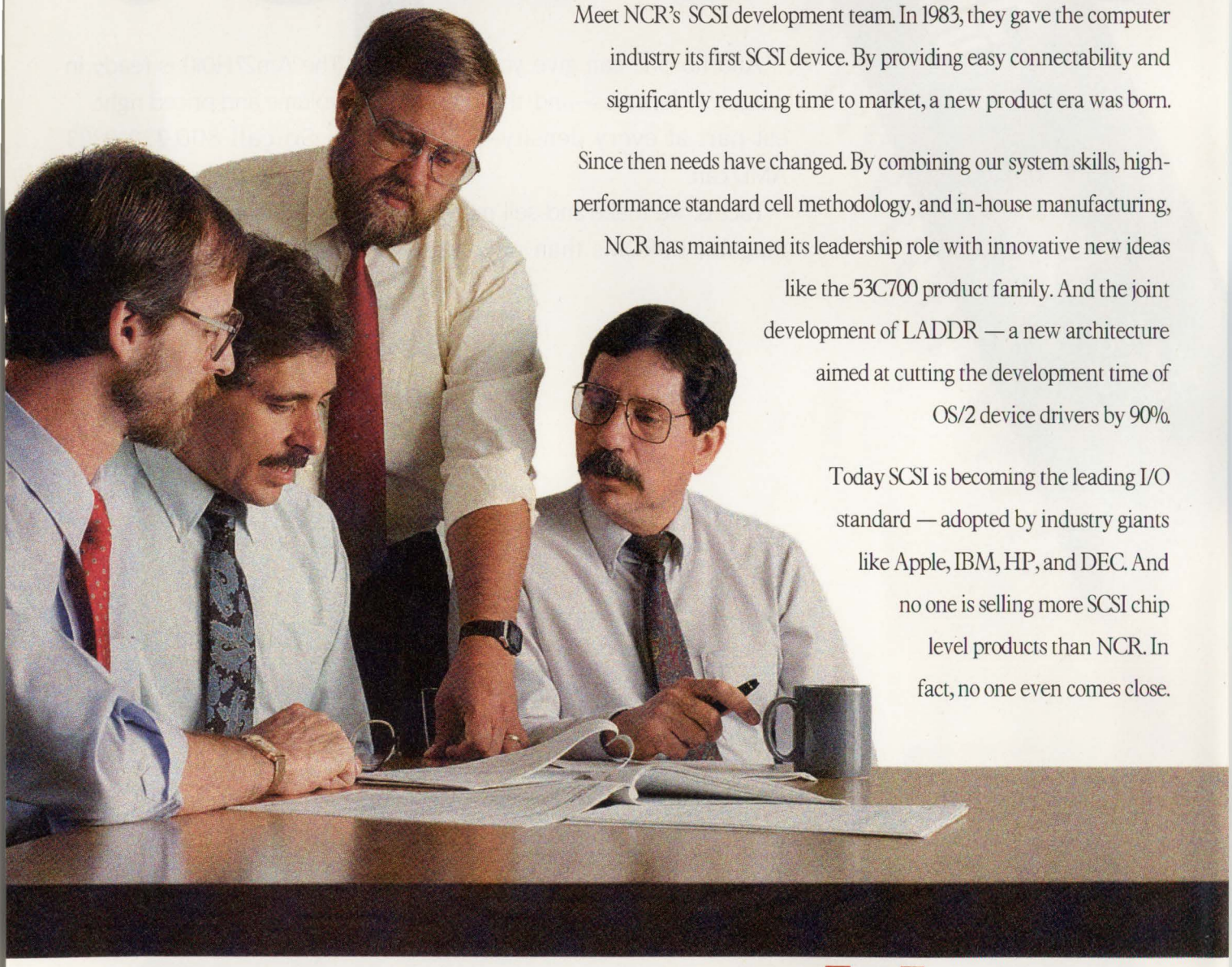
Here's one reason that over half of all SCSI devices sold are NCR.

We created the market... and we still lead the way.

Meet NCR's SCSI development team. In 1983, they gave the computer industry its first SCSI device. By providing easy connectability and significantly reducing time to market, a new product era was born.

Since then needs have changed. By combining our system skills, high-performance standard cell methodology, and in-house manufacturing, NCR has maintained its leadership role with innovative new ideas like the 53C700 product family. And the joint development of LADDR — a new architecture aimed at cutting the development time of OS/2 device drivers by 90%.

Today SCSI is becoming the leading I/O standard — adopted by industry giants like Apple, IBM, HP, and DEC. And no one is selling more SCSI chip level products than NCR. In fact, no one even comes close.



Part of the NCR SCSI Development Team: (left to right) **Jerry Armstrong**, Sr.Software Engineer; **Harry Mason**, Strategic Marketing Manager; **John Lohmeyer**, NCR Sr. Consulting Engineer and Chairman of the ANSI X3T9.2 Committee and **Dave Skinner**, SCSI ProductManager.

North American Sales Headquarters
1731 Technology Drive, Suite 600
San Jose, CA 95110
(408) 453-0303

Here's another.

The NCR 53C700 SCSI I/O Processor… So good, *Electronic Design* named it the product of the year.

"You can't tell a good SCSI chip just by looking at it…" and according to Electronic Design, NCR's 53C700 is the best there is.

The only third generation SCSI device on the market today, it concentrates all the functions of an intelligent SCSI adapter board on a single, smart and extremely fast, chip… for about 15% of the cost.

As the first SCSI I/O processor on a chip, the 53C700 allows your CPU to work at maximum speed while initiating I/O operations up to thousands of times faster than any non-intelligent host adapter. DMA controllers can burst data at speeds of up to 50 Mbytes/s. This new chip cuts down system time hookup to a fraction of what it has been.

Those are just a few of the reasons Electronic Design's "Best of the Digital IC's" award went to NCR's 53C700 last year.

And now the NCR 53C710!

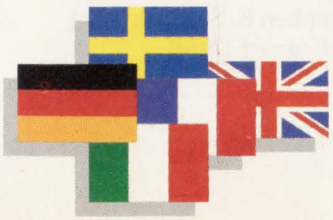
For the complete story on the NCR SCSI product line featuring the new 53C710, as well as the upcoming SCSI seminars with the NCR SCSI Development Team, please call:

1-800-334-5454

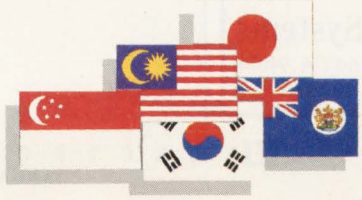
NCR

Creating value

CIRCLE 179



European Sales Headquarters
Gustav-Heinemann-Ring 133
8000 Munchen 83
West Germany
49 89 632202



Asia/Pacific Sales Headquarters
2501, Vicwood Plaza
199 Des Voeux Road
Central
Hong Kong
825 859 6044

FORECASTING TECHNOLOGY TRENDS

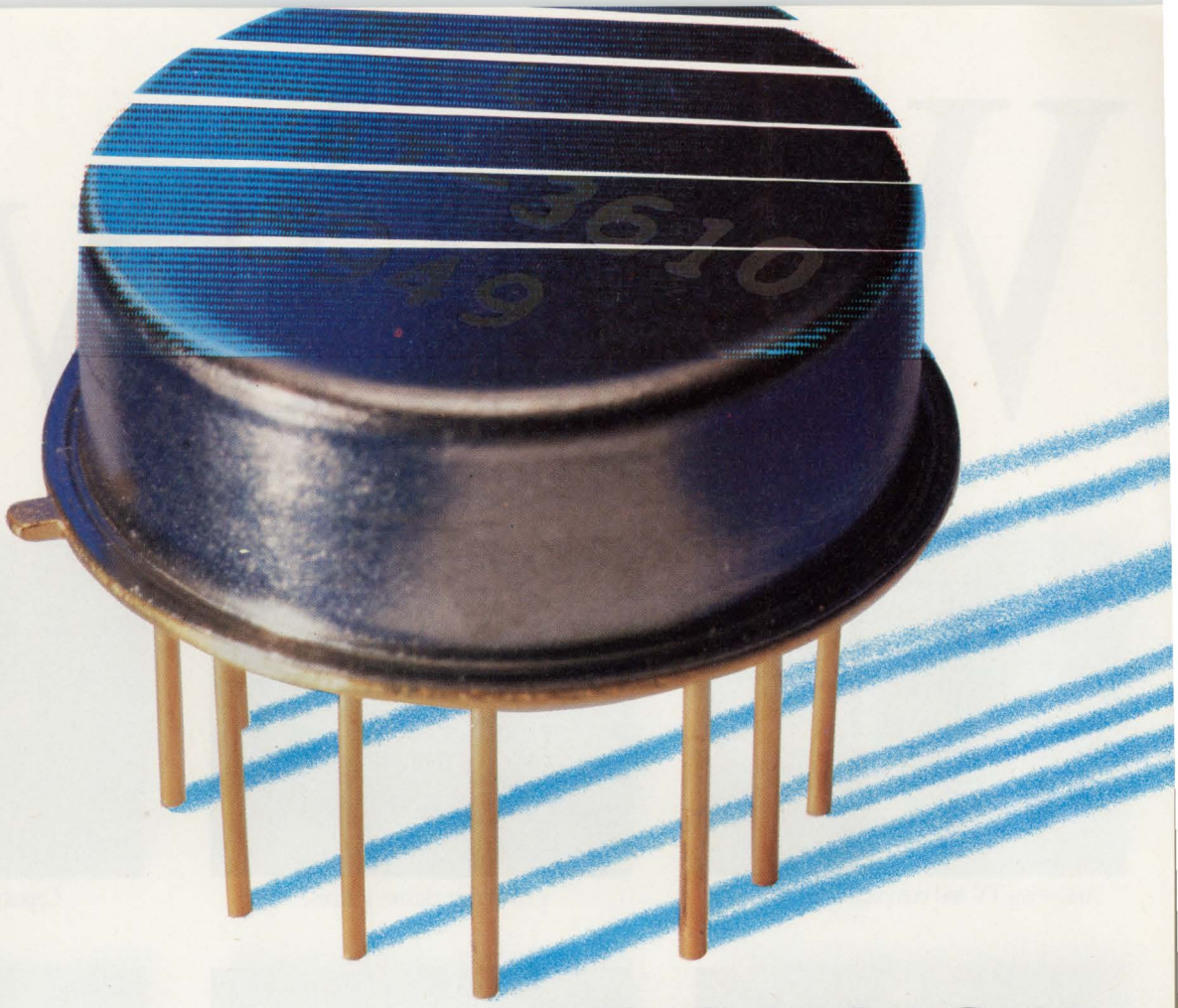
For the past several years, Electronic Design has published its forecast of technology developments in the year's first issue. For 1990, we focused on how computer-aided engineering and application-specific integrated circuits will impact the way designers go about their jobs. In our 1991 Technology Forecast (p. 41), we focus on the emerging "renaissance" design team—a multidisciplinary team with a broad mix of expertise. Such teams will be anchored by concurrent-engineering techniques, and include specialists in designing for testability, for manufacturability, for reliability, and so on.

Many unstoppable forces are shaping today's electronics marketplace—the need for quality, the growing complexity of devices, and the intensified time-to-market pressures, to name a few. When these forces combine with improvements in the raw computing power of workstations, local-network bandwidth and connectability, and more powerful arrays of CAE design tools, concurrent engineering emerges as the accepted method for future product design and development.

The 1991 Technology Forecast is a multi-part package. It begins with two staff-written articles that discuss the need for and growth of concurrent engineering and design for testability. Four contributed technical articles follow: design environments needed to support concurrent engineering; the potential of computer-aided software engineering; coming to grips with time-to-market pressures; and designing for reliability. The report package concludes with a series of seven one-page pieces on future developments in: programmable logic devices, semiconductor test equipment, real-time software, high-density interconnects, packages for complex semiconductor devices, passive components, and power sources.

Finally, the editors of Electronic Design wish all our readers a healthy and prosperous New Year.

Stephen E. Scrupski
Editor-in-Chief



PRECISION TTL-CONTROLLED ATTENUATORS

up to 35dB
10 to 1000MHz
only **$5995**

Now...precision TTL-controlled attenuators accurate over 10 to 1000MHz and −55 to +100°C. Four models are available in the new TOAT-series, each with 3 discrete attenuators switchable to provide 7 discrete and accurate attenuation levels (see chart). Cascade all four models for up to 64.5dB control in 0.5dB steps. Custom values available on request. The 50-ohm TOAT-series performs with 6μsec switching speed and can handle power levels up to 0dBm. Units are housed in a rugged hermetically-sealed TO-8 package to withstand the shock, vibration, and temperature stresses of MIL-STD-883. Connector versions are available. Take advantage of the $59.95 (1-9 qty) price breakthrough to stimulate new applications as you implement present designs and plan future systems.

TOAT-R512 Accuracy (dB)	(+/−dB)	TOAT-124 Accuracy (dB)	(+/−dB)	TOAT-3610 Accuracy (dB)	(+/−dB)	TOAT-51020 Accuracy (dB)	(+/−dB)
0.5	**0.12**	**1.0**	**0.2**	**3.0**	**0.3**	**5.0**	**0.3**
1.0	**0.2**	**2.0**	**0.2**	**6.0**	**0.3**	**10.0**	**0.3**
1.5	0.32	3.0	0.4	9.0	0.6	15.0	0.6
2.0	**0.2**	**4.0**	**0.3**	**10.0**	**0.3**	**20.0**	**0.4**
2.5	0.32	5.0	0.5	13.0	0.6	25.0	0.7
3.0	0.4	6.0	0.5	16.0	0.6	30.0	0.7
3.5	0.52	7.0	0.7	19.0	0.9	35.0	1.0

bold faced values are individual elements in the units

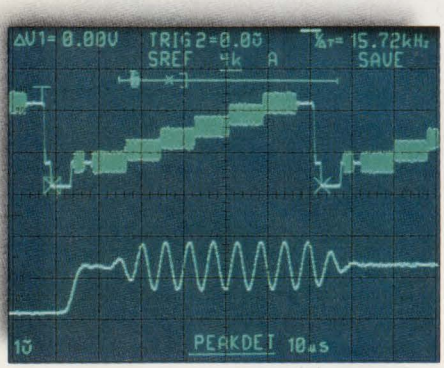
finding new ways...
setting higher standards

Mini-Circuits WE ACCEPT AMERICAN EXPRESS

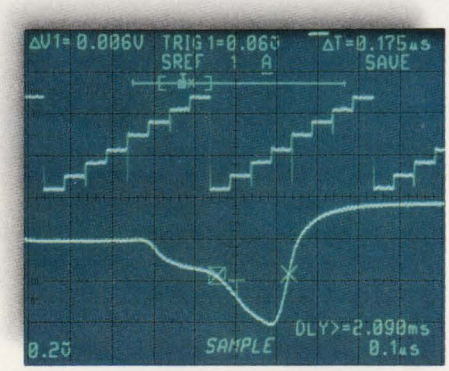
CIRCLE 210

P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500 Fax (718) 332-4661 Domestic and International Telexes: 6852844 or 620156

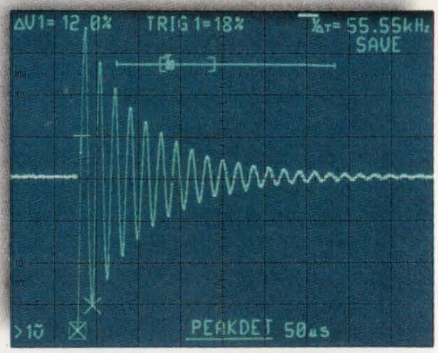
What's you



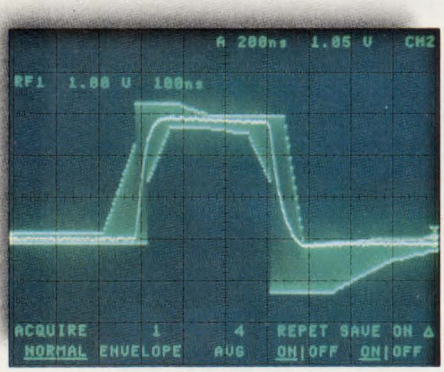
Analyzing TV and complex video signals?



Uncovering elusive glitches?

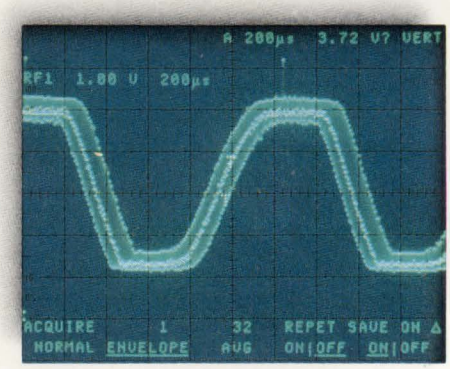


Capturing single-shot events?



Testing telecommunications signals?

Finding aberrations buried within a signal?



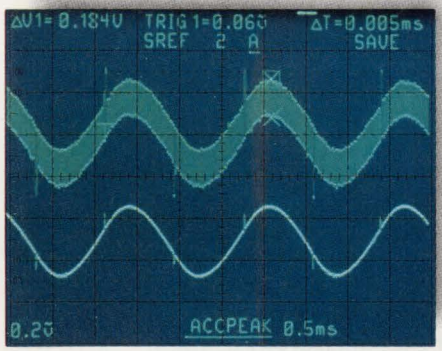
Automatic PASS/FAIL testing?

You can't depend on banner specs alone to solve problems like these. Whether you're trying to measure waveform parameters or analyze long data streams, identify infrequent events or track down glitches as narrow as 2 ns — there's all the difference between the depth of Tek troubleshooting and the trade-offs in other DSOs that compromise your results.

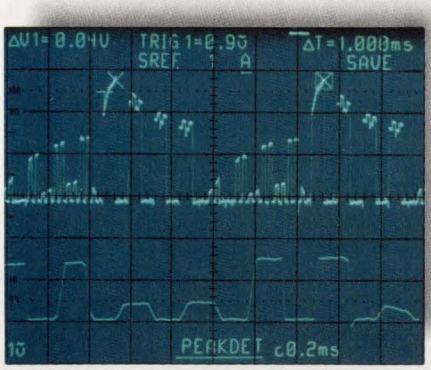
Spec for spec, feature for feature, no other company offers the credentials Tek does to effectively match DSO performance to your application needs. Whatever your criteria, you'll find a perfect solution in our line of problem-solving portable DSOs, from 10 to 500 MS/s.

Select the features to support your application. Tek DSOs offer a diverse set of capabilities including peak detect to uncover elusive glitches. Fast update rate for live signal display. Combined analog/digital operation for real-time verification of your

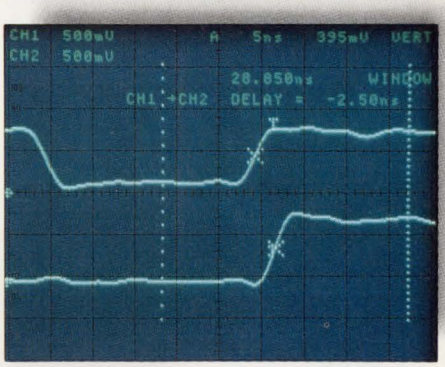
r problem?



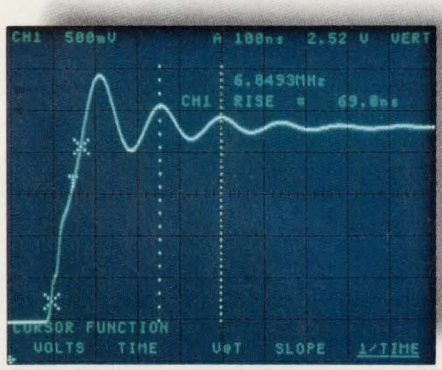
Characterizing signal noise?



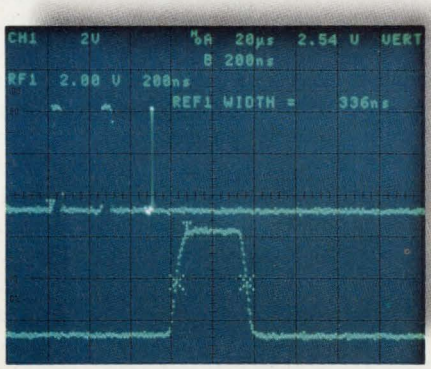
Capturing and analyzing long data streams?



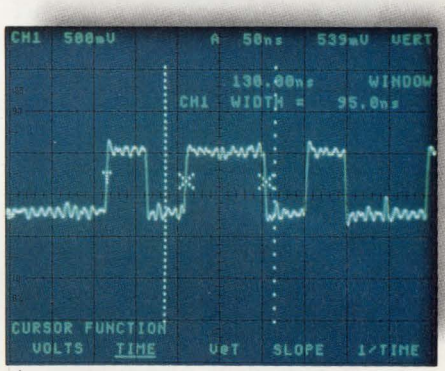
Measuring timing relationship between signals?



Performing complex measurements automatically?



Expanding glitches for close analysis?



Windowing in on signal details?

signal. Or Save on Delta to automatically verify that all parts of your signal fall within prescribed limits. Best of all, Tek's line of 100 MS/s digitizing scopes start at just $3995.

To find out which Tek scope is right for you, contact your Tek representative, return the card or call Tek direct. We can answer your questions and show you a scope that doesn't just look good on paper. It makes your toughest troubleshooting challenges routine.

One company measures up.

1-800-426-2200

MasterCard VISA

Tektronix
COMMITTED TO EXCELLENCE

CIRCLE 129

EUROPE BANKS ON JESSI

If there were a Richter scale recording the world's most significant cross-border cooperative efforts in electronics, JESSI, the Joint European Submicron Silicon Initiative, would register a hefty 7 or 8 on that scale. The numbers for this endeavor, which was launched in 1989 to help Europe catch up with Japan and the U.S. in microelectronics, speak for themselves: JESSI is an eight-year project comprising more than 100 companies from six countries. It calls for some 21,400 engineering man-hours and an outlay of more than $5 billion for R&D until 1996.

In today's European semiconductor industry, JESSI is widely regarded as Europe's last-ditch effort to stand on its own in microelectronics. They want to become less dependent on Japan's memory technology and America's know-how in advanced devices.

"Nothing less than Europe's economic well-being is at stake," says Klaus Knapp, spokesman for the project in Munich, Germany, where JESSI's board of management is based. Knapp points out that Europe's vital—and export-intensive—industries, such as automobiles, machine tools, processing equipment, and precision optics and mechanics increasingly depend on a strong native microelectronics capability. The fear exists that if other regions dominate the microelectronics field, they could manipulate the flow of crucial components to favor their own industries at the expense of Europe's.

Half of JESSI's $5 billion comes from industry and one-quarter each from national governments and the European Commission, the executive branch of the 12-nation European Community. Despite governmental delays in funding, JESSI is on schedule, Knapp says. Adds Raimondo Paletto, chairman of JESSI's management board, "The organization and its programs are in place and the first 50 projects have been started. What JESSI needs now is the full commitment of Europe's national governments to fund and participate in the effort with quick decisions and a minimum of bureaucracy."

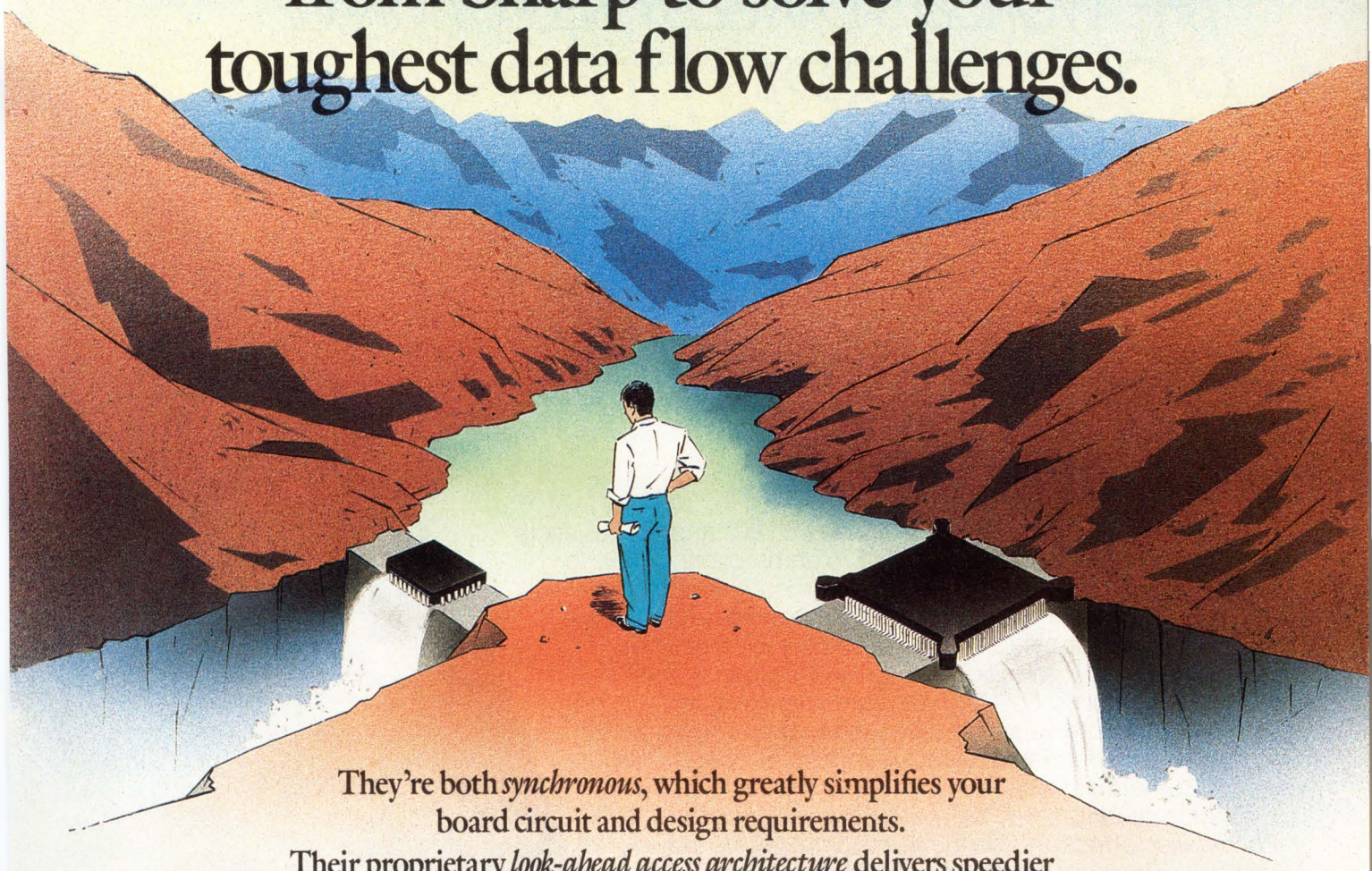
Aimed at acquiring know-how and technology, JESSI is to take device development only to the prototype stage (unlike Mega, Europe's $2-billion product-oriented high-density memory effort; the Mega project ended in 1988 with Germany's Siemens AG and Philips NV of the Netherlands developing 4-Mbit DRAMs and 1-Mbit SRAMs, respectively).

JESSI is often equated to the U.S.'s Sematech program, yet it's much broader in scope. It not only emphasizes production technology and equipment (as does Sematech), but other aspects of microelectronics as well. The project is based on four subprograms: basic research, technology, applications, and equipment and materials. Milestones pinpointed by JESSI for the next half decade include: engineering samples of 0.5-μm devices by mid-1991 and their pilot production by the end of that year, as well as first silicon of 0.3-micron parts by mid-1993 and engineering samples by mid-1994. Such 0.3-micron parts are to be ready for pilot production by the end of 1995.

Mirroring this multiprogram structure is the nature of the cooperating firms. In addition to Europe's semiconductor makers, the more than 100 members include chemical producers, production equipment manufacturers,–and, as device users, communications houses, auto makers, and computer and office equipment companies. Moreover, JESSI participation isn't limited to European firms. If a foreign company has R&D, manufacturing, and marketing activities in Europe, if it proposes a worthwhile project, and if there's reciprocal participation in similar foreign R&D programs, it qualifies as a JESSI member. Because IBM Europe meets all of these conditions, it became a participant in late November. The company cooperated with European firms in work that involved deep ultraviolet lithography and the preparation of gate dielectrics by rapid thermal processing.

JOHN GOSCH
Field Editor

Two state-of-the-art FIFOs from Sharp to solve your toughest data flow challenges.



They're both *synchronous*, which greatly simplifies your board circuit and design requirements.
Their proprietary *look-ahead access architecture* delivers speedier access and cycle times while reducing power consumption.

Introducing: The LH5492 4K x 9 Clocked FIFO.

Sharp's new LH5492 is a dual-port clocked FIFO, with a 4K x 9 configuration. The clocked interface is a significant enhancement in FIFO design over previous asynchronous parts. The clocked enables on the LH5492 eliminate the requirement to shape waveforms, resulting in simpler design tasks, and lower parts count.

Its high-speed clocked interface can be used directly with the typical 40%/60% duty cycle system clock. And a separate $\overline{OE}$ control signal provides independent control over output buffers.

The second enable pin on each part can be directly tied to the flags to simplify external logic requirements.

The LH5492 4K x 9 clocked FIFO comes in a 32-pin PLCC. It is available with access times of 20 ns, 25 ns and 35 ns, and cycle times of 25 ns, 35 ns and 50 ns, respectively.

Introducing: The LH5420 256 x 36 x 2 Bidirectional FIFO.

Sharp's new LH5420 is actually two 256 x 36-bit FIFOs in one. Operating in parallel but opposite directions to provide bidirectional data buffering that would normally require multiple independent devices.

Its 36-bit word width is an industry first. And ideal for interfacing with new generation higher-speed 32/36-bit and 64/72-bit microprocessors and buses. Moreover, a choice of 9, 18, or 36-bit word widths on Port B means efficient word width matching.

Programmable Almost Empty and Almost Full status flags on each port—in addition to Full, Half Full and Empty flags—allow you to either leave the flags set at their initialized setting of 8, or program them over the entire FIFO depth.

The LH5420 comes in a 132-pin plastic QFP package. It is available with access times of 15 ns, 20 ns and 25 ns, and cycle times of 25 ns, 30 ns and 35 ns, respectively.

SHARP®
By Design.
Sharp Electronics Corporation

For more information call: 1-201-529-8757 FAX: 1-201-512-2020.

CIRCLE 120

THE WORLD'S LARGEST SELECTION OF
POWER SPLITTERS/ COMBINERS

2 KHz to 8 GHz *from* $10.45

With over 300 models, from 2-way to 48-way, 0° 90° and 180°, a variety of pin and connector packages, 50 and 75 ohm, covering 2KHz to 8000MHz, Mini-Circuits offers the world's largest selection of off-the-shelf power splitter/combiners. So why compromise your systems design when you can select the power splitter/combiner that closely matches your specific package and frequency band requirements at lowest cost and with immediate delivery.

And we will handle your "special" needs, such as wider bandwidth, higher isolation, intermixed connectors, etc. courteously with rapid turnaround time.

Of course, all units come with our one-year guarantee.

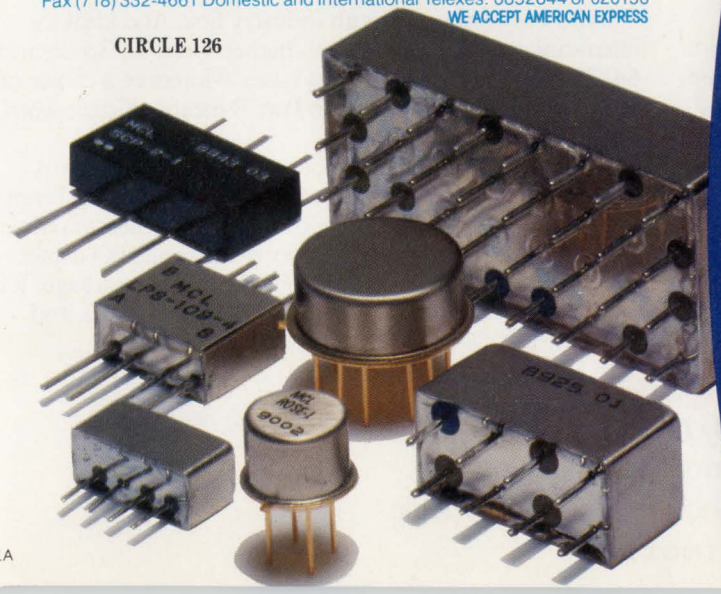
For detailed specs and performance data, refer to the MicroWaves Product Directory, EEM or Mini-Circuits RF/IF Signal Processing Handbook, Vol. II. Or contact us for our free 68-page RF/IF Signal Processing Guide.

finding new ways ...
setting higher standards

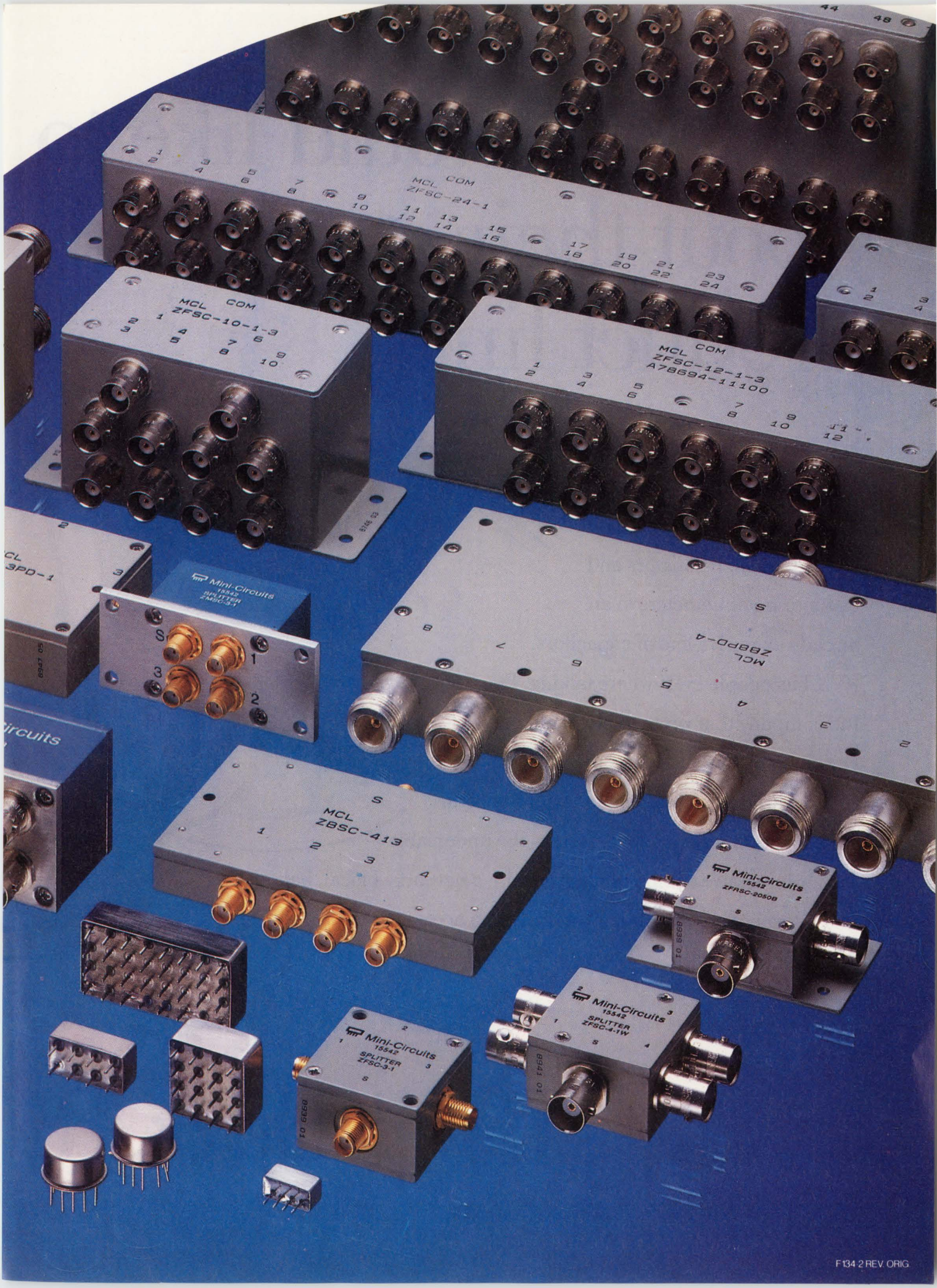
Mini-Circuits

A Division of Scientific Components Corporation
P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500
Fax (718) 332-4661 Domestic and International Telexes: 6852844 or 620156
WE ACCEPT AMERICAN EXPRESS

CIRCLE 126



P134-1 REV.A

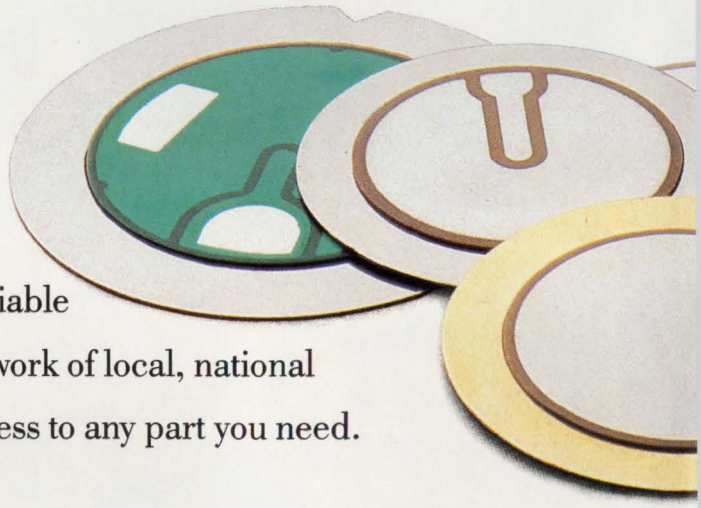


F134 2 REV. ORIG.

AVX would like to about their expanded product line.

Feedback has been tremendous. Since we added clock oscillators, piezo devices, resonators and trimmer potentiometers to an already extensive line of capacitors, AVX has people everywhere talking. Because the company that wrote the book on passive components has added another chapter.

Through our association with Kyocera, AVX has firmly established itself as the undeniable leader in passive components. And with a network of local, national and international distributors, we give you access to any part you need. Anytime. Anywhere.

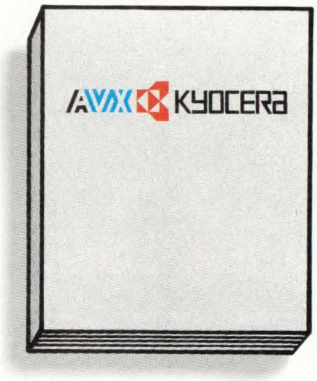


"Beep. Buzz. Ri

make a little noise

Ours is an industry where thinking globally is not just the key to victory, but to survival. That's why we've created distribution capabilities that offer solutions. No matter where you are. Or what you need. Plus the firm commitment to world-class quality, service, technology and manufacturing you've always come to expect. From the company that always makes sound decisions. AVX.

For more information about the AVX/Kyocera product line, contact AVX Corporation today by calling (803) 448-9411, or fax us at (803) 448-1943. Write to: AVX Corporation, 17th Avenue South, P.O. Box 867, Myrtle Beach, SC 29577.



AVX CORPORATION
A KYOCERA GROUP COMPANY

CIRCLE 205

ng. Tick. Hum."


NAT4882
NAT4882
The Only
Way to Reach
Full 488.2
Compatibility
PC/XT/AT
CIRCLE 231
• Industry Standard
• 7210/9914 Compatible
PC AT
• The New Industry Standard
• 16-bit speed
CIRCLE 232
Sun SPARCstation SBus
CIRCLE 233
DECstation TURBOchannel
CIRCLE 234
Macintosh NuBus
CIRCLE 235
IEEE-488.2
Turbo488
1 Mbyte/sec READS
1 Mbyte/sec WRITES
VXI Embedded Controllers
CIRCLE 236
IBM Micro Channel
CIRCLE 237
Macintosh SE/30
CIRCLE 238
Continuing
Unchallenged
Leadership
NATIONAL INSTRUMENTS®
The Software is the Instrument®
Call for a FREE Catalog
(512) 794-0100
(800) IEEE-488 (U.S. and Canada)
6504 Bridge Point Parkway
Austin, TX 78730

INDIUM TIN OXIDE TO IMPROVE IMAGE SENSORS

Indium tin oxide (ITO) promises to be an alternative to polycrystalline silicon in solid-state image sensors, according to Christ Weytens, a scientist at the Philips Research Laboratories in Eindhoven, the Netherlands. Conventional image sensors use polycrystalline silicon gates to convert light into an electric signal. But their poor transparency to visible light is a major limitation on their use in future high-performance imagers. ITO, however, one of the rare materials that's not electrically conductive, is transparent to visible light. To gain insights into applying ITO to ICs, Weytens gives special attention to the material's compatibility with standard silicon processing. ITO films are deposited by reactive dc-magnetron sputtering from an indium-tin target in an argon-oxygen environment. Smooth ITO layers are deposited in a well-controlled, reproducible manner if the oxygen concentration is higher than 25%. A typical deposition rate is 1.7 nm/min., with an applied power of 730 mW and an environment with 41% oxygen. After deposition, heat treatment is necessary to meet resistivity and etch-characteristics requirements. So far, Weytens finds rapid thermal annealing at 950°C to be the best heat treatment. *JG*

SOFTWARE CONSORTIUM PUBLISHES GUIDELINES

The Object Management Architecture (OMA) Guide is a framework and set of implementation guidelines for object-oriented computing environments available from the Object Management Group (OMG), Framingham, Mass. OMG is an international consortium of information-systems vendors, software developers, and users that promote the theory and practice of object-oriented technology in software development. The OMA Guide uses a reference model to explain the major components of an object-oriented environment, including the interfaces needed to facilitate interoperability and homogeneous extensibility. In addition, the guide contains applications, a glossary of terms commonly used in object-oriented programming, and the technical objectives of the OMG. Copies of the OMA Guide are available directly from OMG for $30. Contact Liz Berry at (508) 820-4300. *LM*

CAD CONFERENCING AIDS IN CONCURRENT DESIGN

Concurrent design teams will eventually need to communicate interactively through their computer workstations. Now, engineering teams can assemble such a setup with a CAD conferencing product from Intergraph Corp., Huntsville, Ala. The product enables a computer graphics image to be viewed simultaneously on workstations at as many as eight sites. With an accompanying voice connection, conferees can discuss the on-screen image. Consequently, engineering and management teams around the globe can work on projects together in real time without leaving their offices. During CAD conferencing, participants can redline drawings and engineering-change orders interactively. Moreover, they can sign-off on a project by putting their signature on the displayed image. The product includes conferencing software that manages interactive communication between workstations, a telecommunications interface card for each workstation, and an electronic tablet and stylus for communications and signatures. To input information, the system uses both an on-screen graphical user interface and a graphics tablet. For more information, call (800) 826-3515. *LM*

ELECTRONS ACCELERATED TO 150,000 eV

Researchers at Jerusalem's Racah Institute of Physics claim to have developed a new technique to accelerate electromagnetic waves and electrons to energy levels of 150,000 electron volts. Their ultimate target is 500,000 eV. Such a high-energy beam would be suitable to use in free-electron lasers. The system they built uses a 10,000-eV electron gun and a radar transmitter. Electrons are fired along a tube "immersed" in a magnetic field, the intensity of which is varied along the length of the tube. As the beam passes through the tube, it's forced to follow a helical path, with the speed of rotation depending on the field's strength. Circular-polarized electromagnetic pulses from the radar transmitter are aimed along the axis of the electron beam, with a pulse repetition rate similar to the electron rotational frequency. That way, they say, energy is transferred to the electron beam. For more information, contact the Britain/Israeli Public Affairs Center, 21-22 Great Sutton St., London, EC1V 0DN. Telephone +44(0)714905373. *PF*

How to ge customs witho

Custom IC Solutions

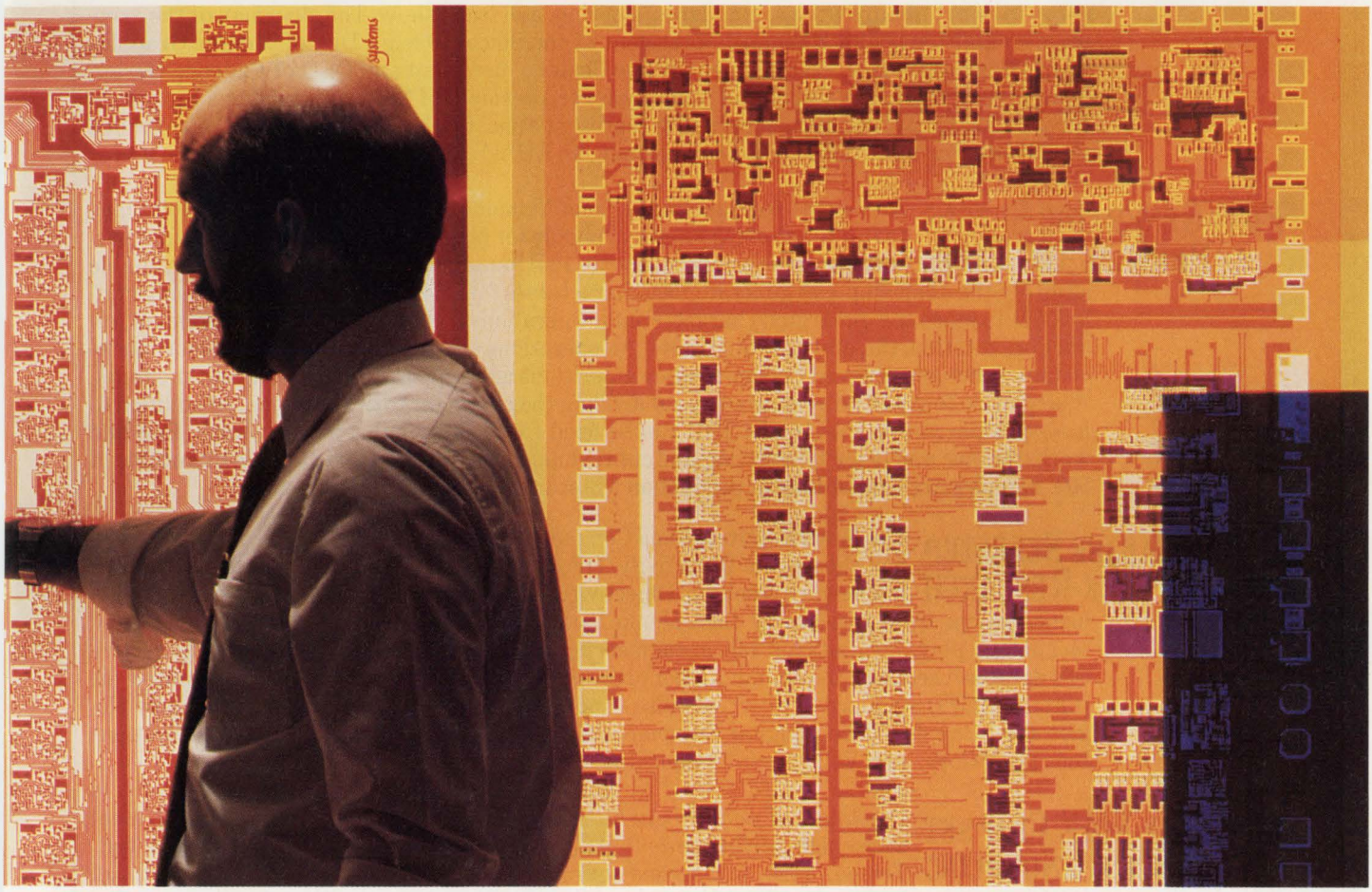
Need a custom IC? You'll bypass the usual red tape by working with an experienced custom IC partner like Silicon Systems.

Our 20 years of experience developing ICs for mass storage, communications and automotive applications means we can move quickly from your inspiration to a working custom prototype in no time.

And speed your custom IC into volume production.

In our MSICs ™ (Mixed-Signal Integrated Circuits) world we combine high-performance analog and digital circuitry on a single chip and allow you to take full advantage of our state-of-the-art design systems. From there we will optimize the performance and integration of your design in CMOS, Bipolar or BiCMOS

et through
out any delays.



process technologies.

Enough said? Move to the front of the line and discuss your custom design requirements with a Silicon Systems representative. Or call us for lit package CUST-1.

Circle 124 for Product Info

Circle 125 for Career Info

Silicon Systems, Inc.,
14351 Myford Road, Tustin, CA 92680
Ph 1-800-624-8999, ext.151 Fax (714) 669-8814
European Hdq. U.K. Ph (44) 79-881-2331 Fax (44) 79-881-2117

silicon systems®

1/4-In. Cartridge Tape Drives Improving

The performance and capacity of 1/4-in. data-cartridge subsystems will continue to rise, according to the Board of Directors of Quarter-Inch Cartridge Drive Standards Inc. (QIC), Santa Barbara, Calif. The group recently adopted a migration path to assure that the performance and capacity goals of the DC2000- and DC6000-class drives are reached. The path outlines performance goals through 1995. The QIC group also made a commitment to ensure that all future drives will be backwardly read-compatible with existing drives, protecting users' investments. The path for the 3-1/2-in. drives surpasses 8 Gbytes with a transfer rate better than 1.5 Mbytes/s by 1995. In the same time frame, the 5-1/4-in. drives should hold 24 Gbytes of data with a 2.4-Mbyte/s transfer rate. These numbers are for drives using data-compression techniques. *RN*

EDAC Re-Elects Management Team

At its annual election, the Association of Electronic Design Automation Companies (EDAC) re-elected all existing committee members for a second term. EDAC's organization consists of an executive committee and four operating committees: communications, standards, steering, and trade show. The chairman of the executive committee is Jim Hammock, president of the Silicon Design Div. of Mentor Graphics Corp., Beaverton, Ore. Co-chairmen are Joe Costello, president and CEO of Cadence Design Systems Inc., San Jose, Calif.; and Alain Hanover, president of Viewlogic Systems Inc., Marlboro, Mass. EDAC has 46 members that represent almost 90% of commercial EDA revenues worldwide. For more information on becoming an EDAC member, call (408) 988-3322. *LM*

Font Generator Speeds Printing 100 Times

An outline font generator from Yamaha LSI, San Jose, Calif., is 100 times faster than software now available for high-quality laser-printer output. According to the company, the GC1001, one of the few font generators available as an off-the-shelf chip, can generate 1000 characters/s for a 64-by-64-dot character using static RAM to store the generated character data. Operations include character enlargement, reduction, rotation, tilt, and a parallel move. All operations are facilitated by built-in coordinate-change functions. Curved-line-generation algorithms add support for almost all outline fonts. A large-size font can be generated by subdividing the character to be displayed. In addition to laser-printer controllers, the GC1001 can be used for desktop publishing systems, PCs and workstations, and large typesetting and cut-text machines. Prices start at $65 in quantities of 500. Samples are available now; production will start in February. *RN***CIRCLE 331**

Database Selected For Framework Research

The Microelectronics and Computer Technology Corp. (MCC), Austin, Texas, has chosen the Objectivity/DB database as a prototyping vehicle for CAD framework research. Objectivity/DB is an object-oriented database management system from Objectivity Inc., Menlo Park, Calif. MCC believes that object-oriented technology plays a significant role in engineering frameworks. The company chose Objectivity's database because of its commitment to the engineering community and CAD Framework Initiative (CFI) standards. Objectivity also announced relationships with Chips and Technologies Inc., Cimplex Corp., Digital Equipment Corp., Matra Datavision, Pie Design Systems Inc., Sony Corp., and Valid Logic Systems Inc. *LM*

Military VME Chip Set Gets Second Sourcing

Designers of military products now have a multiple-source solution to meet their high-performance VMEbus interface requirements. Motorola Inc., Tempe, Ariz., will second source the advanced VMEbus interface chip set (AVICS) currently supplied by Newbridge Microsystems, Kanata, Ontario, Canada. The AVICS solution consists of two CMOS VLSI devices: the CA91C014 advanced-system architecture-control circuit (ACC) and the CA91C015 data/address register file (DARF). The ACC, which can be used in standalone medium-performance applications, is packaged in a 144-pin PGA, while the DARF is housed in a 224-pin PGA. The arrangement between the two companies also calls for the second sourcing of the 64-bit AVICS-64 now under development. With the AVICS 64-bit-block burst capability, which is defined in the IEEE-1014 Rev. D standard, transfers of 60 Mbytes/s are possible. Current 32-bit DARF chips can be upgraded to 64 bits using the pin-compatible solution. *RN*

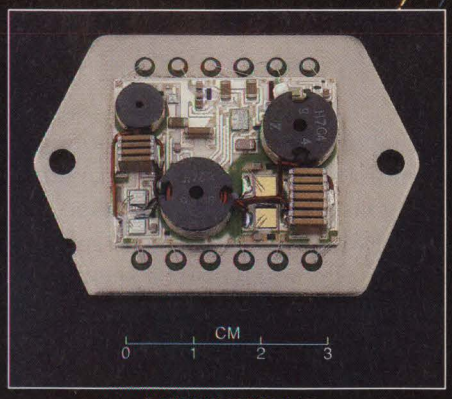
A NEW CONCEPT

DC-DC CONVERTER

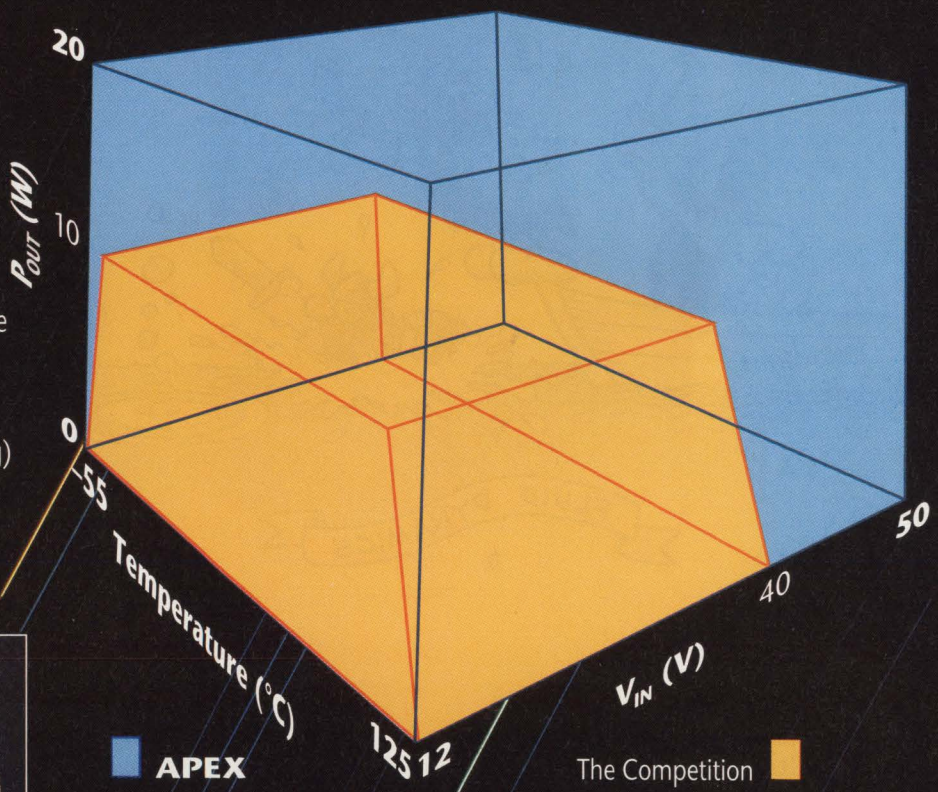
MILITARY GRADE

FEATURES

- Designed and Built for Reliability
- Rugged:
  - —Low Internal Temperatures
  - —Low Component Count
  - —Withstands 5000g
  - —Welded Hermetic Package
  - —Remote Shutdown and Sense
- 28V to 5V, Single Output
- Full Output Power for T_C = -55°C to 125°C (No Derating)
- Wide Continuous Supply Range 16 to 50 volts
- High Power Density 20W/in³



PATENT PENDING



APPLICATIONS

- 28 volt 704D Designs
- Digital Circuit Power Supply
- Isolated Instrumentation
- Parallel Redundant Operation
- High Current, Low Voltage Analog Circuits

APEX...RELIABILITY BY DESIGN

To Place An Order Call
602-742-8601

For Applications Assistance Call
1-800-421-1865

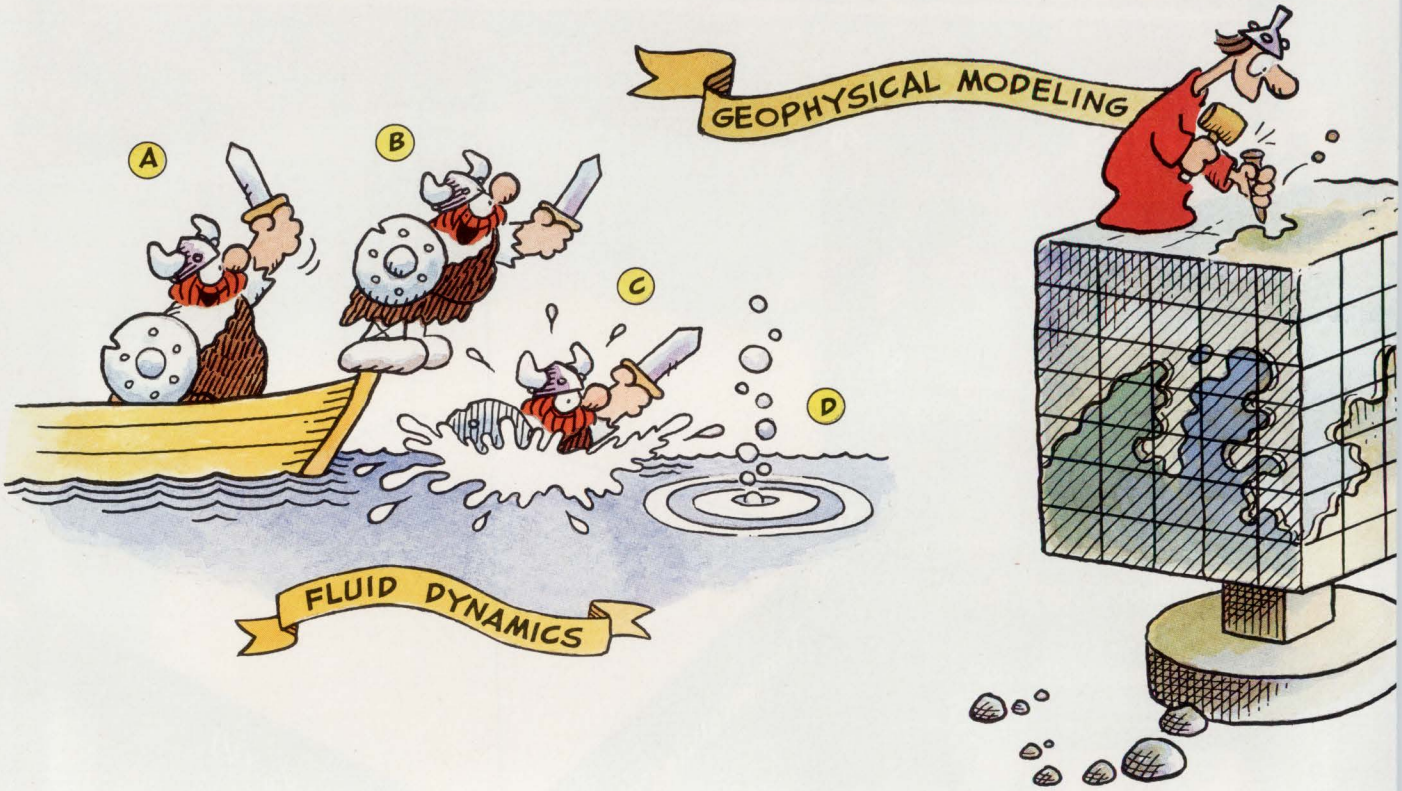
APEX® µtech
DEDICATED TO EXCELLENCE

APEX MICROTECHNOLOGY CORPORATION

To receive your copy of our High Performance Amplifier Handbook please call toll free
1-800-448-1025

CIRCLE 200

The IBM RISC System/ The power you've been seeking



It's a never-ending quest for power seekers. You're always looking for ways to run your favorite applications faster. Well, search no more. The RISC System/6000™ family of POWERstations and POWERservers gives you power that soars as high as 23 MFLOPS and 56 MIPS.

	MFLOPS	MIPS	SPECmark™
POWERstation 320	7.4	29.5	22.4
DECstation 5000-200	3.7	24.2	18.5

When it comes to porting, your ship has come in. Of course, all the speed in the world wouldn't mean much without the applications you need. So the RISC System/6000 family already has more than 2,000 of the most popular technical and commercial applications up, running and running fast. And if you think you know a good thing when you see it, so do software vendors. That's why you'll also be seeing more and more applications coming on board the RISC System/6000 platform all the time. And if you like to build your own solutions, there's a full arsenal of enablers and relational data bases from leading vendors, as well as CASE tools and a host of popular programming languages.

A smorgasbord of solutions. Applications already announced include the IBM engineering design packages CADAM,™ CAEDS,™ CBDS,™

MFLOPS are the results of the double-precision, all FORTRAN Linpack test 100x100 array suite. The Dhrystone Version 1.1 test results are used to compute RISC System/6000 Integer MIPS value where 1,757 Dhrystones/second is 1 MIPS (Vax 11/780). SPECmark is a geometric mean of ten benchmark tests. All performance data are based on published benchmark information.

6000 family. for all your applications.

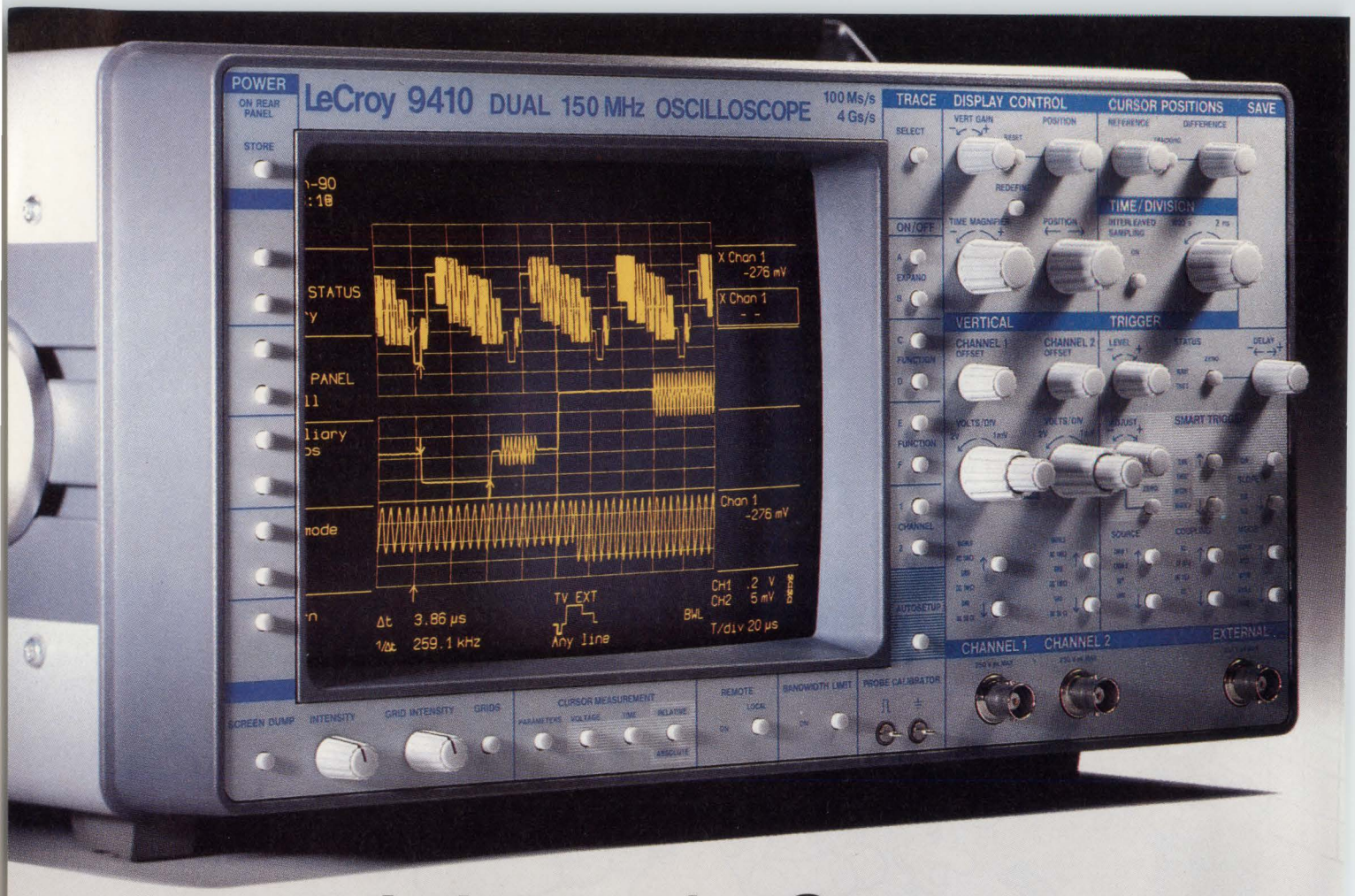
CATIA™ and AES. Also available are a broad spectrum of solutions from vendors like Valid Logic, MacNeal Schwendler, Swanson Analysis, SAS Institute, SPSS, Wavefront, Alias, Polygen, Cadence, Fluid Dynamics International, Western Atlas, ECL Petro and creare.X. Scientific and technical applications are available in areas like physics, structural analysis, chemistry, securities trading, mathematics, earth resources, operations research, visualization, graphics, technical publishing and more. There's also accounting software like FourGen and support for leading UNIX®-based office automation packages. And there are key industry applications for businesses in medical groups, retail stores, newspapers, pharmacies and many more.

Command enormous processing clout.
The RISC System/6000 family is built to boost the performance of the software power seekers use most. It's got the best floating point processor in the business for numerically intensive applications, plus a new superscalar processor and incredible 3D graphics capabilities. To find out more, call your IBM marketing representative or IBM Business Partner. For literature, call 1 800 IBM-6676, ext. 990.

For the Power Seeker.

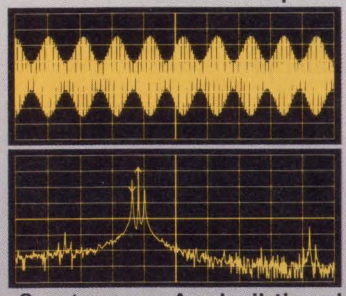
IBM®

CIRCLE 203



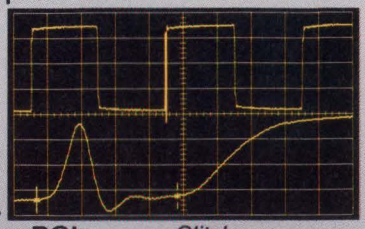
At last, a LeCroy you won't have to beg for.

Now you can get LeCroy Digital Oscilloscope performance for the price of an ordinary oscilloscope. At just **$6,990**, the new Model 9410 offers you unrivaled measurement capabilities. Waveforms are digitized with high signal fidelity into 10K acquisition memories and presented on the sharpest display of any oscilloscope (the above picture speaks for itself). One can zoom in on fine details, expand signals, and use the 9410's digital cursors to get the ultimate in precision.



Spectrum Analysis Option

The Model 9410 doesn't stop there. It also includes LeCroy's SMART trigger that detects buried glitches, timing violations, and logic states (you'll be prepared for the most elusive signals). Internal signal processing calculates time, voltage and frequency parameters in fractions of a second. And all the data can be transferred directly to printers, plotters or PC's using the 9410's high-speed GPIB or RS-232.



Glitch Trigger

Price being equal, wouldn't you rather have a LeCroy?

LeCroy Corporate Headquarters
700 Chestnut Ridge Road - Chestnut Ridge, NY 10977-6499
Tel.: 1-800-5 LeCroy - (914) 425 2000 / TWX: (710) 577-2832
Fax: (914) 425-8967

LeCroy

Innovators in Instrumentation

GLASNOST COMES TO ISSCC AS ADVANCED ICS ARE UNVEILED

This year's forthcoming rendition of the International Solid State Circuits Conference will break with history, hosting a special session on technology in the USSR. A paper from an Eastern-bloc country is more than a rarity at the ISSCC, even though half of the papers to be presented are from European or Asian-based companies. There will be four presentations by Soviet researchers, as well as a technology overview of the state of microelectronics in the USSR by a U.S. delegation that visited the Soviet Union in the fall of 1990.

ISSCC, which will run from February 13-15 in San Francisco, Calif., will also host dozens of papers that show the latest research advances in a number of device areas. These include 4-Mbit static RAMs, 64-Mbit dynamic RAMs, Josephson-junction supercooled circuitry, 32- and 64-bit microprocessors, digital signal processors, math chips, logic arrays, novel communications chips, analog circuits, and analog-to-digital converters. A trio of invited addresses will open the conference with discussions on microelectronics for planetary spacecraft (presented by the Jet Propulsion Laboratory, Pasadena, Calif.), the future of notebook computers (presented by Toshiba Corp., Tokyo, Japan), and the need for design for testability (presented by the Center for Reliable Computing, Stanford University, Calif.)

The special session on technology in the USSR will include papers on a 4-kbit NMOS nonvolatile RAM with an extended 16-kbit nonvolatile memory, n-channel 256-kbit and 1-Mbit flash EEPROMs, and an automated mini-fab for low-volume and fast-turnaround chip manufacturing. A fourth paper describes the use of space-charge waves in two-valley gallium arsenide thin films to process microwave signals—gain, filtering, correlation and other signal-processing functions are possible at microwave frequencies. All four papers will be presented by engineers from the Perceptive Research Institute, Nauchny Center, Moscow.

CRYOGENIC SYSTEMS

In a session on low-temperature circuits, researchers from the T.J. Watson Research Center of IBM Corp., Yorktown Heights, N.Y., describe how they brought the operating temperature of a 4-Mbit DRAM down to 85K, and achieved a three-fold improvement in access time and a charge storage time of over 50 minutes. Such a large storage time could drastically reduce the number of refresh cycles needed to restore the charge, severely cutting the standby power consumed by the memory chip.

Cryogenic systems are also the focal point of a pair of papers from Fujitsu Laboratories Ltd., Atsugi, Japan. The first paper shows a sub-ns-clocking system for Josephson computers. The system connects a packaged 4-bit Josephson microprocessor that's kept at 4.4K to a circuit kept at 300K. The communication occurs over a 60-line cable that enables the system to operate at 1.1 GHz. The second paper shows off an all-niobium 24-bit Josephson carry-select adder that achieves a 360-ps addition speed and a 300-ps carry propagation delay—the shortest times achieved for such a function.

Continuing their push for high speed with GaAs high-electron-mobility transistors, Fujitsu designers upped the integration level for a GaAs memory chip to 64 kbits while keeping the access time to just 1.2 ns. The chip employs ECL I/O levels and consumes close to 6 W—a consequence of the high-speed circuitry. ECL I/O levels for biCMOS memories also yield high-speed chips, but with 64 times the density.

A 4-Mbit static RAM developed by Fujitsu with a 0.6-μm biCMOS process will be described—it accesses in just 7 ns and consumes only about 600 mW in its 4-Mword-by-1-bit organization. Details on a 4-Mbit TTL-I/O biCMOS SRAM with a 10-ns access time, also from Fujitsu, will also be presented.

Able to access in about 4 ns, a 512-kbit CMOS chip with ECL interfaces will be described by IBM designers. The synchronous memory has a 2-ns cycle time and employs a pipelined architecture with self-resetting circuit blocks.

DRAMs are also getting faster, especially if implemented in biCMOS as Hitachi Ltd., Tokyo, Japan, will describe. An experimental 4-Mbit chip built with 0.8-μm features achieves a 17-ns access time and a 40-ns cycle time—in comparison, the fastest commercial CMOS DRAMs available have access times about three times longer than Hitachi's chip. By using a nonmultiplexed address input approach, researchers from the microelectronics laboratory of Toshiba Corp., Kawasaki, Japan, will show off an all-CMOS 17-ns DRAM.

Even the highest-density DRAMs are getting faster—in the session on high-density DRAMs, five of the six papers will detail experimental 64-Mbit chips with access times of 50 ns or less *(see the table)*. The fastest and the smallest of the group comes from Toshiba. The DRAM accesses in 33 ns, measures 9.22-by-19.13 mm, and operates from a 3.3-V supply. The most novel structures come from Hitachi and Matsushita Electric Industrial Co. Ltd., Osaka, Japan.

The Hitachi chip has a

WANT TO GO?

The International Solid State Circuits Conference will be held at the San Francisco Hilton Hotel, Feb. 13-15. To register for the conference, contact Diane Suiters, Courtesy Associates, (202) 639-4355 (phone) or (202) 347-6109 (fax). Advance registration discounts end January 31. For hotel reservations, call the San Francisco Hilton, (415) 771-1400.

novel series-connected cell that reduces cell area considerably over its previous design by eliminating many of the data-line contacts. As many as 64 times the number of cells can be connected to a sense amplifier for an 8-fold reduction in bit-line capacitance, improving access time. With a 4-Mword-by-16-bit architecture, the 64-Mbit Matsushita chip employs a meshed power-line network over the surface of the chip. The network reduces power-line drops that can potentially occur during I/O operations in which all lines are active.

Nonvolatile memories are also improving in density and speed, as papers from Intel Corp., Folsom, Calif., Toshiba, and Mitsubishi will illustrate. A 29-ns 8-Mbit EPROM will be Intel's focal point. The chip employs a novel dual-reference column-address-transition-detection scheme to achieve the short access time. A 16-Mbit EPROM from Toshiba achieves a 62-ns access time by using sense-line equalization and data-out latches that are enabled by the address-transition-detection circuits on the chip. With a comparable 60-ns access time, a 16-Mbit flash EEPROM developed by Mitsubishi was designed for more flexibility—the storage array is divided into 64 subblocks, each of which can be independently erased and rewritten.

The need for such high-density and high-speed memories is driven by the increasingly more complex microprocessors operating at ever-higher clock rates. A 100-MHz CMOS microprocessor with an 80486 architecture will be described by Intel Corp., Aloha, Ore. The CPU chip, implemented with three levels of metal interconnections to keep wire lengths as short as possible, crams 1.2 million transistors onto a 6.8-by-11.8-mm chip thanks to a submicron process.

A 100-MIPS superscalar 64-bit RISC processor that packs two integer units as well as a floating-point processor, instruction and data caches, and enhancements for DSP operations, will be unveiled by National Semiconductor Corp. The devices were developed at National Semiconductor's design center in Herzlia, Israel.

Tackling control tasks, a single-chip microcontroller with a field-programmable 20-MOPS intelligent subprocessor will be unveiled by Hitachi. The subprocessor can schedule up to 12 tasks with 50-ns resolution in real-time applications. With a 64-bit-wide instruction, up to five internal operations can take place every cycle. An on-chip multitask scheduler enables the chip to handle multiple tasks without it having to perform a context switch. Dual EPROM blocks provide the configurability.

A data-driven processor that employs superpipelining was designed jointly by Mitsubishi Electric Corp., Itami, Japan, and Osaka University, Japan. The chip achieves a 32-bit throughput of 50 MFLOPS in vector-processing applications, and employs self-timed circuits and a shared memory that facilitates the processor's use in multiprocessor configurations. Running at 65 MHz, a floating-point coprocessor developed by Texas Instruments Inc., Dallas, and Hewlett-Packard Co., Ft. Collins, Colo., delivers a throughput of 33.2 MFLOPS. Designed as a coprocessor for a RISC CPU, the chip employs 64-bit-wide internal buses and dissipates about 2.3 W when running at top speed.

Able to do a 54-bit mantissa division in just 160 ns, a CMOS divider circuit, jointly designed by Silicon Engines Inc., Stanford, Calif., and Stanford Univ., employs self-timing schemes to reduce delays so that results appear in 45 to 160 ns, depending on the data operands.

Neural Devices

Designers at Adaptive Solutions Inc., Beaverton, Ore., and Inova Microelectronics Inc., Santa Clara, Calif., created an 11-million-transistor neural processor by modeling thought processes with a digital neural-network execution engine. The chip performs 1.6 billion connections/s using a multifield imaging approach. One chip includes 64 processors that execute the same instruction on different pieces of data. A self-learning chip with the equivalent of 336 neurons and 28k synapses will also be unveiled by Mitsubishi. In addition, AT&T Bell Labs, Holmdel, N.J., will present details on an analog neural-net processor that can implement a wide range of network topologies. The chip contains 4096 synapses and achieves a sustained throughput of 5×10^9 connection updates/s.

Dealing with real-world signals, papers in the analog sessions at ISSCC will also show many impressive gains. One of the most novel analog circuits, described in the Emerging Technologies session, is actually based on EEPROM technology—an analog memory that doesn't have to convert data into digital form for storage. The memory achieves a storage density about eight times that of digital memories, and can connect directly to a microphone or loudspeaker to implement a single-chip voice recorder.

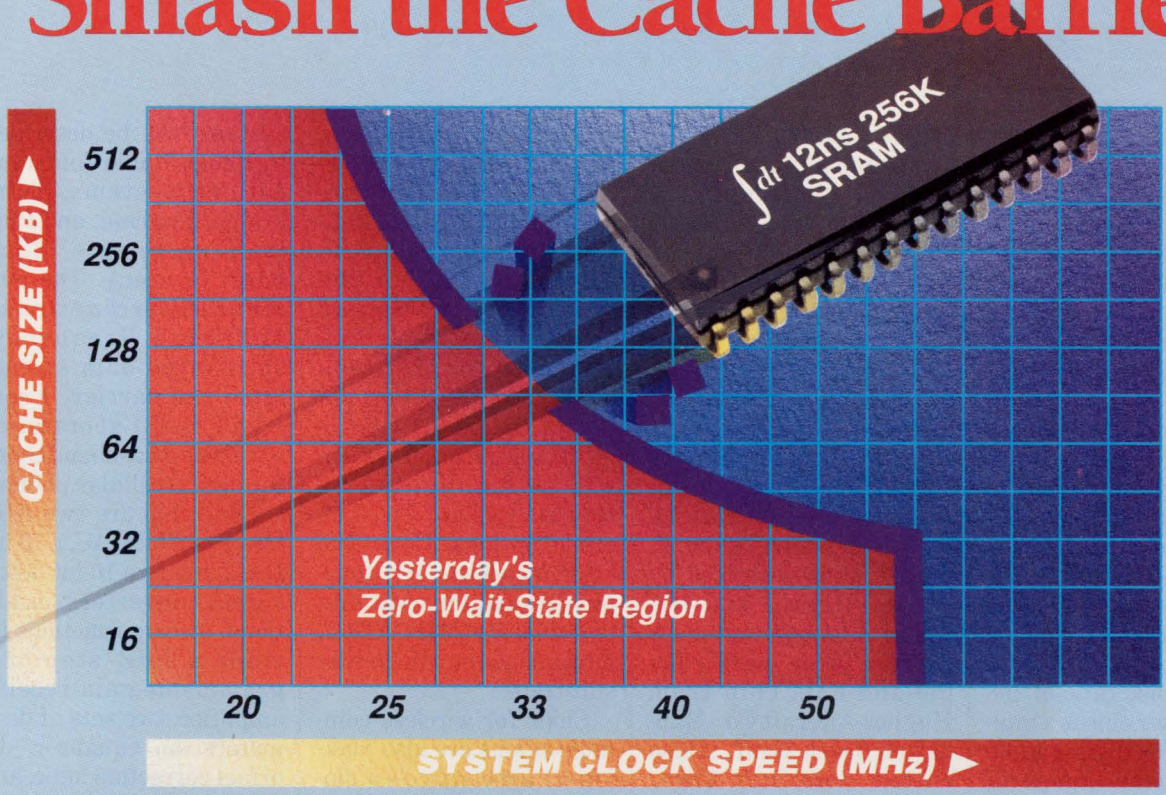
Three papers will highlight advances in ADCs. One paper describes a 500,000-sample/s 14-bit delta-sigma converter from the Catholic University, Leuven, Belgium. Another from the Center for

COMPARING 64-MBIT CHIPS

Manufacturer	Access time	Chip size	Cell size	Storage-cell capacitor
Toshiba	33 ns	9.22 by 19.13 mm	0.9 by 1.7 μm	Asymmetrical stacked
Fujitsu	40 ns	11.27 by 19.94 mm	1.0 by 1.8 μm	N.A.
Mitsubishi	45 ns	12.50 by 18.70 mm	1.0 by 1.7 μm	N.A.
Matsushita	50 ns	10.85 by 21.60 mm	2 μm^2	Tunnel stacked
Hitachi	N.A.	N.A.	N.A.	Crown-shaped stacked

N.A.--Not available

Smash the Cache Barrier



12ns BiCEMOS™ 256K TTL SRAMs

Speed *and* Density

Now you can get cost-effective 12ns speed and 256K density. IDT's 256K BiCEMOS TTL Static RAMs are the ideal solution for high-density cache systems for applications like workstations, file servers, and graphics systems. These new-generation SRAMs provide the highest system speed without sacrificing system chip count or increasing power consumption.

Fastest 256K SRAMs

IDT's 12ns and 15ns 256K BiCEMOS Static RAMs are the fastest available 256Ks today and are the perfect match for optimizing the high performance needs of RISC and CISC processors. These SRAMs smash the barrier to efficient cache operation at the highest clock speeds.

BiCEMOS process technology achieves performance levels equivalent to "next-generation" CEMOS technology and is the path to achieve zero-wait-state processing beyond 33MHz.

Technology for the '90s

IDT's BiCEMOS technology offers the best of both worlds: the low power consumption of CMOS with the high speed of bipolar technology. And BiCEMOS technology makes IDT's SRAMs the pace setters with ever-faster system designs. BiCEMOS *is* the technology for the '90s!

300mil Packaging

All of IDT's BiCEMOS SRAMs are available in 300mil PDIP and SOJ packages for easy design and layout. The 71B258 64K x 4 SRAM is available in 24-pin DIP and SOJ packages, and the 71B256 32K x 8 and 61B298 64K x 4 SRAMs are available in 28-pin packages.

Free Samples Now!

Get your free samples of IDT's BiCEMOS TTL SRAMs today. Just fill out the coupon and send it in by FAX or mail, or call our Marketing Hotline at **(800) 544-SRAM.**

PLEASE COMPLETE AND FAX, OR MAIL IN AN ENVELOPE WITH YOUR BUSINESS CARD

Yes! I want free samples of the fastest 256K TTL SRAMs!

- ❑ Please send me data sheets on IDT's BiCEMOS SRAMs.
- ❑ Please have a salesperson bring me samples of the:
  - ❑ IDT61B298 (64K x 4) **12ns** TTL SRAM w/$\overline{OE}$
  - ❑ IDT71B256 (32K x 8) **15ns** TTL SRAM

Name _____

Title _____

Company _____

Address _____

City/State _____ Zip _____

Phone ( ) _____ FAX ( ) _____

Send to:

FAX: 408-758-4056

IDT SRAM Marketing
1566 Moffett Street
Salinas, CA 93905

Integrated Device Technology

CIRCLE 117

Integrated Systems at Stanford Univ. discusses a 12-bit oversampling ADC with a 1.5-MHz conversion rate. The third paper concerns an 18-bit, 20-kHz dual delta-sigma unit jointly developed by Analog Devices Inc., Wilmington, Mass., and Ensoniq Corp., Malvern, Pa.

A pair of DACs from Philips, Eindhoven, the Netherlands, will also be described in the converter session. The first is an 18-bit-bitstream dual-channel DAC with a total harmonic distortion of 120 dB and a signal-to-noise ratio of 108 dB. The other chip is a multibit DAC for digital audio with a dynamic range of 115 dB. This current-mode 5-bit sign-magnitude DAC operates at 128 times the oversampling rate. A complete codec, operating at 25 kHz, will be the highlight of a paper from NEC Corp., Kawasaki, Japan. The codec includes a 24-bit DSP filter, a 16-bit ADC, and an 18-bit DAC. It has signal-to-noise ratios of 96 and 108 dB, in ADC and DAC operations, respectively.

High-speed data-acquisition circuits, such as 14-bit sample-and-hold amplifiers, will be described by Analog Devices and National Semiconductor. A 20-MHz video-speed sample-and-hold chip from Hughes Aircraft Co., Manhattan Beach, Calif., is also on tap. Both Sony Corp., Atsugi, Japan, and Matsushita will unveil details of 500-MHz ADCs. The Sony ADC delivers 8 bits at 500 MHz with dc linearity within ± 0.4 LSB. The Matsushita chip actually has two 500-MHz ADCs on one chip. The two converters are interleaved to obtain a conversion rate of 1 Gsample/s, and a resolution of 6 bits. A complete 2-GHz 8-bit data-acquisition system will be highlighted by Hewlett-Packard Co., Colorado Springs, Colo. The system consists of a four-phase sampler chip and two dual 500-MHz ADCs, all combined on a thick-film substrate.

Chips for wireless communications are also making an appearance—a single-chip VHF and UHF receiver for radio-paging systems will be described by Philips Radio Communications Systems, Cambridge, England, and Philips Components, Hamburg, Germany. The 500-MHz receiver can extract a 1200-baud frequency-shift-keyed data stream from the carrier. From AT&T Bell Laboratories will come a baseband codec for digital cellular phones. On one chip are two 8-bit DACs, a 9-bit DAC, a 10-bit DAC, and two 10-bit delta-sigma converters. Additional on-chip functions include a 2-dB/step programmable-gain receive amplifier, two sets of decimators, an equalizer, dc-offset correction logic, and control and timing circuits.

DAVE BURSKY

GaAs Switch Turns On 8.5 MW In Nanoseconds

Employing gallium arsenide, scientists at Sandia National Laboratories, Albuquerque, N.M., have developed a photoconductive semiconductor switch (PCSS) that turns on large amounts of power rapidly. In a recent experiment, the PCSS was able to switch 8.5 MW of power using light from an 850-W laser-diode array. Until now, the highest power switched with such a device using the same laser-diode array was 0.25 MW.

The PCSS held off 55 kV until it was activated, and delivered 470 A into a 38-Ω load. Pulse current peaked in just 3.5 ns, even though the optical pulse that triggered the switch had a rise time of 21 ns. Subsequent experiments have illustrated that rise times as short as 0.5 ns could be accommodated.

According to the Sandia researchers involved with the PCSS development, such results provide the foundation for a switch technology that can produce tens-of-kilovolt pulses with subnanosecond rise times at high repetition rates in a compact package.

The PCSS was operated in a high-gain switching mode developed at Sandia. With the "lock-on" mode, the switch is able to trigger rapidly with minimal laser energy.

The switch consists of a small disk of undoped and bulk semi-insulating GaAs about 1 in. in diameter. Such material has insulating properties in the dark. However, when light shines upon on it, the material becomes conductive.

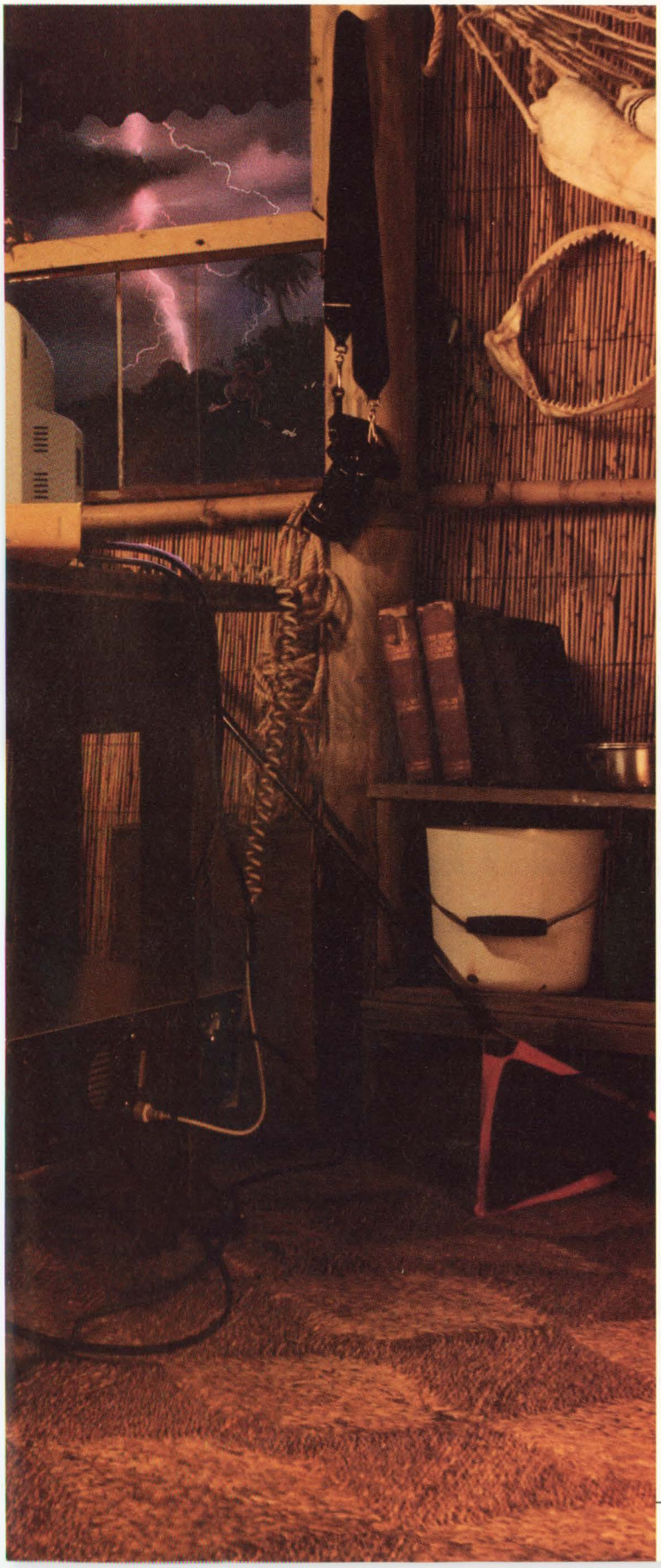
The device has many possible applications. One such application could be a small, fast-rise-time, repetitive switch for ultra-wideband impulse radar. This type of radar is currently being studied at several research laboratories. Other applications include optically activated firesets to trigger explosives, pulse-power systems to drive compact high-power accelerators, and fast-rise-time switches for electromagnetic-pulse testing.

The experiments done on PCSS were carried out by Sandia scientists Fred J. Zutavern, Guillermo M. Loubriel, Daniel L. McLaughlin, Martin M. O'Malley, and Wesley D. Helgeson, in Sandia's Repetitive Pulsed Power Research Division. Assisting the scientists were electrical engineers Paul Stabile and Arye Rosen of the David Sarnoff Research Center, Princeton, N.J., where the laser-diode array was developed.

ROGER ALLAN

From Outer Space to Your Place,

We're Your Best Defense.



By putting our military experience to work in high-volume, low-cost applications, we're giving new meaning to the term *National Defense*. Our Power Supply Supervisory Chips are a good example.

These Raytheon Linear Arrays *(RLAs)* act as a computer's early warning system. They monitor internal voltage levels to 0.3% accuracy—and signal a shut down before power surges can fry the system.

It's "Defense Technology" with a peaceful purpose. And it's helping take computers into places they've never been.

Our RLAs have business benefits, too. If you can't decide between a custom or semicustom device, don't. Our *Win-Win* program lets you get to market quickly with a semicustom array, then shift to full custom as sales increase.

Win-Win is fast, flexible, and makes good business sense because it eliminates the risk of getting into a full custom array before you're really ready.

Raytheon is committed to analog technology. From our design kits and engineering support to our fab and plastic assembly facility. We have the experience it takes to help you develop creative, cost effective solutions.

Find out how. Call **1-800-722-7074** for our new analog brochure.

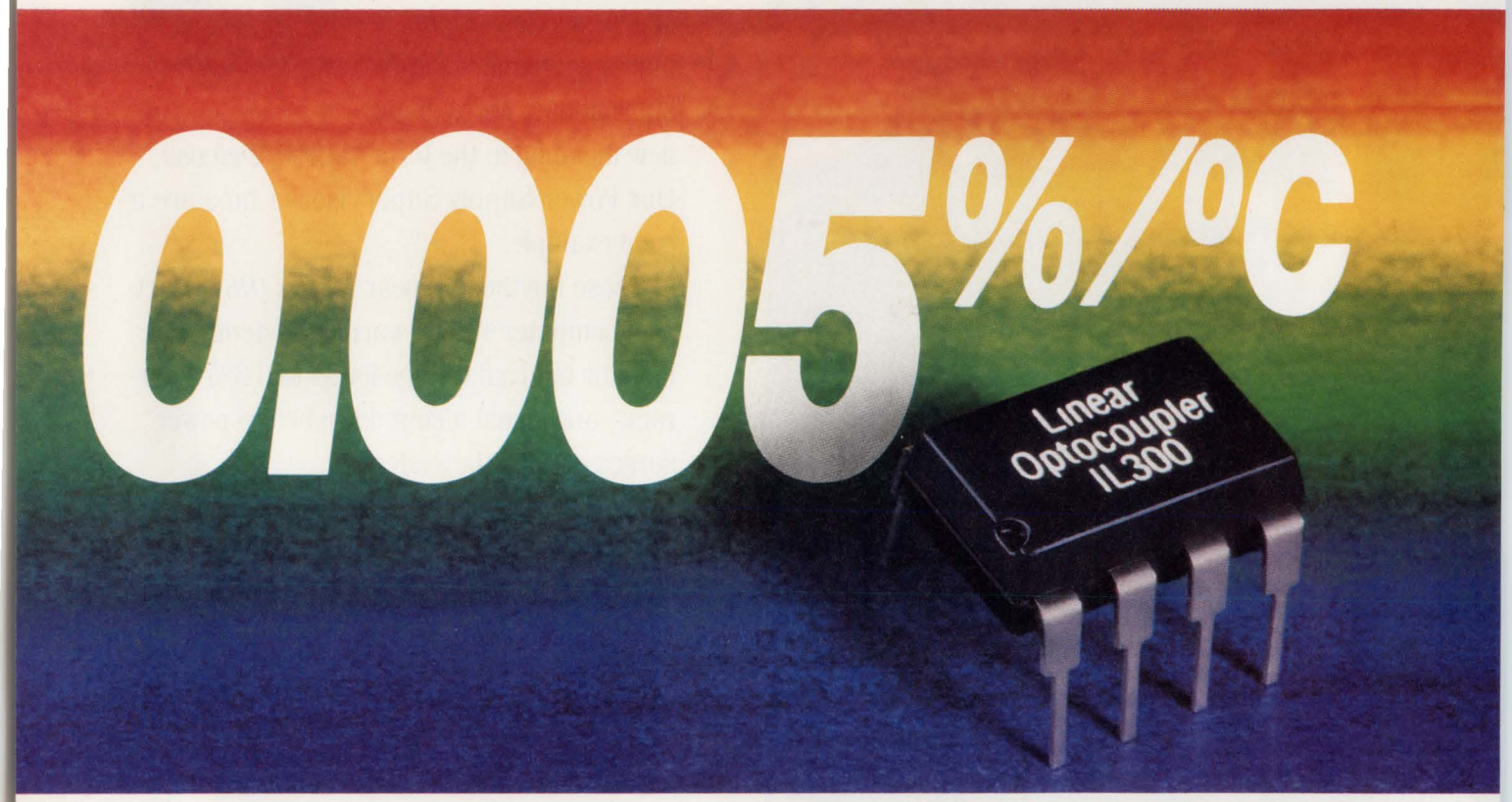
Raytheon Company, Semiconductor Division.
350 Ellis St. Mountain View, CA 94039.

CIRCLE 180

Raytheon

Where quality starts with fundamentals

SIEMENS



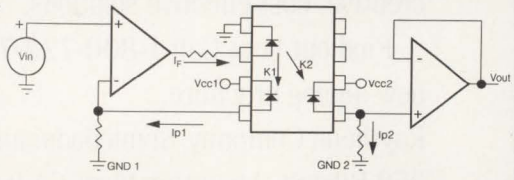
Gain Without Pain.

**New linear optocoupler—
Rx for stability.**

The phrase "linear optocoupler" has always been a contradiction in terms.

Until now.

Siemens new IL300 optocoupler uses a unique, optical feedback loop to neutralize gain and offset drift caused by temperature and LED degradation. The results will change the way you think about optocouplers: DC gain stability of ±0.005%/°C, ±0.01% servo linearity, a wide (>200KHz) bandwidth, power consumption under 15mw, and 7500 VAC Withstand Test Voltage.



The IL300's stable operational characteristics are achieved by controlling the AlGaAs IRLED output flux with an optical feedback circuit. The servo PIN photodiode captures a percentage of the flux and generates a signal that can be used to control the LED drive current. This compensates for the LED's inherent non-linear, time, and temperature characteristics. The IL300's stability and excellent isolation characteristics make it ideal for power supply regulation, medical sensor isolation, audio signal interfacing, digital telephone isolation, and many other applications.

It gives engineers a flexible, cost and power efficient component for applications in which optocouplers were never practical before.

For complete information on our new linear optocoupler, including application tips, call 408-725-3543.

Siemens Components, Inc.
Optoelectronics Division
19000 Homestead Road
Cupertino, CA 95014-1799

The IL300 linear optocoupler. Gain without pain.

Distributors: Advent Electronics, Inc., Hall-Mark, Insight Electronics, Marshall, Summit, Western Microtechnology.

Siemens
Practical Solutions By Design.

CIRCLE 131

TEAMWORK IS THE KEY TO CONCURRENT DESIGN

FUTURE DESIGN TEAMS WILL NEED ALL DISCIPLINES TO WORK IN PARALLEL.

BY LISA MALINIAK

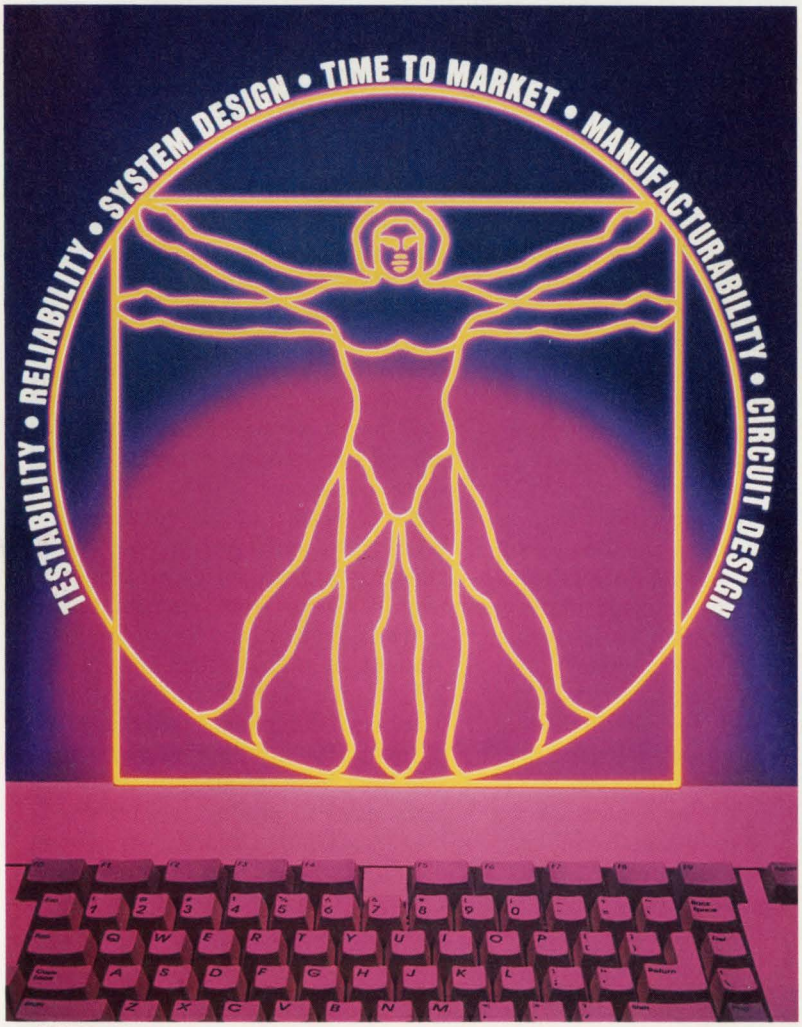


PHOTO: JOE DRIVAS

Increasing design complexity, intense competition, and tighter time-to-market deadlines will soon render the traditional "over-the-wall" operation of a design team obsolete. No longer can the engineering group complete its portion of the design before turning it over to the test group, and the test group finish its segment before the design reaches the manufacturing group, and so on. This serial approach has problems because the designers in the cycle's later stages don't have any input into the design until it's almost finished. In other words, each group hands off not only its portion of the design, but also a slew of problems.

Dataquest estimates that in a traditional serial design environment, the cost of making a change increases by an order of magnitude for each phase of the design cycle. For example, in a large manufacturing operation, a change that costs $1000 during design would cost $10,000 during testing.

To offset these headaches, the design teams of the 1990s and beyond will turn to a multidisciplinary, concurrent approach. In other words, all types of disciplines from every phase of product development will work together up front (concurrently) to define the product specifications *(Fig. 1)*. These disciplines include hardware design, software development, test, manufacturing, packaging, documentation, marketing, and even the customers themselves. The team will work together to make the right trade-offs right from the beginning, when mistakes are less costly and easy to fix *(Fig. 2)*.

This new team will require a change in the design environment, and adjustments in team management and the way engineers interact with each other. Some companies have already begun implementing the changes. In fact, there are successful concurrent, multidiscipline design teams in operation today *(see "A success story," p. 42)*. According to data from the National Institute of Standards and Technology, Thomas Group Inc., and the Institute for Defense Analyses, concurrent-engineering methodologies can reduce development time by 30 to 70%, result in 65 to 90% fewer engineering changes, reduce time to market by up to 90%, and result in quality improvement of 200 to 600%.

Engineers at Digital Equipment Corp., Marlboro, Mass., claim that three resources are needed to implement a multidiscipline, concurrent-engineering environment: human, computer, and methodology *(Fig. 3)*. Human resources are mainly the members of the project teams, but may also include other people inside and outside the enterprise who

will be consulted in the project development. Computer resources consist of the basic hardware, software, and systems that support the project team. Methodology resources are the formal techniques used in decision-making for product and process development. Although they may be supported by special software, methodologies mainly involve engineering philosophies and procedures.

The key to a successful design team is to emphasize *team*. "The biggest problem with design teams is that none of us were taught at home or in school to solve problems in a group environment," points out Dick Jensen, vice president of new business development at Applied Microsystems Corp., Redmond, Wash. "We don't have the mental tools to do group problem solving very well. It's foreign to most people." The most important challenge facing project managers in the future is getting engineers to work well in teams.

In addition to effective team performance, the engineers must be strong individuals and stand up for their own technology and their knowledge. For example, a hardware designer must spell out the hardware requirements very clearly. And the test engineer must specify exactly what's needed to test a design. In fact, all of the disciplines involved in a project affect both the requirement and design stages. They must all defend their own disciplines while still empathizing for the other disciplines.

Concurrent engineering is a different design process than most engineers are used to. Engineering teams must accept and understand the change that's required to move away from today's functionally defined organizations toward multidiscipline teams. "The kinds of problems that will be encountered

A SUCCESS STORY

Two years ago, the Department of Defense commissioned the Institute for Defense Analyses to report on claims of improved product quality at lower costs and shortened product development time through concurrent-engineering practices. The study's results, summarized in IDA report R-338, included many detailed cases of successful concurrent engineering.

One company that successfully implemented the change is IBM Corp., Poughkeepsie, N.Y. The Poughkeepsie mechanical-packaging group designs portions of the company's 3090 mainframes. Before the change, product development took place at the laboratory, and manufacturing operations were done at the plant.

The move to concurrent engineering was initiated by the product's design group. They were concerned about the high level of product-engineering support needed for design changes after the product was released to manufacturing. Many engineering modifications were occurring despite early manufacturing involvement in product development. The design process was serial, and communication between the laboratory and manufacturing group wasn't as effective as it could be.

The laboratory, working with the manufacturing plant, established a Total Concept Facility (TCF). A team of specialists from different disciplines concerned with designing, producing, and supporting a product could work together at the facility throughout all product design phases. The team consisted of about 70 people, mostly from development and manufacturing. Marketing, quality assurance, and field engineering were also represented.

With the TCF, teamwork is more continuous. Manufacturing representatives participate in the product's requirements definition and conceptual development. Team members use digital 3D models so that the manufacturing people can visualize the design and plan the assembly process.

The team established requirements by concurrently analyzing such factors as customer needs and lessons learned from IBM's and competitor's existing products. Requirements included firm targets for performance, cost, and schedule. Goals were set for ease of installation, reliability, availability, and serviceability. Performance objectives included a wide range of factors, such as part-count reduction and lower assembly times and cost. The desired functions were compared to the product's features, manufacturing capabilities, and cost estimates.

Although this requirement-establishment process was not new with TCF, it was done with greater precision and a greater level of detail than ever before. Working within the Total Concept Facility, the first two phases of design—requirements definition and conceptual design—consumed about 25% of the total effort.

The laboratory established a CAD-tool development group for computer support. Coordination between the tool developers and tool users was encouraged by having both parties report to the same manager.

As a result of the changes, there was a greater awareness of shared goals, successes, and problems. Efforts were coordinated more effectively. The reduced amount of engineering changes led to a significant decrease in the number of engineers supporting a product after production started. The time from the start of the design cycle to product announcement was diminished. Fewer people were needed for the design. The product direct-labor costs were reduced 50%, and the process time devoted to customizing products was cut by 65%.

when assembling multidiscipline design teams are problems that relate to the interaction of people on the team," states Robert Crawford, manufacturing and test manager at Sun Microsystems Inc., Milpitas, Calif. "Historically, most electronics companies are engineering driven, and design engineers by nature are egotistical and not very accommodating to other people's inputs. The team leader, therefore, must have good people skills."

This kind of change can't be made overnight. For the new concurrent process, management must alter its style and make a strong commitment to invoke change. Designers' current mind-sets must change from thinking about their own successes to thinking about the team's success. The entire team, including management, must believe in and support the project. Responsibility for the project, however, has to start at the bottom because every team member must carry his part of the project.

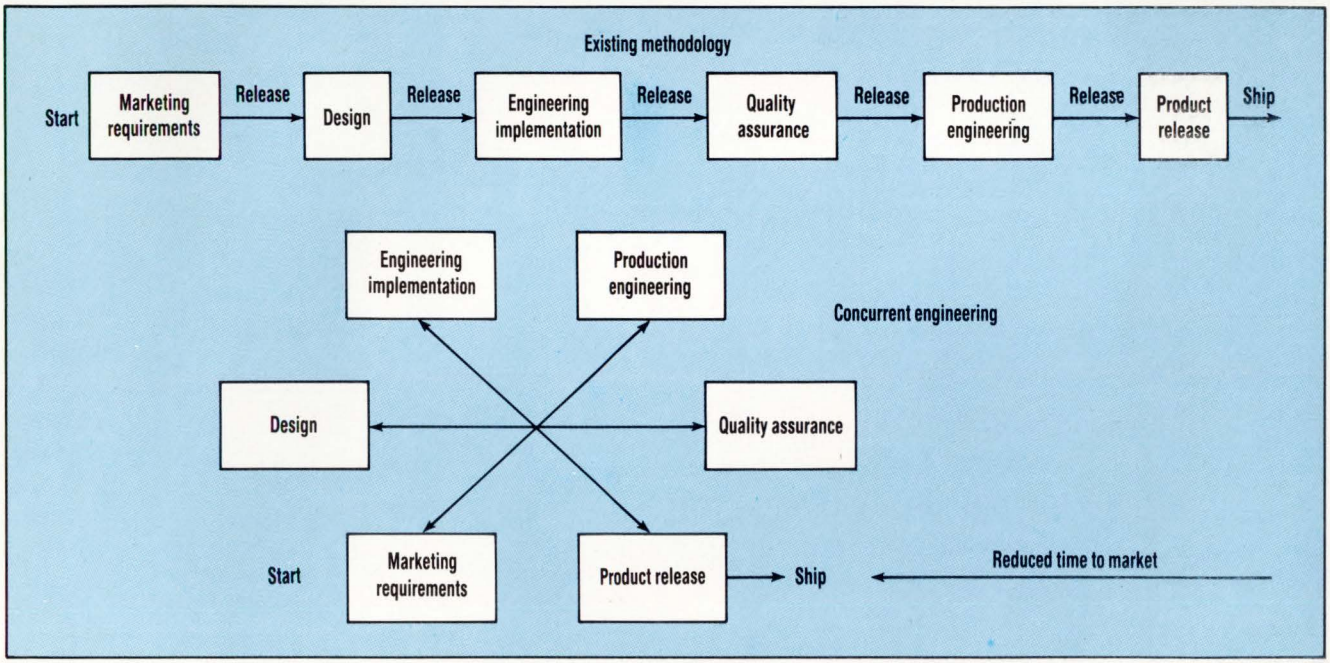
Management can motivate engineers to work well in teams by nurturing a team spirit that makes every member feel good with a job well done. Fostering cooperation and teamwork requires a different reward system. When projects are designed by discrete functional organizations, the rewards are based on the deliverables. For example, design engineering has to develop a hardware design. This reward system is based on creativity and innovation, but not necessarily that the design is testable. That's the test engineer's function; the design engineers aren't recognized for making a design testable.

In the move to a multifunctional team, the rewards can no longer be focused on individual functional organizations. The rewards must concentrate more on the results of that entire team: delivering a product on time within the testability, cost, and quality objectives, as well as all of the broader constraints that were put on the system. The team as a whole must be recognized for a job well done. This new system asks people to expand their focus so they make the correct trade-offs between their part of the design for the overall design's well-being.

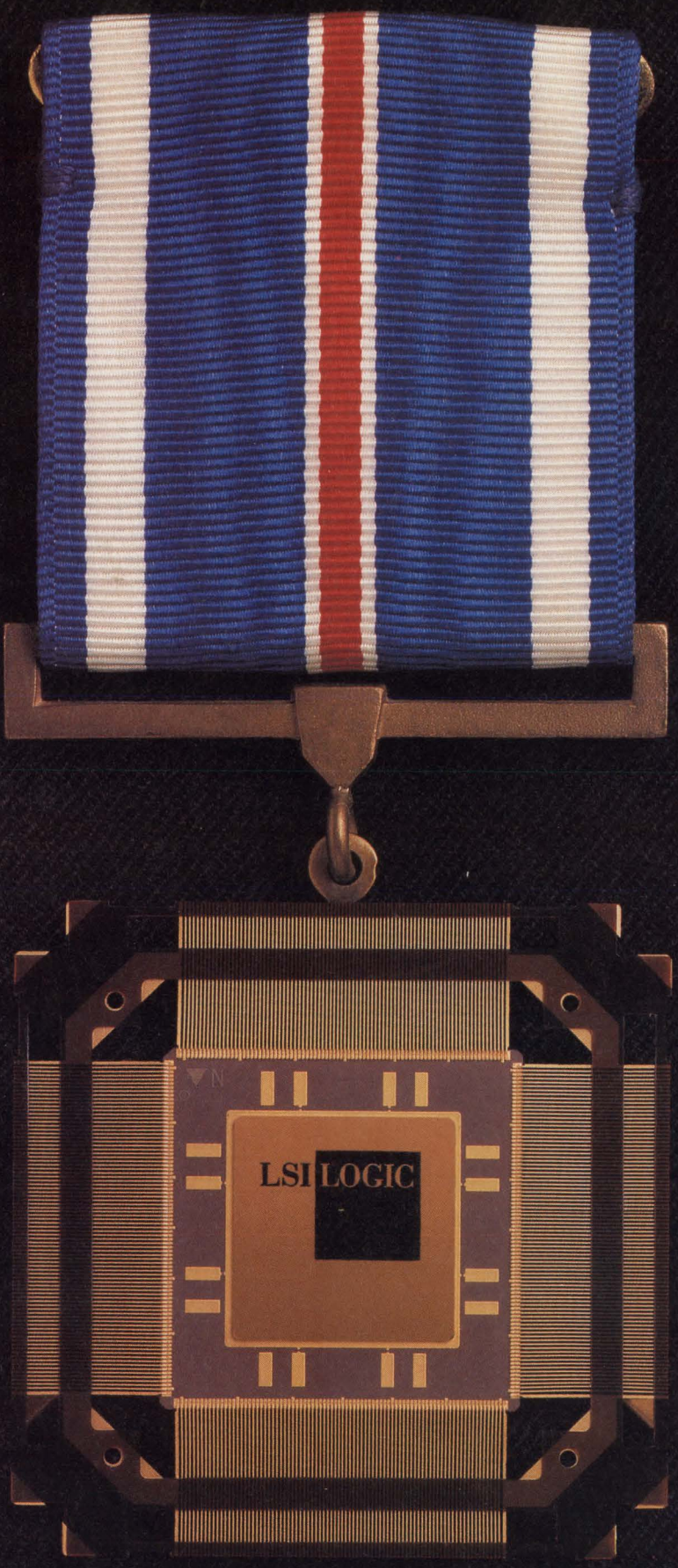
Lines that once divided areas of responsibility must become less rigid. The success of one team member and the failure of another can't be tolerated for a concurrent design team to work. It must be understood by each team member that if one discipline fails, then the development project fails.

The team leader will need to cross-train engineers. For example, the design engineer may have to be taken over to the manufacturing operation and shown the parts that failed because he didn't adhere to the design-for-testability or design-for-manufacturability techniques. Likewise, the manufacturing person will need to be introduced to the engineering department to understand the pressures associated with getting a product design out. In addition, he'll need to know the complexities of using design tools. The design-team leader must create an environment that promotes respect and appreciation of each individual's ability. And each individual must understand all of the requirements of bringing a product to market.

In a serial design process, each engineering discipline has its own vocabulary, priori-



1. Most design teams today use a serial methodology. In the future design environments will use concurrent engineering, which is a group method of product development. The major benefit of concurrent engineering is reduced time to market.


LSI LOGIC

WE'RE STILL ON ACTIVE DUTY.

While many companies have deserted the military ASIC business, our commitment hasn't changed.

So if you're looking for a long term strategic partner, stand at ease.

LSI Logic has earned its stripes by successfully completing more military gate array designs than all other ASIC manufacturers combined. Led by a dedicated Military Aerospace group, we're ready when you are to make those designs a production reality.

At your command are submicron HCMOS ASICs, RISC microprocessors and DSP products which allow system-scale integration second to none.

Our commitment continues as we ready the Silicon 1076, a VHDL system development environment capable of taking you from the highest levels of abstraction right through to actual silicon. Our military arsenal already consists of design software which ensures a first-time hit rate, dedicated manufacturing, radiation hardened processes and package development. Whether your program need is for one design or 30, we've got the capability to hit your milestone targets.

Next time you're looking for a technology upgrade, or need fast time-to-market, enlist the world's leader in military ASICs and RISC microprocessors. LSI Logic.

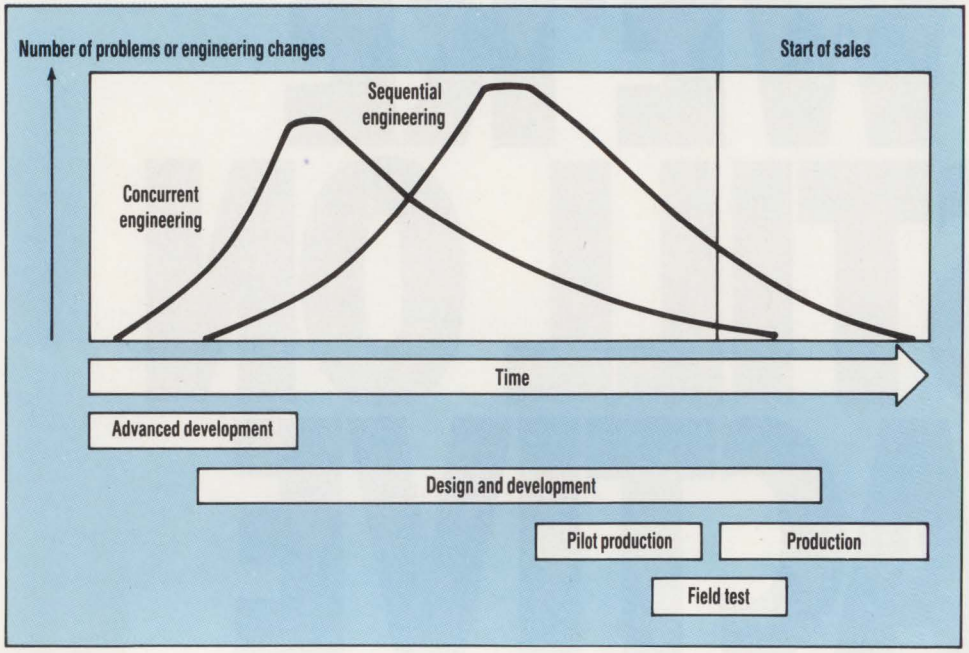
Call us at 1-800-451-2742, or write LSI Logic, 1551 McCarthy Blvd., MS D102, Milpitas, CA 95035.

We'll be there. Because we're always on active duty.

LSI LOGIC®

ACROSS THE BOARD

CIRCLE 105



2. This graph shows the number of engineering changes plotted against time for both concurrent and sequential engineering techniques.

ties, and purpose for doing a design. Proper management is critical to bring these disciplines together into a concurrent environment. Management must help the engineers obtain a commonality between vocabulary, priorities, and purposes in an effort to create a design. It must have a vision, and define what the group is going to accomplish as a team.

Management must keep everybody on schedule. It must also ensure that one team member doesn't sit idle because of dependencies (on other team members or data being produced by other team members). A list of critical-path and noncritical-path jobs will help fill the gaps that are bound to occur should one member be delayed. The importance of concurrency is reviewing progress and reviewing dependencies against the requirements. The requirements must be updated as the team discovers new dependencies.

The emergence of concurrent teams will introduce new disciplines into the design cycle, and will merge and change other ones. For example, according to Don Carter, corporate

technical director for Mentor Graphics Corp., Beaverton, Ore., the discipline that will become most important is to understand the customers' requirements and have everyone participate in defining the product specifications. In addition, the team will need to always correlate its work back to the customers' requirements. Implementing concurrent engineering without capturing the customers' requirements is useless, because the team will produce a better, cheaper product that nobody can use if it doesn't meet the customers' needs.

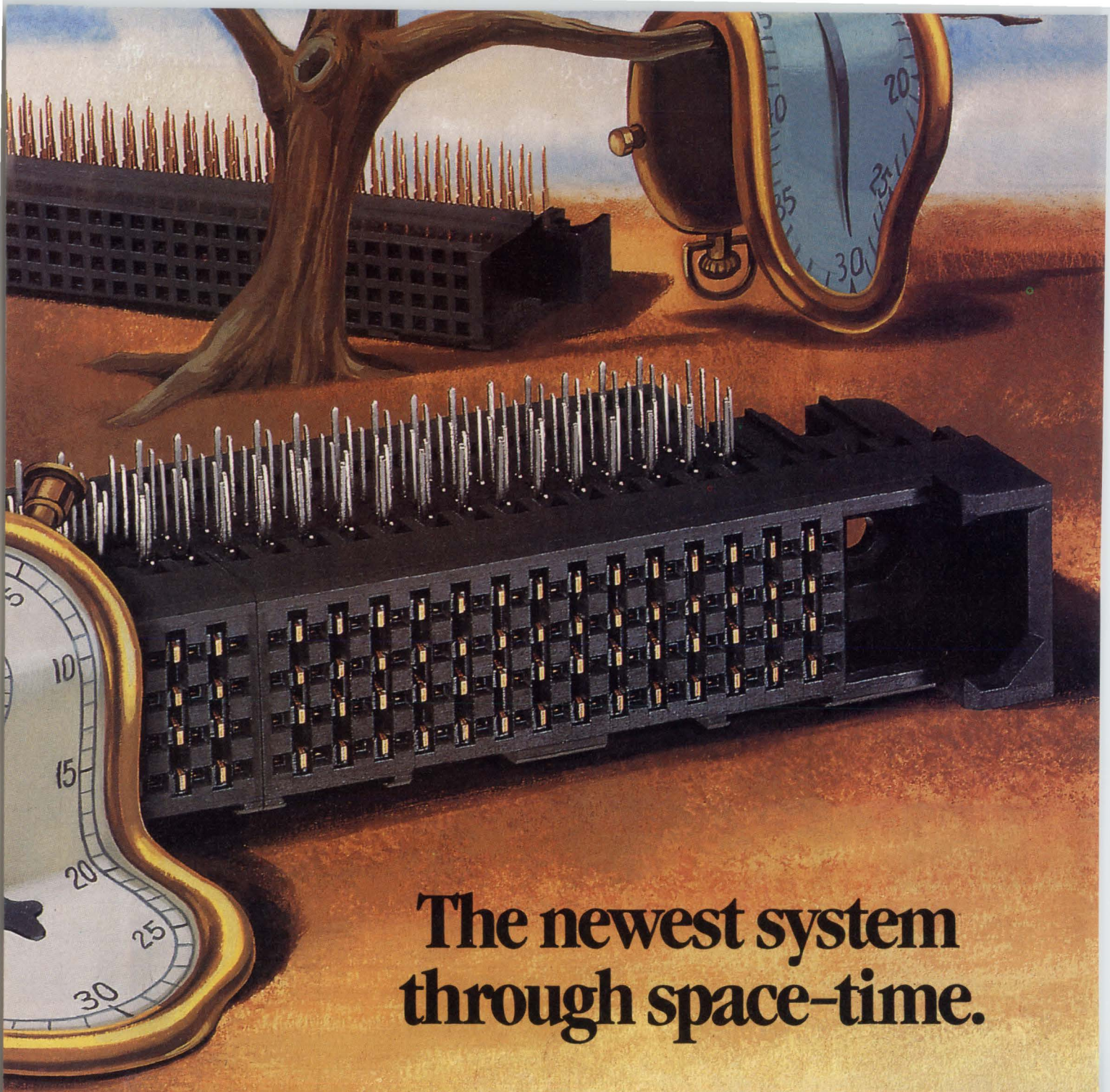
The design process will start with capturing requirements from the customer in a method that's easy to communicate and easy to refer back to as more detailed design is done. In fact, the longest period of time will be spent defining the customers' requirements and the most changes during the design cycle will be caused by changes in requirements. "Today's design teams often don't have an effective, efficient way of capturing, recording, and communicating customer requirements," states Peter Hoogerhuis, director of consulting services for Mentor Graphics Corp., Beaverton, Ore. "But if the team does have solid specifications to build a product on, there are tools in place to build that product."

The emergence of concurrent teams will introduce new disciplines into the design cycle, and will merge and change existing disciplines.

Another important discipline that will appear is workflow management. Carter states that to be successful with concurrent engineering, design teams will need to marry a process with tools. The new workflow-management discipline will be responsible for prescribing a successful design process with the available tools to accomplish effective concurrent product development.

In addition to new emerging disciplines, old disciplines will change. For example, test engineers spend much time making a design testable, and manufacturing engineers spend lots of time making sure it can be fabricated. The tasks of those engineers will change as concurrent engineering enters the picture. Test engineers will consider testability at the beginning of the project instead of working with what's been done. They'll be responsible for inserting scan parts and elements, not just for writing test programs. In addition, test engineers will be more supportive of the engineering process by creating tools that apply their knowledge to make the design more testable.

Also, if manufacturing is involved in the



The newest system through space-time.

The AMP Z-Pack Interconnection System is a scalable, high-density board-to-board/cable-to-board system for nanosecond and subnanosecond applications, in 2 mm and .100" grid sizes to accommodate global packaging requirements.

The fastest members use stripline technology, introducing reference planes between pin columns to retain maximum pin counts in a controlled impedance interface.

The design advantages are immediate: Z-Pack .100" stripline connectors accommodate 250 ps edge rates with no sacrifice in signal density: four rows = 40 lines per inch.

High-temp materials for SMT compatibility.

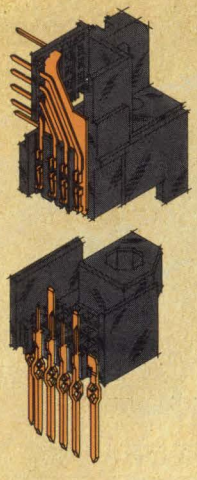
Twin-beam receptacles, 2 mm wipe.

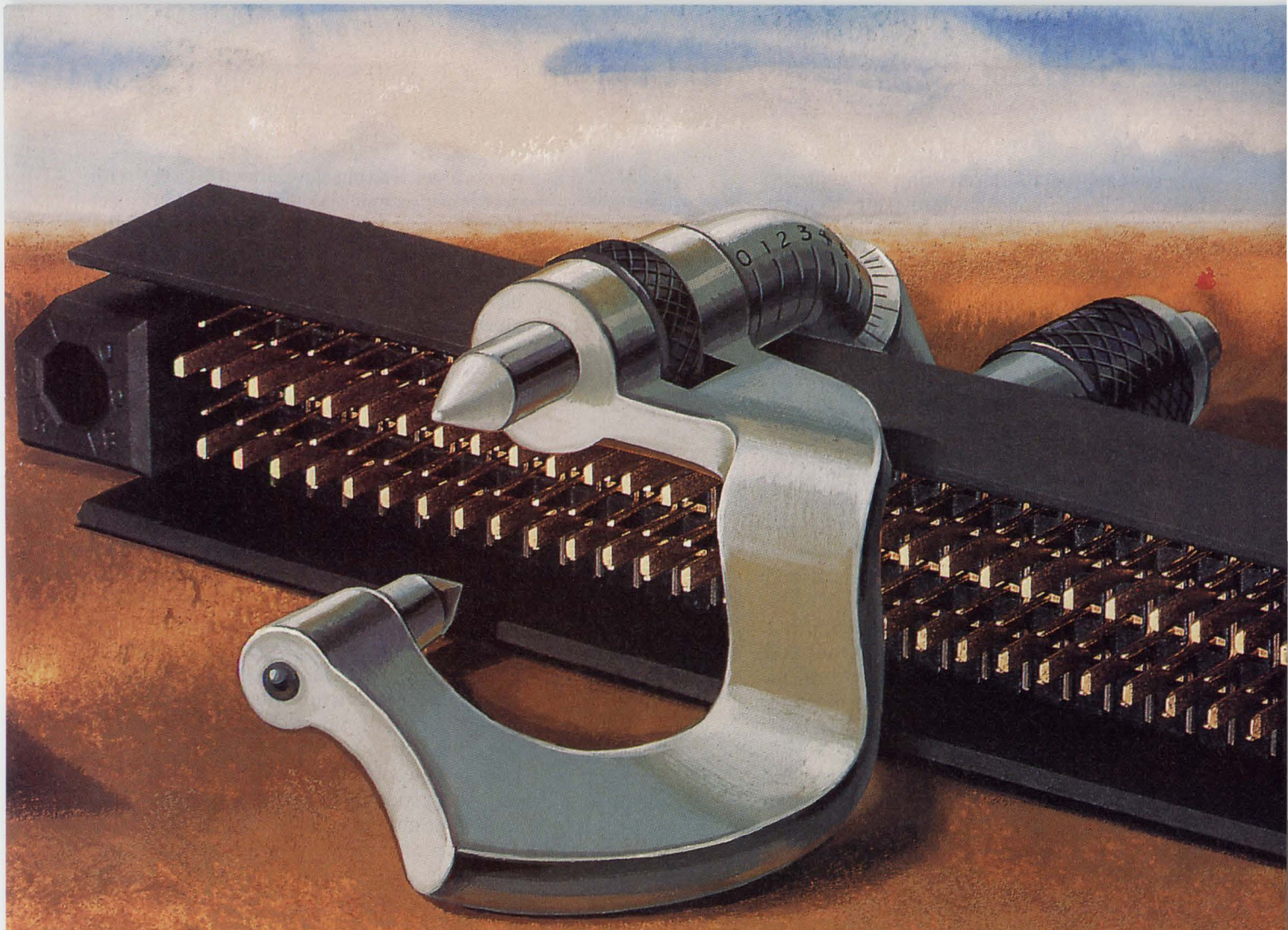
Sequenced mating up to four levels.

2 mm versions accommodate two traces between lands.

Stripline versions isolate pin columns for 50 ohm interface.

Reliable compliant-pin versions available.





Space: 40 lines/inch. Time: 250 ps.

2 mm stripline versions (500 ps) require just one pin row for reference, and open pin field versions in both centerlines handle 1.8 ns rise-times with a 3:1 signal/ground ratio. Standard spacing minimizes board redesign, and system modules stack end-to-end with no loss of signal positions, offering true form/performance scalability in Futurebus-like applications.

For more information on the Z-Pack Interconnection System, call our Product Information Center at 1-800-522-6752. AMP Incorporated, Harrisburg, PA 17105-3608.

For advanced design and manufacturing of complete characterized multilayer backplane systems, contact AMP Packaging Systems, Inc., P.O. Box 9044, Austin, Texas 78766, (512) 244-5100.

THIS IS AMP TODAY. **AMP**

CIRCLE 83

process early on, its engineering role changes because design concerns are addressed up front. Today, the design is typically handed off to manufacturing engineering, who develop a process for making the product. With concurrent engineering, manufacturing engineering works much closer with design engineering up front *(Fig. 4)*. That way, when the design is handed to manufacturing engineering, it doesn't have to be re-engineered. Those people who previously developed breadboards may start creating accurate libraries so that a design can be simulated accurately and a breadboard won't be needed.

Future concurrent design teams will find that the amount of concurrency in the design process is limited by the team's tasks and their functions. For instance, if an engineer is working on a digital logic simulation, other team members can't do all of the layout and ship that layout to manufacturing until its wire lengths are back-annotated for more accurate simulation. Accurate simulation verifies that the layout is correct.

The limits of concurrency comprise one reason why workflow management is key to the whole process. The workflow-management system defines how much concurrency there will be based on the tasks and functions that need to occur, and is therefore technology dependent. For example, building a pc board with ASICs or with standard logic will change the amount of concurrency that can take place.

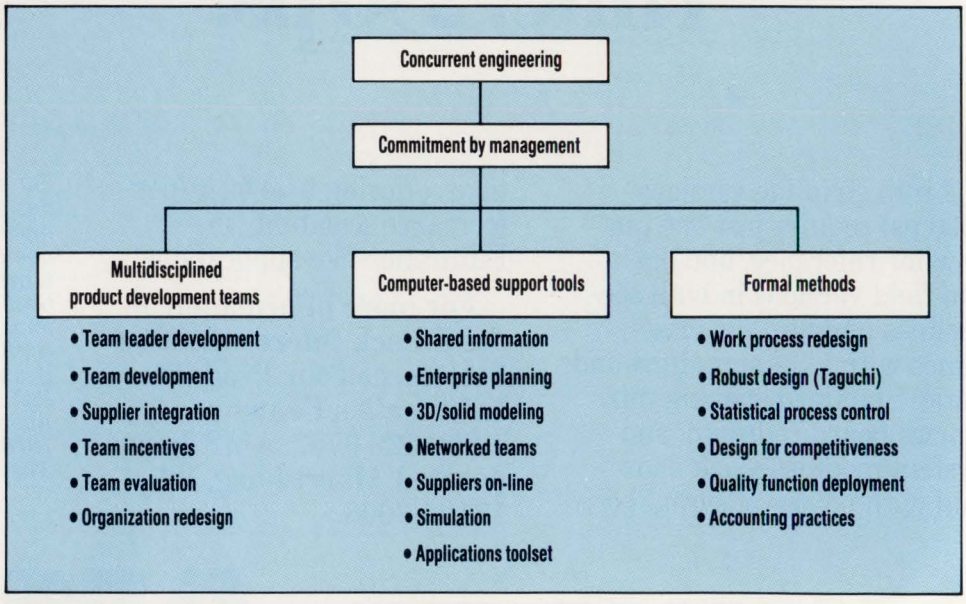
In addition to the design-team management changes, engineers will need to alter their own design processes and how they interact with other engineers. For instance, to ensure a successful design, it's important for the whole team to decide from the start what the critical factors are. As an example, a design team may decide that the most important factor for a product is testability. Teams must decide how they're going to stress such elements as cost, functionality, and time-to-market. And if they haven't nailed down the design philosophy, management won't be able to resolve the disputes that will arise between the disciplines.

Working together, each discipline will very carefully determine all of the product's requirements. They will also set the trade-off philosophy at this requirements level. Setting the trade-offs early, with everyone present, makes for a smooth project flow, because everybody involved knows why the trade-offs are being made. For instance, if a custom chip was being built for a space vehicle that was going to Mars, the test engineers may get 60% or 70% of the chip real estate to use, because the highest priority is reliability. These types of decisions must be made at the requirements level. In fact, requirements analysis will emerge as a new discipline in future design teams.

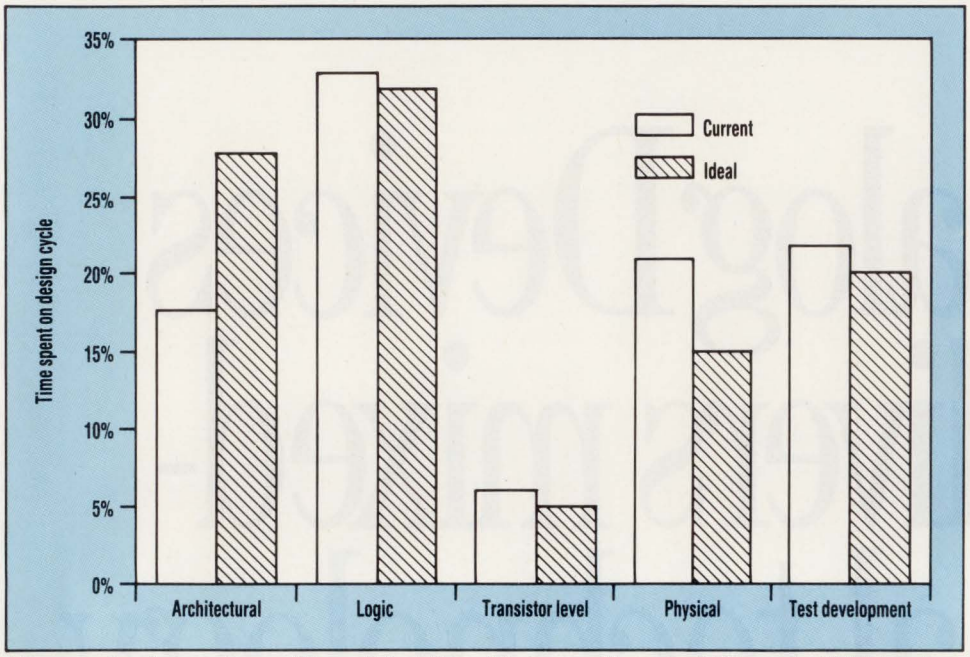
Decision Arbitration

Future teams will need to deal with decision arbitration much more than they do today. This arbitration may be done with a decision-making and rationale-capture system—an electronic forum. With the forum, engineers can electronically input information regarding any topic that's being discussed. If one engineer asks a question, every other engineer can supply input. And all of the inputs are captured, so that decision arbitration can take into account each opinion. In addition, any team member can know the rationale that went into past decisions because everything is recorded electronically. According to Dick Jensen at Applied Microsystems Corp., electronic forums are emerging, but won't be mainstream for five to ten years. One reason is that the software alone can cost up to half a million dollars.

All people-oriented changes should be accompanied by changes in the design environment to accommodate all disciplines working together. For instance, a company may assemble a multidiscipline concurrent-engineering team with whatever tools and hardware it has just by adding a problem-solving

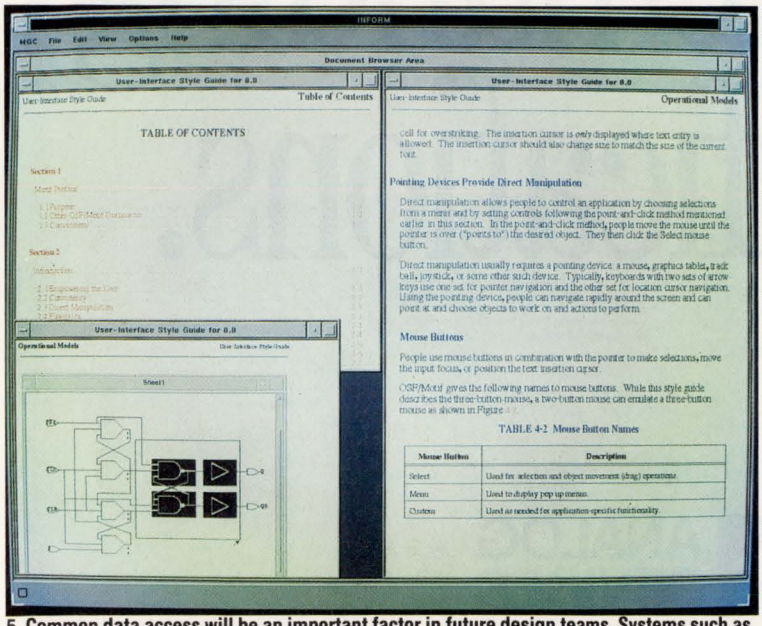


3. Management's commitment to concurrent engineering is the first and most important thing needed to make the process work. Also needed are human, computer, and methodology resources.



4. Concurrent engineering teams will have all disciplines of the team working up front. This graph, which is based on Dataquest information, shows that ideally, engineers want to spend more time working early in the design cycle at the architectural level. Consequently, they want to spend less time later on in every other design phase.

meeting room. However, the team may soon complain about the time wasted going to and from the meeting rooms and the time required to copy data. Therefore, a network is needed. The next step would be to add capabilities on that network with several multitasking Unix stations. And then each discipline must have a set of tools that shares common data. Finally, the team will require common data control and common access to that data control *(Fig. 5)*.



5. Common data access will be an important factor in future design teams. Systems such as Mentor Graphics' Bold on-line information system, pictured above, offer fast electronic access to data for all design-team members.

Most design tools needed for this new environment now exist. Current tools can be used for concurrent engineering, even though they may not work together and aren't optimized for concurrent processes, because management can use internal processes as a bridge. What's needed is improvements in frameworks, databases, data management, control systems, and measurement systems.

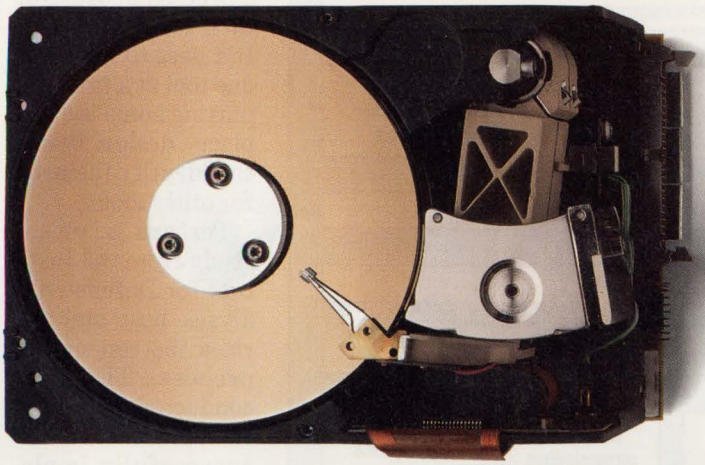
To continually improve the design process, teams should determine a procedure for measuring their methods. No matter what type of engineering is performed, there's a way to measure the process. For example, hardware engineers may measure the number of times a schematic was updated. In fact, establishing the functions and items to measure and how to measure them should be one decision made up front.

Processes should be measured so that the team can locate efficiencies and inefficiencies. Consequently, when the team starts a concurrent project, it will know where to focus its efforts. For instance, by measuring data-access times, the team may find out that the database management system didn't work up to standards. The engineers can then go directly to the database-management-system vendor and ask them to rework the product. If the vendor isn't responsive, the engineers can seek another vendor. Building a successful design team is an iterative process. However, if the team engineers don't measure anything, they won't know what processes to fix. The process matures each time it's repeated.

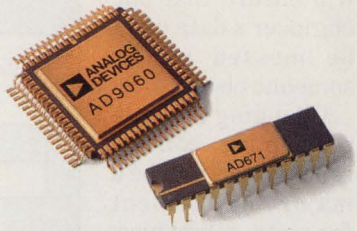
In future concurrent-engineering environments, frameworks will be like operating systems: Something designers expect to have so that processes start working *(Fig. 6)*. Frameworks help the environment by providing constant access to common data, and by bringing a consistency of invocation. Dick Jensen forecasts that "frameworks will be a standard part of operating systems within the next three to four years."

With each engineer sharing ideas and data, one engineer may not understand another's data. If that happens, then the design process isn't meeting the project's overall requirements. The engineering data should be useful

Faster.

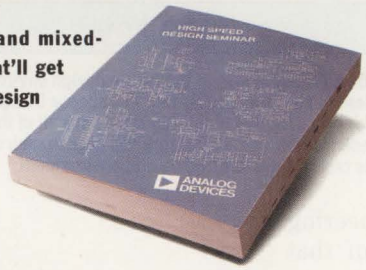


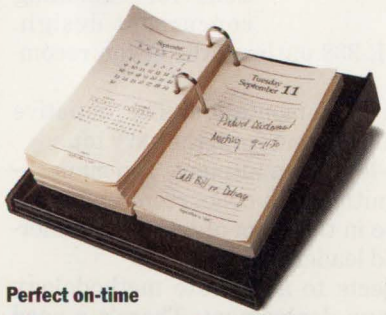
In the disk drive market, you've got to be fast – in both performance and time-to-market. That's why seven of the top 10 disk manufacturers rely on Analog Devices for mixed-signal components.



AD9060 & AD671 – The fastest 10-bit and 12-bit monolithic A/D converters, respectively. The AD9060 guarantees encode rates up to 75 MSPS for unparalleled dynamic performance. The AD671 is twice as fast as any other 12-bit monolithic, converting in under 0.5 μs, thanks to our high-speed mixed-signal ABCMOS process.

Tap into 25 years of experience at our high-speed and mixed-signal design seminars. You'll learn new techniques that'll get your applications to work more quickly, and you'll get design manuals that put all this information right at your fingertips.





AD9712 – The only 12-bit, 100 MHz D/A converter on the market. Ideal for high-speed video and direct digital synthesis, its low glitch and low harmonics combine to deliver a spectrally pure output waveform.

Perfect on-time delivery – it's our goal and at 97% we're getting close, thanks to our continuous improvement process based on Total Quality Management. Over 150 TQM teams make the customer and quality improvement the focus of our entire organization. A focus that gets translated into not just catchy slogans, but real action.

Our Spectrum CAD Tool is 100 times faster than traditional SPICE programs, so it makes quick work of mixed-signal ASIC design cycle time.

ADSP-2101 – Talk about fast – this DSP microcomputer executes a 1024-point FFT in only 2.26 ms. That's faster than other DSPs that operate at almost twice the clock rate. And since our entire ADSP-2100 family is code compatible, your code will run fast on all of our DSPs.

Today, Analog Devices offers more high-performance mixed-signal components than anyone else. And we get them to you fast. So if you want mixed-signal ICs that'll help you design faster performing products, from a company that'll help you get your product to market faster, call us at 1-800-262-5643.

ANALOG DEVICES

CIRCLE 165

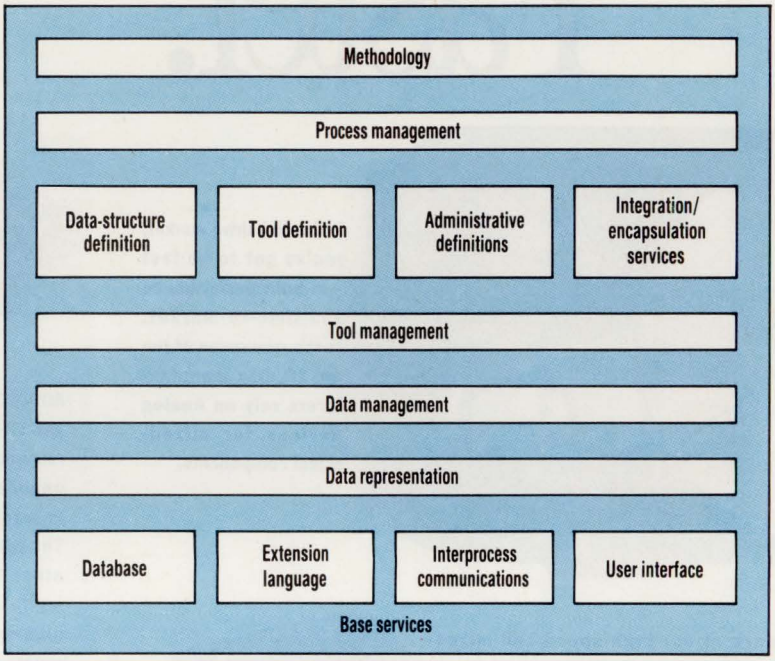
to the whole design team, and every engineer must be able to get at it. A good data-control system will ensure that one engineer's data can't be messed up by someone else.

Changing to a multidiscipline, concurrent process will be a major adjustment for many companies. And whenever there's change, usually something is lost for something else to be gained. Time and money are two factors that typically lose out in an effort to gain productivity. For instance, money will be spent differently to convert from a serial to a parallel process. Instead of spreading money equally from engineering to manufacturing to service, much of that capital will have to be used up front.

There is risk in retraining the work force. While training for a new process, engineers must still do their old job to continue current product development. This can put some strain on an organization that's trying to learn and incorporate these new methodologies.

Although it's disrupting, this transition doesn't happen overnight. It can be implemented through pilot projects so that the team can build some experience and confidence in the new methodologies. The company can then gradually introduce the new methodologies more broadly. Concurrent engineering will not be introduced into a continuing development, but in new development cycles. The success of pioneer groups, both in operational improvements and enthusiasm of team members, will help set the stage for concurrent engineering in other parts of the company. When approached in that manner, the risk is significantly reduced.

A good technique is to add one discipline at a time. For example, a team could start off by having hardware and software engineers working together. On the next project, test engineering could be brought in, then manufacturing, and so on. After slowly evolving the process, the team will eventually become totally concurrent.



6. Frameworks will be an integral part of the future design environments. According to Tony Zingale, vice president of corporate marketing at Cadence Design Systems Inc., San Jose, Calif., frameworks for concurrent engineering must have all of the components depicted in this model. With these frameworks, customers can choose their design methodology and process management to create a customized design environment.

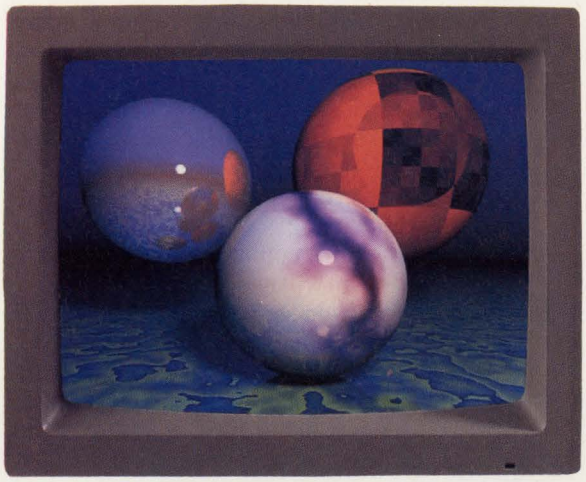
Automated tools don't improve a process immediately. In fact, they slow down a process because of their learning curve. It's best to add only one tool at a time. By putting some tools in place, design teams can identify the need for other tools.

Perhaps a recent study from the Institute for Defense Analyses best summarizes the concurrent process. The IDA conducted a study of companies that are successfully implementing concurrent-engineering techniques. The study's results were used to make recommendations for exploiting concurrent design. IDA report R-338 outlined the seven recommendations:

1. Top-down implementation: The initiative for change must come from the very top.
2. Executive-level commitment: Top management's commitment to concurrent engineering should be in the form of learning, understanding, and leadership.
3. Pilot projects to accelerate methodology and technology deployment: There's a need to select and conduct demonstration programs.
4. Build onto existing programs: Take advantage of the progress made by various existing programs and efforts that relate to concurrent engineering.
5. Education and training: Education is essential, and must start at the top level of management.
6. Method and technology development: A number of methods and technologies have evolved that support the application of concurrent engineering.
7. Identify and reduce barriers and inhibitors: By applying concurrent engineering methods, many barriers and inhibitors stand in the way.□

HOW VALUABLE?	CIRCLE
HIGHLY	538
MODERATELY	539
SLIGHTLY	540

Better.



Picture this – a PC monitor that offers the same color and clarity as a high-end engineering workstation costing as much as 20 times more. Our pin-compatible RAM-DAC is literally redefining the low end of the PC monitor market.

Marball. Original image courtesy of University of California, Davis.

'Try, try again' is a costly way for manufacturers to find the best design solution. So to help our customers find answers to tricky problems the first time around, technical application engineers are just a phone call away. In some instances, they're even located right on the customer's premises.

After analyzing semiconductor suppliers, many of the leading oscilloscope and spectrum analyzer manufacturers chose Analog Devices for their mixed-signal components. One reason is our ability to deliver high performance at high levels of integration – for example, our AD640, which replaces a chain of discrete log-amps for higher accuracy.

With our motion control ICs, several major aircraft companies are staying right on course. High reliability and accuracy are hallmarks of our 2S80, AD598 and the rest of our nearly 400 defense-qualified products.

ADSP-2111 – Better integration on the best architecture in the industry. Adds an 8/16-bit host port to the two serial ports, timer, hardware companding and memory already on the ADSP-2101. And like all our DSPs, it's got fast, flexible arithmetic, wide dynamic range and a single cycle fetch of two operands (on- or off-chip). Plus it's code-compatible with the rest of our DSP family, so what's written today will be useful tomorrow.

ADV7141 – Our new Continuous Edge Graphics™ RAM-DAC gives users of standard low-end color monitors better graphics on their PCs. Graphics that are virtually the same as those produced on expensive engineering and scientific workstations. It does this by eliminating jagged edges, providing photo-realistic colors and shading, and displaying text comparable to a 300-dpi laser printer.

AD75028 – This custom ASIC passes the test for a top automatic test equipment manufacturer. Serving the function of 21 separate 12- and 8-bit D/A converters and providing on-chip static RAM, it also has seven channels of level setting (other monolithics only have four), and can automatically remove gain and offset errors.

Today, Analog Devices offers a better line of high-performance mixed-signal components than anyone else. And no one has a better record for reliability, or more experience in analog, DSP and mixed-signal ICs. If you want mixed-signal components that'll help you design better products, the best thing to do is to call us at 1-800-262-5643.

Continuous Edge Graphics is a trademark of Edsun Laboratories.

ANALOG DEVICES

DESIGN TEAMS EVOLVE TO FACE TESTABILITY

MORE TEAMWORK AND NEW TOOLS WILL HELP MEET THE CHALLENGE PRESENTED BY COMPLEX SYSTEMS.

BY JOHN NOVELLINO

The extraordinary progress in semiconductor technology in recent years has given design engineers outstanding component capabilities to choose from in speed and integration levels. These same capabilities, however, have also brought designers a new challenge. It wasn't long ago that few designers considered the problems involved in testing their handiwork. Now testability is a major factor in the success or failure of new designs. And it must be considered not only by test and manufacturing engineers, but also by designers.

The first designers to feel the constraints of testability problems were those working at the leading edge. At today's top speeds and densities—whether on ICs or pc boards—design-for-testability (DFT) techniques are mandatory to ensure thorough and economical testing. But more and more designers will feel the pinch as today's leading edge becomes tomorrow's mainstream capabilities. Even designers working at slower speeds and lower integration levels will feel the pressure of DFT considerations as companies come to understand the benefits of DFT.

Ensuring testability will require many changes in the way the design team operates. The makeup of the team will change, with test engineers included from the beginning of the effort. The design process itself will change as the team uses a much more structured approach than in the past. Conceptually, synchronous logic and hierarchical designs will be more common. To make these changes the team will need new tools, not just upgraded aids from the past but tools reflecting the new DFT philosophy.

The value of DFT techniques jumps dramatically as design complexity increases. This is because as design complexity increases, the cost of test goes up at a much faster rate, sometimes exponentially. And there's no doubt that design complexity is rising rapidly. In the past, most resources required for product development went into the design effort. Today, test development eats up nearly half the resources. In the future, test development will claim the majority share *(Fig. 1)*.

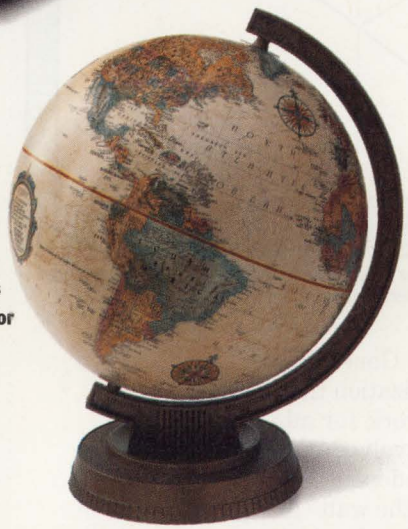
The direct cost of test is only part of the problem. It can take from six months to a year to develop an effective test program to ensure acceptable product quality. In a highly competitive environment, that kind of delay can stretch the time to market to a disastrous level. The alternative—inadequate test coverage—can similarly ruin a product's chances for success.

Although no hard rules exist, there are some guidelines that indicate when the effort needed for DFT is beneficial, or even essential. Frank Binnendyk, marketing manager for test-related products at Mentor Graphics, Beaverton, Ore., says that in the ASIC arena, some thresholds of pain are associated with size. "Generally, the pain starts to be felt in the 7000- to 10,000-gate ASIC design, where the cost and the time to develop an effective set of test vectors is the major part of the design's cost," he states. "That's where a lot of companies are finding themselves."

The next threshold comes at about 32,000 to 40,000 gates, where more advanced designers are at today. At this level, says Binnendyk, "you realize very quickly that unless you use some structured DFT techniques, you cannot effectively develop a comprehensive set of test vectors in a reasonable amount of time. It's an incredible job and you really have to automate the process." Once the IC hits about 80,000 gates, designers must "sign up

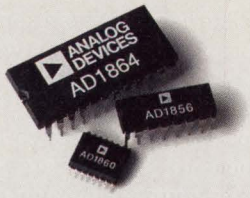
Cheaper.

More gadgets for less money, and make it work better – that's the only way to survive in consumer electronics, the most competitive market there is. That's why three of the top five Japanese electronics firms rely on us to meet their mixed-signal needs in applications ranging from CD players to video cameras.



We're far from your local component boutique. Over half of our $540 million in revenues comes from international sales. And with manufacturing and stocking facilities on just about every continent, getting products to you quickly is a snap. Plus multiple manufacturing facilities allow us to take advantage of the right talent and processes for the job at hand.

With billions of dollars in annual sales at stake, the video game market is anything but child's play. One leader in this market found that with our DSP they could create more realistic and interactive games. As a result, they're driving away with a bigger share of the market.



SOUNDPORT DACs – We've made these DACs cost-efficient by making them complete with output amplifier, reference and digital logic interface. Perfect for high-fidelity digital audio and multi-media applications, these mixed-signal ICs achieve SNRs as high as 108 dB and THDs as low as 0.0025%.

AD712 – If you're working in professional audio and compact disc applications, you'll like the sound of this – an IC that combines two high-performance op amps in one compact package. You get low offset voltage and low input bias currents coupled with superb transient response, ambience, clarity and dynamic range.

ADSP-2105 – High performance DSP at an incredibly low price. So low, in fact, you can now consider DSP in a host of new applications. And since it's pin-compatible with the ADSP-2101, and code-compatible with all of our other DSP processors, upgrading is easy and inexpensive.

Today, Analog Devices offers more cost-effective solutions to your high-performance mixed-signal needs than anyone else. Solutions that are surprisingly affordable, whether they're available off the shelf or developed for a specific application. To find out more about how we can help you develop products more efficiently, or for a free copy of our recent Mixed-Signal Technology white paper, call us at 1-800-262-5643.

ANALOG DEVICES

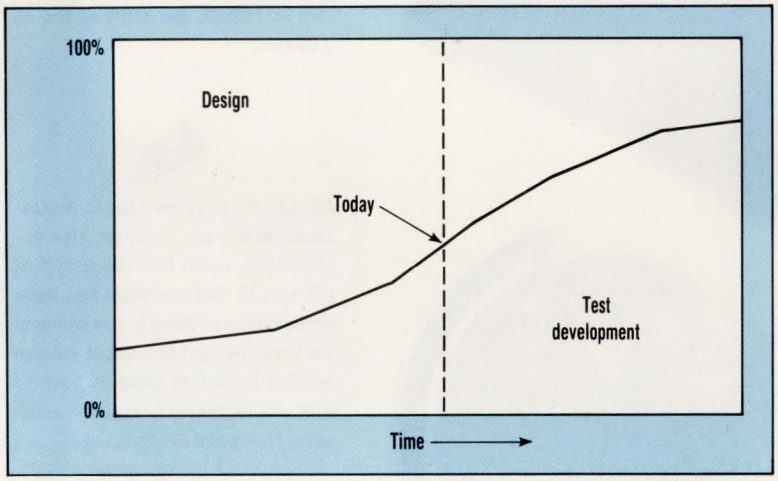
Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106. Headquarters: (617) 329-4700. Offices and applications support available worldwide.

CIRCLE 167

whole hog," he says, using full scan and all available DFT methods to their maximum.

DFT efforts pay off throughout the entire product life cycle. For instance, Vertex Semiconductors, San Jose, Calif., uses a boundary-scan technique that helps during wafer sorting. The company can sort the chips with 99% coverage by accessing only 20 pins on the die, according to Stephen McMinn, vice president of sales and marketing. "If you look at that in terms of not having to deal with a 300-pin probe card, which costs $5000 or $10,000 and creates alignment problems, the manufacturing efficiencies that a company like ours gets are pretty significant," says McMinn.

The move toward increased use of DFT techniques is a slow, evolving process. Not all companies introducing DFT in their design process do so at the same speed. Generally, the first step comes with the realization that the traditional process doesn't work for advanced designs. That procedure involves a designer or design team working independently, then tossing the design "over the wall" to a test engineer, who must then develop test procedures on his own.



1. As test development efforts consume a larger share of the total resources needed for product development, design-for-testability (DFT) techniques take on greater importance.

The next natural step is to include the test engineer in the design-review process prior to releasing the project to manufacturing. The test engineer then evaluates the design specifically for testability. "That seems to help some," says Binnendyk, "because before it's thrown over the wall, at least they give you a chance to catch it. The downside is that most design reviews occur after the design's functionality is completely decided on, and you've already built your prototypes and committed yourself down a path."

Naturally, at that late stage in the process, the test engineer's "advice" isn't always well received, especially if it would lead to significant design changes. So companies generally decide they have to offer the test engineer more clout by giving him some measure of sign-off authority as part of the review process. "That generally helps a lot," according to Binnendyk, "because then the test engineer has some leverage. And after he exercises that leverage once or twice he gets more respect in the organization."

But the real progress in DFT is made not when test engineers get approval over designers' work, but when the test experts actively participate in the project's design. Many companies have already started including test engineers in design teams, and many more firms will do so in the future.

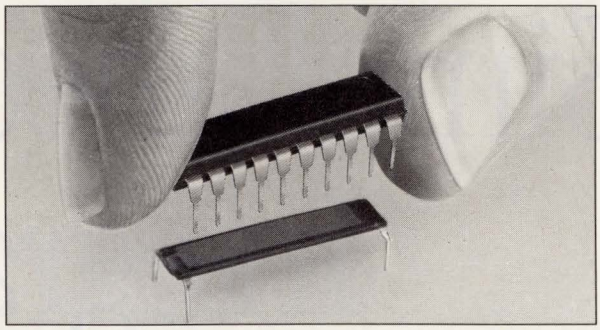
To get the most out of DFT techniques, they must be considered at the project's outset, during the architectural phase, and not just by designers but also by test experts. "You've got to let test engineers help by telling you what the various techniques are and how effective they are," says Binnendyk. "During the architectural phase, the test engineer can work with the principle design engineer—the principle architect—to recommend different types of built-in test or design-for-test strategies." The test engineers would also be responsible for determining how complete those techniques are and for their eventual implementation and execution.

As designs get more complex, critical decisions made at the architectural level affect product testing throughout its life cycle, from design verification to field service. One key DFT technique is scan testing, which requires circuitry partitioning for maximum effectiveness. Therefore, test engineers should be on hand at the beginning, when major block layout is being decided. Although several scan-based techniques have prevailed for a number of years, the one that's expected to predominate in the future is boundary scan. Sometimes called JTAG (because of its origins in the Joint Test Action Group), boundary scan is formally defined by IEEE Standard 1149.1, published last year.

"The time to begin is when the architect starts to define a higher-level architecture," says Prabhu Goel, president of the Systems Solutions Div. of Cadence Design Systems, San Jose. "They can go right from the high-level architecture to an understanding of its implications at every stage of test, whether it's chip, board, or systems test; engineering debug; or field test, service, and repair. The whole thing."

The highest level of the design, the architectural phase, can become a common reference for all those involved in the project.

KILL THE NOISE WITH



MICRO/Q® CAPACITORS

Reduce voltage noise spikes in ICs by as much as a factor of 10. Without redesign. Without using additional space.

With Micro/Q® decoupling capacitors from Rogers.

Micro/Q capacitors mount under the IC. Share mounting holes. To improve noise suppression where it's most effective—at the source.

Best of all, Micro/Q capacitors kill the noise without killing a lot of valuable time.

CIRCLE 112

Micro/Q® is a registered trademark of Rogers Corporation.
Another MEKTRON® Interconnection Product.

For all the facts, including the Micro/Q capacitor track record for noise-reduction in dynamic RAMs, EPROMs, static RAMs and boards that need EMI/RFI fix, call a Rogers' Product Specialist today at (602) 967-0624 (Fax 602-967-9385). And ask for a free sample.

Technology for tomorrow built on TQC today.

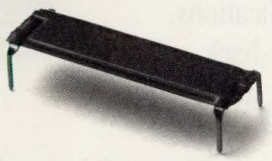
ROGERS

Rogers Corporation
Circuit Components Division
2400 S. Roosevelt Street
Tempe, AZ 85282

DISTRIBUTION: Europe, Japan, Taiwan, Singapore, Hong Kong, Korea, Brazil, Australia

MICRO/Q 1000 STANDARD CAPACITORS

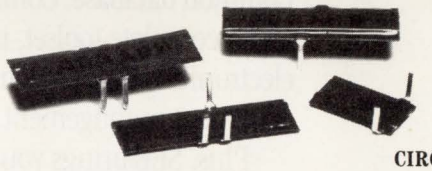
Improve board performance without redesign. Noise problems are solved by retrofitting on existing boards.



CIRCLE 113

MICRO/Q 1000 CUSTOM CAPACITORS

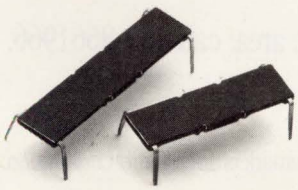
Special pinouts are available to address the wide variety of specialty DIPs such as analog devices, op-amps, and the center pinout advanced CMOS devices. Applications include: decoupling, EMI/RFI filtering, and compensation.



CIRCLE 114

MICRO/Q 2000 CAPACITORS

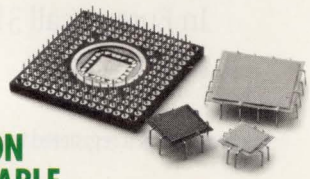
Capacitance levels from 0.01 μF to 0.3 μF in Z5V and X7R temperature stable dielectrics. The unique molded construction provides for maximum environmental protection. Suitable for use in both commercial and military applications.



CIRCLE 115

MICRO/Q 3000 CAPACITORS

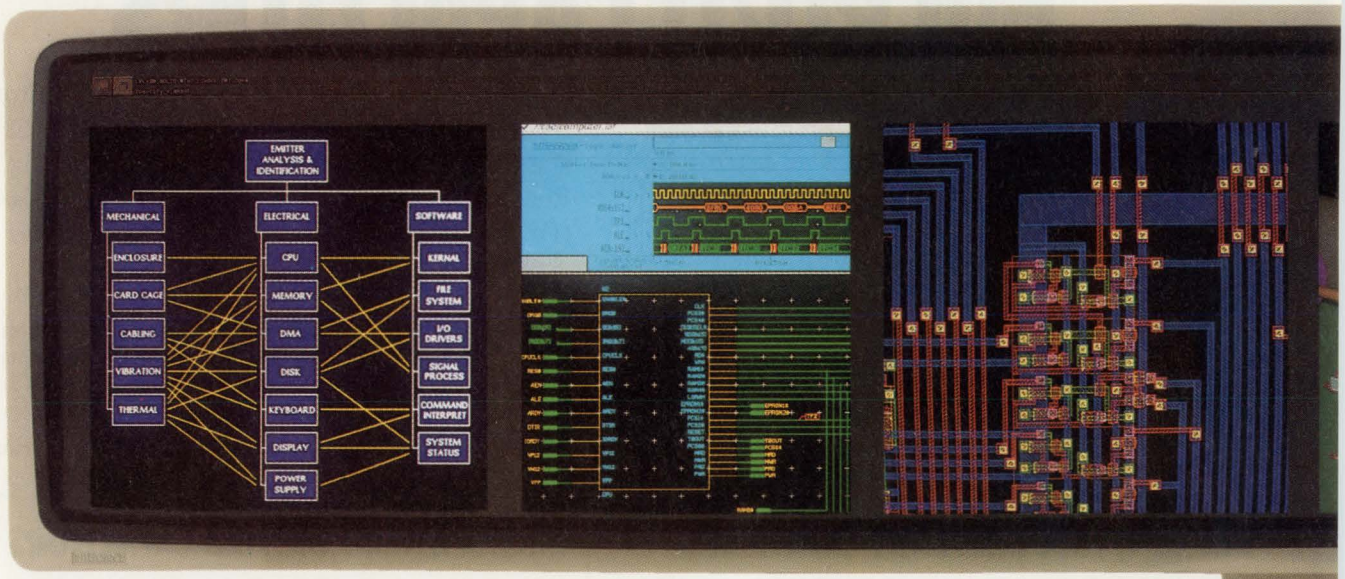
Reduces noise associated with the use of PGA and PLCC devices. Several part sizes are available to address a variety of package sizes, Micro/Q 3000 is designed to be used with all 16/32-bit MPUs, DSPs, GSPs, FPPs, gate arrays, standard cells, and fully custom ASICs.



SMT VERSION NOW AVAILABLE

CIRCLE 116

Our Simultaneous Eng Integrated Fro



What's in it for you?

Intergraph's Simultaneous Engineering Environment (SEE) delivers the EDA functionality you've asked for. Open framework. Common database. Common user interface across applications. And a complete toolset, including solutions for front-to-back electronics design, mechanical design, manufacturing, and document management.

Plus, SEE brings you an important bonus – confidence. The confidence of partnership with the billion-dollar corporation that leads North America in CAD/CAM/CAE sales.

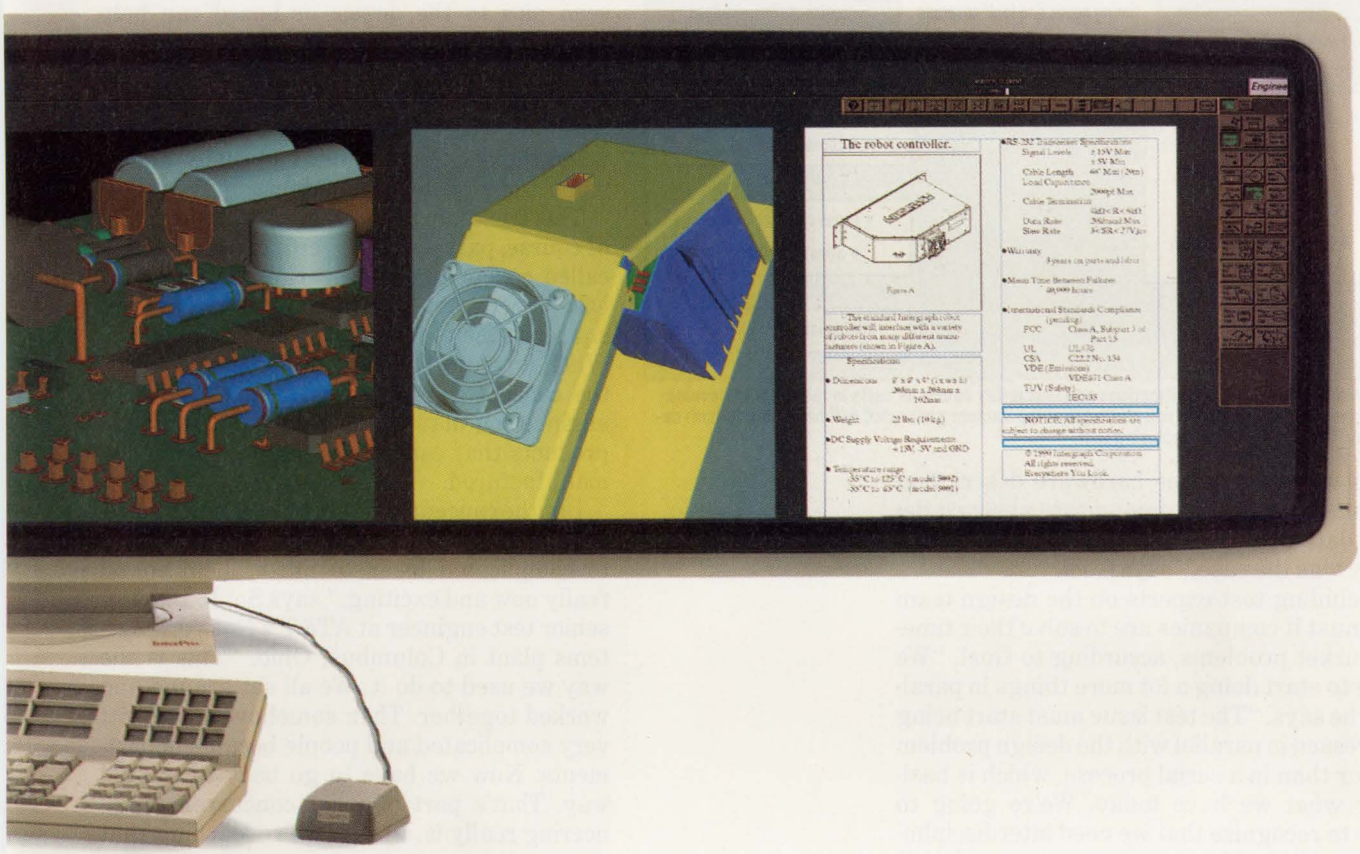
Choose Intergraph solutions, such as our newest MCM and mixed-mode tools. Choose third-party solutions from our InterLink partners. Then let SEE integrate those solutions into a single EDA system – using the same framework that outperformed all others in our recent contract wins with a Big Three auto manufacturer and the U.S. government.

There's more you should know. Call 800-826-3515 or send a fax to 205-730-8344. Ask for document EDA-140. We'll send you a copy of "Simultaneous Engineering: The Facts." It's free.

In Europe: call 31-2503-66333. In the Asia Pacific area: call 852-8661966.

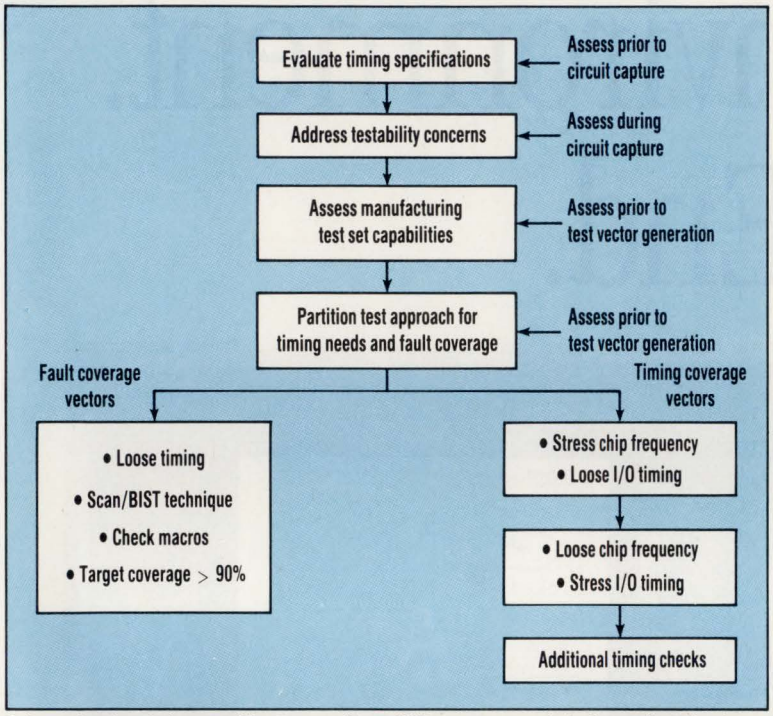
Delivering Now

ineering Environment. m End To End.



INTERGRAPH

Everywhere you look.



2. By evaluating timing specifications and testability concerns early in the product development cycle, the design team will ensure that the vectors generated will be usable in both design verification and manufacturing test.

"You will start to see hardware description languages used to communicate abstract design data at a level much earlier than previously was the case," says Goel.

Including test experts on the design team is a must if companies are to solve their time-to-market problems, according to Goel. "We have to start doing a lot more things in parallel," he says. "The test issue must start being addressed in parallel with the design problem rather than in a serial process, which is basically what we have today. We're going to have to recognize that we need interdisciplinary teams working together on any project."

At this initial phase, designers and test engineers will have to decide many issues before the project can advance. What kind of fault coverage is needed? What kind of test equipment is available? What's an acceptable failure rate and time to repair? Should users be able to diagnose problems in the field? The answers to such questions will lead to the partitioning decisions for scan-based testing.

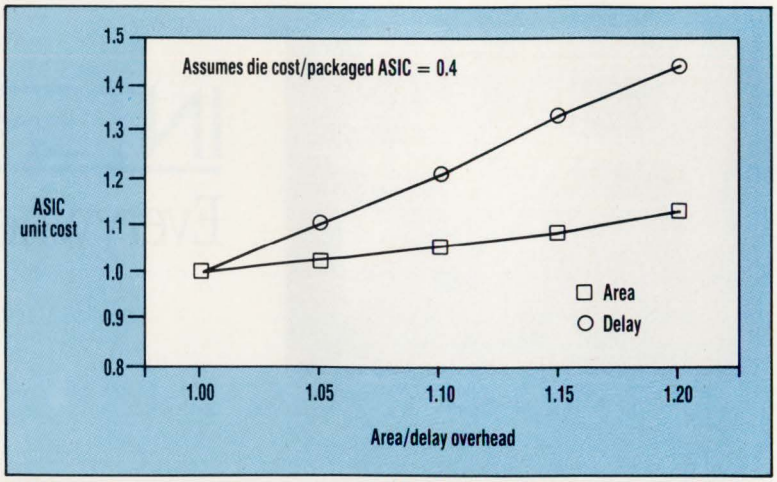
The engineers must address both IC and board-level testing. "If the requirements are only for point-to-point interconnect testing, they can probably just use boundary-scan testing," says James R. Coleman, a section manager in the Test Hardware Dept. of Texas Instruments' Semiconductor Group, Dallas. "But if the design engineer feels he'll have a problem verifying an IC, he'll probably be encouraged to put in internal scan capabilities. There are a lot of trade-offs that need to be made depending on the project's specific requirements."

In fact, easier design verification can be the reward that gets designers to go along with the program. To many designers not yet enlightened about the advantages of more testable circuits, DFT means added circuitry, more real estate, and slower hardware.

That shouldn't be the case says Coleman. "We can show designers that partitioning their designs and adding the four boundary-scan pins to the device or board can help them. They can go in during design verification and actually start out small, with a core function, test it, and then work their way out until they verify the entire circuit. That's when the design engineer will really understand and implement testability up front."

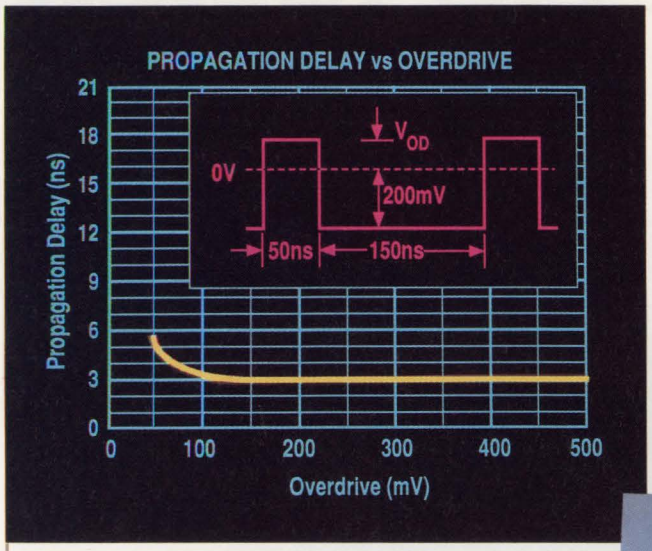
This trend toward parallel development is, of course, part of the larger trend in industry called concurrent engineering. In other areas, concurrent engineering is a way to squeeze time to market down to a minimum. When it comes to electronic design and test, the concept goes even further. Concurrent engineering may be the only way to develop products that can be adequately tested and manufactured.

But the concept may not be as innovative as it sounds. "Sometimes I think we give names to complicated ideas to make them sound really new and exciting," says Sol L. Black, a senior test engineer at AT&T's Network Systems plant in Columbus, Ohio. "This is the way we used to do it. We all sat around and worked together. Then somehow things got very complicated and people became departments. Now we have to go back to the old way. That's part of what concurrent engineering really is. I think we're learning that



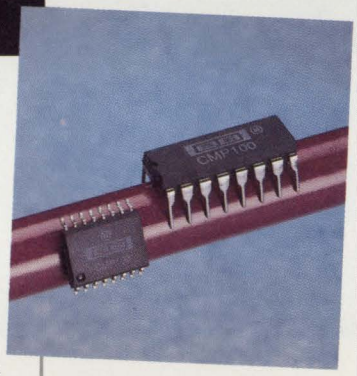
3. Although the increased silicon area needed to implement many DFT techniques adds to an ASIC's cost, the effect is much less than the cost of delays that may occur due to inadequate testability.

New ATE Pin Receiver Handles Signals to ±12V



The speed and accuracy of the CMP100 make it ideal for almost every test head design, from mixed-signal board testing to moderate speed logic, memory, and mixed-signal IC devices.

It can also be used as a threshold detector, and for pulse and transient detection. It's fast enough to detect narrow pulses specified by HIGH and LOW threshold voltages. As shown, it's capable of detecting very narrow pulses.



Key Features Include:

- Propagation Delay: 5ns Max, 100mV Overdrive
- Common Mode Input Range: ±12V
- Input Impedance: 120kΩ || 2pF
- Outputs: Latchable, 10k ECL Compatible
- Supply Voltage: ±5V
- Complete: No External Parts Required
- Temperature Range: -25°C to +85°C
- Packages: 16-Pin Plastic DIP, 16-lead Plastic SOIC
- LOW COST: From $23.20* each in 100s

Consider the CMP100 for your next ATE design. You'll save yourself a lot of time, and money, and get exceptional reliability, too. For complete details, write Burr-Brown Corp., P.O. Box 1400, Tucson, AZ 85734. **Or, call toll-free 1-800-548-6132.**

*USA OEM price in 100s

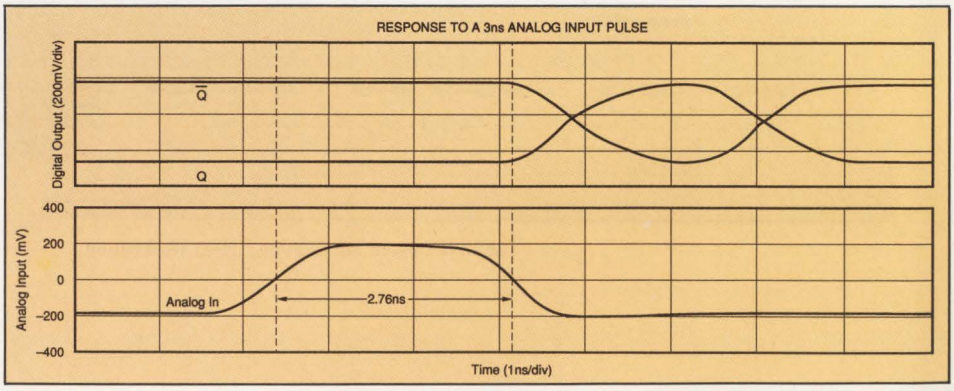
Great Price/Performance Value For ATE Designers

Our new CMP100's unique combination of price and performance make it a true **"must try"** for ATE designers. It's a high-speed dual window comparator specifically designed for use as an ATE pin receiver. It combines a maximum 5ns propagation delay in response to an input step with 100mV overdrive and a wide ±12V common mode input range. Fast enough for many ATE designs, and just right for other signal detection applications.

Then consider its space-saving DIP and SOIC package option, its monolithic reliability, its "no external parts required" completeness, and its low cost. You'll agree that it makes a very cost-effective alternative to building your own.

Hundreds of Applications

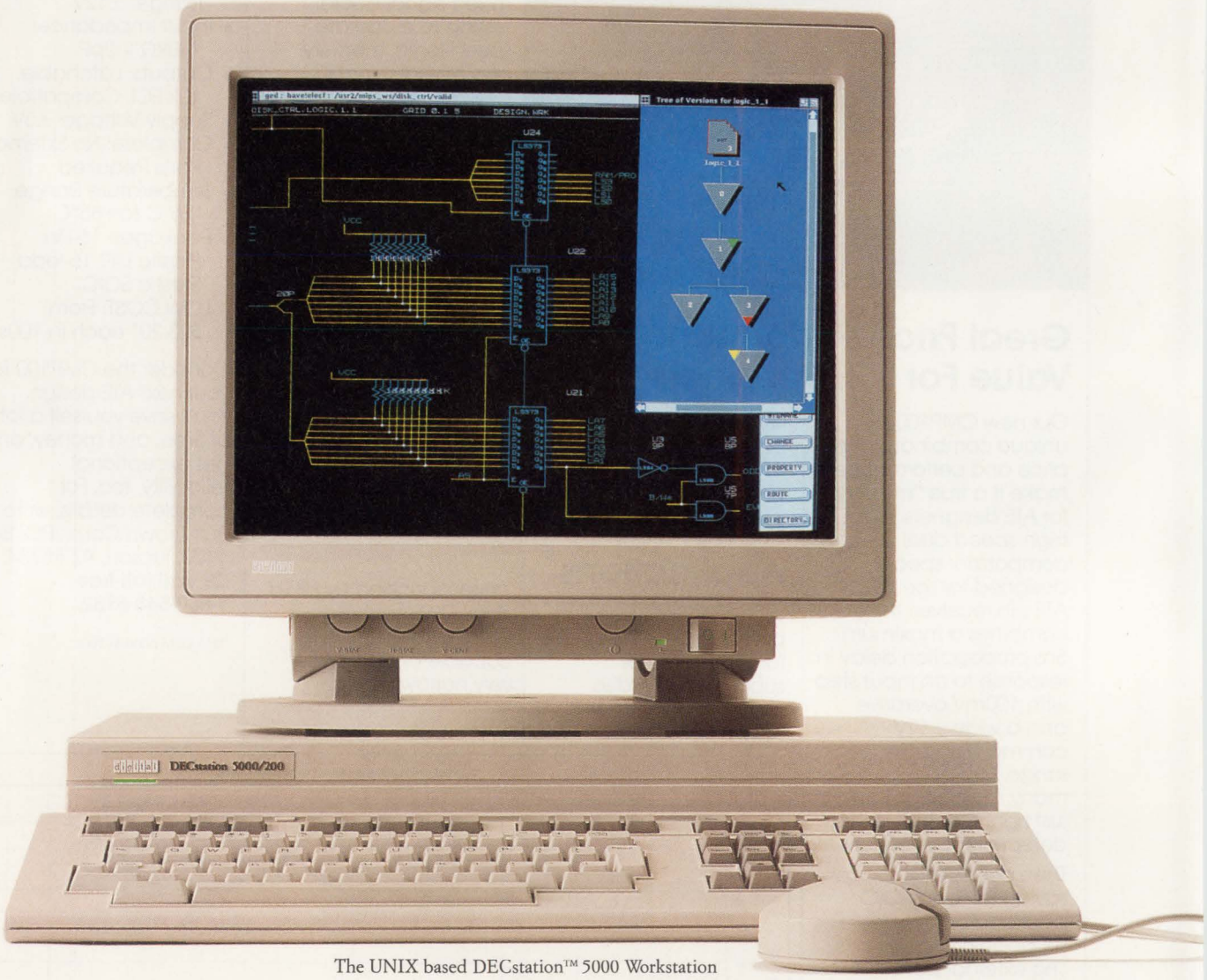
The CMP100 will be particularly useful in ATEs for testing power supplies, ISDNs, disc drives, and VXI boards.



BURR-BROWN®

CIRCLE 85

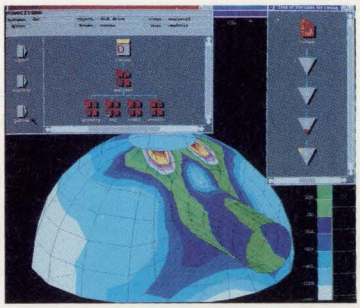
A true leader



The UNIX based DECstation™ 5000 Workstation

digital™

leads by example.



Example #1: Performance

No matter how you measure it, Digital's DECstation 5000 workstation leads all others in performance. Whether it's raw CPU performance, 2D or 3D graphics speed, or price/performance, the DECstation 5000 workstation comes out ahead. In fact, for overall performance, nothing else is close. And we've got the numbers to prove it.

PERFORMANCE COMPARISON CHART (1)	SUN SPARCstation 1+	IBM 320/520	DECstation 5000 cx
Graphics & Windowing (2)	0.24	0.71	1.59
Integer	1.04 (3)	1.34	1.61
Floating Point	1.10 (3)	2.6	1.7
Overall Performance	0.65	1.35	1.63

(1) All data normalized to DECstation 3100. Comparable configurations tested. Geometric mean used to combine results. Performance will vary depending on applications and environment. (2) Graphics and windowing data measured using X11perf benchmark. CPU Integer and Floating Point performance measured from running SPEC V1.0 workload. (3) SPEC performance estimate based on SUN 4/330 results published by Sun Microsystems, Inc.

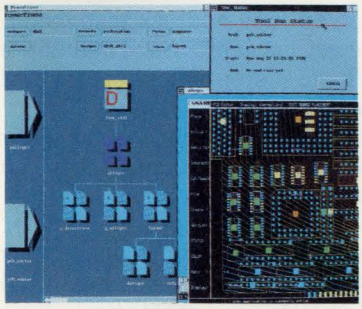
Example #2: UNIX based Applications

When you run with the leader, you know you're in good company. The DECstation 5000 workstation runs more than 1,500 UNIX based applications, including the industry's most popular MCAD and EDA applications.

Example #3: PowerFrame™ for Design Integration.

With Digital's PowerFrame design framework, you can easily integrate the DECstation 5000 workstation with your existing UNIX based EDA and MCAD systems. PowerFrame is the most widely used framework for heterogeneous design management.

And, of course, as the leader in integrated multi-vendor networked computing, you can count on Digital for full service and support. We can help you design, implement and maintain an engineering computing strategy that capitalizes on today's technology, while keeping your options open for the future.



For your copy of benchmark test results and a list of available applications, call 1-800-343-4040, ext. 970. These are filled with examples of what you expect from a leader.

Digital has it now.

we have to work together more."

Black has a special problem in that 90% of the designs he works with come from other sites, mostly in New Jersey and Illinois. He likes to educate the designers on what types of test equipment the plant uses and what problems result from circuits not designed with testability in mind. For the designers in remote locations, that means slide shows during the occasional trips to those sites. Much more effective, says Black, are factory tours for the local designers (from Bell Laboratories in Columbus). They're usually very receptive, because DFT is something they were not taught in school.

One of the key issues that the design team must address early on is how to make sure they come up with manufacture-compatible test vectors, according to J.T. Harrington, supervisor of AT&T Bell Laboratories' Custom VLSI Design Group, Allentown, Pa. That is, vectors should be usable in both design verification and manufacturing test. To do that, the team will address test-vector issues before net-list capture and simulations.

The first step in this approach is to evaluate timing specifications involving clock frequencies and I/O performance, for example, prior to circuit capture *(Fig. 2)*. During circuit capture, the team should handle testability concerns by asking, for instance, whether a special cell or memory block is accessible by an I/O. If needed, the team can add the appropriate DFT logic at this time.

Before generating the test vectors, the team will evaluate the manufacturing test set's capabilities. At this point, Harrington recommends a partitioned approach. Separate vectors should be written for fault coverage and for timing coverage.

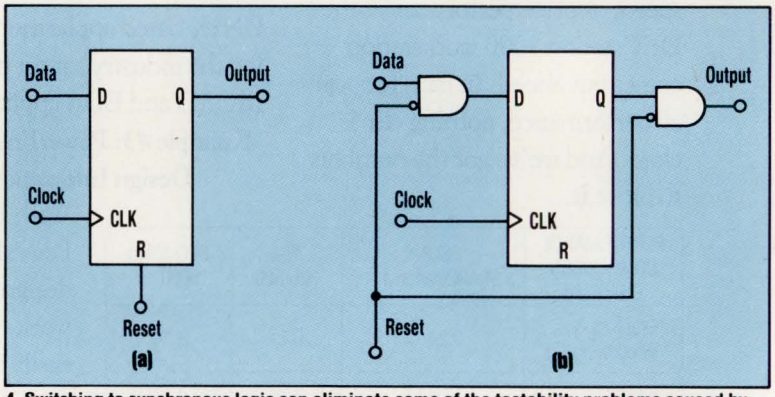
For fault coverage, designers can create vectors for loose timing, to check scan and built-in self-test (BIST) modes, and to check macros by multiplexing I/O pins so they can be uniquely tested. Fault coverage should be better than 90%. In the timing category, vectors should stress the chip's frequency performance, but with relaxed I/O timing. Finally, I/O timing is stressed at a low frequency.

Many companies have initiated the organizational changes that will encourage DFT awareness by design teams. The evidence is apparent in the technical sessions at test conferences, according to Binnendyk, who often leads such sessions. "One of the things I always ask is how many designers are in the group," he says. "Then I ask how many people report into the design group versus into manufacturing."

The answers to those questions have changed dramatically in the last 18 months or so. Formerly, two or three people out of 100 said they had responsibility for test during the design phase. "But the last time I asked this, about 90% of the audience had already or were in the process of effecting the organizational change," Binnendyk says. Those who weren't yet integrated into the design group were anxious to discuss such a move because they felt it was exactly what was needed.

"So that fundamental shift is occurring in a very big way right now," says Binnendyk. "I think that's really good. It's a step in the right direction."

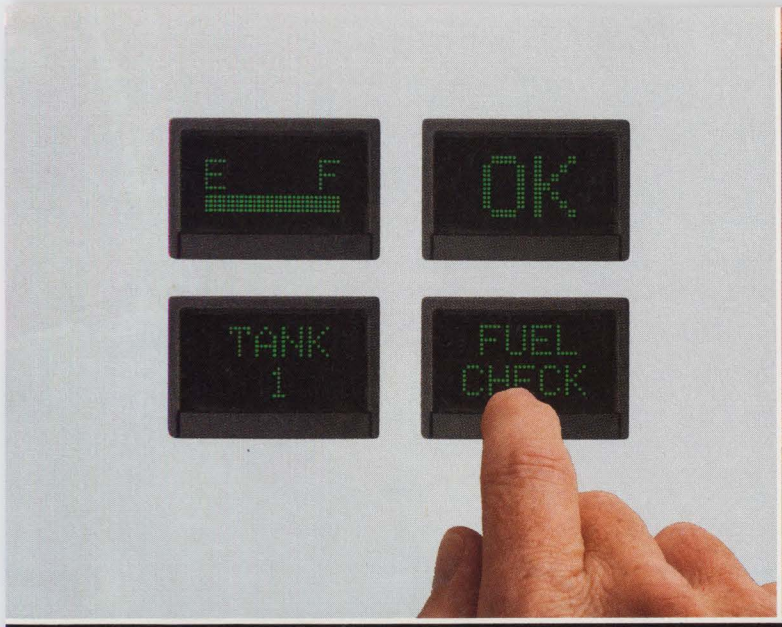
Test engineers should have no trouble adapting to their new roles in the design team. After all, in the old-fashioned over-the-wall process, test engineers must fully understand how the design works before they can figure out all the ways it can fail and how it's going to behave under various conditions. As Binnendyk puts it, "The test engineer has got an extremely aggressive job already, and I don't see that changing. I just see it getting more recognized."



4. Switching to synchronous logic can eliminate some of the testability problems caused by asynchronous designs without changing the designer's goals. In this asynchronous circuit, a reset signal will change the flip-flop's state without applying a clock (a). In the synchronous version, the output still changes state when the reset goes active, although the flip-flop doesn't change state (b). In this case, the Reset pulse must be wider than the clock period.

In fact, that recognition may be the key to the increased acceptance of DFT techniques. At present, too many designers—and the companies they work for—focus only on the cost of DFT in board real estate, components, or design effort. But, as mentioned earlier, the cost of test will become even more significant in a product's life cycle in the future. And the cost of delays that inadequate testability may add to a project's time to market far outweigh the cost of the increased overhead needed for DFT *(Fig. 3)*. That's why more forward-looking companies recognize that DFT's cost is an investment that pays off handsomely, with almost no risk.

The impact of testability—for good or bad—touches all areas of the company: engineering, manufacturing, field service, and



The programmable display system:

The computer interface with the pushbutton feel.

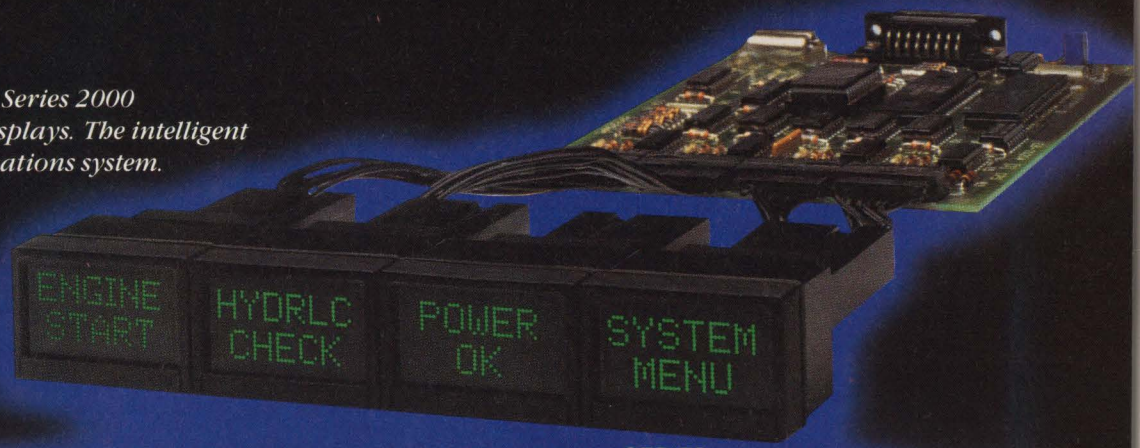
Vivisun Series 2000, now the leading programmable display pushbutton system, interfaces the operator with the host computer. The user-friendly LED dot-matrix displays can display any graphics or alpha-numerics and are available in green, red or amber. They can efficiently guide the operator through any complex sequence with no errors and no wasted time.

They also simplify operator training as well as control panel design. One Vivisun Series 2000 programmable display system can do the work of 50 or more dedicated switches. In short, Vivisun Series 2000 gives the design engineer more control over the design.

Contact us today.

AEROSPACE OPTICS INC.
3201 Sandy Lane, Fort Worth, Texas 76112
(817) 451-1141 • Telex 75-8461 • Fax (817) 654-3405

Vivisun Series 2000 programmable displays. The intelligent communications system.

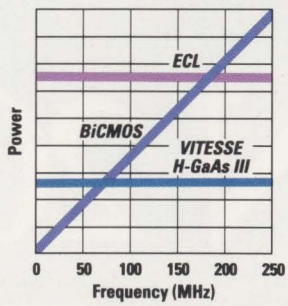


SERIES

VIVISUN 2000™

CIRCLE 82

ONE MILLION TRANSISTORS AND



We're talking better than the best ECL performance at a fraction of the power. And for high frequency designs, Vitesse GaAs chips are lower power than BiCMOS.

Our prices won't sink your budget either– our GaAs chips can give you better performance for your dollar than BiCMOS.

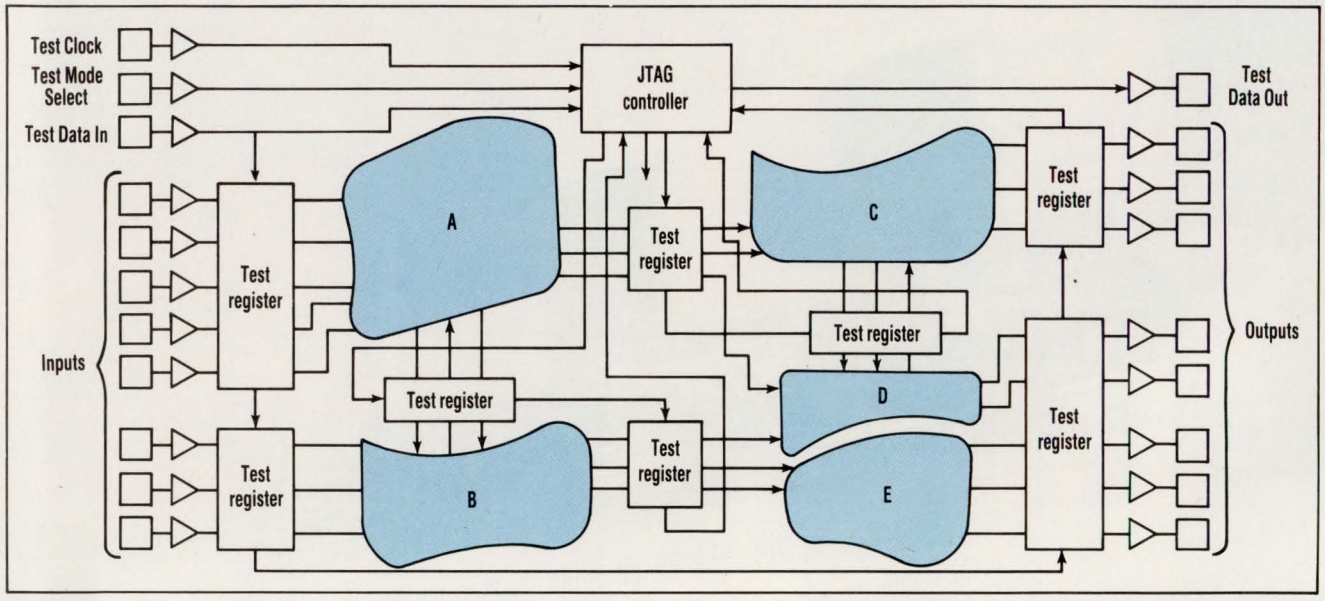
THE BLINDING SPEED OF GaAs.

For more information on our ASIC and standard products with integration levels up to 350K gates, call Vitesse at (805) 388-7455. And leave the competition in your wake.

FX Arrays	Raw Gates	Usable Gates	Availability
FX100K	102,000	Up To 70,000	Now
FX200K	195,000	Up To 137,000	Now
FX350K	353,000	Up To 177,000	Summer 1991

VITESSE
The GaAs Company.™

CIRCLE 169



5. To add internal scan capability to a complex ASIC, the designer partitions the circuitry into blocks (A through E), as is done with a pc-board that employs boundary-scan techniques. Circuit overhead includes a JTAG (IEEE 1149.1) controller, several test registers, and the four JTAG I/O lines.

even marketing because of testability's effect on good will. Unfortunately, individual functional managers aren't usually rated on the their contributions, or lack thereof, to other functions, notes Cadence's Goel.

"Who's the person who heads up all of those organizations and who's measured on the effectiveness of all of them?" he asks. "It's usually the company's CEO. And often he doesn't know what the testability issues are. In order to solve the testability problem, we must have CEOs who recognize that it's a cross-functional problem and who give credit to people who invest in test."

One of the issues that top-level management must address is cost structure. Design teams are given cost goals that their designs must meet, but the goals don't consider the valuable advantages that DFT can bring to the overall project life cycle. Meanwhile, the team feels pressure to increase fault coverage and make testing easier.

Under the typical current cost structure, the design team feels no connection to the cost of developing and executing the test program. That isolation often leads to an attitude of "I can't afford DFT in this design," says Bill Bell, a development manager at TI. "But what if you had spent another $5 on a board for additional components and used JTAG or some other approach? You might have reduced the test program development time from 12 months to 6 months."

Design teams must feel free to ask what effect reduced time to market will have on the project's success. And will that more testable board eliminate the need for a $3 million tester? Or what will the prospect of reduced downtime mean to potential customers? At that point, says Bell, the attitude will become, "I can't afford not to put DFT in the design."

A company's cost structure must enable the design team to have downstream visibility, so that the team can justify the added cost of DFT at the end, says Bell. "To me, that's a big issue in concurrent engineering that must be addressed," he says. "It's a matter of designers making five- and ten-cent decisions that are, in fact, affecting dollars."

But TI's Coleman brings another interesting perspective as to how to convince design teams that DFT is worth the cost. "The way you're going to break down that wall is by the test guy showing the design guy that adding testability will help in design verification," says Coleman. "Trying to tell designers that it's going to help the field sales guy is too far down the pike for them to really appreciate. As a test engineer, the way you really sell and prove yourself to a design team is to show them how you can help verify their design."

Once design teams are convinced of DFT's importance, they'll begin moving toward a more structured approach to the design task. The simpler designs of the past made it possible for designers to use an unstructured, or ad hoc, approach to testability. After the team had selected an architecture, the members would look at it and decide what testability techniques could be added. The process isn't well-defined, so it usually requires lots of experience on the part of designers. The result is a very architecture-dependent solution that's unique to the board or device.

On the other hand, a structured approach by definition follows an established set of rules. Thus, implementation is fairly consistent from one design to another. It can also be somewhat independent of architecture. Because of the overhead involved, a structured

Our new ML2261 8-bit A/D converter takes speed and accuracy to an entirely new level: 670ns.

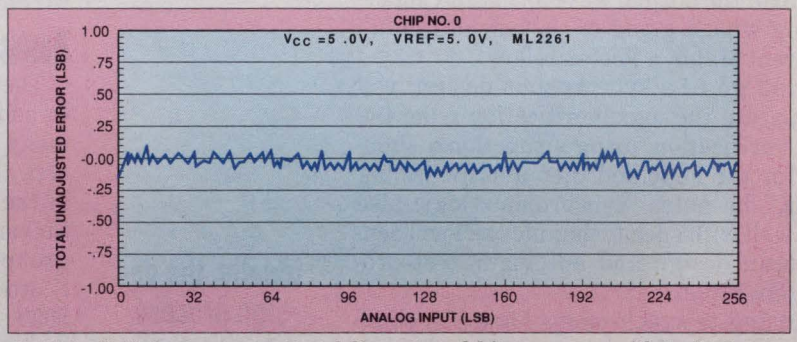
Latch onto Micro Linear's new ML2261. Without question, the fastest, most accurate microprocessor-compatible 8-bit A/D converter on the market. With performance features that'll leave most microprocessors in a no-wait state.

By utilizing half-flash techniques, the ML2261 achieves A/D conversion times of 670ns over temperature and Vcc. It quickly converts an analog 0V to 5V sine wave at 500 kHz to its digital representation with 48 dB signal-to-noise ratio. Digital error correction is used to achieve a total unadjusted error of better than ± ¼ LSB. (Total unadjusted error includes the sum of linearity, zero scale and full scale errors).

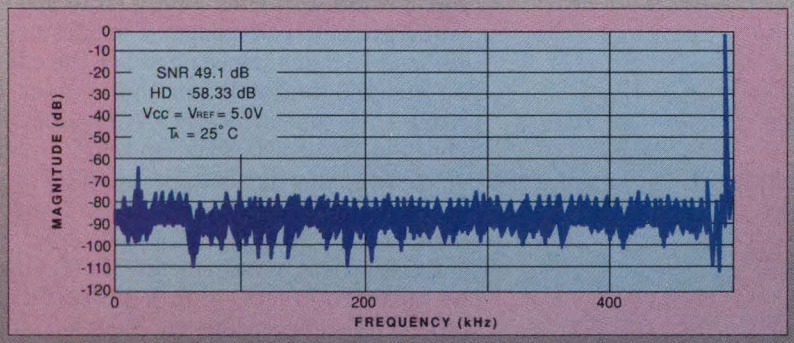
It's also easier to use, because the ML2261's differential architecture provides superior power supply rejection. The analog input is 0V to 5V with a 5V power supply. And because inputs can withstand at least 25 mA, you can achieve better latch-up immunity on analog inputs. The digital interface is also designed to keep up with the fastest microprocessors and appears as a memory location or I/O port to the microprocessor. In addition, no external clock is required and power dissipation is a mere 75 mW. All parameters are guaranteed over the supply tolerance and temperature range.

Combined, the ML2261 gives you the fastest, most accurate, easiest to use 8-bit converter for a wide range of applications including disk drives, medical instrumentation and signal processing. With a price/performance ratio that's significantly lower than comparable converters.

Devices are now available in standard 20-pin DIP or surface-mount PCC packages, with 100-unit prices beginning under $9.00.



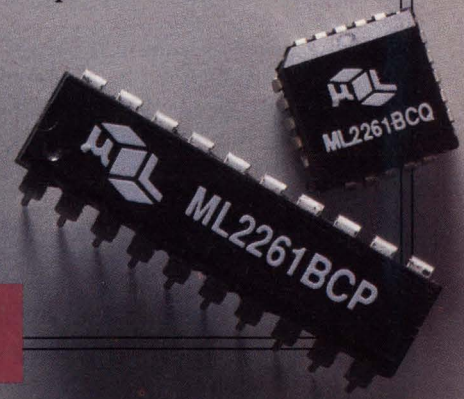
Built-in digital error correction delivers true 8-bit accuracy, with typical unadjusted error of less than ± ¼ LSB.



The ML2261 maintains ideal signal-to-noise ratios independent of increasing analog input frequencies to 500kHz.

For more information.

To find out more about how you can quickly convert your new product design to the ML2261, just call (408) 433-5200. Or write to: Micro Linear, Dept. TFA, 2092 Concourse Drive, San Jose, CA 95131. We'll send you all the specs. In a flash.



Micro Linear

CIRCLE 140

approach to DFT demands that the design team consider testability from the outset to ensure top efficiency. At the board level, this usually means choosing ICs with testability techniques built in.

Looking at the architectural level, DFT considerations will encourage much greater use of synchronous logic. For example, when ASICs get up to the 50,000-gate range, the clever design techniques of asynchronous logic, such as gated clocks and timing delays, start to cause problems *(Fig. 4)*. "Just trying to do a normal event-driven simulation, looking at all of the normal waveforms and understanding what's going on, is very difficult," says Brent Miller, a Vertex fellow.

"If you go to a synchronous design, you can separate the logic verification from the timing verification, using a functional simulation for the logic and then a static timing verifier," he notes. Synchronous logic also works well with such techniques as level-sensitive scan design and automatic test program generation.

Switching to synchronous logic will eliminate some of the innovative timing schemes used in asynchronous designs, but that shouldn't be a problem. "Most designers we've talked to don't know how they would handle those sorts of techniques in very large designs," says Miller. "So I'm not sure that synchronous logic limits them. In fact, it lets them get larger designs done more quickly."

Moreover, synchronous designs will eliminate many of the problems caused by process variations. If everything runs off the same clock, a process shift won't necessarily throw off the design's timing dependencies. In asynchronous logic, these same variations might cause signals to overlap.

"We feel very strongly about synchronous logic, or synchronous design styles, because the overall benefits in terms of yield, the ability to accurately predict what the chip is going to do in all situations, and the ability to automatically generate test vectors just go up exponentially," says Vertex's McMinn. "Asynchronous designs, where you have things like gated clocks and different-frequency signals running around the chip, just create a lot more problems downstream."

Using a more structured design approach will also lead design teams more naturally into the partitioning that scan-based testing requires. In that sense, hardware design is becoming more like software engineering, with hierarchically organized modules or blocks. Ideally, the design process should draw the team toward a partitioned design without forcing members to think "testability." A testable design would simply be the natural outcome of the structured process.

Ideally, the design process should draw the team toward a partitioned design without forcing members to think "testability."

Although boundary scan, as defined by IEEE 1149.1, aims at increasing pc-board testability, the same general principles will help complex-ASIC designers. The design team can carry the circuit partitioning at the board level down to the ASIC level also. Adding some test registers and a JTAG controller then creates internal scan loops *(Fig. 5)*. The resulting BIST capability gives the device higher fault coverage with fewer vectors than otherwise would be possible. Using internal scan, testers can locate errors down to the logic blocks within the chip.

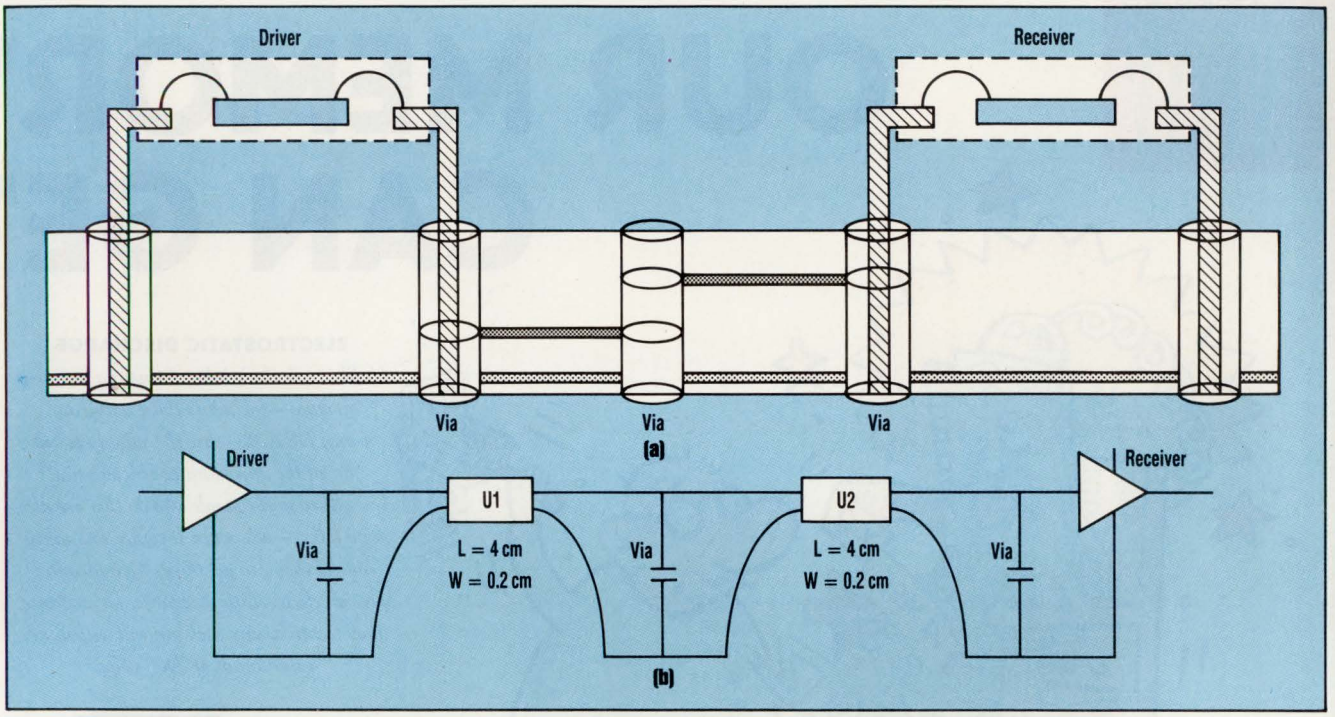
Adding Internal Scan

There's no real breakpoint when deciding to add internal scan becomes automatic. In many cases, it will be a function of the gate-array family available to the designer as well as the size of the basic circuitry, according to Steven Brightfield, the CMOS marketing group manager at Plessey Semiconductors, Scotts Valley, Calif. For instance, if 3000-, 5000-, and 7000-gate arrays are available, the designer probably would not add internal scan to a 4700-gate circuit. The overhead required would bump the design up to the next larger component. On the other hand, a 3400-gate circuit would use the same size array with or without internal scan, which would probably be a worthwhile effort.

As the number of gates increases, however, the number of test vectors shoots up even faster. Consequently, the cost of test development time at some point will outweigh the cost of internal scan circuitry. "If you look at a logic block in the 10,000- to 20,000-gate range, you'll see that a tremendous number of test vectors are needed for high fault coverage," notes Brightfield. "But with JTAG techniques, you can reduce the size of the functional blocks and the number of vectors it'll take to get very high coverage."

One of the more interesting, and tougher, problems design teams will have to solve is testing extremely fast parts. The part's cycle time isn't so much the issue as are the edges' rise and fall times. When those times approach 1 ns, the waveform's equivalent frequency is about 500 MHz, and digital parts behave as analog devices. The analog properties of highest concern are ground bounce and crosstalk, both related to noise. At present, the devices most affected are top-of-the line microprocessors, glue logic parts, and static RAMs, according to Shawn Hailey, president of Meta-Software Inc., Campbell, Calif. ASICs, however, aren't far behind.

Designers and test engineers will have to work together to agree on the testing envi-



6. For very fast circuits, designers need accurate models of all elements, including packaging. In this example, the signal's propagation time on the board (a) depends on the transmission-line characteristics of the areas between the vias, which are modeled by the equivalent circuit (b).

ronment that will yield a device or board that meets customer expectations. The primary concerns will be matching impedances and selecting the packaging. In the past, package selection was usually an afterthought with no electrical consequences. The designer chose the form factor preferred by the end user. That may not be possible with very fast devices.

A complicating factor is the desire to test the device at speed on the wafer so parts can be sorted for performance. "If we want to test these parts at speed on wafer, we have to be able to identify what the effect of the package is going to be," notes Hailey. "And conversely, we also have to know which kinds of packages are most likely to be used, so that circuit designers can tune the output drivers to the package" *(Fig. 6)*.

The critical ingredient for the design team will be accurate models of each component. Some advances have been made in predicting the amount of ground bounce and the delay or clock skews designers can expect as a result of the difference between unpackaged and packaged parts. But more progress is needed. Designers have to know when they must treat a wire like a transmission line and when they must model the on-chip connections as well as the package connections. "We know that signals go at about the speed of light in whatever medium they're in, so there are some basic rules for propagation delay," says Hailey. "Less well-defined rules try to predict how much ground bounce there will be in a package for a given driver type."

Some solutions to the digital designer's speed problems are waiting in the microwave engineering community. "From the education standpoint, there's a real need to bring to those engineers used to working at lower frequencies the kinds of techniques that have been used in microwave design," says Hailey. "But we must also realize that there are some limitations. We can't apply the microwaves solutions entirely because there's no way they can handle the component density and compact size needed by fast digital designs."

The major impediment to design and test engineers working together to create more testable circuits is the lack of common tools. The good news, however, is that people recognize the problem and new tools will be available within the next year or two.

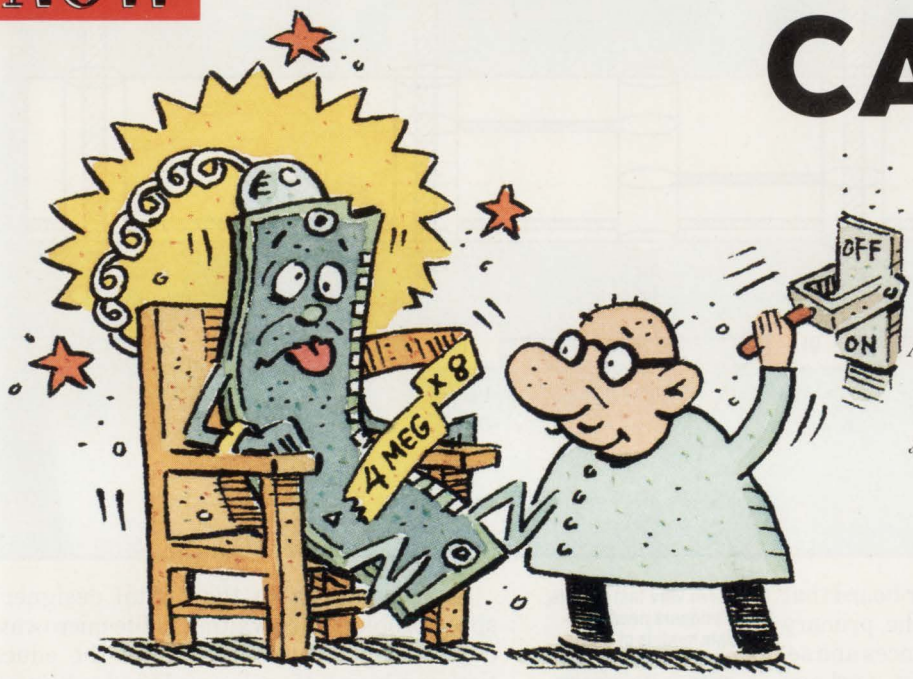
Even design and test engineers integrated into one team have problems communicating with each other. The test engineers come from the manufacturing area and are used to working with logic simulators, fault simulators, and automatic test-pattern generators specific to the tester they use in that environment. But the designers probably have made independent decisions to buy tools that help with their own processes. In most cases, those tools aren't the same and at best require a translation program.

The key is to have both sides speaking a common language, says Mentor's Binnendyk. That means having test engineers working off the design database, eliminating the need for duplicate models, he says.

More automation in the DFT process is also

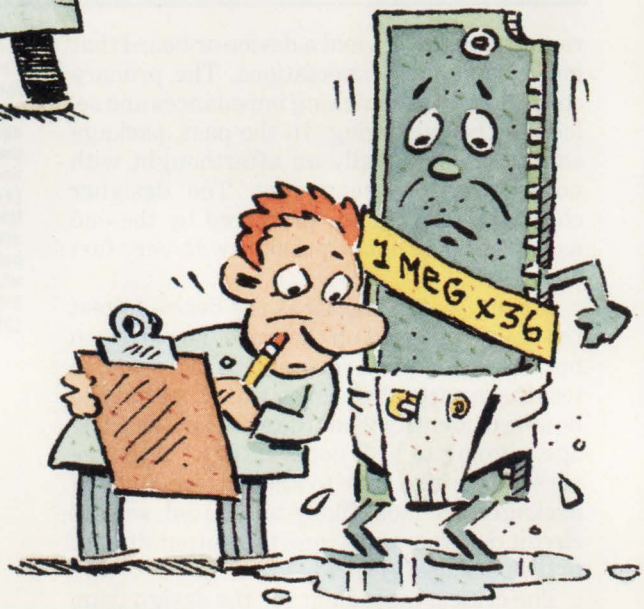
SAMSUNG NOW

OUR MEMORY CAN GET



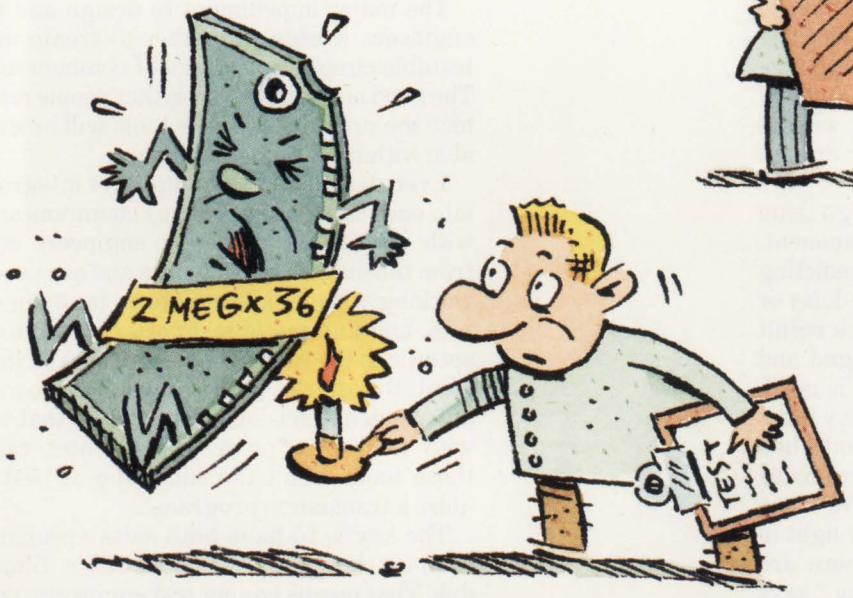
ELECTROSTATIC DISCHARGE

Unlike typical modules, Samsung memory modules—including those using our 4-meg DRAMs—are thoroughly tested for all the important characteristics. And although the people who do this are nice, kind folks—well, when it comes to quality control they can get testy. To guarantee specs on electrostatic discharge, for instance, they test to assure each pin will withstand a minimum of 2000 volts.



FLAMMABILITY

On flammability, our module people take great pains to assure that our products meet standards. As a result, we guarantee that every Samsung memory module meets or exceeds the 94V-O Underwriters Laboratory flame classification.



LEAKAGE

Even in the era of the 4-meg DRAM, there's still such a thing as a module with leaky pins. Many manufacturers just don't inspect for leakage. You guessed it, our team does comprehensive tests. All pins on all modules are 100% tested to the data sheet leakage specification.

MODULE PEOPLE A BIT TESTY.

POWER CONSUMPTION

In this day and age there are enough power-hungry things without your memory modules getting that way. You want them to consume what they say they will. Ours are thoroughly tested not to exceed the spec.

DIMENSIONAL CONTROL

A too-big or too-small module isn't good for much. Samsung modules are tested to perfectly match JEDEC standard dimensions, including 50 ± 3 mil thickness. Since they are, and are also tested on all the other features detailed here, we can't see why you'd ever buy from anyone else. For information on modules with our 4-meg DRAMs, or the rest of our line, write to the testy people at Memory Module Marketing, Samsung Semiconductor, 3725 North First Street, San Jose, CA 95134. Or call 1-800-669-5400, or 408-954 7229.

SAMSUNG Semiconductor

CIRCLE 171

predicted by Cadence's Goel. He compares the situation to the design environment. "If you look at the physical layout side of the business, you'll find that it's starting to become a fairly turnkey process," he says. "Push a button and you get a layout. That's especially true at the chip level, and at the board level it's increasingly headed in that direction. So what's wrong with test? Why isn't test addressable in the same way?"

The answer lies in educating top-level management. Companies must understand that the cost of test is an important factor in any project's success, and an investment in tools which reduce that cost is worthwhile, says Goel.

One major advance that Goel foresees is tools that synthesize DFT logic. They will automatically add the needed circuitry while maintaining optimal placement and timing. Such tools will relieve hardware designers from much of the burden of DFT, so that the process becomes merely an investment in silicon that creates a testable product.

Another important trend in the design environment involves using high-level hardware description languages (HDL). This trend will cross over to the test area in an effort to get the test engineer involved in the project at the earliest stages, when architecture is discussed. Then, as the design evolves and is refined downward, the test engineer will be able to work in sync with the designer, in a true parallel process.

The major impediment to design and test engineers working together to create more testable circuits is the lack of common tools.

What's needed to make this major step are predictive tools. Letting the test engineer work from a high-level, abstract description, these tools will estimate the size of the design and the test task. As a result, the test engineer will be able to forecast the downstream costs associated with design decisions early enough in the process so that they can be changed economically.

"I would say that it's probably going to take a couple of years as test engineers start to adopt the HDL methodology. Then you'll start to see some predictive tools take shape," says Goel.□

HOW VALUABLE?	CIRCLE
HIGHLY	535
MODERATELY	536
SLIGHTLY	537

comPAC

DC Input Power Systems

for Telecommunications and Industrial Applications

10 Watt/in.^{3}

The **comPAC**™ family of high-density DC-Input power systems is designed to keep your system running while shrugging off the sags, surges and transients that your input source hands out. So, if meeting Bellcore, British Telecom or IEC standards for input voltage and transient protection is your problem, in applications from 50 to 600 Watts, comPAC is your solution. And comPAC doesn't talk back . . . it meets Bellcore, British Telecom and FCC/VDE specifications for EMI/RFI.

The low profile package . . . only .99" tall . . . is standard, as is extended input overvoltage capability and reverse polarity protection, output overvoltage and overcurrent protection, trim capability on all outputs, and a master disable. And, every comPAC benefits from the high efficiency and inherently high reliability of our VI-200 family of component-level power converters. So, just tell us what you want . . . 24, 48 or 300 VDC in . . . 1, 2 or 3 outputs, from 2 to 95 Volts . . . output power ratings to 600 Watts . . . we'll do the rest.

comPAC . . . *Vicor's compact solution to your toughest applications.*

VICOR

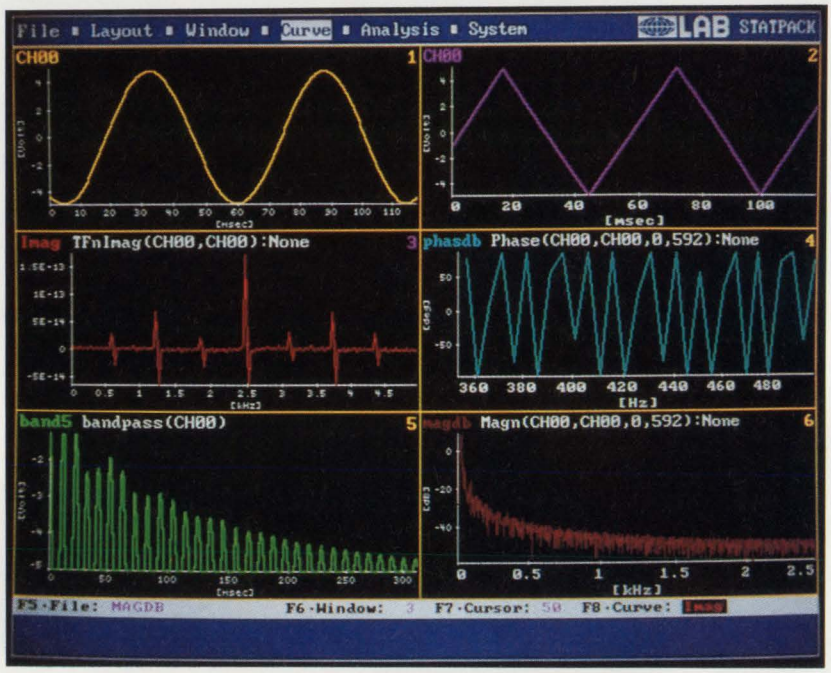
23 Frontage Road, Andover, MA 01810
Tel.: 800-735-6200, 508-470-2900 • Fax: 508-475-6715
Vicor GmbH, Tel.: 49-8031-42083 • Fax: 49-8031-45736

Component Solutions For Your Power System

GLOBAL LAB DATA ACQUISITION SOFTWARE GETS RESULTS FAST

"GLOBAL LAB™ *Data Acquisition provides mouse and menu control for the PC AT and PS/2, while fully supporting the industry's fastest throughput rates.*"

–Fred Molinari, President



GLOBAL LAB *Data Acquisition*

- Errorless data transfers up to 250kHz
- Supports DT2821, DT2831, DT2801 and DT2901 series boards
- Simultaneous acquisition and display
- Quickly displays data in up to 100 windows
- Import/Export data files

STATPACK™ for Advanced Signal Processing

- Spectral Analysis: FFT, auto spectrum, cross correlation
- Windowing techniques: Hamming, Hanning, Blackman
- Standard and custom digital filtering
- Advanced arithmetic operations
- Arbitrary waveform generation
- Thermocouple linearization

GRAPHPACK™ for Report Quality Printing

- Supports all industry standard printers/plotters
- Enhance data with custom text and graphics

GLOBAL LAB *Data Acquisition* $995
STATPACK Signal Processing Module * $595
GRAPHPACK Printing Module * $495
*optional

Site licensing available; all prices U.S. list

FAST 5 day delivery

Call for FREE Demo Package

(508) 481-3700

In Canada, call (800) 268-0427

DATA TRANSLATION®

World Headquarters: Data Translation, Inc., 100 Locke Drive, Marlboro, MA 01752-1192 USA, (508) 481-3700, Fax (508) 481-8620, Tlx 951646
United Kingdom Headquarters: Data Translation Ltd., The Mulberry Business Park, Wokingham, Berkshire RG11 2QJ, U.K., (734) 793838, Fax (734) 776670, Tlx 94011914
Germany Headquarters: Data Translation GmbH, Stuttgarter Strasse 66, 7120 Bietigheim-Bissengen, Germany 7142-54025, Fax 7142-64042
International Sales Offices: Australia (2) 699-8300; Belgium (2) 466-8199; Brazil 11 240-0598; Canada (416) 625-1907; China (1) 513-7766 x1222; Denmark 2 274511; Finland (0) 3511800; France (1) 69077802; Greece (1) 361-4300; Hong Kong (5) 448963; India (22) 23-1040; Israel 52-545685; Italy (2) 82470.1; Japan (3) 502-5550, (3) 5379-1971; Korea (2) 718-9521; Netherlands (70) 399-6360; New Zealand (9) 415-8362; Norway (2) 53 12 50; Poland (22) 580701; Portugal 1-7934834; Singapore 338-1300; South Africa (12) 803-7680; Spain (1) 555-8112; Sweden (8) 761 78 20; Switzerland (1) 723-1410; Taiwan (2) 3039836

CIRCLE 94

CONCURRENT ENGINEERING MEETS DESIGN AUTOMATION

DESIGN TOOLS MERGING UNDER FRAMEWORKS PAVE THE WAY FOR TRUE AUTOMATION OF THE ENTIRE DESIGN PROCESS.

JOSE DECASTRO & PETER HOOGERHUIS

Mentor Graphics Corp. 8500 S.W. Creekside Place, Beaverton, OR 97005; (503) 626-7000.

As the 1990s unfold, the interest in concurrent engineering continues to pick up steam. Concurrent engineering is a methodology that focuses on the intense interaction of all engineering disciplines throughout the design and production cycle. To support the methodology, a lot of effort has focused on developing the necessary design automation infrastructures, such as frameworks that supply common databases and interfaces for a wide range of tools from many vendors. As the framework concept matures, emphasis will be placed on the nature of the framework as well as on the dynamics of how it works to actively support concurrent engineering.

Concurrent engineering, with its multidisciplinary teams, is certain to be around for a long time. Companies employing this methodology have clear evidence that it actually improves product quality while reducing both product cost and time to market. It's also strongly associated with the management principles put forth by Deming, well-known quality guru, and others. Those principles stress continual product improvement, a strong focus on quality, and massive interaction among members of product development teams.

The evolving design-automation environment that supports concurrent engineering has seen the power and scope of its tools expand steadily. One interesting area is the relationship between advanced simulation tools and concurrent-engineering models. As simulation technology grows more comprehensive, designers are approaching the capability to produce "virtual prototypes" that embody all aspects of the product. It will eventually become possible to model the user interface of a product so that customers can interact directly with the virtual prototype. Their feedback can then be incorporated into quality-function-deployment (QFD) maps, which help redirect the design to accommodate their suggestions.

QFD is a discipline in which customer wants and needs are an inherent part of the entire product development process. It ensures that these wants and needs are carefully considered and directly translated into technical requirements. It dovetails with concurrent engineering because it requires that a multidiscipline team formally and systematically consider customer needs very early in the design cycle and then translate them into tangible engineering objectives throughout the design cycle.

As the mid-90s approach, many of the concepts discussed in this article will begin to wend their way into design-automation environments. The merging of concurrent engineering, quality function deployment, and design automation will become a way of engineering life well before we get to the next millennium.

While good management is essential, extensive automation support will ultimately enable and promote concurrent engineering. The design automation industry has responded by evolving a design environment that promotes the integration of tools, data, platforms, and operating systems. As a result, designers will soon see one environment that can embrace electrical, software, IC/semicustom, mechanical, and pc-board design, as well as support reliability analysis and technical documentation. These diverse disciplines will share common libraries, user interfaces, and data management.

Furthermore, the various disciplines will have intercommunication channels open between them. Managers will thus gain unprecedented flexibility in how they configure their design environments to promote the principles associated with concurrent engineering.

This first phase of developing the proper infrastructure for concurrent engineering is similar to building a stage set—the real action occurs when the drama is played out upon it. And in the case of concurrent engineering, the scope of this drama can be vast. As the design group increases in size, the number of possible communication paths between individuals goes up by the following function, where n is the number of members on the team:

$$\text{communication paths (n)} = (n^2 - n)/2$$

Consequently, a 10-person project team has 45 possible communication paths, while a 100-person team has 4950, and a 1000-person effort has 499,500. The rapidly escalating number of paths is why the issue of communication and organization has become paramount in managing concurrent engineering.

Obviously, as a project grows, the potential for anarchy grows disproportionately to its size. To counter this, there must be structures in place that channel these communications in a way that promotes overall productivity. Design-automation tools have been advancing to meet this goal *(Fig. 1)*. In the first and second stages of tool development, individual tools and tool integration are fairly complete. The emergence of a framework like Mentor's Falcon Framework enables the third stage—design process support. This stage includes such functions as managing data concurrency and ensuring that tools are used in the proper sequence, as well as monitoring

overall design parameters as the project evolves.

The final stage, automated concurrent engineering (ACE), will be a product not only of supporting framework technology, but also of profound changes in product development methodology as companies begin to understand the nature of change and manage it to their competitive advantage. According to one authority in the field, Peter Drucker, professor at Claremont College, Calif., "Systematic innovation therefore consists in the purposeful and organized search for changes, and in the systematic analysis of the opportunities such changes might offer for economic or social innovation."

Fundamentally, a company's competitive advantage grows out of the value it can create for its buyers which exceeds the firm's cost of creating it. In the 90s, the market will increasingly reward companies that understand and capture the value they provide by managing change and its associated costs. There appear to be two keys to managing change in organizations: reducing the need for unnecessary or fruitless change; and increasing positive and effective response to necessity or fruitful change.

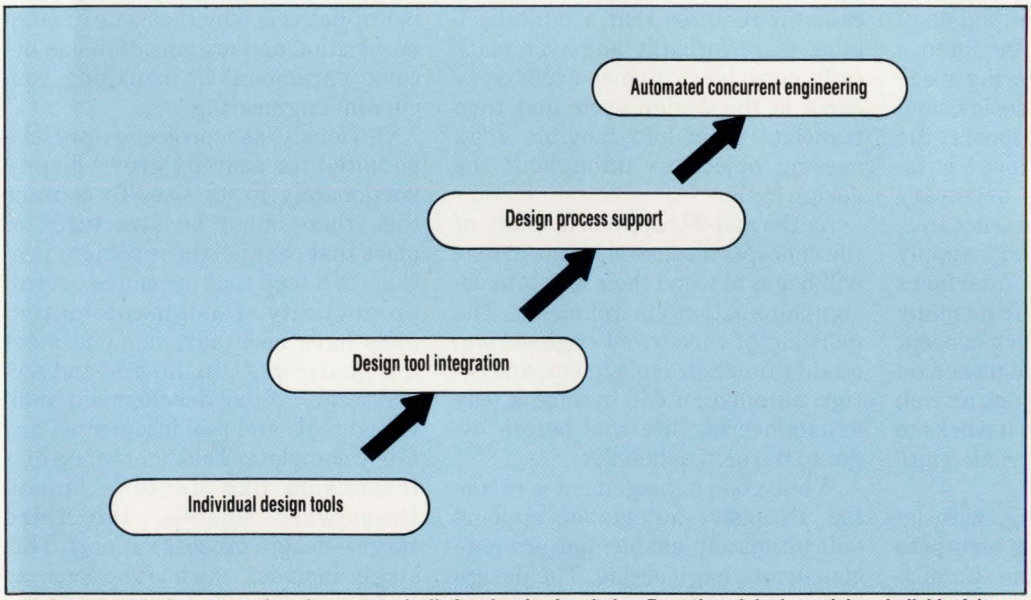
Consider a hypothetical example of a company, XYZ Corp., that makes electronic pagers and would like to plan for its second generation product. The company's marketing strategy is to satisfy a larger consumer market in addition to the professional market, which its current pager addresses. A multidisciplinary project team consisting of representatives from marketing, engineering, manufacturing, support, etc., is put in place and tasked to bring the new product from concept to market. Through numerous interactions with potential customers, XYZ identifies that the new pager should be more affordable, smaller (easily fit in shirt pockets), operate longer on its batteries, provide more storage for incoming calls, have wider geographic coverage, and so on.

A company's competitive advantage grows out of the value it can create for its buyers which exceeds the firm's cost of creating it.

Even in this simple example, the project team faces many implementation options. These decisions may include the choice of lithium batteries instead of alkaline, VLSI CMOS surface-mounted chips instead of DIPs, increasing memory from 4 kbytes to 16 kbytes, etc. There are also mechanical and packaging decisions (design for snap-fit assembly i.e. no screws, ...); software and firmware decisions (writing a phone number management function, ...); service and support decisions (satellite links for global coverage, ...); manufacturing and production decisions (estimated production rates, ...), among others. Now consider that there are interrelated cost and schedule implications associated with each implementation decision that involves change. One quickly notices how the complexity of the situation rapidly climbs.

To deal with situations like this, ACE must become an active partner in the enterprise, and actually represent a collective engineering intelligence that transcends individual contributions *(Fig. 2)*. Such a partnering must support multidiscipline teams practicing concurrent engineering. The horizontal axis represents increasing intelligence in the interaction of disciplines. The first step is simple data sharing, where one tool can import and represent data from other tools without interpretation. The second step is communication, where tools and their users analyze the data in some way and engage in a dialogue with tools and users in another discipline.

The final step is collaboration, where tools not only have a dialogue, but advance toward predetermined goals. The vertical axis indicates the progression of data representation, from primitive data to the transfer of complex knowledge. At the bottom of this axis would be raw binary information,



1. In the area of design automation, there are typically four levels of evolution. From the original standalone individual design tools, the design-automation field is evolving to integrate the tools together and then provide an integrated environment to support the design process. The final evolutionary stage is the knowledge-based automated concurrent-engineering environment, in which the tools have a very active role in defining the product to be designed.

When you're the first and fastest, what do you do for an encore?

Whatever it is, it better be good.

After all, our EL 3200 was the first 68020/030 development system with 33 MHz speed.

So, while others were just getting into the act, Applied Microsystems upped the ante.

We made the EL 3200 a more powerful performer. So you get an advanced event system for easier tracing and debugging of complex 32-bit designs. Support for the memory management unit, floating point, cache burst and synchronous cycles. And a graphical interface to set breakpoints more quickly and a powerful macro language to simplify lengthy routines.

All this comes with full Ethernet network support to maximize your investment in workstations and PCs. Plus installation, training and application assistance to help you finish your designs faster.

For a free demonstration, call Telemarketing at 1-800-343-3659 (in WA, 206-882-2000).

Because folks, it's show time.

Applied Microsystems Corporation

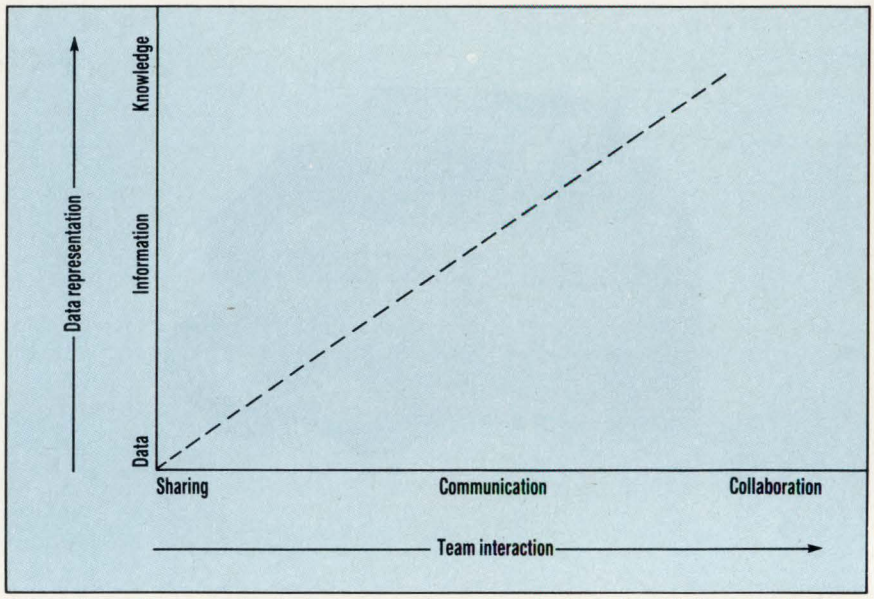
such as "10000100." The midpoint would be symbolic information, like "CLK 50 MHz," and at the top would be such knowledge as "Our goal is a clock speed of 55 MHz, provided it doesn't increase the unit cost more than 1.5%."

All successful teams can deal with these levels of representation. However, today's design-automation environments still can't cope with or support the collaboration of design disciplines. The current evolutionary path toward this goal is represented on this graph by the diagonal line, with the upper right point representing the ideal situation.

One Step At A Time

A closer look at the four stages of evolution leading to ACE illustrate how it will gradually become a reality. Much of the effort now going into frameworks will come to full fruition as the industry moves up this evolutionary ladder. In the first stage, the quality and performance of individual tools will be significantly enhanced as tool developers concentrate on core algorithms and draw upon the framework for user interface and data-base-access building blocks. That will produce better tools that are less expensive and faster. Those improvements are based on estimates that indicate about 65% of the engineering effort for new tools goes into the user interface and database access portions of the product.

As design tools integrate, the support for concurrent engineering begins to appear. Rather than develop exclusive interfaces between tools, all tools can communicate through a set of system-wide services offered by the framework. One example is the availability of on-line documentation and information, which becomes accessible to engineers regardless of the specific tool they're currently using. In addition to providing documentation that makes design tools easy to learn and use, on-line information can make up-to-date parts catalogs and models available, or even provide access to "design cookbooks" and research papers. Another example—common procedural interfaces for net lists—permits each tool to easily exchange information with other tools.



2. As projects get more complex, design teams must move from simply sharing data to communicating more easily. Eventually, all knowledge should be pooled together in an effort to improve the final product and meet the design objectives.

As these system-wide services continue to mature, they will eventually reach the point where they mirror the transactional models currently employed in "enterprise computing." In the enterprise model, procedural interfaces to the database can incrementally update and query the data, rather than operate in a batch-oriented mode.

The next stage of integration enhances the interaction of design teams by aiming not at the tools themselves, but at the overall engineering process. In such a scenario, a set of data management and process control services allow a wider view of the design that transcends that of individual tools. At the base of these services is the concept of a design object, a view of the design that hides all of the computer filing system conventions from the designers and lets them view their design in much more intuitive terms.

Rather than develop exclusive interfaces between tools, all tools can communicate through a set of system-wide services.

Various object types can be defined to encapsulate application-specific information (for example, schematic, layout, simulation, and documentation objects) and map this information into a set of data management operations that are more consistent across all design disciplines. It could also support concurrency by allowing objects to include such information as who has been looking at them, whether they've been formally approved, and so on. Furthermore, the design environment could offer convenient mechanisms to register the structure of new design tools and data.

This stage also makes it possible for team members to graphically navigate through design data and easily understand cross references, such as the association of schematic symbols to physical parts. It also allows management of versions—a vital attribute in concurrent engineering, where constant interaction of team members continuously modifies the design. Versioning mechanisms ensure that if problems arise, there is a known version that engineers can fall back on. Likewise, this "view from the top" must permit configuration management, which

GETTING TO KNOW KNOWBOTS

One central theme of design automation has been the application of software-based "tools" to the engineering process. The very concept of a tool implies that it's actively manipulated by a worker to produce some end result. In coming generations of design automation, a new software-based entity will surpass the idea of a tool and allow engineers to become managers of armies of specialized workers that do the user's bidding, whether or not the user is present. These active agents are sometimes referred to as "knowbots" because they can operate independently and draw their input directly from databases or other knowbots, instead of from users.

In practice, designers could construct many different knowbots that carry out a wide variety of procedures over extended periods of time. For instance, knowbot number one might meander through a design database several times a day looking for parts that achieved a certain price/performance ratio.

When it discovers data that fits the template, it might hand this off to knowbot number two, which accumulates this information until some predetermined quantity is present. In turn, this knowbot might present the aggregate part data to knowbot number three, which converts it into graphical form to present on the workstation display.

With knowbots running on a network, CPU cycles could become far more efficient. Many workstations that are idle after working hours could be continually employed by knowbots. These knowbots could be programmed to "wake up" and roam the network during off-peak hours.

In the long run, the knowbot concept may have far-reaching impact on the engineering process itself. Today, most tools are used with an all or nothing strategy in mind. For example, one doesn't invoke a simulation unless there's a good possibility it will succeed. If it fails, the time spent on it yields nothing. In an environment populated by knowbots, it would be possible to employ brute-force methods, where knowbots could explore many different possibilities with no time loss for the user.

Ironically, this new design automation would be better described by biological metaphors than computer ones. In a process much like the evolution of a species, many individual efforts might meet with failure. Nevertheless, the design as a whole would be robust enough to survive and flourish because the widest range of possibilities had been explored.

would allow sets of related design objects to be operated on as a unit. For example, releasing a configuration that includes the schematics, layouts, and specification documents. Or locking a configuration so that while one designer edits the schematic, another could not change the layout.

SET DATA BOUNDARIES

In a highly automated, multidiscipline engineering effort, there will be an enormous amount of data that could be potentially included in defining a design. One important task will be to draw data boundaries that will meet design objectives, yet keep the design database within reason. One example might be a pc-board-based circuit design. In some applications, it might be sufficient to only include references to actual parts. However, in cases where traceability is an issue, it might be necessary to expand the data to include specific part information. With configuration management, managers can define the scope of the data required, and then let the system automatically round up the appropriate files to build the design.

Another important capability at this stage is regulating the flow of design processes automatically throughout the product development cycle. A simple example might be a mechanism that prevents schematics from going to layout without undergoing simulation first. In any case, with multiple designers, disciplines, and design modules, there needs to be the engineering equivalent of a traffic-control system that is universally used and understood.

Lastly, the ultimate goal of realizing the automated-concurrent-engineering environment can be achieved. In that environment, the system itself becomes a participant in the engineering effort. To achieve that level, designers must be well into the upper right quadrant of the graph *(Fig. 2, again)*. Only then can they establish a level of communication that cuts across multiple disciplines and integrates the project as a whole. Once this is accomplished, it becomes possible to look at the collective output of all participating tools, synthesize the information, and then send directions to individual tools that keep the design on track. This means that multiple product parameters can now be optimized concurrently; for instance, the trade off of reliability vs. cost. It also means that the impact of early design decisions on downstream product parameters can be analyzed. For instance, the impact of proposed hardware functionality on power consumption and enclosure space could be estimated.

The ability to automatically analyze tool outputs in pursuit of project-wide goals will play a critical role on concurrent-engineering efforts. Prototypes for such analyses already exists in the form of sophisticated design specification tools that can analyze the interdependencies between various aspects of a product, and thus analyze the "ripple effect" when any aspect of the design is changed. Another important application will be the ability to design the product and the product development process simultaneously. By the time a product reaches manufacturing, the vast majority of manufacturing and test issues have already been resolved, and procedures are in place to handle them.

The next aspect is determining what kind of conceptual entity will

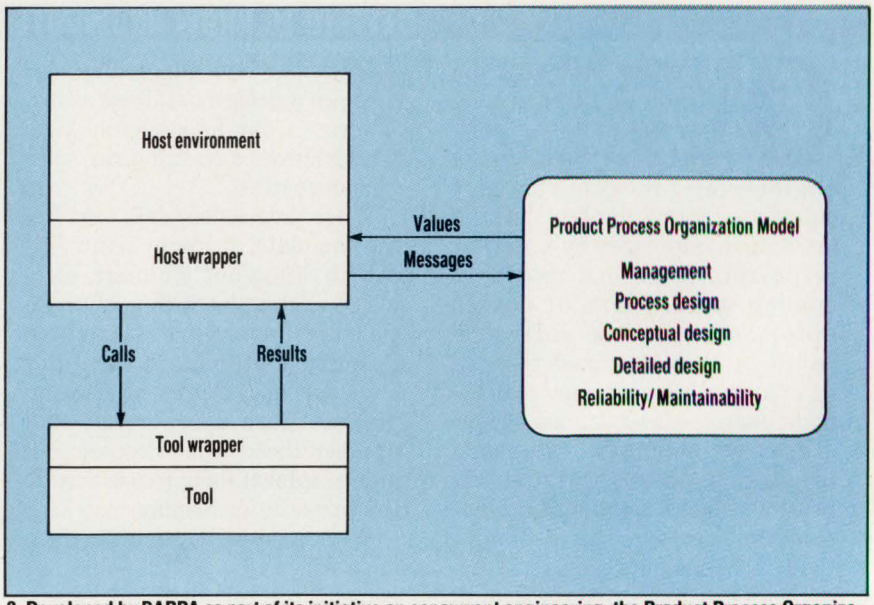
support the automation of concurrent engineering. Whatever it may be, it will most probably be an abstraction that overlays an existing design automation framework. One generalized model that can exist independently of any given computer environment was developed by the DARPA initiative on concurrent engineering (DICE). It's based on a data depository called the Product Process Organization (PPO) model that embodies all aspects of product development *(Fig. 3)*.

At the front end, the DICE concept includes conceptual design, including parametric models, design rules and constraints, and initial architectures. Detailed design would include specific circuitry and mechanical components, and functional models. Reliability and maintainability embraces failure modes and effects, and field support. Management includes feature history, planning and scheduling, and life-cycle costs, while process design looks at precision geometries, manufacturing rules and constraints, and process planning.

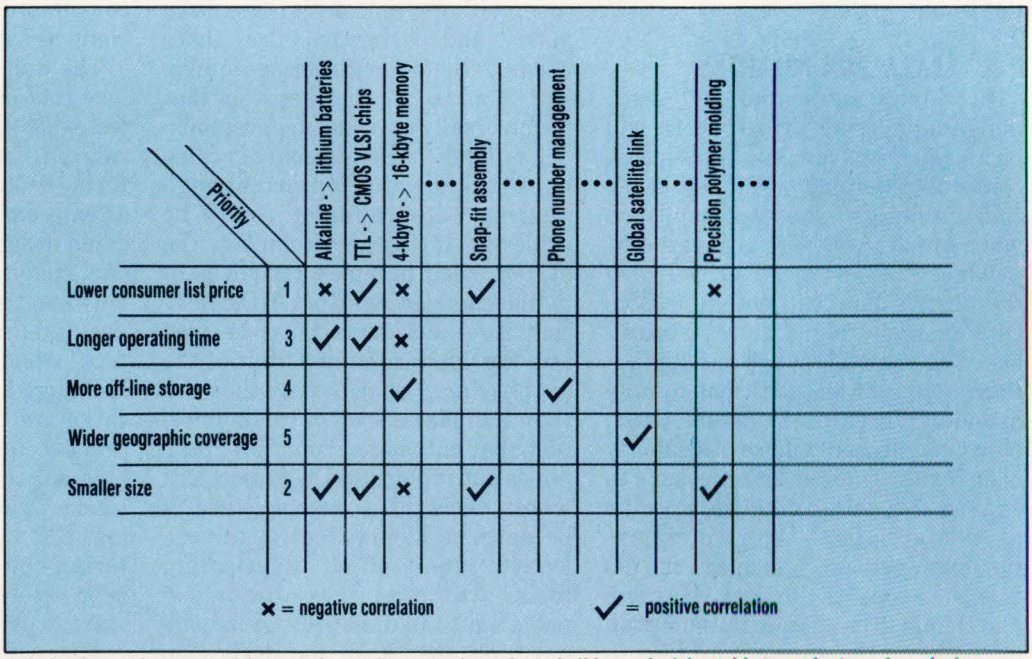
This data model would participate in a specific host computer environment through a host-specific "wrapper" that would query the data model and receive values from it. In turn, this wrapper would communicate with tool-specific wrappers that would take calls for data and produce results. In this type of model, it would be possible to rapidly assess the state of the design and navigate through all of its aspects. It might even employ such advanced concepts as "knowbots," software entities that can travel through the data space and report back on their findings either in real-time or in response to preprogrammed triggers *(see "Getting to know knowbots," p. 83)*.

With this model, real-time data links can also be established between designers operating in different disciplines. For instance, if a manager was analyzing trade-offs between various aspects of a product, such as cost and estimated life and weight, a matrix could be constructed that would be filled by specialists from various disciplines, including manufacturing and mechanical engineering. Moreover, this matrix would be dynamically updated as the various specialists refined their work. There could also be more naturalized interfaces to the PPO model, like designer's notebooks that used drawings, spreadsheets, and charts dynamically linked to the workof others participating in the system.

This model produces some essential questions. How can the team identify and focus on the key changes that will result in the most benefit? How can the team ensure



3. Developed by DARPA as part of its initiative on concurrent engineering, the Product Process Organization (PPO) model is a data depository that embodies all aspects of product development. Tools and the host environment interact with the PPO and mask the basic data structures from the user.



4. A simple matrix or spreadsheet can be used as a starting point to build up a decision table to evaluate various design aspects on a product, which in this case is trade offs for a pocket pager.

When Time Is Money ...

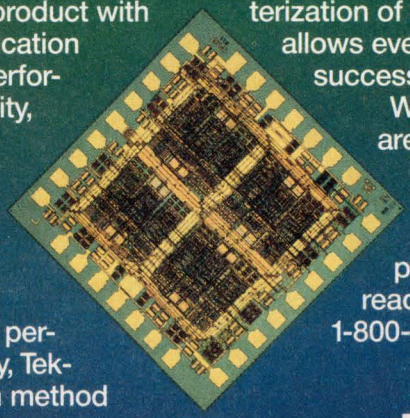
Tektronix QuickCustom™ ASICs

Tektronix' QuickCustom ASICs make it easy for you to create your own analog designs fast. And error free.

Our high speed QuickCustom family of bipolar products, together with Tek's QuickCustom design system, help ensure that your design works right the first time, reducing development time and cutting costs.

◆ Tektronix QuickChips™ help you move from concept to finished product with minimum design and fabrication time. ◆ For even higher performance and greater flexibility, the Tektronix QuickTile™ design method offers standard building blocks for fast implementation of analog and mixed signal functions. ◆ And finally for optimum performance and functionality, Tektronix' Full Custom design method is also available.

All three QuickCustom products provide convenient access to our high performance bipolar process (f_T = 8.5 GHz and $LV_{CEO} \geq 8$ V) with Schottky diodes, JFETs, NiCr resistors, and PNPs. Typical applications include high speed data converters, L-Band amplifiers and mixers, and low noise transducer amplifiers. Our advanced QuickCustom design system, which includes complete CAD tools, thorough characterization of all devices, and support, allows even the first time user to successfully complete the design.

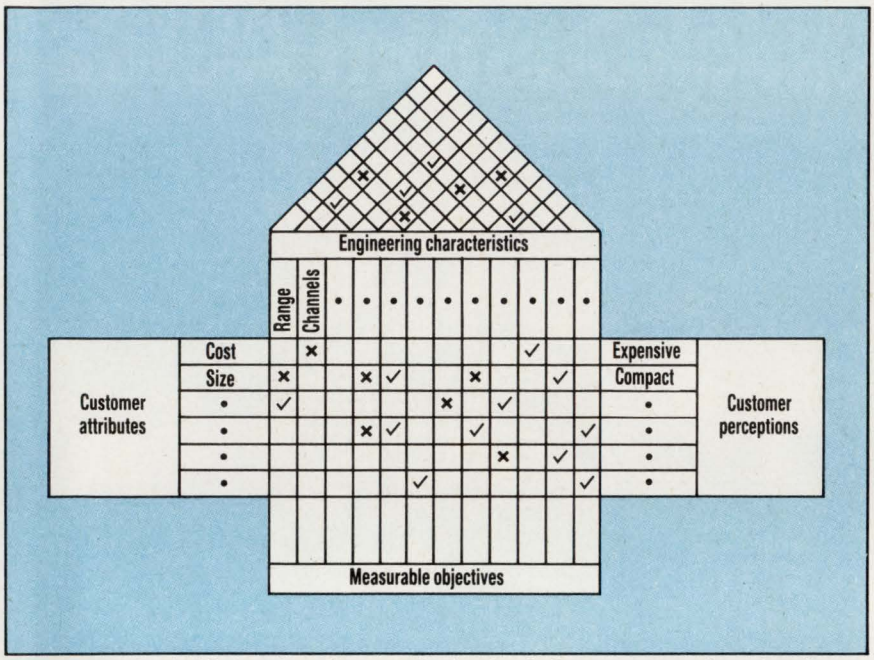


When time and performance are critical, choose QuickCustom from Tektronix. Your quickest solution.

For more information, please circle our reader number, or call 1-800-835-9433, extension ICO.

Tektronix®
COMMITTED TO EXCELLENCE

CIRCLE 129



5. A more complex decision matrix employs a quality-function-deployment conceptual map that allows more inputs and more degrees of relationships than previously possible with a spreadsheet. Relative importance values are assigned to the customer attributes on the left while the column on the right links the attributes to customer perceptions. On the top, various engineering characteristics are also added into the evaluation through the "roof" matrix that ties everything together.

that decisions made early in the process consider the whole product life? (For example, including the side effects and downstream effects of decisions.) How can the team take advantage of change during the detailed design and production phases while remaining consistent with the goals of the project? (e.g., new components, fabrication technologies, services, ...) Are there technologies that will provide the support required to enable better decisions earlier in the process?

Systems engineering tools and product information management systems do exist on the market today. These technologies are definitely in their infancy, but they hold the promise of allowing project teams to start answering these kinds of questions. Instead of diving into the different approaches these tools take, it's best to observe some simple examples of how this information can be represented and analyzed.

One way of organizing this product and project information is in a form of a decision table *(Fig. 4)*. The desired customer attributes are listed with their respective priorities along the left side of the table, and the initial engineering decisions are shown along the top edge of the table. The table could then be filled with checks or crosses that indicate positive or negative correlations between that what the customer wants and the various engineering characteristics. Such a matrix could be easily represented in a spreadsheet.

If the table is applied to the pager example suggested earlier, the choice of lithium batteries would probably increase the list price of the pager, even though it's likely to result in longer operating time and smaller size. On the other hand, it appears that the only benefit of adding more memory to the pager would be more off-line storage for phone numbers, which is a potential detriment to price, operating time, and size. Given the priorities shown, it seems that the change to lithium batteries will bear much more fruit than adding more memory to the pager.

The decision table is somewhat simplistic in the kind of product information being represented and the decision process involved. However, it does serve to illustrate the kind of thinking the project team needs to go through before spending too much in time and resources. In fact, the table can be extended to include values for benefits of a positive correlation vs. costs of a negative correlation. In addition, the correlation itself cou$d go beyond simple checks and crosses to give some indication of the degree of correlation (e.g., strong positive or weak negative). This would allow relatively important estimates of any one engineering characteristic to be computed, enabling the project to focus on the key success factors.

The concept of concurrent engineering has become closely tied to a related concept: Quality Function Deployment (QFD).

Quality: The Final Frontier

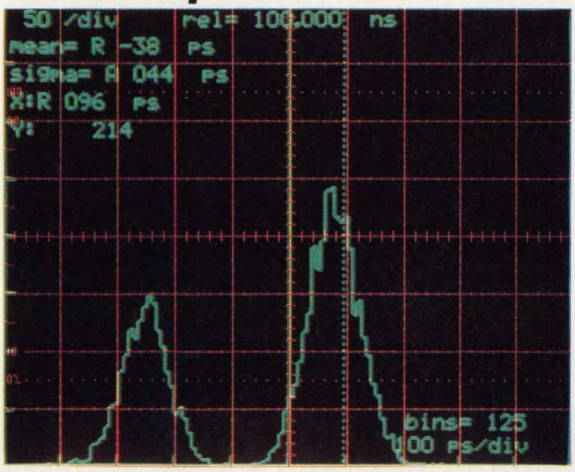
The concept of concurrent engineering has become closely tied to a related concept: Quality Function Deployment (QFD), which radically restructures the way products are defined and built. Ultimately, automated concurrent engineering must accommodate and integrate the paradigm of QFD.

At the core of QFD is a conceptual map that links with customer requirements *(Fig. 5)*. The left-hand rows list customer attributes and assign numbers that list the significance of each attribute. The right-hand rows link these attributes to customer perceptions of how the current product is viewed in the marketplace compared to others. The columns on the top list all engineering characteristics related to these attributes. At each appropriate point in the resulting matrix, a value is entered that suggests either a positive or negative correlation, or no correlation at all. The rows at the bottom list measurable objectives, such as power consumption, and so on.

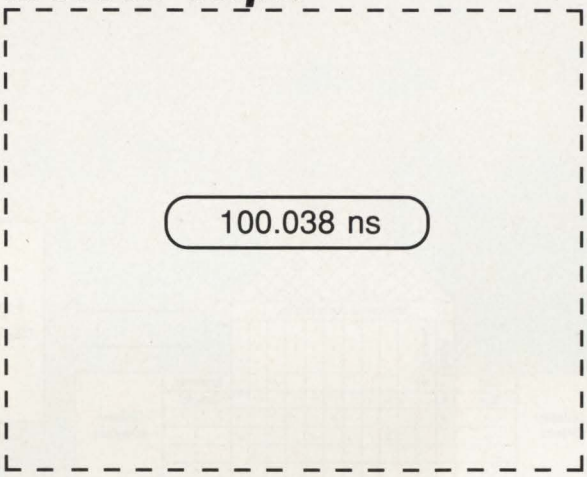
Finally, all of the information is tied to together through the "roof," which is a matrix that defines the relationships between engineering

A picture is worth a thousand points in a time interval measurement.

SR620 Output



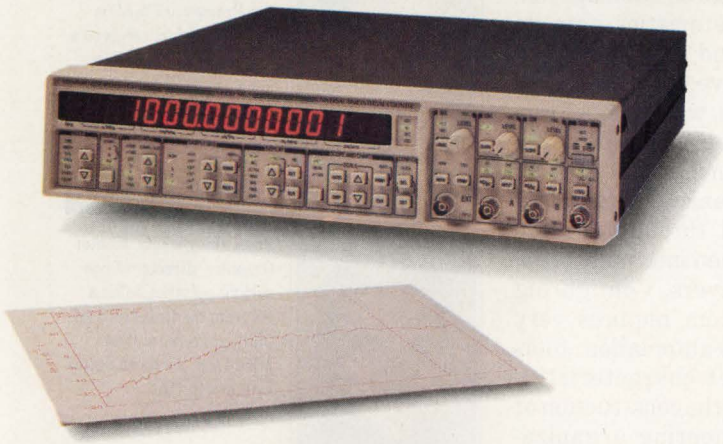
HP5370B Output



The SR620 brings graphic statistical analysis to time interval and frequency measurements. The SR620 shows you more than just the mean and standard deviation - multimode frequency distributions or systematic drift for example. Histograms or time variation plots are displayed on any X-Y oscilloscope, complete with Autoscale, Zoom, and Cursor functions. Hardcopy to plotters or printers is as easy as pushing a button.

Of course, the SR620 does everything else you'd expect from a high resolution universal counter, such as frequency, period, time interval, pulse width, rise / falltime, and phase measurements. The SR620 offers 25 ps single-shot time and 11 digit frequency resolution and complete statistical analysis, all for a fraction of the cost of comparable instruments.

For the whole picture, call SRS and ask about the SR620.



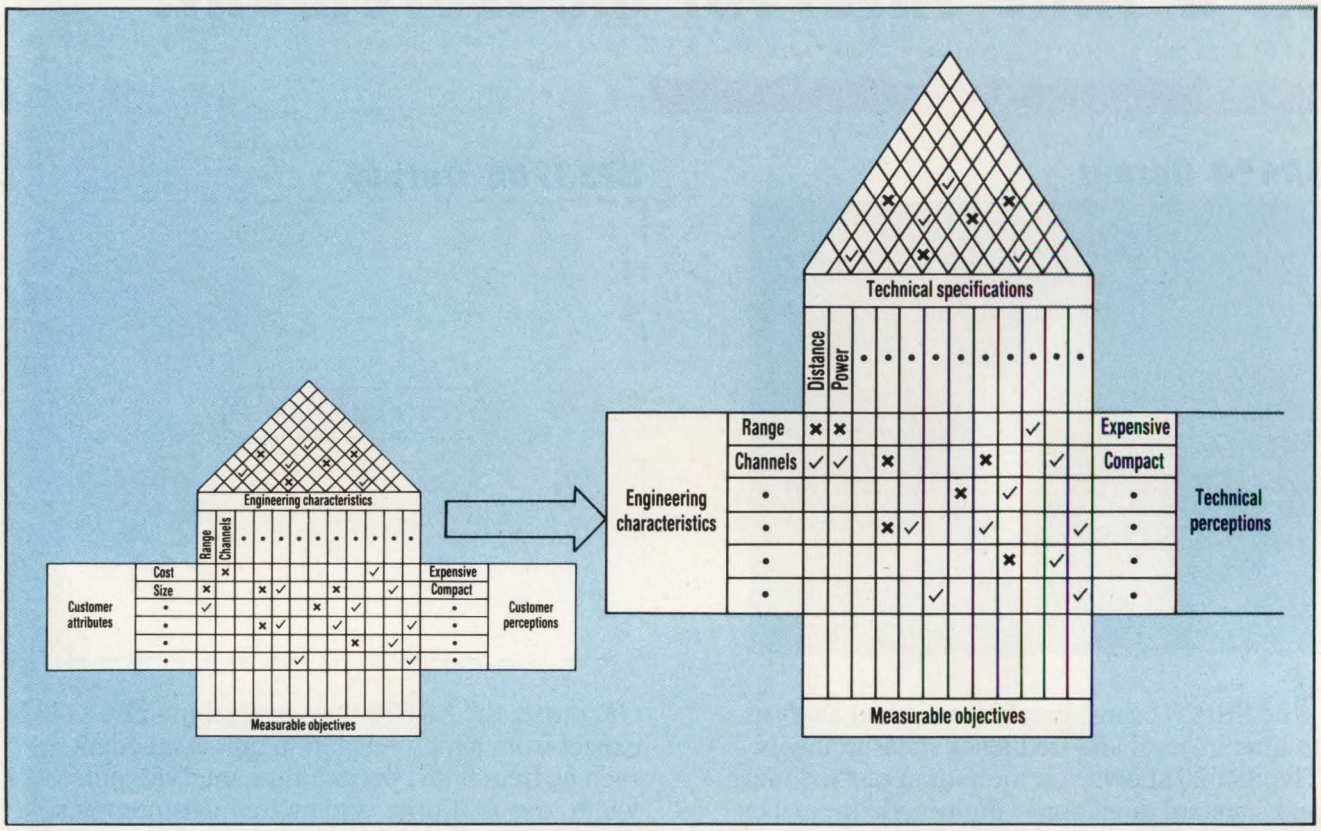
SR620 $4500

- 4 ps single shot least significant digit
- 25 ps rms single shot resolution
- 1.3 GHz maximum frequency
- 10^{-9} Hz frequency resolution
- Sample size from 1 to 1 million
- Frequency, period, time interval, phase, pulse width, rise and fall time
- Statistics - mean, standard deviation, min max, and Allan variance
- Analyzer display on any X-Y oscilloscope
- Hardcopy to printer or plotter
- GPIB and RS232 interfaces
- Optional oven timebase

SRS **STANFORD RESEARCH SYSTEMS**

1290 D Reamwood Avenue, Sunnyvale, CA 94089 TEL (408) 744-9040 FAX 4087449049 TLX 706891 SRS UD

CIRCLE 128



6. Multiple levels of QFD mapping charts can be employed on complex products to develop a hierarchy of trade offs at each stage of a product's definition/development.

characteristics and defines the degree of reinforcement or conflict between them; in other words, the tradeoffs. In practice, engineers can go to areas of conflict—product weight vs. battery life, for instance—and refer back to customer requirements when designing solutions. In one case, it might turn out that customers place a large premium on battery life compared to weight, and that a solution optimizing battery life is preferable.

One approach to QFD and other similar forms of analysis is the use of conventional spreadsheets. Unfortunately, spreadsheets are rather cumbersome and make it difficult to manage the resulting data. To make things easier, several software packages are now available that automate QFD data entry through user-friendly forms and format the QFD conceptual map.

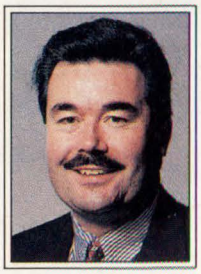
More importantly, existing QFD applications tend to be isolated, standalone systems. To bring the true value of QFD into the design process, it should be integrated with ACE. When that happens, the QFD concept map can be extended to an even deeper level *(Fig. 6)*. All of the items from the engineering characteristics column should in turn be fed into concept maps for each engineering discipline. In these submaps, engineering characteristics now go into the right-hand rows and such items as alternative technologies go in the top columns, with the roof representing the trade-offs within the particular discipline.

In such an organization, all disciplines are linked through the top QFD layer, and then internally organized in lower layers. Configuring this type of system requires very high-level design-automation tools with spreadsheet characteristics that help simplify the construction of automated engineering organizations. Once this type of system is set in motion, it needs the resources of a data scheme that manages product, process, and organizational information. In turn, the PPO model needs the resources of a design-automation framework that supplies the fundamental integration of tools, data, platforms and interfaces.□

JOSE DECASTRO

Jose DeCastro, product and technical marketing manager for the decision support system component of Mentor Graphic's Falcon Framework for Concurrent Design, received a BSEE degree from Nanyang Technological Institute, Singapore.

PETER HOOGERHUIS



Peter Hoogerhuis, Mentor Graphics' director of consulting services, holds a BS from the University of Calif. at Irvine and an MBA from Portland State University, Ore.

HOW VALUABLE?	CIRCLE
HIGHLY	544
MODERATELY	545
SLIGHTLY	546

WILL COMPUTER-AIDED SOFTWARE ENGINEERING COME OF AGE IN THE 1990s?

LAGGING ABOUT FIVE TO SEVEN YEARS BEHIND THEIR CAE COUNTERPARTS, CASE TOOLS WILL EVOLVE IN A SIMILAR FASHION.

READ T. FLEMING

Cadre Technologies Inc., 222 Richmond Street, Providence, RI 02903 (401) 351-5950

In the last decade, CASE (usually defined as Computer-Aided Software Engineering) has emerged as a highly touted technology for building software and systems. Vendors have offered software developers hundreds of products claiming to do CASE. However, with all of the hype surrounding this topic, the perceptive potential user would do well to pause and ask a couple of fundamental questions:

Is CASE the revolutionary advance that many proponents make it out to be? Or is it just a buzzword, another bottle of snake oil for desperate software developers?

The answer is it's neither. CASE simply combines two other emerging and evolving disciplines: software engineering and design automation. By keeping this in mind, you'll gain a realistic understanding of CASE, where it stands today, and where it's going.

The term "software engineering" was widely used after NATO-sponsored conferences highlighted the subject in 1968 and 1969. Although CASE has come remarkably far in the two decades since then[1], it still struggles to become a true engineering discipline, involving much art and personal style.

Many life-cycle models for software development have attempted to show how it's done. Despite differences in the models and the debate about their relative merits, most experts agree that any software-engineering process must include the following essential activities:

Requirements analysis: Determine what the system is supposed to do.

Design: Transform a specification of what the system is to do into one of how it's going to do it.

Implementation: Create the actual product—this is what is usually meant by programming.

Validation: Ensure that you're building the right product.

Verification: Make sure that the product is built right; that is, it meets the requirements.

Configuration Management (CM) and Version Control (VC): Maintain the development histories of individual parts of the system (VC) and their relationships within aggregates (CM).

Documentation: Record engineering decisions for those who must maintain the system, and create training and reference materials for those who use it.

Project management: Plan and track the course of development.

Today, we accomplish these activities in many ways, which is reflected in the broad range of CASE tools that are available. Software engineering is in the experimental stage, like aeronautical engineering was in the first half of this century. For example, most current standard methods don't yet have a rigorous theoretical or semantic basis, but they make sense to engineers and they work. Anything new, no matter how rooted it might be in "science," must meet these simple criteria to be successful. And to find out if it works, it must be tested.

The Object-Oriented Frenzy

An example of a software methodology is the current interest in object-oriented technology. This is software's equivalent of oat bran: there's a strong marketing push behind it and, while few truly know if it's good for you (or if too much of it can kill), everyone feels compelled to consume it.

Object-oriented methods are simply ways to partition a problem and give structure to its solution. The first object-oriented programming languages (Simula and Smalltalk) were conceived more than twenty years ago. It's only now that we're broadly experimenting with and validating object-oriented technology. The marketing frenzy will die down as significant results are reported. In fact, this process is already starting, and it's becoming clear that object orientation will probably be the biggest influence on analysis, design, and implementation over the next three to five years. A good engineer in the future, drawing on the knowledge that we're accumulating, will know when to use object-oriented technology—and when not to.

However, object orientation isn't the only trend in software engineering. Other areas are also gaining interest:

"Rapid prototyping" combines implementation (constructing a prototype) with validation (testing it to see if it's what the customer wants). Until now, most rapid prototypes have been user interface mock-ups. A very different but complementary form of prototyping is to "simulate" an executable specification or model. This helps to validate the system architecture at a high level of abstraction and to predict its performance early in the development cycle. Expect to see a number of simulation products in the next few years that

are based on methods already familiar to CASE users.

After a decade of obscurity, "formal mathematical specification" is making a comeback[2]. The idea is to make an implementation correct by construction and avoid the massive testing that has become the traditional way to verify software. The challenge to proponents is to make this technology understandable to the average software engineer.

The realization by many that "you can't control what you can't measure" has made metrics a hot topic. The debate—what to measure and what to infer from the numbers—will continue to rage until we can agree on what we mean by "software quality." Such agreement will take a few more years.

"Software reuse" is shaped more by economic and socio-organizational issues than technological ones. Large-grained (program, subsystem, library, specification) reuse exists today, and there will be more in the future as organizations realize that it's often less expensive to buy than to make. Much of the handwringing about this issue focuses on the lack of a small-grained, implementation software-components industry. However, we should ask ourselves if this lack is really a problem, since no one has yet shown that the payoff from this level of reuse is worthwhile.

Related to reuse is "reverse engineering." It's relatively easy to extract structure from an implementation, and turn ugly bad code into nicely formatted bad code. The next three years will see many tools do just that. However, what buyers really want is automated "software archaeology."

The tools will help in eliciting the structure, but they're subordinate to the much more difficult intellectual task of extracting intent. Organizations must decide whether this effort is worthwhile.

You might note that the earlier run-down of software-engineering activities is fairly generic and could be applied to a wide range of creative disciplines. What is it that makes software so special and such a challenge? Why is it that successful engineering project managers with a decade or more of experience find software-intensive development projects so unmanageable? And, why doesn't CASE fix the problem?

Two broad answers can answer those questions. First, software engineering is a young discipline that's not widely practiced. It takes time for a discipline to develop a base of knowledge and a collective wisdom, and then make that the common knowledge of individuals and organizations. It even takes time to develop standard terminology *(see "Notation, method, and methodology," above)*. Second, we consistently underestimate the complexity of the problems to which we apply software.

There is a wide range of organizations using software engineering that have varying levels of expertise and sophistication. *(see "The seven stages of expertise," p. 101, and "The five ages of methodological sophistication," p. 102)*. Most organizations, however, are still relatively unsophisticated. For them, introducing CASE tools is likely to have little or no positive effect.

There is one simple reason for this lack of effect: If development process isn't understood, it cannot be automated. Software engineering must be learned first; throwing technology at the problem isn't a solution.

Although, improving the application of software engineering principles has not been easy, individuals and organizations are making progress.[3]. These positive experiences add to our knowledge base and collective wisdom, while competitiveness forces others to advance. In this way, the technology moves forward.

NOTATION, METHOD, AND METHODOLOGY

Three terms are commonly heard in discussions about CASE tools, especially those for requirements analysis and design—Notation, Method, and Methodology. Yet, it appears that mose CASE users (and a number of self-proclaimed Software Engineering Experts) confuse their meanings. It's not surprising, given the way the CASE industry has, like many other new technologies, abused the English language. Here are three definitions to help straighten things out:

A *Notation* is a means to organize and express an idea.

A *Method* is a set of techniques, rules, and guidelines for tackling the problem, measuring the quality of a solution, and expressing it with a notation.

A *Methodology* is an ordered set of tasks that apply methods to get one from a starting point (e.g., customer request) to an end point (deliverable product) in the development process.

Today, the majority of CASE tools are still at the notation support stage (schematic capture, in CAE terms). Most of those going beyond that level support one or more methods (and by implication their associated notations), and leave methodology concerns to another part of the development environment.

Users can quickly test a claim by comparing the actual product (and not the vendor supplied feature list) against the definitions that are explained above.

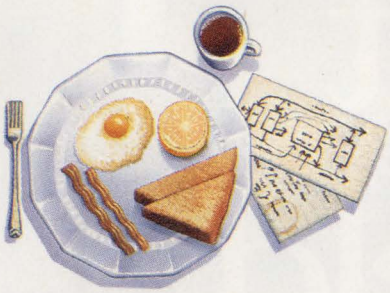
We can expect CASE to be included in concurrent engineering, which until now has been the exclusive domain of the traditional CAD disciplines.

Dealing With Complexity

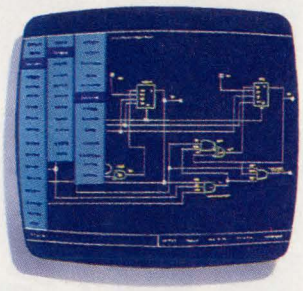
Even if we were all experts living in an Age of Software Engineering, each project would still have to deal

Food For Thought About Field Programmable Gate Arrays.

Be Brilliant At In Productio

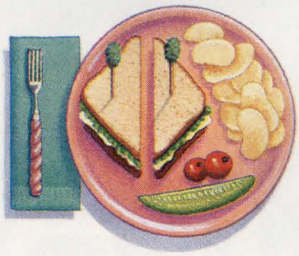


7:05 am : Breakfast
Suddenly, between bites, the answer to that new system design jumps right into your brain. But how to make it work in silicon? Use an Actel field programmable gate array!



8:50 am : Design
You warm up the design program on your 386 and put in the final touches. Then a quick rule check and 25 MHz system simulation with the Action Logic System software.

11:00 am : Place & Route
You watch the system place and route all 1700 gates (out of 2000 available) in under 40 minutes. 100% automatically! A final timing check. Then think of something to do until lunch.



12:00 pm : Lunch
Remember lunch? Normal people actually *stop working* and have a nice meal—right in the middle of the day! With Actel's logic solution, this could become a habit.

Actel Field Programmable Gate Array Systems.

They're a feast for your imagination.

Actel's ACT™ 1 arrays bring you a completely new approach to logic integration. Not just another brand of EPLD, PAL® or LCA™ chips. But true, high density, desktop configurable, channeled gate arrays.

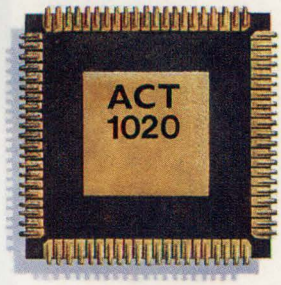
They're the core of the Action Logic System, Actel's comprehensive design and production solution for creating your own ASICs. Right at your desk. On a 386 PC or workstation. With familiar design tools like Viewlogic,™ OrCAD,™ and Mentor.™

And do it in hours instead of weeks. Even between meals.

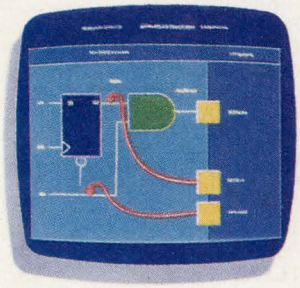
How? With features like 85% gate utilization. Guaranteed. Plus 100% automatic placement and routing. Guaranteed. So you finish fast, and never get stuck doing the most

Actel FPGA Product Family		1010A	1020A
Equivalent Gates	Gate Array	1200	2000
	PLD/LCA	3000	6000
User I/O		57	69
System Clock (MHz)		20-40	20-40
Availability		NOW	NOW
Technology (micron)		1.2	1.2

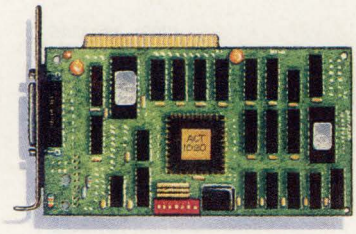
Breakfast And n By Dinner.



1:15 pm: Program
You load the Activator™ programming module with a 2000-gate ACT 1020 chip and hit "configure." Take a very quick coffee break while your design becomes a reality.



1:25 pm: Test
You do a complete, real-time performance check, with built-in test circuits that provide 100% observability of all on-chip functions. *Without* generating any test vectors.



4:00 pm: Production
Your pride and joy is designed, created, tested, and off to the boys in Production. And you're finished *way* ahead of schedule! Better think of something to do until 5:00.

6:00 pm: Dinner
Remember dinner? Normal people actually *go home* and eat with their families. On your way, start thinking about how Actel's logic solution can help you be brilliant tomorrow.

tedious part of the job by hand.

Design verification is quick and easy with our Actionprobe™ diagnostic tools, for 100% observability of internal logic signals. Guaranteed. So you don't have to give up testability for convenience.

In fact, the only thing you'll give up is the NRE you pay with full masked arrays. You can get started with an entry level Action Logic System for under $5000. Guaranteed.

And Actel FPGAs are even 883 mil-spec compliant.

You can be brilliant right now with 1200- and 2000-gate devices, and a whole new family of 8000-, 4000- and 2500-gate parts are on the way. Call **1-800-227-1817, ext 60** today for a free demo disk and full details about the Action Logic System.

It could make your whole day.

Actel

Risk-Free Logic Integration

ACTEL CORPORATION DIRECT SALES OFFICES

955 E. Arques Ave.
Sunnyvale, CA 94086
Tel: (408) 739-1010

8130 McFadden Ave., Suite 109
Westminster, CA 92683
Tel: (714) 373-4488

425 N. Martingale Rd., Suite 800
Schaumburg, IL 60173
Tel: (708) 706-3866

1740 Mass Avenue
Boxborough, MA 01719
Tel: (508) 635-0010

9101 Guilford Road, Suite 107
Columbia, MD 21046
Tel: (301) 604-0111

2350 Lakeside Blvd., Suite 850
Richardson, TX 75082
Tel: (214) 235-8944

DOMESTIC REPRESENTATIVES

ALABAMA
Rep Inc. (205) 881-9270

ARIZONA
Luscombe Engineering (602) 949-9333

CALIFORNIA
Centaur Corporation (Calabasas) (818) 704-1655
Centaur Corporation (Irvine) (714) 261-2123
Centaur Corporation (San Diego) (619) 278-4950
I^2 Inc. (Santa Clara) (408) 988-3400
I^2 Inc. (Orangevale) (916) 989-0843

COLORADO
Luscombe Engineering (303) 772-3342

CONNECTICUT
CompRep Associates (203) 269-1145

FLORIDA
Sales Engineering Concepts (Altamonte Springs) (407) 682-4800
Sales Engineering Concepts (Deerfield Beach) (305) 426-4601

GEORGIA
Rep Inc. (404) 938-4358

ILLINOIS
Carlson Electronic Sales Associates (708) 956-8240

INDIANA
Giesting & Associates (317) 844-5222

IOWA
Carlson Electronic Sales Associates (319) 378-1450

KANSAS
DLE Electronics (316) 683-6400

MARYLAND
New Era Sales (301) 544-4100

MASSACHUSETTS
CompRep Associates (617) 329-3454

MICHIGAN
Giesting & Associates (Livonia) (313) 478-8106
Giesting & Associates (Comstock Park) (616) 784-9437

MINNESOTA
Gibb Technology Sales (612) 835-3370

MISSOURI
John G. Macke Co. (314) 432-2830

NEW JERSEY
Nexus (201) 947-0151

NEW MEXICO
Luscombe Engineering (505) 888-0333

NEW YORK
L-MAR Associates (Apalachin) (607) 687-1828
L-MAR Associates (E. Rochester) (716) 381-9100
L-MAR Associates (Poughkeepsie) (914) 462-8025

NORTH CAROLINA
Rep Inc. (Charlotte) (704) 563-5554
Rep Inc. (Morrisville) (919) 469-9997

OHIO
Giesting & Associates (Cincinnati) (513) 385-1105
Giesting & Associates (Cleveland) (216) 261-9705
Giesting & Associates (Columbus) (614) 486-5616

OREGON
L^2 Ltd. (503) 629-8555

PENNSYLVANIA
Omega Sales (215) 244-4000

TENNESSEE
Rep Inc. (615) 475-4105

TEXAS
OM Associates (Austin) (512) 794-9971
OM Associates (Houston) (713) 789-4426
OM Associates (Richardson) (214) 690-6746

UTAH
Luscombe Engineering (801) 565-9885

WASHINGTON
L^2 Ltd. (206) 827-8555

WISCONSIN
Carlson Electronic Sales Associates (414) 476-2790

CANADA
Clark-Hurman Associates (Quebec) (514) 426-0453
Clark-Hurman Associates (Ontario-Brampton) (416) 840-6066
Clark-Hurman Associates (Ontario-Nepean) (613) 727-5626

INTERNATIONAL DISTRIBUTORS

AUSTRALIA
Reptechnic (Neutral Bay, NSW) (2) 953.9844

BELGIUM
Acal Auriema N.V.S.A. (Zavenlem) (2) 720.5983

DENMARK
Nordisk Electronik AS (Herlev) (42) 84.20.00

EGYPT
SEE (Cairo) (2) 665.948

ENGLAND
Gothic-Crellon Ltd. (Wokingham) (0734) 78.88.78
Manhattan Skyline Ltd. (Maidenhead) (0628) 75.85.1

FINLAND
OY Fintronic AB (Helsinki) (0) 69.26.022

FRANCE
ASAP (Montigny Le Bretonneux) (1) 30.43.8233
SCAIB S.A. (Meylan-Zirst) (76) 90.22.60
SCAIB S.A. (Rungis Cedex) (1) 46.87.2313

HONG KONG
Twin-Star Trading Co. (Yau Tong Industrial City) (852) 346.9085

INDIA
Benchmark Systems (Madras) (44) 413.866

ISRAEL
A.S.T.Ltd. (Herzlia). (52) 58.33.55

ITALY
LASI Elettronica S.p.A. (Milan) (3) 499.8351

JAPAN
Innotech Corporation (Tokyo) (3) 499.8351
Matsushita Electronics Corporation (Kyoto) (75) 951.8151

KOREA
Eastern Electronics, Inc. (Seoul) (2) 566.0514

NETHERLANDS
Transfer B.V. (Enschede) (53) 33.43.81

NORWAY
Nordisk Electronik AS (Hvalstad) (2) 84.50.70

SPAIN
Semiconductores S.A. (Barcelona) (93) 217.23.40
Semiconductores S.A. (Madrid) (1) 742.2313

SWEDEN
Traco AB (Farsta) (8) 93.00.00

SWITZERLAND
Omni Ray AG (Dietlikon) (1) 835.21.11

TAIWAN
SEED TECH Corporation (Taipei) (2) 521.1100

WEST GERMANY
bit-electronic AG (Munich) (089) 41.80.070
ECN Component Network (Ismaning) (089) 96.09.080

DOMESTIC DISTRIBUTORS

Actel products can be purchased from the major distributors listed below:
Wyle Laboratories: call (714) 851-9953 for the number of the office nearest you.
Pioneer Standard Electronics and **Pioneer Technologies:** call (516) 921-8700 for the number of the office nearest you.

CIRCLE 80

with the complexity of the problem at hand. Theoreticians express digital system complexity as the minimum product of space (transistors or bits of memory) and time necessary to solve the problem. Engineers' intuition and experience often tells them when a problem is easy or hard, and when a solution is too complex (overkill) or maybe too simple.

An example of a complex solution to a simple problem is using a microcontroller in the control of an automatic dishwasher. Traditionally, control is accomplished with an arrangement of rotating cams and relays. An electronic solution might replace the cams with a four-bit microcontroller with 1 kbyte of read-only memory. While the electronic solution might make economic sense, it's overkill from a complexity standpoint, because the problem doesn't demand that level of computing power. On the other hand, a software engineer might be quite happy: the problem is small, bounded, and there's excess capacity in both time and space.

Unfortunately, most software problems don't have these properties. An example of a very complex software-based system is the new National Airspace System[4], which will control aircraft traffic throughout the continental U. S. Like many systems, it's partitioned so that software does the functions that are too hard, expensive, or changeable to do in hardware. The system must operate in real time. This constrains the time side of the complexity equation, while space is constrained by hardware and memory decisions that were made before the software was even designed. Such approaches pose a continuing challenge to engineers and their managers, and make software development seem harder than it ought to be.

Design Automation

Another kind of complexity is that inherent in the development process itself. For example, tracking the versions and configurations of work products can be a very complex task. Design automation, used in the broad sense, is an aid to managing all kinds of complexity. It's an essential tool in the battle for intellectual control of a project. As electronic designers have found, many products could not be built without it.

Regardless of the problem domain and level of abstraction, a system for design automation must support these tasks:

Capture: Get the design into the system.

Traversal: Allow users to move around in and make queries of the design space.

Partitioning: Help designers (re)organize the design into manageable units.

Rule checking: Measure the design against conformance and consistency rules.

Simulation: Execute a design at some level of abstraction to better understand its behavior.

Synthesis: Transform a design from one form to another (typically to a lower level of abstraction).

Process management: Help designers and others stay within an engineering methodology.

CASE tools are, in many ways, where electronic CAD tools were about five to seven years ago. They will also evolve in a similar way: competition will force (and advancing hardware technology will allow) CASE vendors to offer more breadth of coverage, depth, and more capacity for the same or lower cost than today's tools.

A majority of today's analysis and design CASE tools only perform capture and traversal. Within this group of tools, most are intended for data entry and drafting, and provide little direct help to designers. Most DOS PC-based CASE tools fall into this category, and could be classified as documentation aids. Over the next three years, these single-user products will become a commodity, as has happened with schematic capture tools, and prices will fall precipitously.

Tools at the next level of sophistication help with partitioning and rule checking, in addition to doing design capture and traversal. To accomplish this, tools must deal with methods. This is where CASE tools have an effect on the market for methods, and therefore the course of software engineering. For a new method to gain wide acceptance by software engineers, it must have adequate tool support. Such support doesn't guarantee acceptance, but it is a necessary condition.

Some see this as an opportunity for creating rule-based CASE products that could, in theory, be adapted to any method. Advocates claim that users would then potentially have their own set of methods. Opponents to this approach point out that there are too many methods now, and that adding more just makes the problem worse. It's likely that CASE vendors will take a middle path, where the technology will be used to support variations in standard methods.

A few CASE tools support simula-

THE SEVEN STAGES OF EXPERTISE IN SOFTWARE ENGINEERING

A person's success in using software engineering depends on the underlying methodological knowledge that he or she possesses. A typical person passes through each of the stages in sequence, spending a period ranging from a few months to a few years in each stage. If you asked them what they know about software engineering, you might get the following responses:

1. Innocent: "Never heard of it."
2. Exposed: "I read an article."
3. Apprentice: "I took a course,"
4. Practitioner: "I've applied it seriously, but I probably need help."
5. Journeyman: "I use it all the time. It works for me."
6. Expert: "I've been doing it for a long time and successfully train others."
7. Researcher: "Have you seen my latest book on the subject."

You might get the last response from a person at any stage of expertise, so caution is advised.

This categorization is from Meilir Page-Jones of Wayland Systems Inc. For a more complete treatment, see reference listing no. 5.

tion. This requires rigorous semantics that most analysis and design methods lack. CASE suppliers have followed the methods experts and are codifying the rules that make this level of design automation possible.

Simulation gives CASE something to offer to systems engineers, and in the process, brings CASE and electronic CAE closer together. As software is already a critical part of most electronic products, expect CASE to be included in concurrent engineering, which until now has been the exclusive domain of the traditional CAD disciplines. This will take several years—CASE and concurrent engineering are exceedingly complex on their own.

Excluding compilers, the largest number of CASE synthesis tools are "code generators." Some generate code skeletons or frames from design information. Others generate all of the code for a program, but the term "generate" can be misleading. To generate code, the design may have to be completed to a level of detail that's equal to the code itself, with all of the effort that entails. On the other hand, some tools really do generate complete programs from a high-level specification. They can do this for a highly constrained design space, where most architectural and policy decisions are made and all applications look similar in implementation. Mainframe Cobol application generators fall into this category of tools. In the near future, we may see these types of tools for other specialized environments, such as programmable industrial controllers.

Process management is a relatively new area for CASE tools. Given the lack of a software process in most organizations, this isn't surprising. However, tool integration, which has close ties to process management, has become one of the most discussed subjects in CASE (as it has in other CAD disciplines), and will remain so for some time. This is because customers want it.

But, integration isn't simple. All parties involved ultimately expect a lot from it: coverage of all software engineering activities; linkage to other disciplines; adaptation to existing and future environments; something that's economical, supportable, easy to use; and so forth. Several groups (including users, integrators, tool builders, framework suppliers, and platform vendors) often have conflicting interests in how integration is done. For integration to become widespread, there must be standards for software interoperability in large, distributed, heterogeneous environments. There also must be some agreements on data integration (where data resides, how it's described, granularity, and so on), and control integration (how tools communicate).

With these expectations, developing comprehensive, high-quality software-engineering environments will be an iterative, drawn-out process. Current integration framework efforts and attempts at standardization should be viewed as experiments. They and their successors will help suppliers determine the technologies that work and make economic sense, and they will help customers prioritize sometimes conflicting requirements.

With all this in mind, here are some predictions for the next three to five years:

- Most advances in integration technology will be incremental in nature, requiring few changes to a user's computing environment, existing tools, way of doing work, or budget. This implies "lightweight" mechanisms, such as message-based control integration.
- Database technology will continue to limit the size of development environments. During this period, we will find out if objected-oriented database technology is help or hype.
- Economics (customers don't like spending money on frameworks), support, and interoperability concerns will make operating system and platform vendors the main suppliers of integration technology. Third-party framework suppliers will survive as consultants and system integrators, or they will cease to exist.

THE FIVE AGES OF METHODOLOGICAL SOPHISTICATION

Organizations, like individuals, also pass through sequential stages as they improve at applying software engineering. Advancement from one stage to the next usually occurs after a major disaster. The percentages are the author's guess at the distribution of sophistication across all development organizations.

A. Age of Anarchy (60%): Anything goes.
B. Age of Folklore (25%): Wisdom is passed from one generation of engineer to another, over beer and pizza.
C. Age of Methodology (10%): The way software is to be engineered is documented, and is actually done that way.
D. Age of Metrics (4%): Both the products and the process are measured in standardized ways.
E. Age of Engineering (1%): Productivity is achieved through continuous quality improvement, much like it is in manufacturing.

If an organization isn't doing software engineering at level C or better, they will have significant problems implementing CASE.

This categorization is from Meilir Page-Jones of Wayland Systems Inc., and is based on work done by the Software Engineering Institute.

WHO'S USING CASE?

When offered software engineering and design automation, what kinds of organizations buy it? This is an important question for CASE users and suppliers. CASE vendors tend to build and sell products that target one, or maybe two market segments. Knowing the customers that drive a vendor make it easier to decide from whom to buy tools, and where new technology might come from.

For our purposes, the CASE market can be divided into four segments:

Management Information Systems/Data Processing (MIS/DP): The applications are generally database oriented, not real-time (on-line transaction processing is a notable exception to the latter). Examples include financial and administrative

reporting, and decision support. The delivery platforms are IBM mainframes, minicomputers, and, increasingly, PCs. The development platform is often the same type as that used for delivery. This is the biggest market for CASE, making it one of the most competitive.

Commercial: This category includes applications that are developed primarily for resale. System software, word processors, CASE tools—all of these are developed by organizations in this market segment. Obviously, the platforms for delivery and development can be almost anything. This diversity combined with the not-invented-here syndrome that pervades many such organizations makes it a very difficult market segment for CASE vendors to penetrate.

Technical: Applications are technically oriented, often real-time or numerically intensive. Examples include simulation and industrial process control. Delivery and development platforms are often the same, typically in the form of minicomputers, workstations, or PCs. The technical market isn't as big as the MIS/DP market, but on average, the users are more sophisticated in the ways of software engineering and are more willing to invest in tools. For this reason, most leading-edge CASE technology is targeted at this segment.

Embedded: The term means that a computer is in the product, but it's not the actual product. Sometimes, industry analysts consider this a part of the technical market segment because the customers and applications overlap so much. Applications include telecommunications, avionics, and just about anything with a microprocessor inside that doesn't call itself a computer. Development platforms are similar to those used in the technical market. The biggest challenge concerning software engineering and CASE is that these are the "mission-critical" systems that we increasingly depend on for safe, reliable operation.

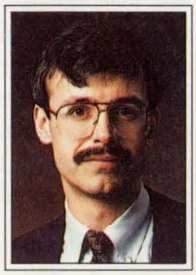
Market analysts believe that the penetration of CASE into any of these market segments varies on the low side, at about 5 to 20%. Technology isn't holding back CASE, but rather the limited use of software engineering. The leading CASE vendors recognize this problem and give educational services a high priority. Customers are responding by buying training (from many sources) and putting it to work immediately. The result is a win-win situation: the customers are more likely to have successful projects, and the vendors get success stories and happy users. This translates into greater sales.

Plenty of technical challenges still face CASE suppliers in the coming decade. We'll find out what works and what doesn't in object-oriented technology, if simulation can take the guesswork out of systems engineering, if formal specifications can replace testing, if we can build seamless tool integration, if we can handle extremely large projects... It's going to be exciting.□

References

1. Shaw, M., "Prospects for an Engineering Discipline of Software," IEEE Software, Vol. 7 No. 6 (November 1990): 15-24.
2. Woodcock, J., and Loomes, M., *Software Engineering Mathematics* (Mass.: Addison-Wesley, 1990).
3. Cobb, R.H., and Mills, H.D., "Engineering Software under Statistical Quality Control," IEEE Software, Vol. 7 No. 6 (November 1990): 44-54.
4. Pozesky, M.M. (ed.), Special Issue on Air Traffic Control, Proceedings of the IEEE, Vol. 77, No. 11, (November 1989).
5. Page-Jones, M., "The Seven Stages of Expertise in Software Engineering," American Programmer, Vol. 3 Nos. 7-8, (July/August 1990).

READ T. FLEMING



Read Fleming, vice president and fellow of Cadre Technologies, received an ScB in electrical engineering from Brown Univ., Providence, R.I. He cofounded the company in 1982.

HOW VALUABLE?	CIRCLE
HIGHLY	550
MODERATELY	551
SLIGHTLY	552

CAE Technology Report

January 1991
Vol. 2, No. 8

Is U.S. Technological Leadership Threatened?

While some chief executives are concerned over the U.S. losing its technological leadership, others like Stanley Hyduke, President of ALDEC Co., Inc., claim "we are losing only in our erroneous perceptions because we still keep the same scoring system despite that the technology game has changed."

As the competition in the 90's moves from physical manufacturing to information processing, the U.S. software industry will play a major role in increasing the competitiveness of U.S. industry. Software companies such as Microsoft,™ Novell,™ etc., are becoming the core of new U.S. industrial strength. This information processing orientation of U.S. industry will allow it to be very responsive to the fast changing environments of the 90's.

The U.S. is also leading in development of new information processing related technologies that will create new industries within the coming decade. The technology game has changed and the U.S. is still the world's technological avant garde.

Redefined EDA Ready For The 90's

A major change is taking place in the EDA field as vendors try to get their bearings for the 90's. The 90's will be the years of disposable products, niche markets and tight world-wide competition. This requires broad design automation to assure product quality, low design cost and minimum design time. While the 80's were years of EDA gurus, the 90's are the years of EDA for the engineering masses. Easy to use, fully automated and low-cost EDA tools that operate in real-time are the way of the 90's. Such products are already appearing and they sell fast. **Circle 101**

SUSIE is a trademark of ALDEC Co., Inc.
TEL: (805) 499-6867
FAX: (805) 498-7945

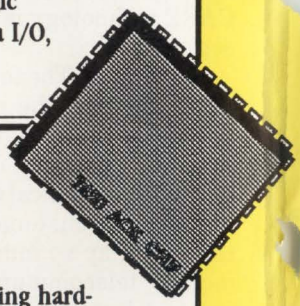
Microsoft, Novell, FutureNet-5, Actel and Xilinx are trademarks of their respective holders.

FPGA-Based Designs Take Only Hours

Designs with multiple Xilinx™, Actel™ and other FPGA and PLD parts can now be instantly simulated with the new SUSIE™ 6.0 logic simulator from ALDEC that simulates these designs with picosecond accuracy. SUSIE allows you to verify FPGA designs, together with other system components, in minimum time because all problems such as timing violations, bus conflicts, etc., are automatically captured and displayed by SUSIE. Since SUSIE compiles all user entries within microseconds, working with SUSIE is like working with real hardware. SUSIE pricing starts at $1995; options and some libraries are extra. (FAX: 805-498-7945) **Circle 102**

New Hot Schematic

One of today's hottest schematic capture products is FutureNet-5™. At $895 ($499-10 pcs), it provides workstation performance on the PC. New features include pop-up menus and dialog boxes, undo/redo, continuous zoom and symbol browsing. It also supports concurrent work by several designers on the same hierarchical schematic. Excellent for FPGA and system-level design, FutureNet-5 works closely with the hot new SUSIE 6.0 logic simulator. Contact Bruce Rodgers, Data I/O, (206) 881-6444. **Circle 106**



Simulators Gain Major Momentum

New logic simulators are closely imitating hardware breadboarding and lab instrumentation. Based on incremental compilation, the simulators respond instantly to the designer's inputs. For example, the designer can replace ICs, change the design of Xilinx parts, load new JEDEC and hex files, etc., all with microsecond speed.

Moreover, the designer can instantly return to previous locations in the simulation process and resimulate the design with new test vectors, different switch positions or with an entire new set of ICs, etc. Some CAE vendors, like ALDEC, report big increases in simulator sales. **Circle 103**

OUTRUNNING THE PACK IN FASTER PRODUCT DEVELOPMENT

HOW COMPANIES CAN OVERCOME 15 COMMON BARRIERS TO TRIMMING PRODUCT-DEVELOPMENT CYCLES

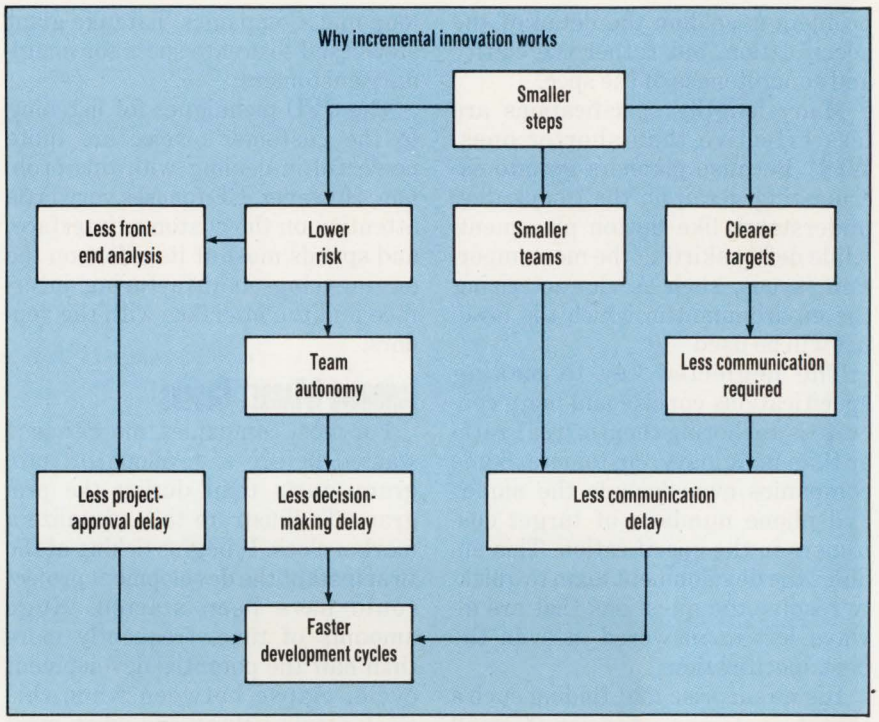
DONALD REINERTSEN

Reinertsen & Associates, 600 Via Monte D'Oro, Redondo Beach, CA 90277-6649; (213) 373-5332.

Achieving rapid product development can be an elusive goal. And as more companies strive for speedy development, gaining a decisive lead in this area becomes even more difficult. The question is: With everyone running on a faster treadmill, how do you stay ahead of the pack?

The best way is to pay attention to problems your competitors ignore. Curiously, companies turning to exciting new techniques to trim development cycles exploit only a few of the opportunities that exist. Such techniques as quality function deployment (QFD) and concurrent engineering (CE) are valuable. But they still leave lots of cycle time on the table.

At least 15 barriers prevent companies from trimming development cycles. Why not clear these barriers while your competition still believes that the development process is simple enough to be fixed with one technique? Let's look at each barrier that hinders speedy development.



1. Taking giant technical steps makes a project riskier, more complex, and more expensive. In contrast, innovating with smaller technological steps is safer, costs less, and trims development time.

Many companies are doomed to fail before they start because they try to pack too much innovation into one product. By going after new applications, in new markets, with new technologies, these companies compound technical and market risk in a way that virtually guarantees late product introductions.

Taking Giant Steps

Giant steps make the engineering task more complex, riskier, and more expensive. The development cycle stretches out, forcing market planners to look even further into the future. But the future is fuzzy. As a result, when we make big, risky bets on a fuzzy future, we spend much time at the front end of the project trying to evaluate and manage risks. This further lengthens the development cycle.

To counter this, Japanese companies and many American firms are turning to incremental innovation *(Fig. 1)*. They take a series of small steps and use actual product introductions to do their market research. Because they make a series of small bets, they don't have to spend months analyzing and agonizing at the beginning of a development program. They manage risk by taking small steps—not by trying to analyze it away or by using complex and time-consuming project-management systems to control it. Neither QFD nor CE addresses this problem.

Hitting Moving Targets

Too many development programs unnecessarily change their target once underway. Changing targets isn't a crime when it's a response to an important and unpredictable change in the market. However, it's a capital offense when all the information to make the correct decision was available from the beginning of the project.

A change in objective is damaging for two reasons. First, it creates rework. Even small changes can ripple through a complex project, causing massive revisions of already completed work. Second, unnecessary changes in objectives demoralize the development team. Members stop running at top speed when the goal keeps shifting to a different end of the field.

Some companies try to safeguard against such changes by making their product specifications more detailed. This rarely works because the

problem is seldom the detail of the specification, but rather the clarity and concreteness of the spec.

Many lengthy specifications are less effective than shorter ones. Why? Because planners go into excruciating detail on the issues they understand, like button placement, while deftly skirting the most important issues, such as characterizing the environment in which the product will be used.

The neglected key to making specifications concise and more concrete is anchoring them on real, rather than imaginary, customers. Some companies even include the names and phone numbers of target customers in the specification. This enables the development team to quickly resolve the questions that are always left unanswered in even the best specifications.

It's no surprise that finding such a target customer is easier if small rather than large steps are taken. Nor is it surprising that a short cycle is less vulnerable to change than a long one. Companies that take giant steps tend to create specs for imaginary customers.

The QFD techniques for listening to the customer's voice are quite powerful in dealing with this problem. However, CE focuses very little attention on the customer interface, and spends most of its effort on the engineering-manufacturing interface and the interface with the vendors.

Ignoring Market Clocks

For most companies, more time is wasted before a development program starts than during the program. To illustrate this, visualize a market clock. It begins ticking at the first instant the development project could have been started. Huge amounts of time, frequently more than half the potential development cycle, elapse between when this clock starts ticking and when most companies put a full team to work on a project.

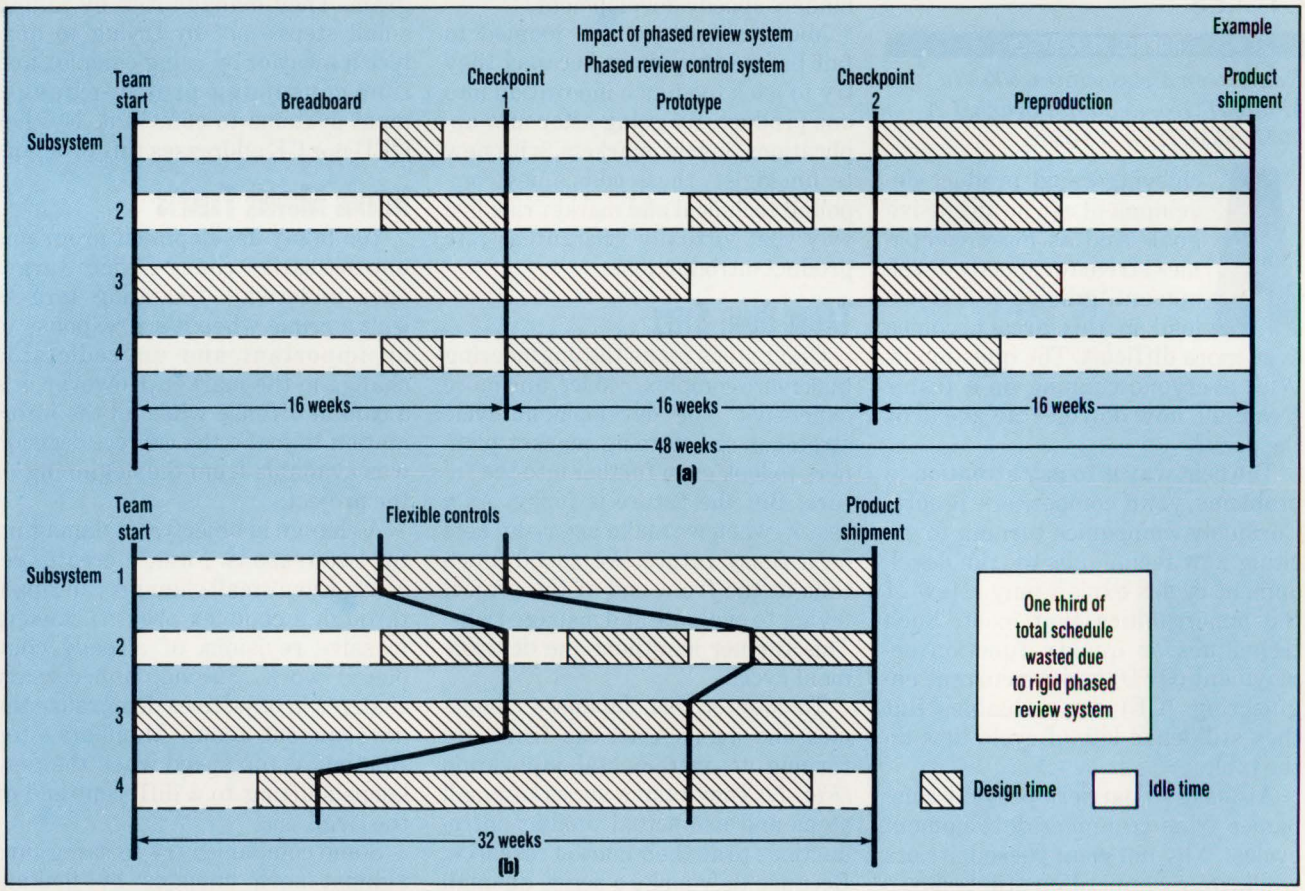
What causes the delays? Getting approval for the project, doing market research, freeing up the team members to do the work? The reasons always sound good, but the result is that some companies start development years after their more agile competitors. No matter how fast you run, you can't win if you start late. Both QFD and CE manage to skirt this problem.

Overloading Capacity

Perhaps the most popular mistake is starting so many projects that the development organization is constantly overloaded. When engineers are assigned to 10 different projects, 9 out of 10 projects sit idle at any moment. In other words, every project spends 90% of its life sitting motionless in someone's in-basket.

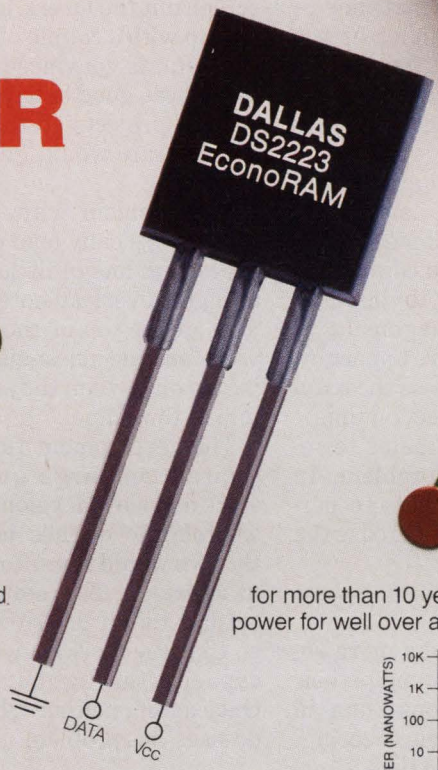
Overload occurs because product ideas are always more abundant than engineering capacity. Nobody likes to make the tough choices of which projects to concentrate on. As a result, we do them all.

Many managements live in a fan-



2. A rigid phased review system is unsuitable for cutting development speed. Progress grinds to a halt for a product with multiple parts or subsystems. When a part completes its activities in a phase, it must stop and wait for all other parts to catch up (a). In contrast, flexible controls cut idle time and reduce overall development time by one-third (b).

MASQUERADING AS A TRANSISTOR



Actually, it's a 256-bit SRAM. Our memory chip is disguised as a 3-pin transistor because the TO-92 case is cheap. Which helps make the DS2223 EconoRAM the lowest cost read/write memory there is.

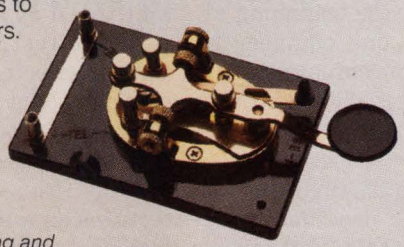
Priced for Everyone

The EconoRAM will set you back a mere 25 cents.* Same as a phone call. And you can have one **FREE** just for asking.

Along with low cost comes low overhead. EconoRAM is small, so it conserves expensive PCB real estate. And it takes up only one microcontroller port pin.

A Single, Very Busy Pin

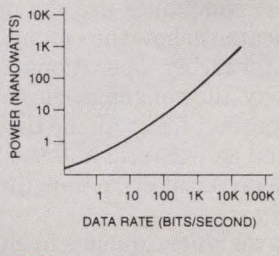
Using a creative multiplexing scheme, EconoRAM reduces address, data, and control lines to one pin. It does this through an internal time measurement reference that compares pulse widths to encode binary numbers. The other two pins are power and ground.



DOT–DASH–DOT... The DS2223 sends and receives data through long and short pulses, like Morse code.

Downright Stingy on Power Consumption

Designed to be made nonvolatile, EconoRAM consumes minute amounts of power: 0.2 nanoamps in standby mode (*typical*) and 36 nanocoulombs to read or write the entire memory! In fact, a pea-sized battery can retain data for more than 10 years and supply operating power for well over a million accesses.



EconoRAM consumes minute amounts of power.

Avoid Identity Crises

To help you keep track of your equipment and components, a special version of EconoRAM (DS2224) includes a serialized ROM in the first 32 of its 256 bits. That ROM is laser-printed with a unique ID code at the time of manufacture in Dallas. The remaining 224 bits are read/write memory for variable data.

If all you need, however, is a unique number, try our two-pin, 64-bit version, the DS2400 Silicon Serial Number. The number acts as a license plate and can be read by probing even when the circuit board isn't powered.

If you're tight on space and short on cash, call us.

For a free sample, call (214) 450-0448.

*In quantities of 100,000.

CIRCLE 93

DALLAS SEMICONDUCTOR
4401 SOUTH BELTWOOD PARKWAY
DALLAS, TEXAS 75244-3292
TELEPHONE: 214-450-0448
FAX: 214-450-0470

tasy world, where they continue to add projects and assign aggressive introduction dates to them. The deadlines are so absurd that they're ignored from the beginning of the project. Management pauses to scratch its head and wonder why projects are late. Then it adds more projects to the list.

Rapid product development requires that engineers be assigned to no more than two development projects at a time. If you assign more projects, expect them to be late. Tough choices by management in setting priorities are more important than tough words to harass the team into completing the project on time.

Neither QFD nor CE helps to reduce this overloading problem. In fact, the time requirements to perform QFD properly may increase the overload.

Ignoring Queue Time

Most companies are far more sophisticated in how they manage their manufacturing operations than in the way they manage engineering. In manufacturing, queue time is recognized as wasteful and the largest single driver of cycle time through a factory.

Yet we ignore queues in engineering. A typical development program probably spends 80% of its time in queue, not in operation time. A draftsman completes a drawing in four hours after it spends several days waiting in his in-basket. Queue time is where the body is buried.

But where do most companies dig? They focus on operation time. They spend thousands of dollars for computer-aided design systems to reduce the drawing time from four to two hours. They don't spend a nickel to reduce the queue time.

This may strike you as bizarre, and it should. Queue time is usually much less expensive to reduce than operation time. Curiously, the solutions are available in the lessons we've learned from just-in-time manufacturing but forgotten when we manage engineering. Neither QFD nor CE is explicitly concerned about managing queue time.

Many years ago, consultants convinced companies that because so many things went into development and so few things came out, the development process resembled a funnel. We start lots of little projects, screen out the losers, and eventually end up with a couple of winners. The consultants convinced management that it was good to have a large portfolio of projects so that even a low success rate would guarantee some winners.

The problem with this model is that we typically load up a few engineers with lots of little projects, creating the overload noted earlier. Projects at the top of the funnel spend years moving at a snail's pace, speeding up only when they reach the bottom of the funnel.

The development funnel virtually guarantees large queues of idle work and slow development. Why do we tolerate queues in engineering that we would never tolerate in manufacturing? The solution involves setting tough priorities on projects so that the workload is balanced to capacity throughout the process. Once again, neither QFD nor CE addresses this problem.

Burn Rate Management

In most companies, management time is spent where the dollars are spent. For development programs, this is just before product introduction when large teams costing thousands of dollars a day wrap up the design. The project is burning money, and management is paid to worry about money.

But where should management spend its time? At the beginning of the project when one engineer is working on the conceptual design? This wouldn't be practical, because dozens of projects are at the beginning of the funnel.

Yet this is where the time is spent most usefully. The decisions made during the first month of development are typically most important. They determine most of the cost, product performance, and schedule. Yet these decisions are made without management's guidance.

If we could influence these decisions, we wouldn't need to fight as many fires as these programs near completion. And, if we ignore them, for every minute of management time saved at the front end, we will consume an hour when the project nears completion. Neither QFD nor CE draws management attention to the fuzzy front end of the development process.

Lack Of Concurrency

CE's strong suit is its emphasis on concurrency. CE recognizes that product and process can be developed concurrently. That concurrency shortens development cycles and improves engineering efficiency, along with the quality of the design. The approach is sound. Nonetheless, it could be strengthened in two ways.

First, concurrency should be a business decision, not simply a philosophy. If you quantify the cost and value of concurrency, you can decide how far to go to pursue it. Second, impressive savings are available by increasing the degree of concurrency within engineering, not simply overlapping the product and process design methods. CE emphasizes only product and process concurrency. QFD doesn't address this issue.

One great untapped source of increased concurrency lies in selecting product architectures optimized for rapid product development. These architectures permit maximum overlap during the development of different subsystems. By properly dividing design functionality and specifying interfaces in a simple, stable, and robust fashion, you can design many subsystems at the same time.

Inattention To Architecture

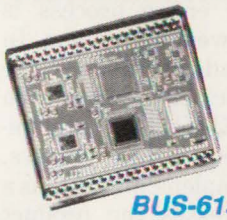
In contrast, if product architecture is selected poorly, it virtually condemns the product to a sequential design process. And that's what happens at most companies.

Many firms choose product architectures as a technical solution to a technical problem. The application drives the architecture. They ignore the intimate connection between architecture and development speed, and miss the opportunity to use product architecture as a tool to speed development. Neither QFD nor CE addresses this issue.

Most companies fail to empower their development teams with enough decision-making authority. Companies talk big and give the

LATEST DEVELOPMENTS IN 1553

COMPLETE INTEGRATED 1553B NOTICE II STANAG 3838 TERMINAL

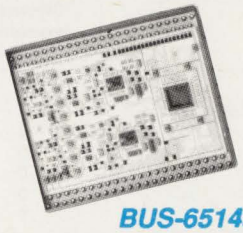


BUS-61559

DDC's BUS-61559 advanced integrated MUX hybrid with enhanced RT features (AIM-HY'er) is the most complete MIL-STD-1553B Notice II, as will as STANAG 3838 remote terminal (RT), bus controller (BC), and bus monitor (MT) terminal. Packaged in a 78-pin DIP or 82-pin flat package. The AIM-HY'er, features low-power transceivers, protocol, memory management, 8K x 16 shared RAM, and internal three-state buffers. Software features include internal RT illegalization, separation of broadcast data, variable sized circular buffers for multiple messages per RT subaddress, and an interrupt status register. It operates over the -55° to +125°C temperature range and military screening is available.

Circle 150 for Sales Contact **Circle 151 for Literature**

UNIVERSAL MULTI-PROTOCOL 1553 RT

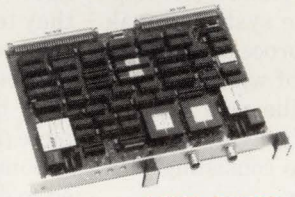


BUS-65149

The world's first stand-alone, dual-redundant, universal MIL-STD-1553 Remote Termial, the BUS-65149 is compatible with more aircraft manufacturer's protocols than any comparable product. The universal transceivers and programmable protocol supports: MIL-STD-1553 A/B, Notice I and II; McAIR A3818, A5232, and A5690; General Dynamic's (F16) 16PP303 and 378A protocols; and Grumman SPG151A custom specifications. The BUS-65149 universal RT is compatible with all microprocessors with its direct memory access or shared RAM "mailbox" allocation scheme. Illegalization of any command through the use of an external PROM, PAL, or RAM device is supported. It operates over the -55° to +125°C temperature range.

Circle 152 for Sales Contact **Circle 153 for Literature**

1553 VME/VXI INTERFACE CARD ASSISTS SYSTEM DESIGNERS



BUS-65522

The BUS-65522 provides a full, intelligent interface between the dual redundant MIL-STD-1553 Data Bus and the parallel VMEbus and VXIbus. Software control enables the BUS-65522 to function as a Bus Controller, Remote Terminal, or Bus Monitor and enables avionic and weapons system designers to simulate, develop, and test MIL-STD-1553 systems. The BUS-65522 supports all dual redundant mode codes and message formats. An on-board 8K x 16 dual-access, double-buffered RAM prevents partially updated data from being read by the CPU or transmitted to the 1553 data bus. All MIL-STD-1553 functions such as address recognition, Manchester coding validation, bit count, and mode response are provided without subsystem intervention.

Circle 154 for Sales Contact **Circle 155 for Literature**

MIL-STD-1553 DESIGNER'S 3RD EDITION OFFERED FREE

DDC's comprehensive, 624 page MIL-STD-1553 Designer's Guide (3rd Edition) offers a complete copy of MIL-STD-1553B interspersed with a paragraph-by-paragraph commentary on the 1553 Standard and a direct comparison with the earlier "A" version. Changes to the original Standard and copies of the ASD Validation Test Plan and RT Production Test Plan are incorporated along with sections on Notice I and II. The Guide includes a discussion of system hardware and software considerations. Guidelines for interfacing 1553 components to microprocessors, single-chip microcomputers, and a dual-port RAM are presented in the Applications Section. Send for a free copy by completing the bingo card.

Circle 156 for Sales Contact **Circle 157 for Literature**

The BUS-65519 is a turnkey system used to automate the protocol tests of the SAE (AS4112) RT Production Test Plan (PTP). The board also supports Microsoft "C" and Pascal drivers with a library of run-time routines for user defined multiple-RT's/BC/MT applications, tests and simulation for MIL-STD-1553A/B Notice I or II systems.

With the BUS-65519, the test engineer characterizes the Unit-Under-Test (UUT) via the user friendly windows and help screens, of the menu driven PTP software. Once this is done, the configuration can be saved to disk. The BUS-65519 can execute the ENTIRE production test plan in under 20 seconds. A report detailing the results of the test is automatically generated.

BUS-65519
PRODUCTION TEST PLAN TESTER AND SOFTWARE

An optional parallel I/O card can be used with the BUS-65519, to control RT address and Status bits of the UUT. An IBM PC/XT/AT or compatible computer can be used to host the BUS-65519 MIL-STD-1553 Interface card and parallel I/O board. This configuration of hardware and software supports MIL-STD-1553B Notice I and II, RT PTP automatic testing and can be used to simulate BC, multiple RT's, and actively monitor bus activity using the driver run-time library of routines.

Circle 158 for Sales Contact **Circle 159 for Literature**

DDC
ILC DATA DEVICE CORPORATION

HEADQUARTERS AND MAIN PLANT: ILC Data Device Corporation, 105 Wilbur Place, Bohemia, NY 11716, (516) 567-5600, TLX: 310-685-2203, FAX: (516) 567-7358, (516) 563-5208
WEST COAST (CA): GARDEN GROVE, (714) 895-9777, FAX: (714) 895-4988;
WOODLAND HILLS, (818) 992-1772, FAX: (818) 887-1372; SAN JOSE, (408) 236-3260, FAX: (408) 244-9767
WASHINGTON, D.C. AREA: (703) 450-7900, FAX: (703) 450-6610
NORTHERN NEW JERSEY: (201) 785-1734, TLX: 130-332, FAX: (201) 785-4132
UNITED KINGDON: 44 (635) 40158, FAX: 44 (635) 32264; **FRANCE:** 33 (1) 4333-5888, FAX: 33 (1) 4334-9762
GERMANY: 49 (8191) 3105, FAX: 49 (8191) 47433; **SWEDEN:** 46 (8) 920635, FAX: 46 (8) 353181
JAPAN: 81 (3) 814-7688, FAX: 81 (3) 814-7689

TEARING DOWN BARRIERS TO FAST PRODUCT DEVELOPMENT

	Most common barriers	Concurrent engineering (CE)	Quality function deployment (QFD)
1.	Taking giant steps	0	0
2.	Not anchoring the specifications on real customers	0	++
3.	Ignoring the market clock	0	0
4.	Overloading development capacity	0	0
5.	Ignoring queue time	0	0
6.	Using the development funnel	0	0
7.	Burn rate management	0	0
8.	Lack of concurrency	++	0
9.	Inattention to architecture	0	0
10.	Failure to empower teams	+	0
11.	Phased development systems	+	0
12.	Inappropriate testing strategies	0	0
13.	Failure to quantify the problem	0	0
14.	Insufficient focus on communications	++	+
15.	Inappropriate make/buy decisions	0	0

++ Very valuable
+ Valuable
0 No impact

team lots of responsibility, but they send conflicting signals when it's time to spend money or make decisions. They want engineers to work nights and weekends, but travel requests to vendors still must be submitted three weeks in advance and signed by a vice president. To alter the product specification after the project starts requires the approval of God.

Moving Locus Of Control

Rapid product development requires moving the locus of control down to the team level. In simple terms, let the team manage the team. Managers should facilitate the team's progress rather than attempt to control it.

Control is achieved by selecting good people for the project, jointly agreeing upon realistic goals (not giant steps), and supporting the people with the training and resources to get the job done.

Such empowerment is particularly important when doing rapid product development with extensive concurrent activities. These projects simply get too complex for management to retain decision-making authority without stalling the project.

Although QFD doesn't address team empowerment, CE has started in that direction. CE recognizes that concurrency is too messy to manage without empowering people.

If we rely on management to manage the project, we have a control problem. The most common strategy to solve this problem is to control key decisions using a phased development system. These systems break the development process into discrete phases, each of which must be completed before the next one begins. The end of each phase is marked with a gate consisting of a management review.

Phased Development Systems

These systems are best suited for two objectives. First of all, they reduce risk by allowing us to kill a project early, instead of continuing to pour money down a rat hole. This is useful when you are working slowly on lots of risky projects, as we've described earlier.

The second point is that these systems conserve management time. They make it possible for management to control many months of work simply by attending one short meeting. There's no messy wandering about the development lab to see how things are going. In a meeting, everything is laid out neatly, and management approves or disapproves of the project's moving to the next phase.

Unfortunately, these systems aren't suited to cut development speed and, in fact, they slow progress. For example, in a product with multiple parts or subsystems, each one of these parts may progress in its design at a different pace. When a part has completed its activities in a phase, it must stop and wait for all other parts to catch up.

Then finally, after a management review, all parts are released to the next phase. This process looks like an elephant being digested by a boa constrictor. The entire process is paced by the slowest subsystem. In addition, overload and queues are guaranteed at the beginning of each phase *(Fig. 2)*. QFD doesn't eliminate this phased review process. When properly implemented, CE as a minimum compresses the product and process design phases.

Inappropriate Testing Strategies

Many companies fail to exploit opportunities to shorten development cycles through smart testing strategies. They chronically miss opportunities to separate market and technical testing. They may wait until they have a physical prototype before they test customer reactions. Often, they could construct a model that is sufficient to begin market research long before the prototype is complete *(Fig. 3)*.

Sometimes companies are tempted to do lengthy analysis and modeling for problems that could be resolved quickly by empirical testing. In other cases, companies bypass analysis entirely and resort to trial and error. The mix of empirical testing and engineering analysis should not be rigidly built into the process, but rather chosen to meet the needs of specific programs.

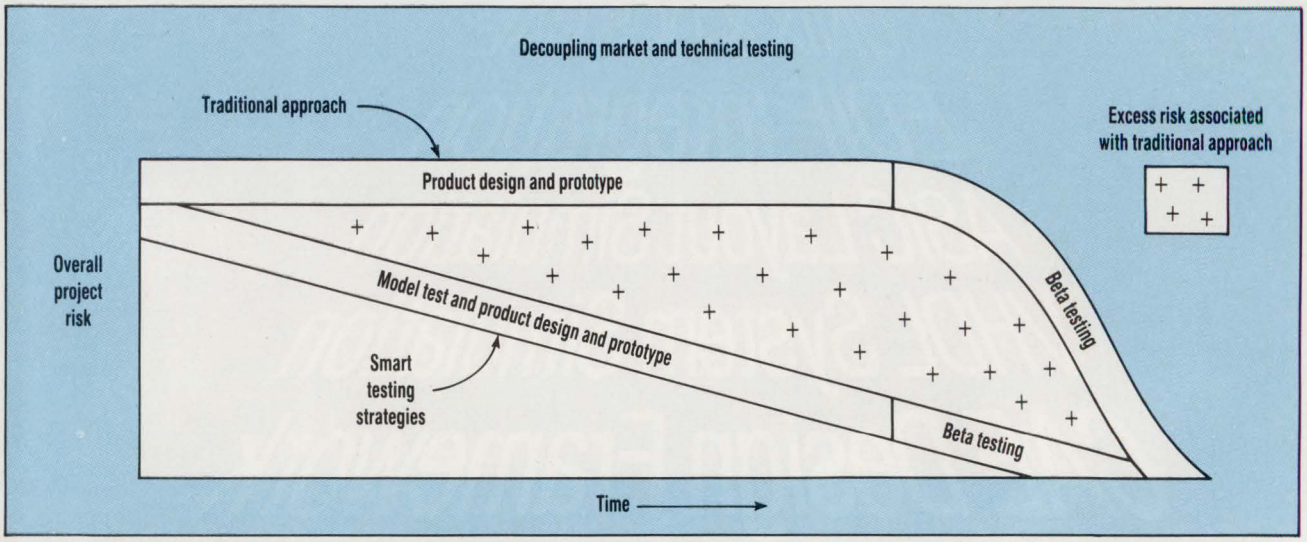
As a general rule, tests should be done at the lowest level subsystem possible and as early in the process as possible. As one manager says, "Don't be afraid to build a tall junk pile."

On occasion, companies decide to centralize testing and model-making because of the special skills and equipment required. They often discover they have created an unresponsive bureaucracy. To develop products rapidly, testing speed is usually more important than the cost of testing. Neither QFD nor CE addresses this problem.

Failure To Quantify The Problem

Ultimately, as you try to shorten development cycles, you must decide how much to spend to speed things up. This business decision to exchange money for time can be made only if you know the value of time.

Yet most companies have no clue



3. Delaying market testing until the end of the development process exposes the program to too much overall risk. By constructing a model, a company can often begin market research long before the prototype is finished.

as to whether a six-month reduction of development cycles is worth $10 or $10,000 or $10 million. Nowhere else in our business do we blindly spend money without asking to know the return.

Most companies conclude that it must be hard to quantify the benefits of a shorter development cycle and choose to rely upon their guesses and gut feelings. Unfortunately, in this case, the quantitative gut feeling is derived from a string of programs that were never quantified—a pretty silly way to develop a gut feeling. This is the same gut feeling that allowed American manufacturing to miss the boat on JIT (just-in-time inventory).

Focus On Communication

The solution is to treat business as business, and try to quantify the effect of shortening the development cycle. We can develop rules of thumb to guide the team and have everyone in the organization understand the financial consequences of delay. You simply cannot get good decisions without knowing what you can afford to spend. Neither QFD nor CE treat rapid product development as a business decision to be traded off against other investments of time and money.

Both QFD and CE recognize the crucial role of communication in developing products rapidly *(see the table)*. QFD is powerful in the systematic and logical way it organizes information. It helps get everyone marching to the same drum early in the process.

CE has responded to the increased complexity of the concurrent design process by developing tools to achieve better communication. Most CE efforts move team members to the same location to increase the flow of information. In addition, engineers may travel extensively to vendors. And databases can be shared between engineering and manufacturing.

Make/Buy Decisions

Good communication is essential when you're performing many activities concurrently. This is what happens when you try to develop products rapidly.

Good make/buy decisions create major opportunities to cut development time. Sometimes it's better to perform tasks inefficiently, but quickly, inside the company. For example, an in-house print shop can often outperform outside vendors, who operate with more of a backlog. In other cases, outside vendors outperform internal service departments, because they can bring more capacity to bear in a short time.

Unfortunately, most companies make these decisions based on cost rather than speed. Because they have no idea what speed is worth, they can't make a business decision that buys them time. Neither QFD nor CE addresses this problem.

It should be clear that most of the barriers to rapid development belong to management; they're not technology problems. The bad news is that vendors sell only technology, and because you can't buy a box of management from them, you have to solve the problems yourself.

When Efforts Pay Off

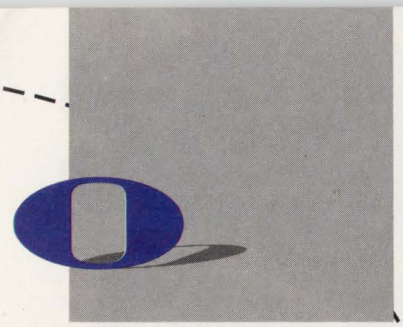
The good news is that experts estimate that QFD and CE efforts take two to five years to pay off. You could start tearing down today at least 10 of the barriers to rapid product development that we've just talked about.

By the time your competitors—who may be focusing only on QFD and CE—are ready go further, you will have a two- to five-year head start. By then, it may be too late for them to catch up.□

DONALD REINERTSEN

Donald Reinertsen heads Reinertsen and Associates, a Redondo Beach, Calif., consulting firm that specializes in product development issues. He cowrote the book *Developing Products in Half the Time*, recently published by Van Nostrand Reinhold.

How Valuable?	Circle
Highly	541
Moderately	542
Slightly	543



OBJECT DESIGN

Object Design, Inc.
One New England Executive Park
Burlington, MA 01803
TEL 617-270-9797
FAX 617-270-3509

Introducing

ObjectStore ODBMS

The *Only Choice* For Design Applications.

The 1980s brought a new class of powerful, design-oriented applications based on single-user workstations. The challenge for the '90s will be to enable developers and knowledge workers to share these applications in workgroups. Collaboration among multiple users and the sharing of objects–not files–will provide the next major gain in productivity.

ObjectStore is an object-oriented database management system for applications written in C++. ObjectStore provides complete DBMS functionality for highly interactive, design-intensive applications.

ObjectStore offers:
- easy migration of existing C applications
- interactive performance comparable to single-user file-based applications
- complete distributed DBMS functionality
- version and configuration management
- concurrency control for collaborative work
- choice of C++ library interface or full object query language

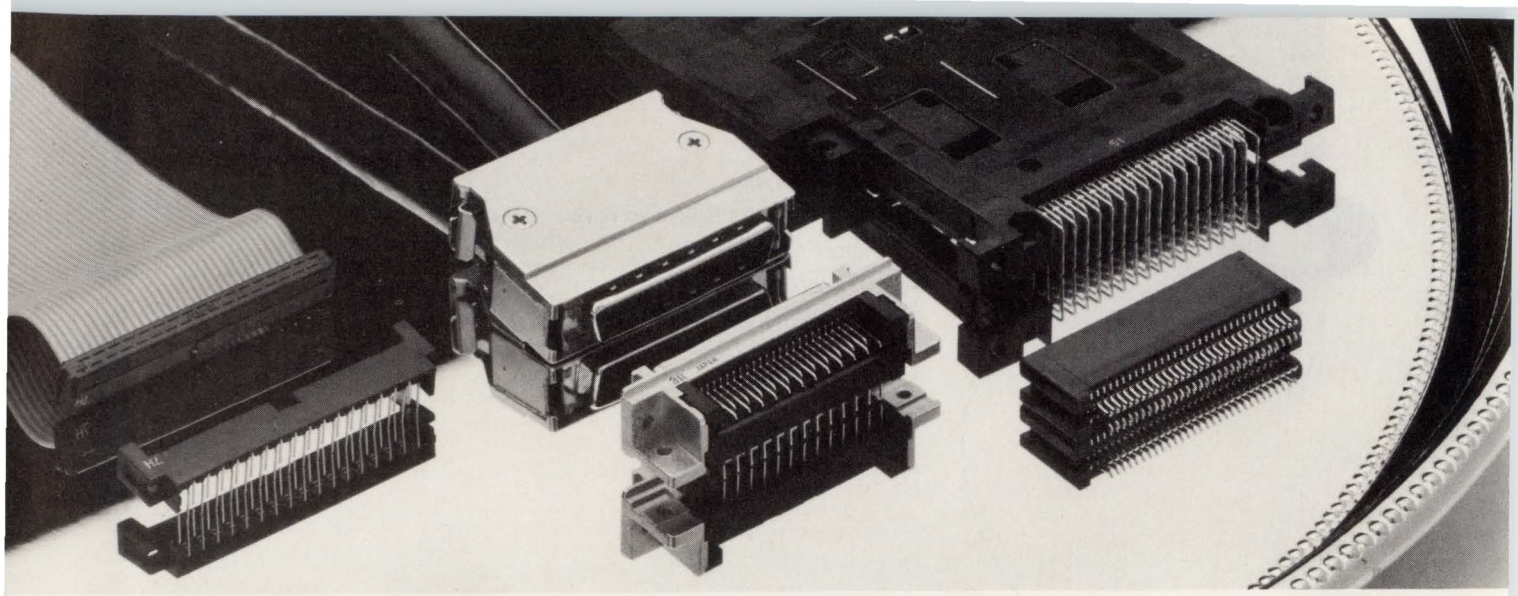
ObjectStore is available now for the Sun-based LAN configurations. To attend a training course or ObjectStore Seminar near you, please call 617-270-9797, ext. 132.

Design Applications

- ECAD
- MCAD
- A/E/Construction
- CASE
- CAP
- Multimedia
- Imaging

CIRCLE 190

LEADERSHIP BY DESIGN



Well connected.

To find the best value in connectors, choose the company offering the most valuable connections: Fujitsu Component of America.

Form a working partnership with Fujitsu and you'll get more than just the industry's largest selection of high-density high-performance connectors. You'll also receive the valuable extra services that come from being well connected.

Like our advanced design expertise. Years of experience creating connectors for our own products have made us the industry's foremost real estate expert in maximizing today's smaller system boards.

Product Selection Guide

Series	Contacts	Current (ADC)	Part Nos.
FCN-210	30 to 120	2 (IDC:0.5)	FCN-215QXXX-G/O FCN-217JXXX-G/O
FCN-220 Card edge	30 to 120 (S-type: 112 to 187)	2	FCN-225JXXX-G/O FCN-228JOXX-G/O-01
FCN-230	34 to 68	2 (IDC:1)	FCN-235DXXX-G/E FCN-237RXXX-G/F
FCN-560 Mem card	68	L:2 E, G, F: 1	FCN-565P038-G/O FCN-565P068-G/X
FCN-790 Low profile	10 to 40	1	FCN-794P0XX-L/O FCN-795P0XX-L/O FCN-797P0XX-L/O

The standard bearers.

Today, Fujitsu can connect you with a full line of connectors that meet SCSI, RS-232, and IPI standards. Making our products an easy fit with your existing systems as well as your next generation of designs.

The power of choice.

When it comes to today's smaller PCs, nobody makes more connectors to fill more needs than Fujitsu. Just look at our newest series:

• 210 Series. Down-sized connectors that use 40% less space. • 220 Series. Card-edge connectors that fit reduced heights and board sizes. • 230 Series. Cable-to-board and board-to-board connectors that meet SCSI II, RS-232, and IPI standards. With optional EMI shielding. • 560 Series. The first line of PC Card connectors to meet both PCMCIA and JEIDA standards. • 790 Series. Slim ribbon connectors that reduce height requirements by a third, while using standard board layouts and low-priced cable.

Make the connection.

Talk to Fujitsu yourself. Inside California, call 1-800-441-2345 and ask for ext. 238. Outside CA, call 1-800-556-1234, and ask for ext. 238. And find out how our connectors can improve your connections, every step of the way.

FUJITSU

Every step of the way.℠

Fujitsu Component of America, Inc.
3545 North First Street · San Jose, CA 95134-1804.

CIRCLE 202

DESIGN FOR RELIABILITY RESHAPES DESIGNING

RISING CUSTOMER EXPECTATIONS ARE DRIVING DESIGN FOR RELIABILITY. THE GOOD NEWS IS THAT IT DOESN'T RAISE COSTS OR TAKE ANY MORE TIME.

ROY WHEELER

Hewlett-Packard Co., Colorado Springs Division, P. O. Box 2197, Colorado Springs, CO 80907-2197; (719) 590-1900.

Here's a story by an old design engineer written specifically for design engineers. But don't look for a slick new circuit aimed at revolutionizing the industry. I want to do something far more fundamental—that is, convince you to take another look at the way you do your job.

If I've learned one thing in 35 years of engineering work, it's that if you want to lose out, just remain satisfied with what you're doing and how you do it. Then someone will come along with a new idea and you'll lose. This maxim holds true whether you're pitching horseshoes, playing baseball, or designing vacuum cleaners. A new idea in our business has come along that we all need to pay attention to: design for reliability.

We're faced with this new idea because of rising customer expectations. Your own expectations of manufacturers have changed in the last 10 years. What was a pleasant surprise when you bought your first Japanese car or TV or camera has now become an expectation. The product that doesn't meet that expectation loses. In the same way, our customers just won't tolerate poor reliability any more—their expectations have risen.

The good news is that it doesn't cost more or take more time to design for reliability. A proper design for reliability costs less to manufacture than one that cuts corners to reduce cost. We have found that a design that's reliable in the customer's hands is also reliable during manufacture.

The result is less scrap, less rework, lower manufacturing cost, more profit, and happy customers. In much the same way, a design for reliability also takes less time than one where you cut corners to save time. Such a design addresses the reliability issues early. That way, they can be integrated into the overall design effort instead of patched up in a crisis—in the last minute before shipments start, or even worse, under the pressure of a product recall.

Design for reliability results in fewer design iterations, fewer last-minute specification changes, and less catch-up design work. And projects are done on time.

I had occasion to think about how I do my work some 20 years ago when Dave Packard spoke before the division of Hewlett-Packard where I work. Some of his words still stick in my mind: "The way you do design work is test—fix—test until you're satisfied with the results of the test." If you think about it, even if you use the most sophisticated CAD system, you will eventually get involved in testing a prototype, fixing the problems, and retesting it in a continuous loop until you're satisfied with the results.

IMPROVEMENT MODEL

Packard was successful using this method. At HP, we've taken this simple idea, formalized it, and dressed it up. We've named it the continuous design improvement model *(Fig. 1)*. Indeed, designing for reliability boils down to focusing the CDI model on reliability issues.

I will use that model as a framework to pull together many different ideas focused on just one goal—more reliable products. I know these ideas work because I've been involved in a 10-year implementation of this product-design approach at Hewlett-Packard.

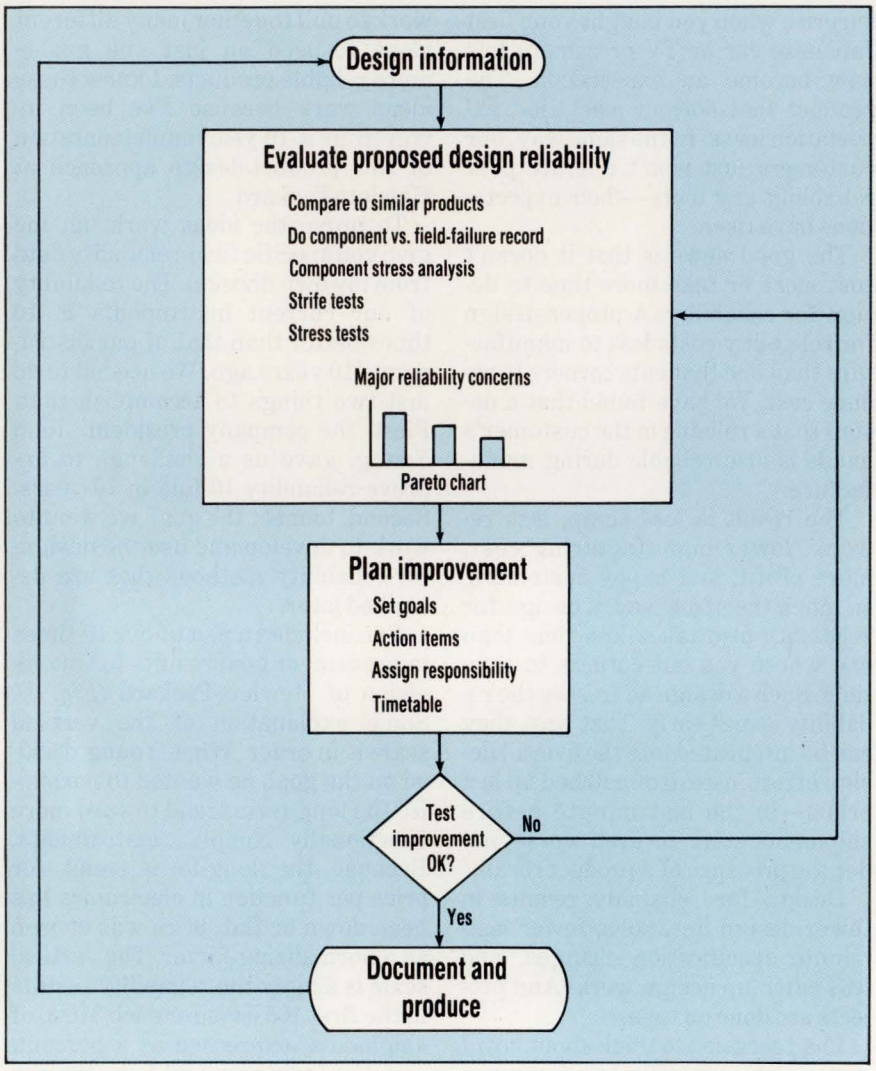
To prove the ideas work, let me give you specific field-reliability data from my own division. The reliability of our current instruments is 10 times better than that of our instruments 10 years ago. We needed to do just two things to accomplish that. First, the company president, John Young, gave us a challenge to improve reliability 10-fold in 10 years. Second, to meet the goal, we went to work to develop and use the design-for-reliability methods that are described later.

I've included a plot of our 10-times improvement goal results for my division of Hewlett-Packard *(Fig. 2)*. Some explanation of the vertical scale is in order. When Young decided on the goal, he wanted to normalize the long-term trend toward more functionally complex instruments. Because the long-term trend for price per function in electronics has been down or flat, price was chosen as a normalizing factor. The vertical scale is simply the reliability results in the first 105 days for each $1000 of shipments, expressed as a percentage. Confusing isn't it? Let's try it in math terms:

$$\text{failures\%/\$1000} = 100 \times \text{failures}/(0.001 \times \text{shipment\$})$$

John Young chose the 105-day period because it was the warranty period for the computer divisions of HP, and we found that most of our failures occur in the first 105 days. In the instrument divisions, our warranty period historically has been one year. We currently give a three-year warranty on some of our higher volume instruments. On those instruments, the 54500 series of digital oscilloscopes, the average MTBF is currently 60,000 hours, based on field reliability data during the first year of service.

Let's walk a bit more through the CRI model, then get started on applying it to the problem of design for reliability, and finally round it out with some case histories. Looking at



1. The model for continuous reliability improvement serves as a framework for the design process. Once the basic design idea is down on paper, a designer needs to look at it critically in terms of reliability (the block called evaluate proposed design reliability).

the model, you see that it begins with design information. That data usually comes from marketing studies, customer inputs on previous designs, field failure data, and reliability testing done on previous designs. In the beginning, you gather this data and integrate it into a design idea that you think will meet all of the customer's requirements.

Once you have nailed down the basic design idea on paper, you need to take a critical look at it from a reliability standpoint. Are there fundamental weaknesses in the idea that will cause trouble later on? Does the design require a big stretch in your company's available technology and manufacturing capability? Will you push the limits of some key component? Do you really understand what your customer will do with the product? Do you know what environment they will be operating in? These questions come under the block called evaluate proposed design reliability.

The first few times, the design idea should all be done on paper, concentrating on fairly macro-sized issues. Don't be in a big rush to start designing and building hardware. A hardware design iteration takes a lot longer than just thinking and doodling on paper. And hardware is much tougher to change when you discover a major problem.

For the purposes of this article, I will stick to reliability issues. Of course, you will be thinking about all of your design's attributes during this time, and you must integrate all of these things into a common framework.

This early investigation is the most critical part of the design process. The entire success of your later effort is built on what's done initially. Do it right and don't move on until you've attained what you want.

This will be tough, because to the casual observer, or your boss, it looks as if nothing is happening—no schematics, no hardware to play with, and so on. This part of the process tests your powers of persuasion. The rest is easy. When you're satisfied that the basic design approach is right, begin to generate the details and build hardware. When it finally tests out okay, celebrate. Finally, document what you have learned, because you or somebody else needs it to build on for the next project.

Predicting Reliability

Now let's turn to hardware design as it relates to reliability. A fundamental difficulty in designing for reliability is: how to know when you've done the right thing? If I design an amplifier for 500-MHz bandwidth, the way I find out if I've achieved my goal is to build a few and measure the bandwidth.

If I'm a little more sophisticated, I measure a large enough sample to determine the amplifier's bandwidth at the 2 or 3 sigma limits of the manufacturing process. In addition, I will measure the bandwidth at the limits of the amplifier's temperature specs. For reliability purposes, the measurement is difficult, but not impossible. Let's talk about some of the ways to measure reliability—ways I've used that really work.

The simplest way to measure reliability is to count parts. A fundamental principle of reliability design is that a design with fewer parts has a higher reliability than one with more parts. Sometimes this won't be true because of the differences in failure rates of various individual parts. For the usual mixture of parts in any reasonably complex circuit, these differences average out. You discover that a simple count of parts is a good indicator of relative reliability. There is much more freedom to reduce part count than you might

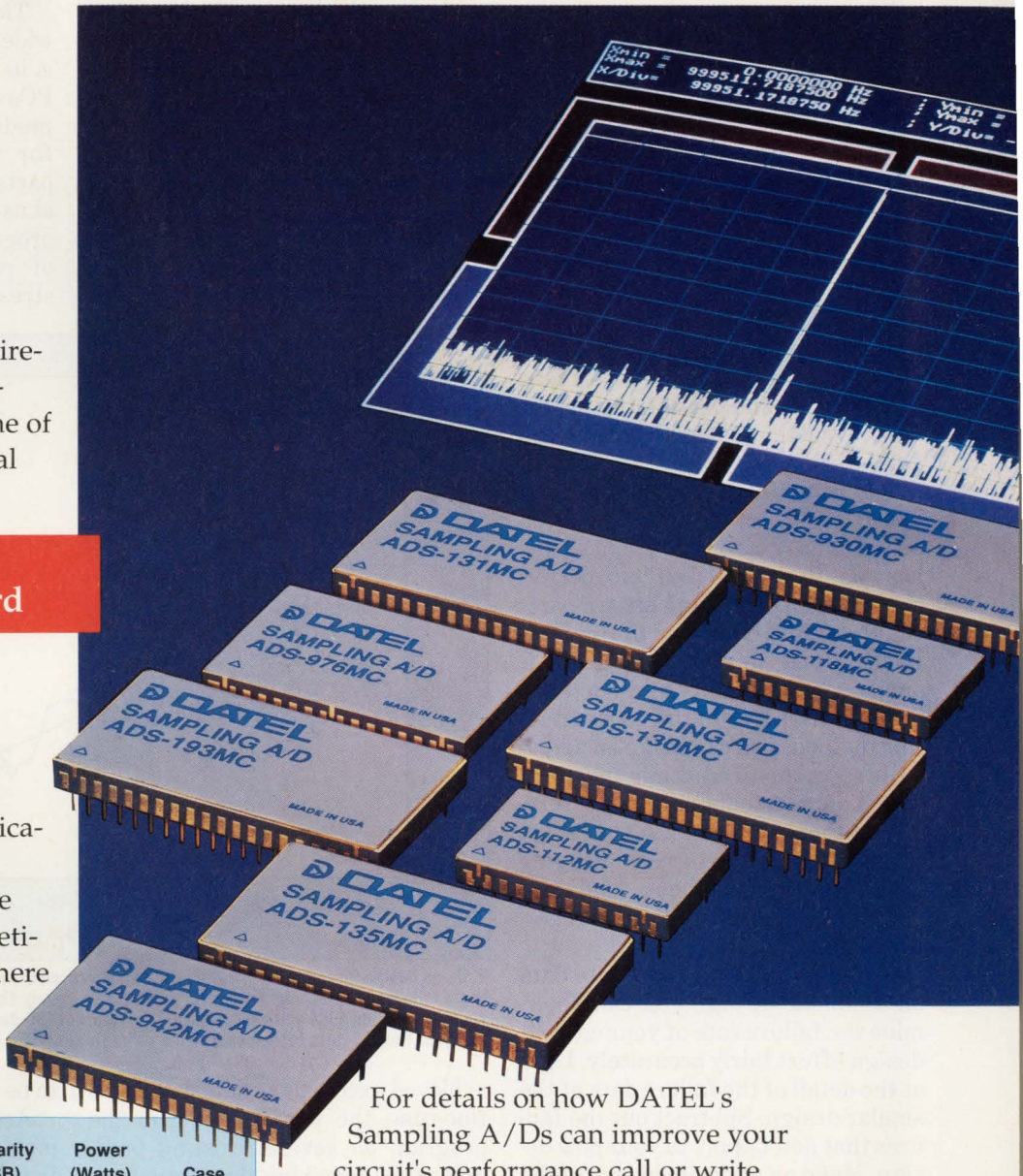
Sampling A/Ds

There's only one complete source.

No matter what your requirement, you will find the answer in DATEL's broad line of Sampling Analog-to-Digital Converters.

Fast becoming the industry standard

Characterized through Nyquist operation, these converters offer superior Signal-to-Noise ratios and harmonic distortion specifications.
Bottom line, compare these converters with any competitive units, and you'll see there is no reason to look anywhere else.



Model	Bits	Throughput (MHz)	Linearity (LSB)	Power (Watts)	Case
ADS-111	12	0.500	±1/2	1.3	24-PIN
ADS-193	12	1.0	±1/2	1.3	40-PIN
ADS-112	12	1.0	±1/2	1.3	24-PIN
ADS-117	12	2.0	±3/4	1.4	24-PIN
ADS-132	12	2.0	±1/2	2.9	32-PIN
ADS-118	12	5.0	±3/4	2.3	24-PIN
ADS-131	12	5.0	±3/4	3.8	40-PIN
ADS-130	12	10.0	±3/4	4.0	40-PIN
ADS-924	14	0.300	±1	1.3	24-PIN
ADS-928	14	0.500	±1/2	2.9	32-PIN
ADS-941	14	1.0	±3/4	3.1	32-PIN
ADS-942	14	2.0	±3/4	3.2	32-PIN
ADS-976	16	0.200	±2	0.9	32-PIN
ADS-930	16	0.500	±1 1/2	1.8	40-PIN

For details on how DATEL's Sampling A/Ds can improve your circuit's performance call or write DATEL, Inc., 11 Cabot Boulevard, Mansfield, MA 02048.

Let DATEL convert you.
***Call now* 800-233-2765**

DATEL

INNOVATION AND EXCELLENCE IN PRECISION DATA ACQUISITION
DATEL, Inc., 11 Cabot Boulevard, Mansfield, MA 02048 (508)339-3000

CIRCLE 161

think. Some of that basically comes from clever design. I remember an instance when a clock synchronizer circuit was reduced from 23 logic gates in several packages to just a few gates. That new version worked better than the original design.

Another thing to do is question the functional necessity of every part. I think of the many decoupling capacitors that are used at times. A large board may include hundreds of capacitors. Individually, these capacitors aren't a high failure rate item. However, because there may be more of them than anything else, they might have the highest total failure rate of any part in the design. As a result, they will pop up in our failure-rate prediction analysis as a concern. An analysis of the design may reveal that you really don't need all of these capacitors.

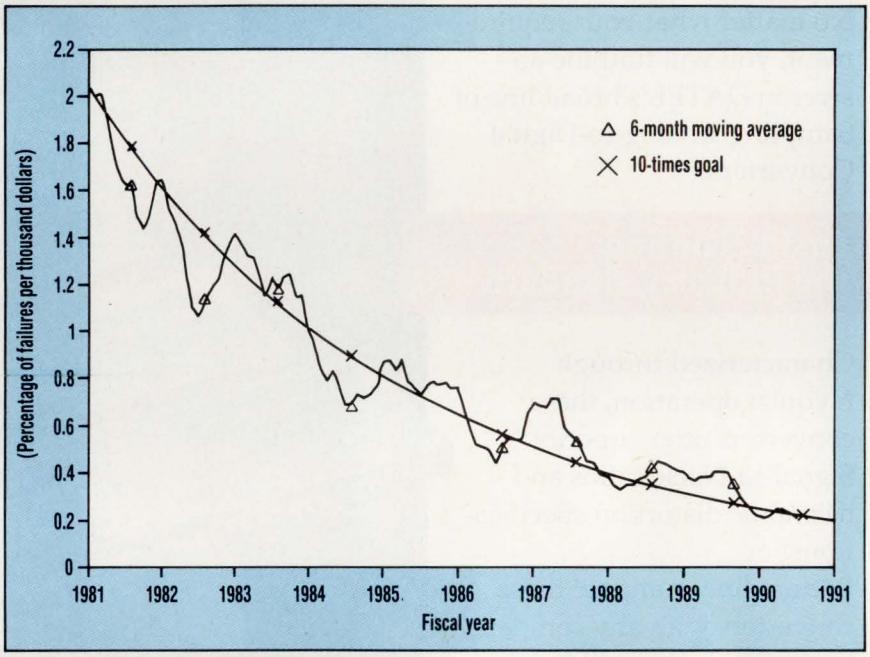
The eventual reduction in part count saves money, greatly improves the board's reliability, and has no impact on circuit performance. Along the same lines, a parts count method described in the MIL-HDBK-217D military handbook is similar in concept but more detailed in application to counting parts. With this method, you can make an actual failure-rate prediction without stress data on individual parts. It requires that you have a material list and access to the generic failure-rate tables in the handbook, and also know the equipment's general operating environment.

If you have field failure-rate data on a similar design, you can determine the failure rate of your current design effort fairly accurately. Look at the detail of the failure data of the similar design. Subtract out the failures that don't apply to your new design. Make an estimate by one of the other reliability prediction methods for the portions of your new circuit that aren't the same as the similar design. Add this result to the result of the subtraction you did before. This sum is the predicted failure rate. This method is more or less accurate depending on how much of each circuit is the same. Always use this method if a reasonably large part of the two designs is the same.

Finally, I recommend using a commercially available software package for predicting reliability. Any selected package calls for your good judgment because they all have some parameter values that must be chosen with care. A good program should be based on something on line with the Arrhenius reaction rate model (more about that later). The program also should have a good database of field-failure experience for the various kind of parts you use and be reasonably easy to operate.

At HP, we use a program called Relcalc 2 from T-Cubed Systems Inc., Westlake Village, Calif. After doing some fine-tuning to suit our particular application, we've achieved excellent results with it. To fine-tune the parameters, run the program on several existing products while tweaking the parameters until you get a model that fits your field failure rates. Because this takes lots of work, you may want to just start using it on your actual predictions. Use your best guess for parameters and keep track of the results to compare with field failure data. It takes time, but with patience, you'll eventually have an accurate field-failure predictor of your new products. In the meantime, the program tells you the components and design areas most likely to fail, and whether your design changes are improving your design's reliability. In other words, even without fine-tuning, the program tells you on a relative scale how reliable the design is. This alone makes it worthwhile.

These software packages have a wide price range. At $2000, Relcalc 2 is in the mid-range and runs on any PC-compatible computer. Note that prediction programs won't account for workmanship errors, faulty parts, shipping damage, customer abuse, and so on. In other words, the programs predict the random failure of parts under various levels of stress. Other kinds of problems need to be eliminated by different means.



2. Using design for reliability, Hewlett-Packard improved the reliability of its instruments 10-fold in 10 years following a challenge from HP president John Young. The percentage of failures has dropped steadily between 1981 and 1990, measured in terms of 105-day reliability per $1000 worth of instruments shipped. The 105 days corresponds to the warranty period for HP's computer division.

Accelerated life testing is a common method of predicting reliability that I've found to be almost worthless. We tried for years to develop an accelerated life test, which could be done in a reasonable time, that would predict field failure results. The effort was a miserable failure. Wayne Nelson of General Electric's Corporate Research & Development Center, Schenectady, N. Y., is a recognized expert in the field. I attended one of his courses on the subject several years ago. The bottom line is that except in the very simplest situations where only a very few known

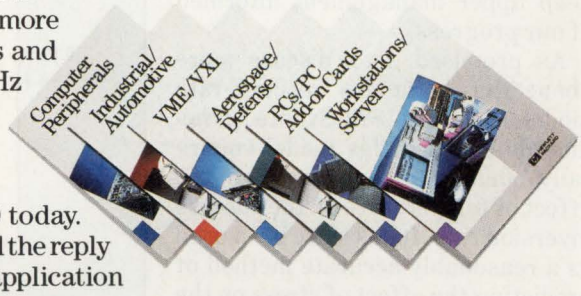
Frustrated with microprocessor system debugging?

Here's free help in making the connections.

Plug into our new series of application notes today. And learn how to save time and aggravation when you're debugging microprocessor systems and busses.

Find out how an HP preprocessor literally makes it a snap to connect your microprocessor to an HP logic analyzer. And see how completing your HP logic analysis sy 'em with a preprocessor will speed and simplify measurements and data analysis. You'll also discover the industry's broadest selection of preprocessors – over 60 models support more than 70 microprocessors and busses including 100 MHz support for RISC and high-performance CISC processors.

So call **1-800-752-0900** today. Ask for **Ext. 1404** or mail the reply card and we'll send the application information you need from our FREE series of six industry-specific application notes.



There is a better way.

HEWLETT PACKARD

failure modes must be dealt with, accelerated life testing is hopeless.

The choice of methods for predicting reliability depends on the situation. If your product is nearly the same as an existing product with failure-rate data available, use the field failure data on the existing product. Be careful, though. If the product's application is different, it can make a big difference in the field reliability results. Different environments and models of different uses need to be considered and factored into your final prediction. This method can help you with design decisions if you look at the details of what failed, and it can determine what caused the failure. It will tell you what kind of overall reliability to expect. The simple "fewer parts—more reliable" method doesn't give you a predicted failure rate, but it will help make some fundamental design decisions. The computer-aided method can, with proper care, do both things for you: help with design decisions and predict field failure rates. You can do the same thing the programs do by using the MIL-HDBK-217D methods. Prediction programs are usually based on this database and prediction method. Doing this manually presents a very difficult task for a circuit of any complexity. I wouldn't recommend it.

Here's something else that may be a helpful tip. We do these predictions five or six times during the development cycle. This data is then published to show our progress toward our reliability goal. We can use this data to predict when we will reach the goal. It's also a useful tool to keep upper management informed of our progress.

As promised, let's discuss more about the Arrhenius reaction-rate model *(Fig. 3)*. In 1889, Svante Arrhenius determined this model empirically in his experimental study of the effect of temperature on the sucrose inversion rate. It has since been used as a reasonably accurate method of predicting the effect of stress on the reliability of semiconductor devices. I'm not aware of any successful attempt to derive this relationship theoretically. The model does work, though, so why not use it? The activation energies (Ea) for various failure mechanisms and types of devices have been measured and are included in the software for reliability-prediction programs.

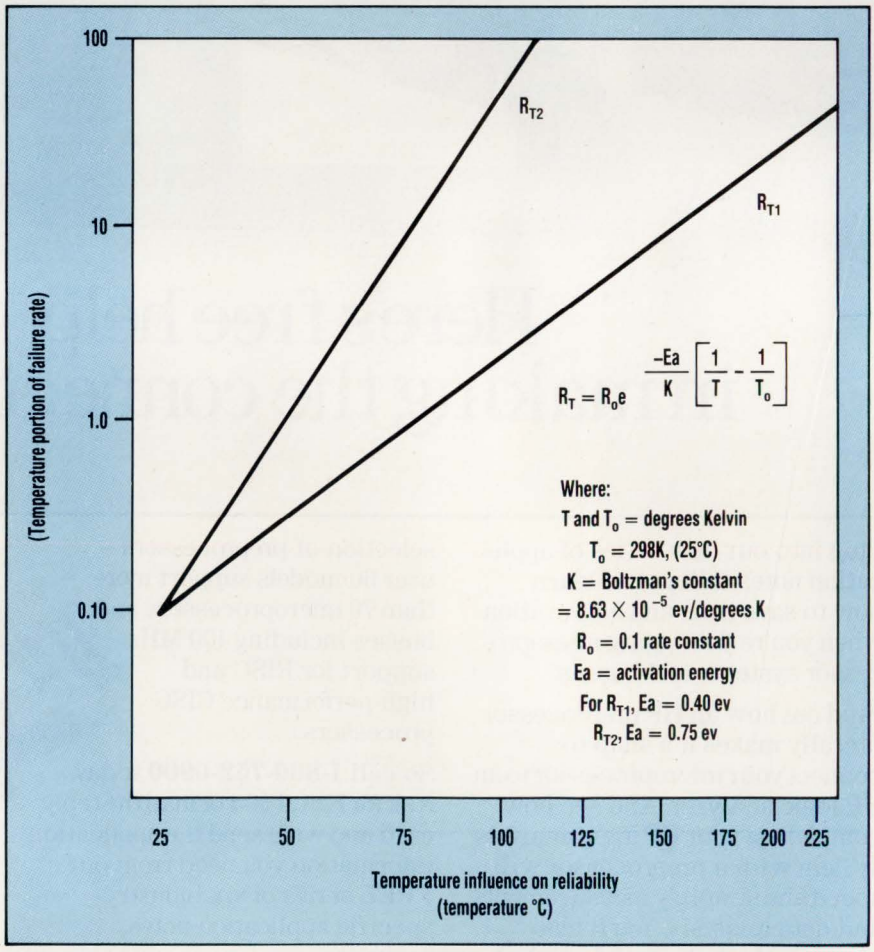
Another lesson from the Arrhenius model is that stress kills electronic designs. The exponential nature of this relationship clearly shows that the three most important things you can do to improve the reliability of your designs is to derate, derate, and derate. Don't operate at rated power, voltage, current, junction temperature, and so forth.

We have found a target level of less than 50% of rated stress gives overall failure rates less than one-tenth the ones at rated stress based on field failure data. We're now designing to less than 40% of rated stress on a critical project. You won't always achieve less than 50% because of the various other restrictions placed on your design. But derating should be your top priority when considering how to improve reliability. Derating has played a big part in achieving a ten-fold improvement in reliability.

Board Layout

One aspect of design for reliability that's often overlooked is the effect of board layout. The obvious concern is the effect of board layout on the temperature of sensitive components. Unfortunately, there's no simple set of rules to solve this issue. Sometimes, you may want to place a high-power component in the cooling airstream next to the inlet air to maximize its cooling.

In other circumstances, you may want to set the component next to the outlet to minimize the effect on the temperature of the cooling air in the box. In general, avoid blocking the airflow with large, high-profile



3. The Arrhenius reaction rate model predicts the effect of stress on the reliability of semiconductor devices. The activation energies (Ea) for various failure mechanisms and types of devices have been measured and are included in the software for reliability-prediction programs. The exponential nature of this relationship shows that derating a design boosts reliability.

National Semiconductor

Our quad high-side driver is the perfect switch for your intelligent environment.

Offering four independent 1A switches.

The LMD18400, the industry's first and only quad high-side switch, truly has a mind of its own.

Our intelligent solution has four independent power switches, each with a separate ON/OFF control. They're capable of driving 1A continuous and 3A peak loads. Together, they have a rating of 6A peak.

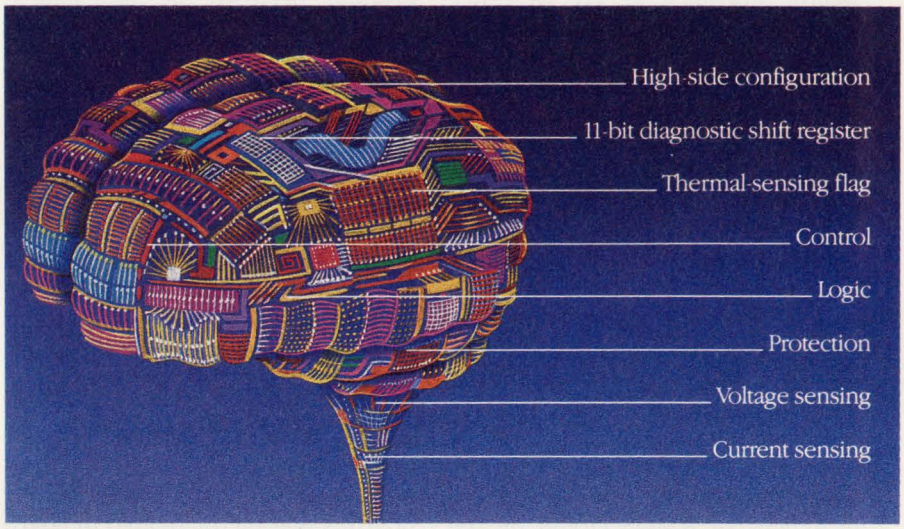
Our quad design achieves a higher level of integration and saves you a valuable chunk of real estate.

What's more, it drives every possible load: resistive, capacitive, and inductive. Making it the ideal design for automotive and far-reaching industrial applications.

Communicating with 11 diagnostic checks.

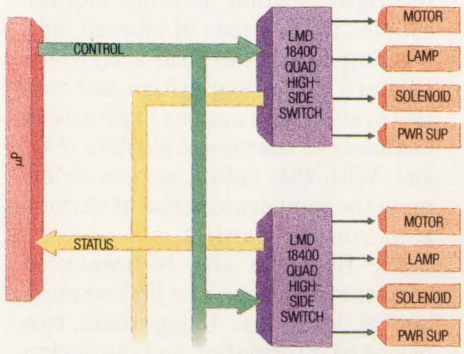
With a built-in serial interface, the LMD18400 provides extensive diagnostic data to a μC or μP, including switch status readback, output-load fault conditions, and thermal and overvoltage shut-down status.

Which results in bidirectional, real-time communications that can prevent blowouts, minimize downtime, and maximize your system performance.



Providing unparalleled protection.

By integrating CMOS, DMOS, and bipolar on the same chip, we're able to deliver an optimized, mixed analog+digital technology for power, control, *and* protection.



Parallel operation of LMD18400s

Fail-safe protection. Which means a two-stage thermal warning system that sends a distress flag to the host system at 145°, giving you ample time to take corrective action. And should the temperature reach 170°, the device automatically shuts down. A critical feature that can make your design less susceptible to damage.

It also means voltage and current sensors, which prevent burnout with an instantaneous power limit of 15W. And due to its high-side configuration, an accidental short wouldn't ground the battery.

Make the intelligent switch.

For your LMD18400 design kit, call or write us today.

And get an inside look at the brains behind the brawn.

1-800-NAT-SEMI, Ext. 107
National Semiconductor Corp.
P.O. Box 7643
Mt. Prospect, IL 60056-7643

National Semiconductor

CIRCLE 109

components. Heat sinks and heat exchangers need large surface areas to transfer heat to the cooling air. It is better to have turbulent flow over a heat exchanger's surface than laminar flow. The advantage of turbulent flow for cooling is diminished by taking more fan power to maintain flow rate when turbulence exists.

There must be a textbook somewhere that addresses these issues, but a fairly limited survey I made recently turned up only two references. We have an internal thermal design reference at HP. Another helpful source is Bell Telephone Labs' *Physical Design of Electronic Systems*, (Englewood Cliffs, N.J.: Prentice-Hall, 1970).

Board layout also affects electrostatic discharge. This discharge can come from external or internal sources. It's important to keep conductors connected to sensitive circuits away from any potential sources of high voltage. Several years ago, I was working on a high-voltage power-supply design for the CRT display of an oscilloscope. My power supply was working fine, but every time I tested the supply by shorting the output filter capacitors, an expensive NMOS circuit on the sweep board—way over on the other side of the scope—failed.

After several days' work I discovered that the ground I was shorting the capacitor to had enough series inductance to move several hundred volts in a very fast-rise pulse from the arc. This in turn coupled through a filter capacitor to the +15-V supply connected to the NMOS circuit. I solved the problem by improving and isolating the high-voltage supply ground.

Another hazard of board design is leakage currents into high impedance circuits. They might work fine in all of your tests, but six months later in the customer's humid environment, they may develop a leakage path of sufficient current to cause a failure. Several things can be done to prevent this problem. Using test-fix-test is your last line of defense and requires a week or so in a humidity chamber for each test. We usually identify these sensitive circuits early and design in isolation from leakage sources by putting grounds between the high impedance circuits and the potential sources.

These can be ground lines that you need anyway. Just route them through the critical areas—assuming this doesn't conflict with another requirement. Finally, board layout is critical to the success of your overall design. Though it may be unpleasant, board layout requires engineering attention—it's not something you can turn over to a board-layout technician.

Thermal Design Measurement

Measuring the results of the thermal design you've proposed for your board is one factor related to board layout. If your designs are similar to ours, this measurement is often needed long before the actual parts are available for testing. We've done this two different ways.

The simplest route involves building a prototype instrument and a test board with the correct power loading created by loading resistors in about the right location, locating thermocouples in the areas of interest, and running a test. We use a Hewlett-Packard 3497A acquisition and control system with options to give us 40 channels of thermocouple data *(Fig. 4a)*. With this setup, we can determine the temperature rise at various points on the board.

Air flow can also be measured with this approach at a limited number of locations. Using these two pieces of information and the design parameters of the various devices to be used, we're able to do a good first cut job of thermal design on our new circuit board. This is usually a fairly rough cut. The real test comes when the actual prototype board is available for doing the thermal scan and some more test-fix-test design work.

In our business, testing is often fairly late in the design process because the critical devices on the board are almost always ASICs. To solve this problem, we've obtained a custom circuit from a proprietary source to generate the required power to simulate the new ASIC in its package. This clever device can be packed in the same package as the new ASIC and adjusted to dissipate the same power that the ASIC is predicted to dissipate. This device also contains several diodes to measure the IC's temperature rise. We put this circuit together with the other available circuit elements on a prototype board and do the thermal scan *(Fig. 4b)*.

This gives us a good measure of the board's thermal design, including the expected junction temperature of the new ASIC parts long before the actual parts are in our hands. We're just getting started with this procedure, but I believe it will allow us to avoid the last-minute thermal design problems that were sometimes experienced in the past. At present, this part isn't commercially available, but may be in the future. Another possibility is to build a breadboard version of this circuit or to ask your friendly ASIC vendor to provide a test circuit.

If you're in the electronic design business, chances are you're also interested in the mechanical design of your products. The mechanical aspect can mean the difference between whether your electronics survive or not. Because this area of design effort often gets less than its share of attention, these problems occasionally escape detection during

SELECTING A GOOD SUPPLIER

Technology

Processes (first-hand observations)
Yield (data, consistency)
Documentation (accuracy)

Quality

Goals (written and visible)
Data (production-quality records)

Responsiveness

Open, honest atmosphere (at all levels)
Willing partner
Mutual trust
Mutual benefit

Delivery

Production flexibility
Production capability
Capacity
Turnaround time

Cost

Price
Reliability (cost of ownership)

Business

Cost
Financial position
Quality of management

the design process.

Several years ago, we were made well aware of this problem when we had a serious field failure problem with a "plug-in" board in one of our first-generation digital scopes. Because we had an exchange program in place for this board, we got all of the failed boards back at the factory for repair.

When we tested these returned boards on our production test equipment, more than 30% were found to have no problem. Soon we began to notice the same boards turning up again and again for repair with the same result: no trouble found. Careful inspection of a board revealed a capacitor with the insulation scraped off a small area of its edge.

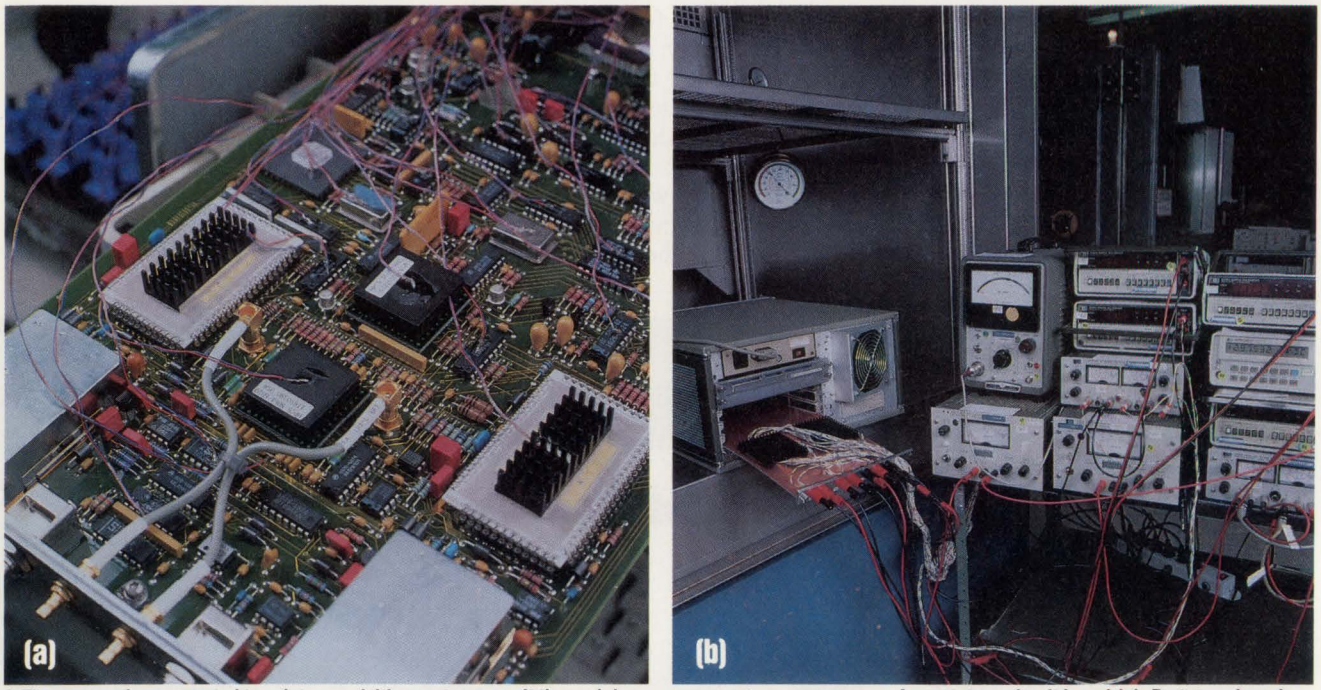
Eventually, it was discovered that each time the board was installed, this capacitor scraped against the side of the instrument. The resulting damage left a short circuit across the capacitor's terminals, forcing the instrument power supply into current limit and creating a failure. When we tested them in our factory system, the short was cleared and no problem was found. This was a simple mechanical design problem of not allowing enough clearance between the component and the chassis to account for the variations in the capacitor's position during wave solder.

Finding this problem was difficult and expensive. Preventing it would have been easy. Paying the same attention to clearances and fits as we do to current, voltage, and power would have done the trick.

The biggest mechanical design killer of electronic equipment is shock and vibration. Your equipment must survive two kinds of mechanical environments to be reliable: shipment to your customer and the customer's environment. We test for both in a separate set of vibration and shock tests. These tough tests aim at eliminating any problems in all but the most severe conditions. They're loosely based on the specifications for MIL-T-28800D class III type 3, or 5, depending on end use.

The biggest difference between the MIL-T-28800D tests and ours is that we account for the mass of the instrument in specifying shock tests to maintain a constant-velocity change and test for vibration to a higher frequency. In the tests, amplitude is varied according to frequency of vibration for a constant power spectral density. Our field studies show that these tests closely simulate the real-world environment our instruments must survive.

Much of this shock and vibration design is just the old test-fix-test routine. However, you can get a jump on this process. First, measure the environment your components must live in relation to the environment where your instrument resides. These measurements are often very different because of what mechanical engineers call transmissibility (Qa). This



4. Thermocouples connected to a data-acquisition system permit thermal rise measurements on many areas of a prototype circuit board (a). Prototype boards for instruments are typically built late in the design process because the critical devices usually are ASICs. To solve this problem, HP's engineers package a proprietary circuit to mimic the ASIC's power dissipation and temperature rise. The device goes on the prototype board along with the other circuit elements to undergo a thermal scan (b).

number is just the ratio of a system's response acceleration to the input or excitation acceleration. The fact that it's called Qa is no accident because it is simply a measure of the mechanical system's Q. Various resonances exist in any mechanical system. These resonances can cause significant damage to the component parts of the system.

Materials Engineering

Five to ten times acceleration gain isn't unusual. Fix those problems first. You might want to ask your mechanical engineers to consider doing a finite-element analysis of the chassis design to see these problems and design them out of your equipment. When you've finally got the mechanical design to pass whatever specification you're working to, I would recommend one final test. Do a series of shock tests varying pulse width and amplitude to discover where the "damage boundary" of your instrument is located. There should be sufficient margin between the boundary and the specified performance to ensure that normal manufacturing variations won't result in an instrument that will fail during shipping or use.

At HP, we have the luxury of a separate group of materials engineers. This is an important part of achieving highly reliable products. It's also a very specialized engineering skill that requires lots of time and training to master. Even a small company would be well advised to have at least one engineer dedicated to materials engineering. In a broad sense, materials engineers have four main functions: they help the design and production engineers with component selection; along with the purchasing agents, they select suppliers for those components; they deal with the technical problems that arise in relation to those components and suppliers; and they help select the correct technology for the specific application.

Selecting components requires expert knowledge of what's available in the marketplace, what's going to be available in the future, and what's about to become obsolete. The technology that best suits which application and how to apply the part in the current circuit must also be known. Another issue that materials engineers must resolve is how to deal with unspecified parameters, how these parameters affect the end product reliability, and how these parameters are likely to vary from supplier to supplier. Obviously, the list shows that the materials engineer is typically an experienced engineer with a broad knowledge of the materials being used by the designers in your company. This is a knowledge gained by years of experience and lots of first-name contacts in the supplier factories.

Product reliability problems are frequently caused by faulty or misapplied components. When this occurs, the materials engineer's expertise is your best defense. This is the person who knows the supplier and knows who to work with to get the problem solved. He will also be working with your in-house people as well as the supplier's failure-analysis people to determine the cause of any perceived component problem. Why should you, as a design engineer, care about all of this?

Because guess who the *company* is going to come to for a solution when there's a field-failure problem. You already know the answer. It's a pretty helpless feeling when this happens, not having a clue as to what the cause of the problem is. At this point, the materials engineer becomes your best friend.

Another attribute that can be of great value is his ability to find good

suppliers for the parts you use. There are usually several choices for any given part, some better than others. The materials engineer can help you avoid future problems, such as using a part that's about to go obsolete or a vendor that has a history of late deliveries or that is about to go under (no deliveries at all).

Searching For Suppliers

I've included a short checklist to help as a guideline if you're forced to select your own vendors *(see the table)*. If you find yourself in the role of selecting vendors, you need to understand that the people you're dealing with are typically honest, ethical business people. But even the best of them look out for their own best interest, and you may not be told everything you need to know. I always assume that the "law of the jungle" applies until I've had enough positive experience with the persons involved to feel confident they'll tell me if there's a problem.

Another issue to consider when selecting components is quality level. Our typical field repair costs $1000 to $5000 to accomplish. Say, hypothetically, that if you save 20% of the part cost on a $5 part in exchange for a reliability loss of 0.1% a year, you will spend your savings in repair cost in the first year and make 0.1% of your customers mad at you. Go for the high-quality, high-reliability parts. When you consider the unmeasurable cost of lost business, it's hard to justify using anything but buying the most reliable parts.

I didn't say the most expensive parts you can buy. Buying reliability achieved by inspections at the end of the production process isn't going to help. Use all of the tools of the materials engineer to determine a vendor for your parts that can produce consistent, reliable, and quality parts. They might not be the cheapest, but may turn out to be the lowest cost.

I addressed the issue of reliability testing briefly in the section on reliability prediction. I told you that accelerated testing doesn't work as a method of predicting reliability. I've found that reliability testing can help reveal weaknesses that need to be fixed. We have used that method in our pursuit of John Young's 10 times goal.

Early on, we found that a series of rapid temperature cycles would accelerate early failures. The test that we've used effectively cycles temperature between the extremes of our operating specification at 10°C per minute or faster while cycling power on the instrument.

Power is off during the cool-down part of the cycle and on during the warm up. We dwell in temperature at the cold and hot extremes for one half hour so that the instrument can catch up to the ambient temperature, and to do some testing. We run a continuous self test during the cycle any time the power is on to catch and re-

port any serious malfunctions to the controller. We use this test as part of the qualification testing of new products, during development and for the first 100 or so new instruments. Currently, we find few problems with this test because it's intended to find design weaknesses. In addition, with our present use of design for reliability, few of these problems are left to find.

If you decide to use this kind of testing, some customizing of the test will need to be done for your own products and customer use environment. This can be done on a production instrument by running the test on some percentage of your shipments and carefully monitoring the resultant field failure rate.

In 1985, we found that on our 1630G instrument, the failure rate of the tested and repaired instruments was about one third that of the untested instruments (4.1% on the tested instruments vs. 11.4% on the untested ones). The customizing is done by looking for improvement in the field failure rate of the tested instruments when compared to the untested ones.

Test conditions that are too severe will result in worse field failures for the tested instruments. Test conditions that are too lenient fail to produce a difference in field failure rate. Some electronic-equipment manufacturers use stress screening similar to what I've just described on all of their production instruments to find and fix problems before shipment. I prefer to design out the problems rather than screen them out as part of the production process.□

ROY WHEELER

Roy Wheeler, product quality engineering manager at HP's Colorado Springs Division, has a BSEE from the University of Illinois. He has 37 years of engineering experience, most of it in research and development.

HOW VALUABLE?	CIRCLE
HIGHLY	547
MODERATELY	548
SLIGHTLY	549

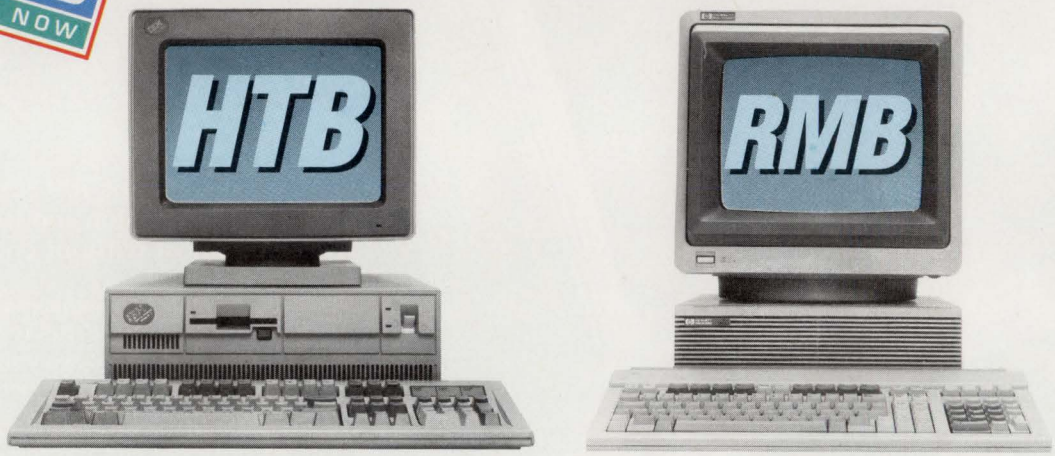

BITS OF INFINITY.
The Nicolet 400 Series provides precision and flexibility almost without end.
High precision and modular design help the Nicolet 400 DSO Series test virtually everything . . . especially your imagination. Choose from 224 different configurations!
Every 400 starts with a built-in MS-DOS disk drive, FFT and averaging. Even a LEARN mode to automate test sequences. The rest *you* design . . . bit by bit.
First choose two or four channel operation, with 64K to 256K memory in each. Then select eight or 12 bit digitizing resolution, or even a combination of both. Single ended or differential inputs. And anywhere from one to 200 MS/s digitizer speed.
From there, maybe add a 44MB removable hard disk or 40MB internal disk for awesome memory capacity. Then continue with a dual timebase, and powerful *Nicolet-Windows* PC software for instant remote control. It all adds up to high precision that's made to order . . . and not one bit less!
Discover the world's new DSO technology of choice, only from Nicolet. Send for a new 400 brochure today.
Nicolet
INSTRUMENTS OF DISCOVERY
Nicolet Test Instruments Division
5225 Verona Road, Madison, WI 53711-4495
608/273-5008 or 800/356-3090

CIRCLE 136

All the features of HPBASIC, and more.

For less.

TransEra HTBASIC 3.0 ORDER NOW



HTBasic	BASIC FEATURES:	HP BASIC
YES	IEEE-488 GPIB (HP-IB), RS-232 Instrument Control	YES
YES	Integrated Environment: Mouse, Editor, Debugger, Calculator	YES
YES	Supports 16 Megabytes of Memory (breaks DOS 640K barrier)	YES
YES	Engineering Math: Matrix Math, Complex Numbers	YES
YES	High Level Graphics: Screen, Plotter, Printer	YES
YES	Structured Programming with Independent Subprograms	YES
YES	Runs on Industry Standard Personal Computers	NO*
YES	Industry Standard Graphic Printer Support: Epson, IBM, lasers, etc.	NO
YES	Industry Standard Network Support: Novell, IBM, Microsoft, NFS, etc.	NO
YES	Industry Standard IEEE-488 Support: National Instruments, IOtech, etc.	NO
YES	Exchange data files with Industry Standard PC applications	NO*
YES	No-charge Telephone Technical Support	NO
YES	Instant on-line HELP system	NO

A Costly Situation. Every engineer needs the power and features of a "Rocky Mountain" BASIC workstation, but not everyone can have one. They simply cost too much. Fewer workstations, less productivity. **The Best Way.** TransEra HTBasic software provides the *only* way for serious technical computer users to turn their PC into a workstation without having to add costly hardware. Powerful workstations for everyone means greater productivity. **Extraordinary Versatility.** In addition, TransEra HTBasic works with the Industry Standard Personal Computer hardware, software, and networks. It even allows you to easily exchange data between your favorite DOS programs and the files you create in the BASIC workstation environment. All at a fraction of the cost of other solutions.

More compatibility. More versatility. More possibilities. Less expense. Less hassle.

To find out more, call 1-801-224-6550.

TransEra
Engineering Excellence for 15 Years™

CIRCLE 133

INCREASED DESIGN-TEST INTEGRATION WILL CUT DEVELOPMENT TIMES

TODAY'S CAD/CAE TOOLS HOLD THE KEY TO FUTURE AUTOMATION OF TEST DEVELOPMENT

Designers of electronic equipment are under rising pressure to reduce product development time. This is especially true among ASIC vendors, whose survival depends on fast delivery of new designs. For these manufacturers, and their customers, the future holds hope on two fronts: integration of design and test, and increased automation and leveraging of the test program development process.

Current CAD/CAE systems form the foundation for integrating design and test. The industry has focused on the tools needed for IC design: schematic capture, circuit simulation, layout, and so forth. With these tools have emerged frameworks and consolidated design databases. It should now be possible to include test circuit information into these frameworks and databases.

A good starting point would be the ability to "sketch" a schematic of a proposed test setup. The IC would be a black box at the schematic's center, with connections to the load board and the test system placed along the circuit's outer edge. The sketch would show the connections between the IC pins and test system channels, as well as local components. Other symbols would represent tester instrumentation and load-board components. At the simulation level, models that represent tester performance and limitations would allow the IC designer to ensure basic testability as the design is brought up.

The intent of this scheme is not to make the designer responsible for detailed test development, but to share ideas between the designer and the test engineer, each of whom maintains his or her own expertise. Given easy access to the sketch and to appropriate tools, the test engineer could build on the designer's rudimentary sketch. Similarly, if tester models are readily available to designers, they might throw a "reality switch" at certain points in the design process and get a feel for the tester's bandwidth limits. On the digital side of a mixed-signal IC, a simulation using ideal logic states, but including the tester's timing restrictions, may suffice.

For this scheme to work, CAD/CAE vendors must give test engineers appropriate tools. Schematic modification and circuit simulation must be a natural process, not another expertise to be learned. Furthermore, emerging mixed-signal simulators must be able to model test instrumentation and load boards.

Test system vendors also must meet several challenges. Vendors must supply concise, simulator-independent descriptions of tester instrumentation. They must also consult with CAD/CAE vendors to develop standard ways of exchanging netlist and stimulus/response data. In general, tester vendors must move from a "testercentric" viewpoint to a vision in which design and test engineers share development tools and data.

For semiconductor manufacturers, the challenge is cultural. They must stop regarding design and test as separate processes and consider them to be one process performed by a team of engineers with differing expertise. By doing more in parallel and sharing information at early stages, they will reduce the overall development time and cost.

Besides improvements in the integration of design and test, the mixed-signal test development process is becoming more efficient and more highly automated. For example, advanced tester simulation now permits test development on a workstation, which is a more accessible and less expensive resource than the tester itself.

Also, the test engineer's dependence on computer language syntax is being reduced. Testers' traditionally passive instrument status displays can be enhanced to allow graphical setups of simulated or actual instrumentation. The test language needed to program those setups can even be generated automatically. In the future, displays could conceivably be derived from the test schematic discussed above.

Even larger gains are possible if the test development environment supports the reuse of previously debugged test methods. For that to happen, engineers must be able to encapsulate or modularize tests, then easily modify and assemble the modules into new programs.

These test modules can be entire tests (such as leakage or supply-current tests), test algorithms (linearity or signal distortion, for instance), or special ac waveforms or critical sections of a digital pattern. Besides leveraging a test developer's effort, such a system would improve code consistency and, therefore, maintainability.□

BRUCE WEBSTER

Bruce Webster, manager of system applications at Teradyne's Industrial Consumer Div. in Boston, received his BSEE from Worcester Polytechnic Institute. He helped develop test systems for data converters and telecommunication devices, and is now focussing on computer-aided test-development software.

FASTER, MORE CAPABLE PLDS WILL INCREASE DESIGN FLEXIBILITY

BUT AS PROGRAMMABLE DEVICES PROLIFERATE, TOOL VENDORS MUST RUN HARDER TO KEEP PACE

As both the variety and complexity of programmable logic devices (PLDs) continue to increase, more and more designers are finding these devices a quick and cost effective alternative to gate arrays and other high-end ASICs. After explosive growth in the number of programmable logic architectures in the 1980s, these devices are now mainstream components. And their use continues to grow faster than any other type of ASIC.

The coming years will see several major trends affecting PLDs, including: increased usage, continuing time-to-market pressures, greater capability, and new manufacturers of PLDs.

We have already seen designs using 150 PLDs per board. In the 1990s, the number of boards using programmable devices will continue to rise, as will the programmable gate count per board. However, increased programmable device complexity and package size will shrink the absolute number of programmable device required per board.

Increasing time-to-market pressures, as well as shorter product life cycles, will add to the growth in PLD use. Earlier devices were not fast, dense, complex, or cheap enough for many high-volume production applications. As a result, PLDs were often used in low-volume runs or in prototypes of high-volume designs. But today's devices address the former limitations head on, offering designers a way to get products to market quicker.

Even though today's PLDs are much more complex than those of a few years ago, systems engineers continue to require more density, performance, and speed from devices. Many semiconductor vendors are responding with faster parts that contain unique features. These features include multiple flip-flop types, buried nodes, XOR gates, folded arrays, and completely new architectures that deviate from the traditional sum-of-products PLD.

Other vendors are responding with unique programmable architectures. The most notable of these are the field-programmable gate array (FPGA) from companies such as Actel, Xilinx, Plessey, Plus Logic, and Peer. We expect that FPGAs will be the largest PLD growth area, with design teams using FPGAs growing from a current 10% worldwide to 40% by the mid 1990s. All told, the marketplace holds over 300 unique architectures from over 20 vendors.

The number of device types will continue to increase as designers embrace the concept of reprogrammability. To accommodate this trend, flash technology, now used in memory devices, will be adopted in the logic arena.

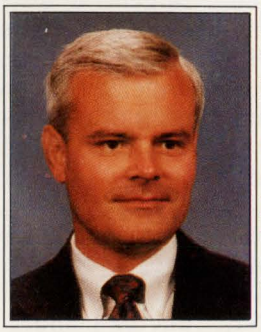
Another major shift will be in who is manufacturing PLDs. Currently, the U.S. is the dominant producer. By the mid-1990s, however, the market will be too large for Japan and the four tiger countries (Korea, Taiwan, Singapore, and Hong Kong) to ignore. At first, Japan will most likely focus on developing high-volume architectures and may become a major force in FPGAs by 1995. The four tigers will tend to concentrate on less complex, mainstream devices but will do so in large volume.

Although these trends are positive, they are not without problems. More device types mean more options for users, but also a heavy burden on design tools. New devices will create a need for partitioning capabilities to help designers assign portions of the circuitry to different devices. Future tools must also handle designs that are an order of magnitude larger than before.

Other tool capabilities that may be needed include syntax to describe new features, new optimization algorithms, more simulation capabilities, and changes to the algorithm that generates the fuse map. But most important will be the need to allow device- and technology-independent design entry, coupled with intelligent, computer-assisted device recommendation.

Many tools offer a universal front end, but what is needed for the 1990s is a back end that incorporates device-specific optimization, or a "device fitter." This will offer users the advantages of a universal entry and the ability to achieve complete device utilization.

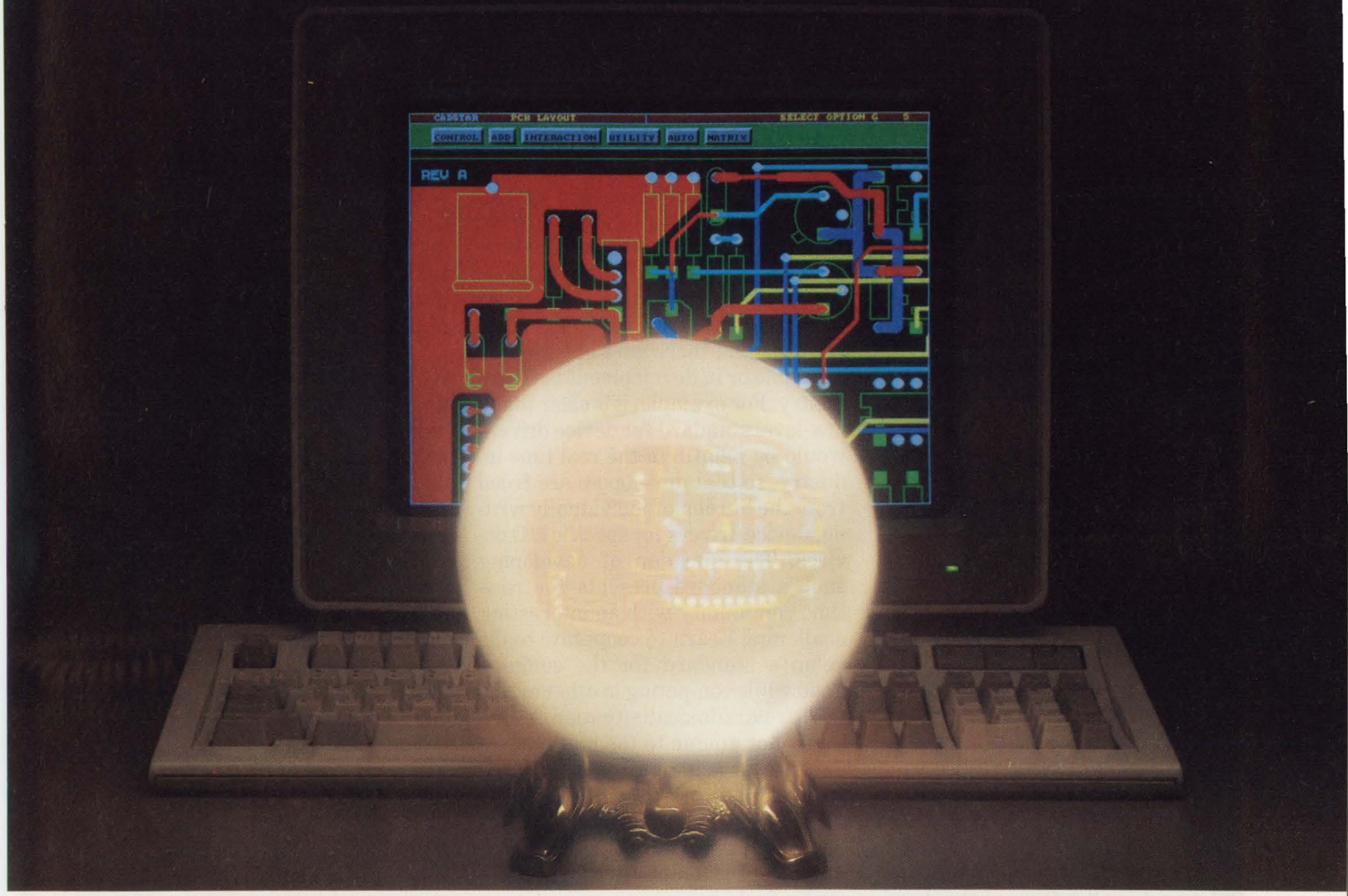
Consequently, silicon and tool vendors will have to work more closely together than in the past. Design solutions can be implemented in either the tool or the device. Some problems are better solved by adding intelligence to a tool, and others by adding more resources to the silicon. Cooperation between silicon and tool vendors is imperative if this tradeoff is to be optimized.□



THOMAS R. CLARK

Thomas R. Clark, senior vice president and general manager of product operations at Data I/O Corp., received his BSEE from Ohio State University. Before joining Data I/O in 1985, Clark served in various management and engineering capacities at Tektronix.

Introducing The New CADSTAR...



IT ALMOST READS YOUR MIND.

CADSTAR's revolutionary new user interface almost reads your mind, anticipating your next move and intelligently defaulting to the most likely action. For example, if you pick a part, CADSTAR lets you move it without selecting an action from a menu. If you pick a connection, you can manually route it instantly.

CADSTAR's new Motif style graphical interface has clear, logical menus integrated across all functions. The best part is, you'll rarely need to use those menus! Imagine software so smart, it knows what you want to do next. CADSTAR is easy to learn, and it drastically reduces keystrokes, saving you hours.

The Power Remains

CADSTAR remains the most powerful design software you can run on a PC. Unique features like comprehensive, automatic/interactive routines for placement, gate and pin swapping, and routing give you remarkable design flexibility. Racal-Redac continues to enhance the design technology used by thousands of engineers worldwide. CADSTAR includes:

- Integrated Schematic Capture, PCB Layout, Autorouting, Manufacturing Outputs
- 5,000 part library
- Double sided SMDs
- Curved tracks & copper, teardrop pads
- Copper maximization
- Blind & buried vias
- Toll Free hotline support

CADSTAR works with Racal-Redac's 386 Advanced Router, the most powerful PC based router available. It features 32 bit, gridless, shove aside, rip up and retry technology for 100% routing completion.

Is There A CADSTAR In Your Future?

Call or write for your free CADSTAR demo disk and brochure. See for yourself how powerful, and easy to use, new CADSTAR really is. Call (508) 692-4900.

CADSTAR™

RACAL-REDAC

Racal-Redac, Inc.
238 Littleton Road
Westford, MA 01886-9984, USA
Phone: (508) 692-4900
Fax: (508) 692-4725

RACAL

CIRCLE 182

STANDARDS PACE REAL-TIME OPERATING SYSTEMS

VENDORS MUST LEARN TO COOPERATE ON STANDARDS WHILE COMPETING IN OS TECHNOLOGY

If we were to sit in on the design meetings of users working with real-time operating systems, we might conclude that three trends will influence the development of future systems: standards, standards, and standards.

The need for standards is indeed important, and vendors are responding with cooperative efforts and proposals to the IEEE standards bodies. Of course, there also are major trends in the technology: operating systems that feature fully distributed architectures supporting multiple and heterogeneous processors.

The customer/market-driven evolution clearly is toward the adoption of standard interfaces at all levels of the operating system, which poses great challenges and has some interesting ramifications. For existing standards, each real-time operating system vendor can adapt to the standard interface on its own, with no interaction or cooperation required among vendors. Examples of such existing standards already widely supported include: the C language, the C standard I/O interface (stdio), TCP/IP and Berkeley 4.3bsd sockets for networking, and MS-DOS disk file format. The efforts of the IEEE Posix Working Group in adding real-time extensions to the Posix interface is another example of an emerging standard that will be of critical importance to the real-time industry. In the Posix case, real-time operating system vendors can chhose to participate in the process or just implement the results of the efforts.

The more interesting case arises when there is a need for standard interfaces and there isn't one already available or in development in the industry. For example, it is clear that a low-level standard for device drivers would be helpful in the real-time industry, so that developers are freed from the burden of individually writing device drivers for specific I/O devices. The question of developing such a standard presents the real-time community with an interesting challenge: Learn to cooperate to develop a standard for the common good while competing in other areas.

This paradoxical situation is certainly not unique to the real-time industry, but is identical to that faced by a number of other American industries—most notably the semiconductor industry, which has failed in a number of attempts to cooperate in such a fashion.

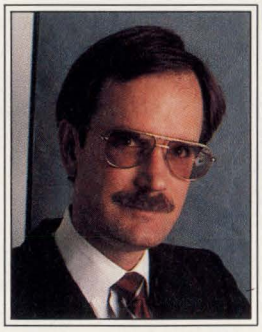
Fortunately, a number of vendors, both hardware and software, have formed the Real Time Consortium to bring about the development standards for the real-time industry. Its first effort is OBIOS (the Open Basic Input/Output System), a low-level, operating-system-independent interface for device drivers. The consortium members include Force Computers, Ready Systems, Heurikon, Lynx Real Time Systems, UniFlex, 88open and Wind River Systems. The OBIOS effort is making substantial progress with the IEEE Microprocessor Standards Committee.

The clearly heard call for standards is being accompanied by an equally clear requirement for distributed architectures. Further, specialized processors will also be included in these distributed systems so that future applications will run on heterogeneous hardware platforms. Such systems will have to support both tightly coupled and loosely coupled multiprocessor systems. One difficult part of loosely coupled multiprocessing is ensuring deterministic response times over the network, since in many cases the underlying network technology is unpredictable.

Future real-time operating systems will have to provide a uniform programming interface that will hide this multiplicity and heterogeneity of processors. Tasks written in different programming languages running on different hardware will access the same operating system services for intertask communication and synchronization.

Although operating system functionality is important, the development environment is equally critical. Development and debugging will occur without concern for processor boundaries. By interfacing to the powerful networking capabilities of workstations, real-time development tools can minimize the differences between host machine capabilities and the (usually) resource-constrained real-time target machines. Cross development will evolve toolchains equal in functionality to those found on modern workstations.

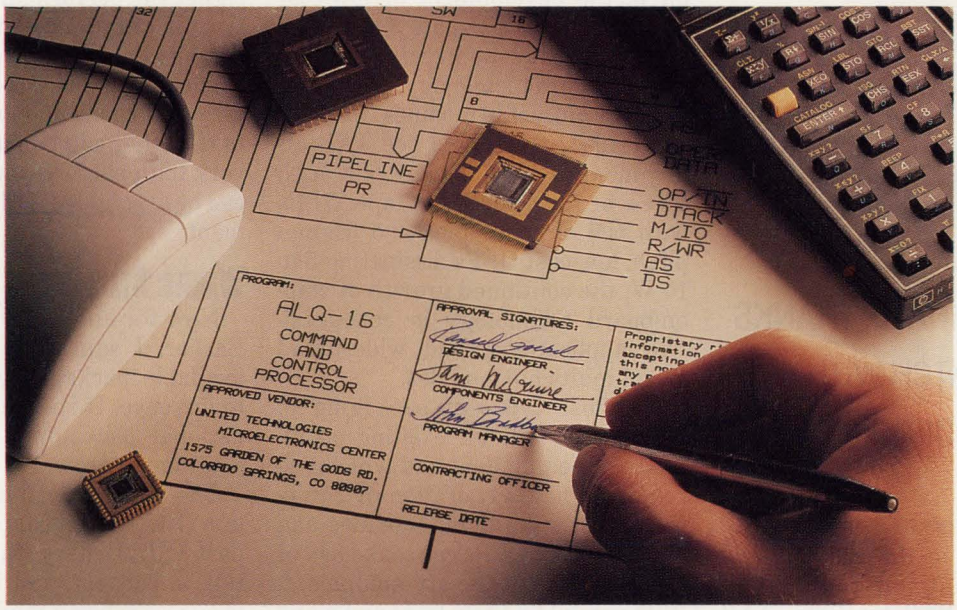
At a higher level of abstraction, visual representations of the real-time software architecture will be available to demonstrate the feasibility of the design before committing it to implementation. Designers will be able to verify that a design based on a particular operating system and application structure meets the real-time requirements.□



JAMES READY

James Ready is the founder and Executive Vice President of Ready Systems Corp., Sunnyvale, Calif. He holds a B.S. from the University of Illinois and an M.A. from the University of California at Berkeley, with both degrees in physiological psychology ("the study of neural nets—the real ones," he points out).

At last, radiation survivability is standard procedure.



You can sign-off on it.

Forget about special screening, SCDs, and lot-by-lot testing of non-hardened parts. Now you can sign-off on radiation survivability with off-the-shelf RAD-SPEC[sm] products from UTMC. Our RAD-SPEC circuits are guaranteed to meet MIL-M-38510 radiation levels M, D, R, and H after irradiation. And you get guaranteed M- and D-level RAD-SPEC products at a small premium over standard non-hardened parts. RAD-SPEC is possible because UTMC has developed the hardest production-proven CMOS process in the industry. And we've ramped-up production of military-standard and semicustom products. You can select from 1553 bus interface components, 1750 RISC processors, 75 MFLOP IQMAC vector floating-point DSP, SRAMs, and gate arrays with up to 50,000 gates. You can order RAD-SPEC products to Level S, 883 Level B, and SMD to simplify procurement procedure. Whether you need kilorad levels for a tactical program or megarad-plus for a space-borne system, RAD-SPEC guarantees better pricing, delivery, and performance. So end the confusion. Remove the risk and high cost from your radiation-survivable program. Call UTMC for more information on our complete line of off-the-shelf RAD-SPEC products.

UTMC ★★★ RAD SPEC[SM]

RAD-SPEC is a service mark of
United Technologies Microelectronics Center, Inc.

1-800-MIL-UTMC
1575 Garden of the Gods Rd.
Colorado Springs, CO 80907

UNITED TECHNOLOGIES MICROELECTRONICS CENTER

DEDICATED TO MILITARY AND AEROSPACE

CIRCLE 141

A CAUTIOUS LOOK AT PACKAGING TRENDS IN THE 1990s

MULTICHIP MODULES COULD DOMINATE, THANKS TO THEIR MATCH WITH EXISTING EQUIPMENT

A quick take on packaging trends in the 1990s would say that pin counts will reach 1000 by 1992, TAB will be the savior of the packaging world, and multichip modules will answer everyone's prayer. But sometimes, predictions go awry. Back in 1985, for instance, I was one of many who predicted that surface-mounted technology (SMT) would surpass through-hole technology in IC packaging by 1990. But that hasn't happened; a recent report titled "Advanced IC Packaging Applications and Markets," published by Electronic Trend Publications, Saratoga, Calif., says that in 1989, surface mounting accounted for just 26.8% of IC consumption.

Surface-mounted technology as we know it today will be a major player in 1995. The reasons are installed base and capital costs for new equipment. That's not to say that fine pitch, TAB, and multichip modules won't be used by the leading-edge systems builders, but most users will work in 50-mil-pitch SMT.

There's a growing gap between what the average designer uses and what the leading-edge designer uses. Not only that, but the packages designers can choose from will continue to increase in an apparently endless stream.

Let's look at what will probably happen to packaging on the leading edge. Today in the U.S., we see TAB attachment of 500 or more pins with two-conductor tape, quad flat packs (QFPs) with 208 pins and 0.5-mm pitch, the development of low-cost QFPs that will dissipate 3 to 5 W, a growing interest in wire-bonded chip-on-board technology, and the infancy of multichip modules.

By 1995, we should see TAB attachment of 1000 or more pins with three- or four-conductor tape, QFPs with 500 or more pins and 0.3-mm pitch, low-cost QFPs dissipating 5 to 10 W, the continued growth of chip-on-board technology in cost-sensitive applications, and widespread use of multichip modules.

Of these types of packaging in 1995, which will use existing manufacturing equipment and which will require a new generation of equipment? Only multichip modules and higher power QFPs can make use of today's state-of-the-art equipment. With capital budgets tight and many companies carrying debt, multichip modules could become the stars of the '90s.

With multichip modules, the user has the advantages of the high-pin-count silicon, short interconnection lengths, boundary scan built into the module's silicon substrate, and the ability to put it on a board with existing equipment (with perhaps slight modifications). This is a major plus that's often overlooked in glorifying a technology for technology's sake.

A multichip module that could be placed on pc boards with today's equipment would have gull-wing leads with a pitch no finer than 0.5 mm, but preferably 0.65 mm. Or it would be a pad-grid array with pads on no less than 50-mil pitch to minimize the footprint. Their body size would be no larger than 40 mm on a side to ensure that vision systems could see all sides of them. To gain the maximum benefit, they probably would have active silicon substrates with boundary scan built into the substrate so testing wouldn't be too difficult or expensive. They would be placed on the board and mass reflowed to minimize assembly cost.

Such modules would give the designer the performance and integration of very-large-integration components linked with very short interconnections. They would also have very fast cache memory placed close to the other components. This yields very high-performance circuits that can be assembled with today's equipment.

WANTED: STANDARDS

Now for another word of caution. Earlier, I said that the variety of available packages would continue to increase. If so, the need for international packaging standards will continue to grow.

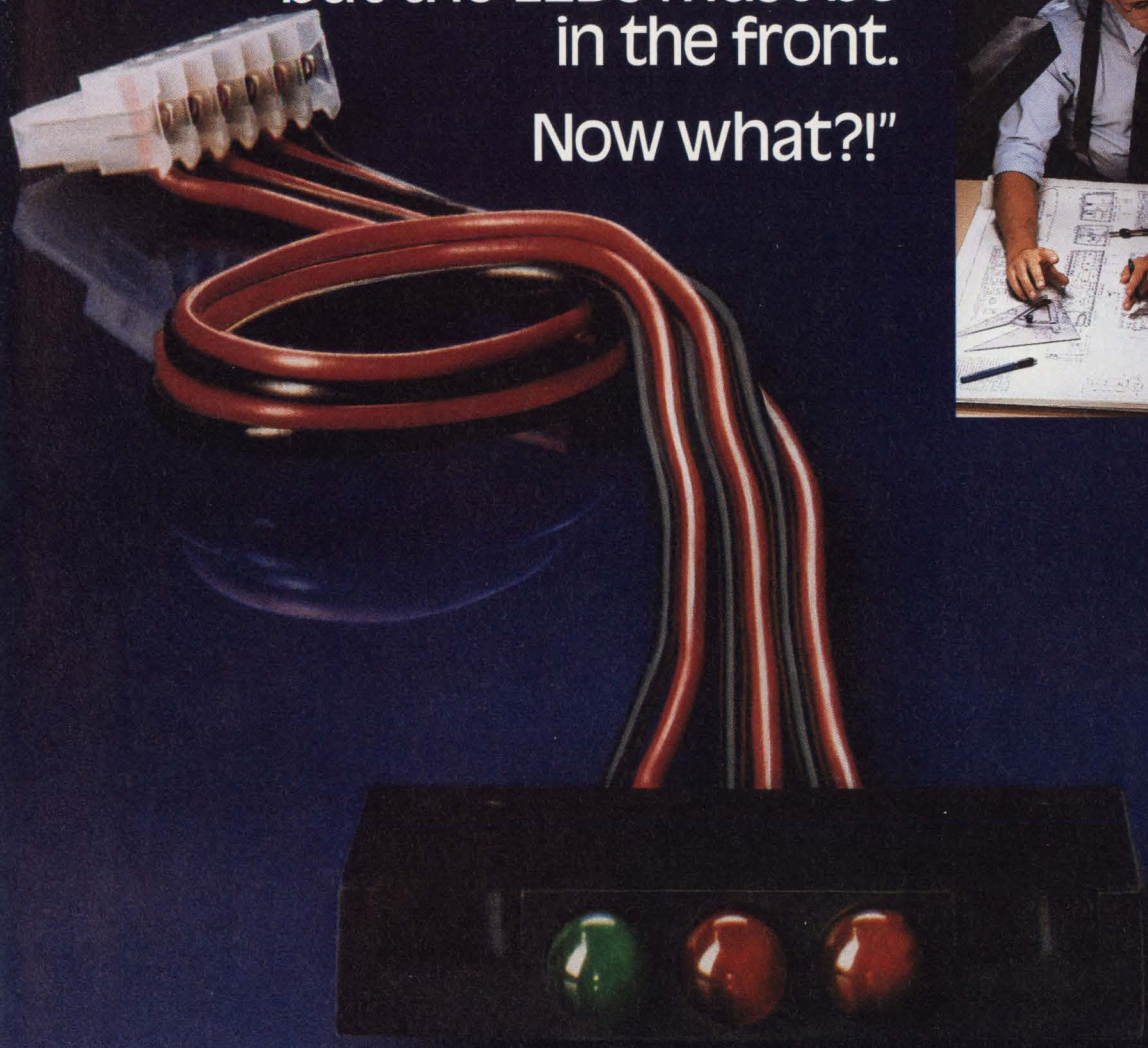
The Electronic Industry Association (EIA) and its Japanese counterpart (EIAJ) have finally begun to talk in earnest, and it appears that progress is being made. The recently approved "Jedec metric" versions of the EIAJ packages are gaining acceptance in Japan.

It's extremely important for users and suppliers alike that the various worldwide associations agree on standards for QFPs, TAB, multichip-module packages, and other types of packages. This must be done very early in the life cycle before there are too many different tooling sizes, which makes setting tight standards very difficult. We've learned many lessons from the mistakes made in the past 10 years. One is not to repeat those mistakes.□

EUGENE R. WOLFE

Eugene R. (Gene) Wolfe is packaging strategy manager for the ASIC Division of the Semiconductor Group of Texas Instruments Inc., Dallas. He holds a BSEE from Rice University and has been a director of the Surface Mount Technology Association since 1987.

"The final design has the circuit board in the back, but the LEDs must be in the front. Now what?!"



All indications are Dialight.

Call it a problem that could have lead to considerable expense. The customer thought he'd have to add several steps to his assembly process. Instead he called Dialight.

As the leader with over half a century of experience in every type of indicator light, for Dialight solving problems is standard operating procedure. Applying our engineering expertise in optoelectronics and utilizing state of the art CAD equipment, we rapidly proceeded to custom design the ideal solution – a totally integrated, remote LED indicator. Not only did it fit the unit perfectly, but it also saved the expense and effort of cumbersome wiring, soldering, and testing. Plus it added the reliability of a push-on connector for easy assembly. All while being low cost. And, thanks to our extensive in-house tool fabrication and molding facilities, we delivered it virtually overnight.

Saving costs while solving problems is something we've long done with our panel mount and circuit board LEDs. Over the years customers have asked us to pair, gang, piggyback, right angle mount, recess, bicolor, tricolor, slant, standoff, snap-mount, bin, do whatever you can imagine to them and we haven't been stumped yet!

So, the next time you think there's a remote chance of finding the right solution to an indicator design issue, remember that no one has more solutions than Dialight.

DIALIGHT CORPORATION

1913 Atlantic Avenue, Manasquan, NJ 08736 201-223-9400

CIRCLE 173

LOW-VOLTAGE SUPPLIES: WINDS OF CHANGE ARE BLOWING

THERE'LL BE A SHIFT TO DISTRIBUTED POWER SCHEMES AS TOTAL SYSTEM-POWER NEEDS RISE

The power-supply output voltage used most often is still 5 V. Because this voltage continues to dictate the design topology of most new power-supply series, any attempt at predicting trends in supply design must look at supplies with voltage levels of 5 V and below.

Until recently, virtually all power systems have been configured using a centralized architecture with switch-mode power supplies operating at frequencies in the 20-to-200-kHz range. But in terms of cost, performance, reliability, and packaging density, this technology is behind that of other typical processors and telecommunication systems.

Only recently have strides been made to boost power densities and to improve costs as measured in dollars per watt to keep up with industry needs. Unfortunately, the ever-increasing functionality of systems ultimately requires that the system's net power be vastly increased, even though the power per function has been steadily decreased. As a result, the power supply is an ever increasing percentage of the cost and size of a typical system.

In the forseeable future, power architectures will shift from the present centralized or bulk power supply to a localized or distributed power system. Choosing a design philosophy will be governed by economics and power density. At present pricing levels, distributed power seems to make sense at power levels above 1 to 2 kW. The crossover point from a centralized to a distributed power system will drop as the cost of the basic ultra high density (UHD) modules falls and the product becomes available from multiple sources.

In the near term, the direction for low-voltage supplies will be dictated by components, both passive and active: active components by the shift in the supply-voltage levels, and passive components by their influence on size and cost.

In terms of voltage levels, semiconductor manufacturers are developing more components that call for supplies in the 1.2-to-3.3-V range. One would think that logic chips requiring less than 5 V would bring a corresponding decrease in system power. But if history is any indication, this is not the case. Equipment end users demand more options in the equipment at higher computing speeds, which uses more power.

As supply voltages fall, the efficiency of present power-supply topologies decreases significantly. Any drop in efficiency causes more power to be dissipated within the power supply. The additional power means that higher temperature and/or more expensive components will be used in the supply. The result is either higher cost or a larger unit for more heat sinking. Neither option is desirable in today's market.

The trend toward lower supply voltages will hasten the change to distributed power. At lower voltages, assuming the power either remains the same or continues to rise, more current at these lower voltages will be required. As a result, the distribution of low-voltage power, which is a problem at the present time, will be almost impossible. A 200-mV drop from the supply to the load, or across the typical backplane, is not a problem when using today's 5-V logic. But it will be intolerable to the newer 3.3-V-or-lower ICs. Maintaining a very low gradient across the backplane means using many sources.

The most viable solution is, of course, to use localized power supplies, each supplying a minimum of current and located close to the load cards. At worst, a separate unit for each card could be used.

Downsizing power supplies will be impossible without innovation from component makers. The main contributors to the volume of a power supply are the input-filter capacitor, heat sinks, and the magnetics.

The size and cost of input-filter capacitors is dictated by the capacitance-voltage product for a given capacitor lifetime at a maximum internal temperature. Little change in capacitors has been seen by OEM power-supply makers, and we anticipate no outstanding improvements.

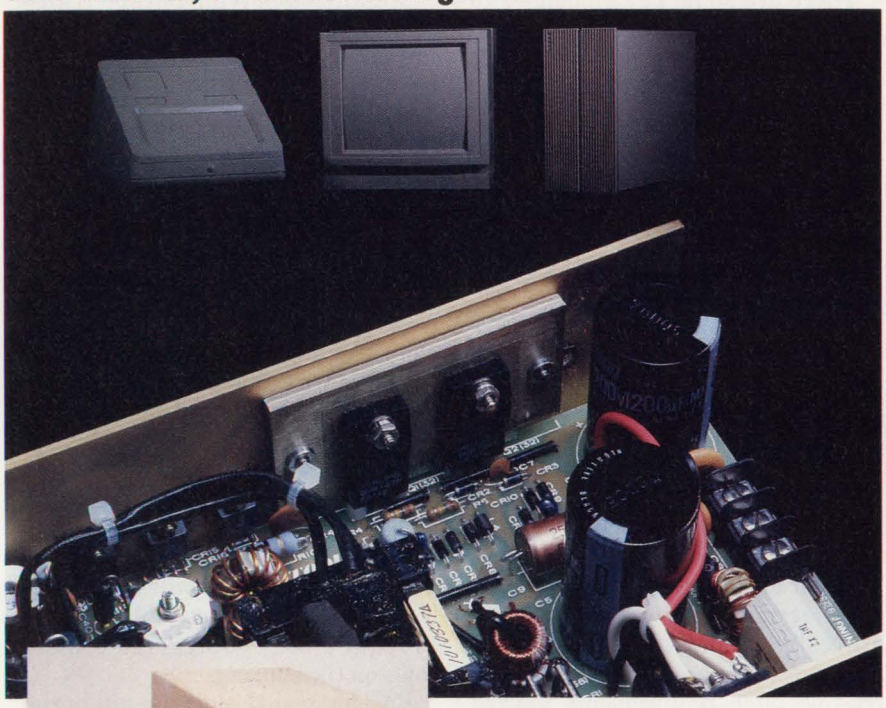
A new European specification, IEC 555-2, limits all harmomics on the ac power line. To economically meet this specification, a topology using a boost converter is best. A boost converter steps up the rectified input voltage to a fixed value of dc voltage higher than the peak value of the largest ac line voltage. This voltage is independent of the ac line voltage. Less input capacitance would be required because low line conditions would not be a factor. In addition, because the energy stored in a capacitor is (1/2) CV^2, and the volume of a capacitor is proportional to the CV product, stepping up the voltage would mean a much smaller case for the same energy level. A 50% size reduction is likely.□

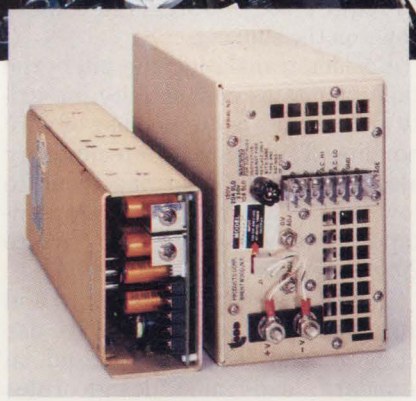
MYRON A. KOSLOW

Myron Koslow is director of field marketing at Lambda Electronics Inc., Melville, N.Y. Koslow, a 30-year veteran of the electronics industry, holds a BEE and MEE from City College of New York and an MBA from Long Island University. He joined Lambda in 1974.

Power Source Up-Date

Single Board Construction Shrinks 750W Size and Cost: 58% Smaller, 30% Cost Savings





Designed for high-end computer products, TODD's MAX-750 combines a compact size, 13.5" x 5" x 2.6" compared to the typical 5" x 8" x 11" shoebox switcher (see photo insert), and very competitive pricing. OEM product designers can reduce product size with a MAX-750 or build in power supply redundancy, replacing one "shoebox" switcher with two MAX-750's in the same space.

The small package size, high power density of 4 watts/in., high peak current for motor starting, and cooling options, make the MAX-750 the power supply of choice for VMEbus systems, workstations, file servers and mini-computer systems. The switcher provides 120 amps of +5 volts for logic and memory, and features up to three auxiliary outputs providing high efficiency, tightly regulated 12 volts or −5.2 volts at up to 20 amps. Designed for world wide use, the series offers AC power fail, AC autoline select, and meets International Safety standards and Class A RFI requirements of FCC and VDE 0871.

Call 1-800-223-TODD, or Circle # 191

High Efficiency DC Converters Fit AC To DC Footprint

TODD's DC to DC converters provide up to 350 watts from 48 volts DC input. Designed as companion units to TODD's standard line of AC input power supplies, they are fit, form, and function compatible with the MAX-350, MTC-250, MTC-350, and certain single output SC series products.

Available in a 250 watt "DC" single output series and a 350 watt multi output "DCX" series these power supplies have up to 50 amp main output of tightly regulated 5V power, two fully regulated, high-efficiency, post-regulated mag-amp outputs and one low-power three-terminal regulated output.

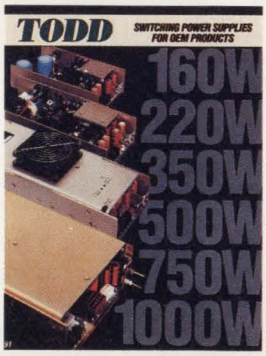
Call 1-800-223-TODD, or Circle # 192

New Technology Shrinks 500 Watt Power Supply

TODD's MAX-500 switchers pack 25% more power into TODD's 400 watt package size (11.5" x 5" x 2.5"). The series incorporates a new SMT circuit, newly-available components, improvements to TODD's VERI-DRIVE current-fed inverter topology, monocoque construction, and a high efficiency FLUX-GATE switching mag-amp auxiliary post regulation. Result: higher performance, higher reliability (approaching 100,000 hours MTBF) and lower cost.

Call 1-800-223-TODD, or Circle # 193

New Products Featured In 1991 TODD Catalog



TODD has just released its 1991 switching power supply catalog of over 100 standard switching power supplies ranging from 150 to 1000 watts, including several new products. Available in single and multiple outputs, ac to dc and dc to dc, these switchers meet a broad range of requirements for telecom, computers, industrial controls and medical electronics applications.

The catalog also provides details on TODD's approach to quality and innovative manufacturing, and capabilities for producing modified, repackaged and fully custom switching power supplies.

Call 1-800-223-TODD, or Circle # 194

More information on these and the full line of TODD Switching Power Supplies can be obtained in EEM File 4000, by circling the response card numbers, or by contacting:

TODD
PRODUCTS CORP.
50 Emjay Boulevard
Brentwood, New York 11717
(516) 231-3366 or 1-800-223-TODD
FAX (516) 231-3473

SYSTEMS LOOK TO MAXIMIZE I/O DENSITY FOR FEWEST DOLLARS

NEW TECHNIQUES HELP SLASH COST AS I/O DENSITY ESCALATES—BUT WATCH FOR HIDDEN COSTS

Most observers agree that the industry is crossing into a new, yet perplexing packaging era for I/O-intensive ASICs, VLSI, and ULSI chips. A few short years ago, the silicon-embedded functions of such chips were spread across several large pc boards. Back then, cost was foremost in engineers' minds. Nothing has changed that thinking, and if anything, sheer competitiveness has made cost loom large.

In the intense push for compactness and higher performance, driving down costs goes hand in hand with prudent design disciplines. Tried-and-true principles must be adhered to. In this regard, smart system-design managements reach the market quickly and maintain an aggressively competitive posture by minimizing radical departures.

Advanced chip packaging and system manufacturing, in particular, fall into a "caveat emptor" category. Although the industry is rife with new, expensive, and untested assembly technologies, such as some multichip-module, silicon-on-silicon, and solder-bump techniques, systems houses should resist discarding time-proven wire-bonding production. Moreover, they should tenaciously stay the course while searching for ways to cost effectively move to higher I/O densities.

There are some key guidelines to keep from wandering down the wrong path. One is to deal with ASIC vendors who have carefully plotted, long-term packaging and customer-relationship strategies. Most ASIC vendors have internal long-term strategies, as well as strategies formulated for given customers. It's important to note that these may be different, and thus exercise discernment when examining a customer strategy so as not to incorrectly infer a global strategy from it.

In addition, one should sound out an ASIC vendor's plans for near-term, cost-effective solutions for interconnection structures. Make sure an ASIC vendor isn't supplying you with something that's going to be too difficult to interconnect to.

Other guidelines include:

- Investigate and analyze evolutionary programs that comply with ultra-fine pitch requirements toward the 1992-to-1995 timeframe.
- Make it possible to move into higher I/O density without major equipment changes.
- Monitor ASIC suppliers' directions into single and multi-chip packaging and their efforts to hold down costs.

Talk is plentiful on multi-chip modules' (MCMs') promise for advanced system packaging. Tape-automated bonding (TAB), a long-standing technology, has more recently been aligned with MCMs. This combination certainly shows great potential, but at a premium. With the increasing push toward greater I/O density and tighter pin pitch, one must be wary of emerging hidden costs and related design issues associated with TAB alone and then combined with MCMs.

Systems designers seek a low-cost, highly efficient I/O lead frame with strong potential for carrying surface-mounted packaging well into the I/O counts of 450 to 500 forecasted for the mid-1990s. Don't overlook the fact that wire bonding is a proven technology that's highly efficient and relatively low cost.

Metallized-polyimide-tape-translator technology in either single surface-mounted or MCM packages, for example, appears to be a cost-effective candidate for meeting high-I/O-density requirements. This technique uses a wire-bondable tape surrounding a VLSI chip inside a standard 0.5-to-0.65-mm-pitch package. Thin conductive fingers, backed by the insulating tape, extend from the package's inner periphery to the chip. The inner-lead bond to the silicon is a wire bond. The outer-lead bond is a TAB thermal-compression bond from the tape to the lead frame.

In effect, the tape translates the external pin pitch down to the bond-pad spacing on the VLSI chip. From a wire-bond standpoint, a pitch of 125 μm or less between leads is difficult if not impossible. Thus, tighter pitches require use of staggered contact rows on the silicon.

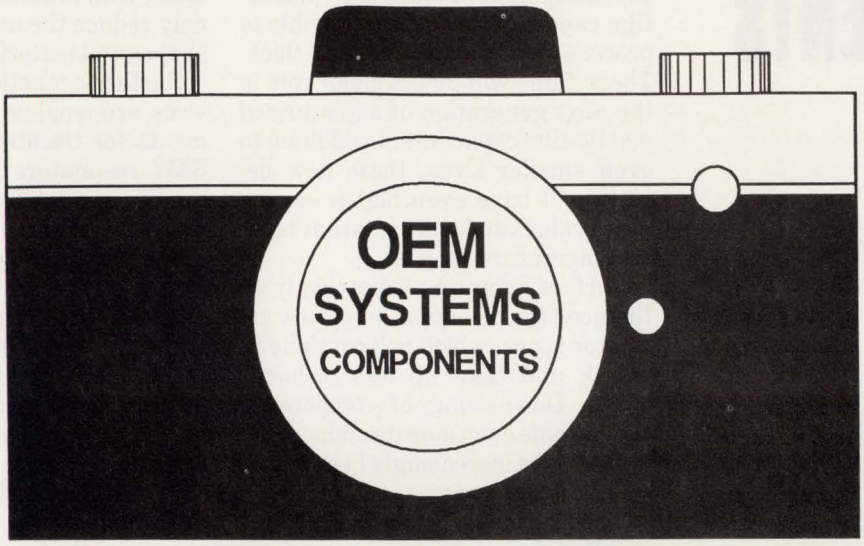
Besides translating the pitch, the tape maintains connectivity integrity and permits continued use of wire bonding. Tape-translator technology also triggers an emerging trend to low-cost, lead-frame-less chip-on-tape, which will prove to be five to 20% more cost-effective than TAB.

Consider also that 250 inputs and outputs is the limit for effective use of wire-bond technology based on standard lead-frame design rules dictating a 0.25-mm inner-lead pitch. TAB comes in to provide finer lead pitch, but with a hefty capital investment either at systems houses or with the ASIC vendor. In the latter case, added costs are passed on to system houses.□

JAMES N. ARNOLD

Dr. James N. Arnold, department head of IC packaging technology at AT&T Bell Labs, Allentown, Pa., has 16 years of experience in mechanical engineering and its application to system and IC packaging. He holds a BS in nuclear engineering and an MS and PhD in mechanical engineering from UCLA.

SHARPENING THE (OEM SALES) FOCUS:



SysComp

THE OEM SYSTEMS COMPONENTS CONFERENCE & EXPOSITION

June 19-21,1991
Santa Clara Convention Center
Santa Clara, California
(Running concurrently with the Supercomputing Show)
for:
ELECTRONIC OEM ENGINEERS, ENGINEERING MANAGERS & TECHNOLOGY MANAGERS

A technical conference and related exposition, primarily encompassing computer technology. Targeted for those involved in the design and integration of OEM systems and sub-systems for industrial, commercial, and military/aerospace applications.

For further information, call, fax, or write:
MultiDynamics, Inc.
12747 Barrett
Santa Ana, CA 92705
Phone (714) 669-1201 Fax (714) 669-9105

CIRCLE 119

PASSIVE COMPONENTS TAKE ON HIGH-TECH ROLES

MATERIALS ENHANCEMENTS WILL SPUR WIDER APPLICATION OF SOME PROVEN TECHNOLOGIES

Often thought to be passive in image as well as in function, passive components nonetheless are moving rapidly into higher technology roles. There, they will continue to play an important role in the future of the electronics industry. Passives include capacitors, ceramic components, and interference-suppression devices for a wide range of applications.

The significance of this product range is underlined by the types of products developed for dedicated applications. Major trends include the continued move towards miniaturization and surface-mounted technology (SMT), and the development of new ceramic and ferrite materials, as well as submicron-film technology for capacitors.

The capacitor's ability to store energy and discharge it rapidly makes it indispensable in all kinds of electronic circuits. And despite a turbulent marketplace, the worldwide demand for capacitors will grow.

We use a wide range of capacitor technologies (including plastic dielectric for stacked film, aluminum dielectric, and tantalum). The trend is toward tailoring designs to fit a customer's needs.

Submicron multilayer technology is already having a major impact on the production of metallized plastic-film capacitors. It is now possible to process layers only 0.5 μm thick. These films will play a major role in the next generation of miniaturized plastic-film capacitors. In addition to even smaller sizes, these new devices will have even higher capacitance values and will operate at higher temperature ranges.

Surface mounting has strongly influenced the development of new capacitor types, which will continue to shrink and take up less pc-board space. Downsizing of components will become even more prominent because of the increasingly higher densities on pc boards.

Another development trend has resulted from advances in surface-mounting technology in the production of pc boards. The total ferrite system of cores, bobbins, and assembly clips is being designed for automatic winding and assembly. Automatic assembly will be mandatory if the magnetics industry is to meet the rigid requirements of the future. The system, in any case, must be designed for automation at the outset.

In the area of ferrites, more emphasis is being placed on process capability, statistical process control, and reduction or even elimination of incoming inspection. Trends in ferrite-product development focus on new core materials with even higher initial permeability and improved saturation-flux density. Telecommunication applications, in particular, are driving this need. New high-frequency power materials are needed with lower loss at 1 MHz and higher operating temperatures. This will become even more important in wideband transformers as ISDN gains acceptance.

Even non-functional cosmetic standards are being raised. Over the next several years, new topologies (shapes) will appear, optimized to specific applications. For instance, board-mounted modular supplies for telecommunications require low component heights. Automation requirements, along with process-quality demands, may reduce the number of different shapes and materials.

Surface-acoustic-wave (SAW) devices are smaller, low cost replacements for traditional LC networks. SAW resonators are used in high-quality oscillators and filters. They operate in the "fundamental applications" mode as opposed to conventional quartz circuits, which use cumbersome frequency multiplication requiring more power and space. Growing future applications include UHF remote controls, garage-door openers, security systems, and so forth.

The increasingly high sensitivity of components in today's electronic circuits calls for optimum overvoltage protection. Because of their overall suitability and high reliability, metal oxide varistors have become indispensable as the protective component for a wide range of applications requiring overvoltage protection. Response times will become even faster in the future. Another feature is the exceptional current handling capability, especially on the larger "block" styles. In the future, we will see even lower clamping-voltage characteristics.

We will also see a wider variety of varistors manufactured as surface-mounted devices, using the proven monolithic and ceramic multilayer construction. These varistors will guarantee optimum protection at lower operating voltages. The role of surface-mounted varistors will also grow in protecting automotive electronics—especially on-board computer systems, display panels, ignition systems, and dc motors.□

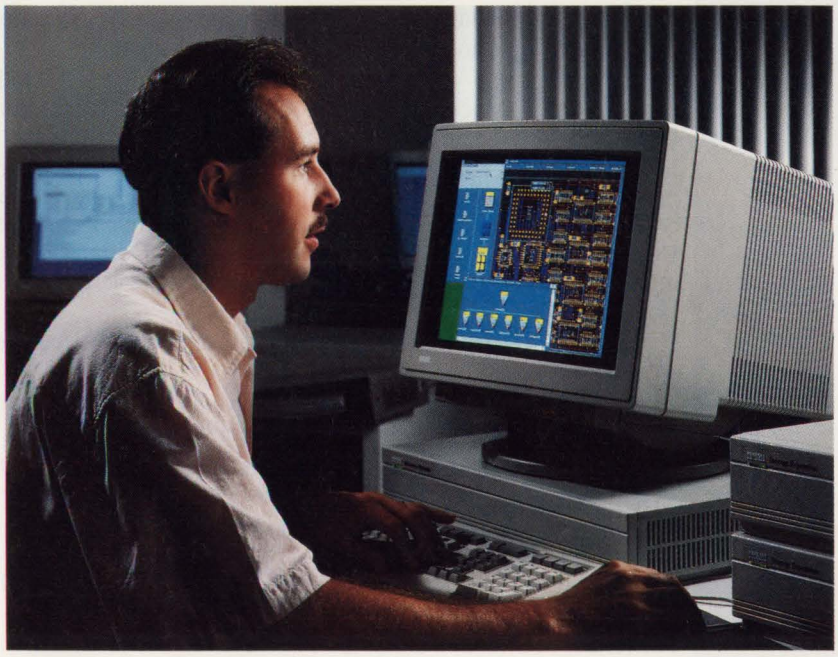
KLAUS BAHR

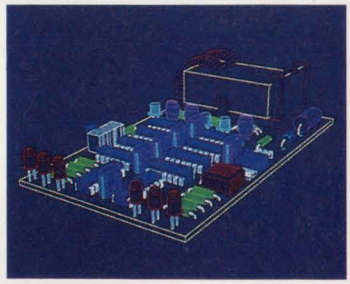
Klaus Bahr is vice president and general manager of the Special Products Division of Siemens Components, Inc., Iselin, N.J. Bahr, who joined Siemens in 1967, earned an MS from New Jersey Institute of Technology, Newark, N.J., in 1966, and a BSEE from Ohmpolytechnikom, Nuernberg, Germany, in 1956.

CUSTOMERS LIKE OUR FRAMEWORK BECAUSE IT'S FULL OF IFS, ANDS, OR BUTS

bringing the best together...

If our choice of schematic capture, layout or documentation tools doesn't meet your needs, we'll change it. And you can easily encapsulate your own point solutions in our framework as well. But if you agree with us that Viewlogic's Workview Series schematic capture and simulation, SCICARDS placement and routing, AutoCAD's drafting and documentation, and Thermax thermal analysis are the best in the industry, they are standard in our framework. We've brought them together in PowerFrame™ –a common design environment with an open architecture that lets you add or replace any of the tools in the front-to-back design process. A framework based on the fact that somebody makes the best of something, but nobody makes the best of everything. We offer theirs, ours, and yours, and make it all work within a true framework integration that tracks and controls design data from start to finish. And it's available now on the Sun and Digital platforms. When we say "bringing the best together," what's best is up to you.





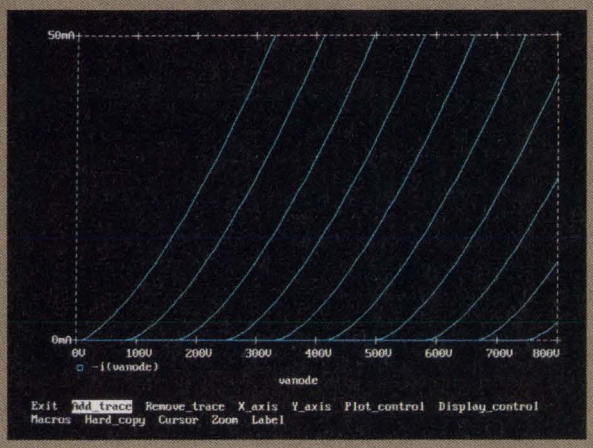
HARRIS
SCIENTIFIC CALCULATIONS DIVISION

7796 Victor-Mendon Road
P.O. Box H
Fishers, NY 14453
1-800-4-HARRIS Ext. 4432
1-800-344-2444 (Canada)

PSpice

MicroSim Corporation

The Standard for Circuit Simulation



I-V curves of a triode vacuum tube

Analog Behavioral Modeling

The Analog Behavioral Modeling option for the PSpice Circuit Analysis package allows you to describe analog components, or entire circuit blocks, using a formula or look-up table. Linear blocks may be described using either a Laplace transform or a frequency response table. Once defined, you can use these blocks in all PSpice analyses, including DC, AC, and transient.

Modeling entire blocks of circuitry is a powerful aid in designing a system from the top down. You can describe a functional block by its behavior without worrying about how that function will be implemented. Later on in the design process, you can replace the block with the actual circuitry.

Another application is the modeling of electronic components which are not built into PSpice. The photo shows an example of simulating the DC characteristics of a 3/2-power-law device.

Since its introduction over six years ago, MicroSim's PSpice has sold more copies than all other SPICE-based programs combined. PSpice provides broad capabilities, accurate results, diverse options, and availability across a wide range of computer platforms. PSpice includes an extensive device library of 3,000+ analog parts and 1,300+ digital parts, at no extra charge.

Besides Analog Behavioral Modeling, PSpice provides the following options:

Digital Simulation: simulation of mixed analog/digital circuits with feedback between the analog and digital sections.

Monte Carlo Analysis: calculates the variations in a circuit's performance allowing for component tolerances. This option performs statistical analyses: Monte Carlo, Sensitivity, and Worst Case.

Probe: acts as a "software oscilloscope" to provide an interactive viewing and processing environment for simulation results (see photo).

Parts: is a parameter extraction program allowing the extraction of device model parameters from data sheet information.

PSpice is available on the PC (running DOS, Protected Mode DOS, or OS/2), Macintosh II , Sun 3, Sun 4, and SPARCstation, DECstation 2100, 3100, and 5000, and the VAX/VMS families.

In addition to the Circuit Analysis package, the PSpice family of products also contains the Circuit Synthesis package, which consists of our two filter synthesis products: Advanced Filter Designer and Standard Filter Designer. Filter Designer is an interactive design aid for synthesizing and analyzing active filters. Features include:

- Analysis of low pass, high pass, band pass, and band reject filter types.
- Synthesis of all available filter types using Butterworth, Chebyshev, Inverse Chebyshev, and Elliptic (Cauer) functions.
- Capability to synthesize arbitrary transfer functions and delay equalization filters (only available in Advanced Filter Designer).

Each copy of our Circuit Analysis and Circuit Synthesis programs comes with MicroSim's extensive product support. Our technical staff has over 150 years of combined experience in CAD/CAE, and our software is supported by the engineers who wrote it.

For further information about the PSpice family of products, call us at (714) 770-3022 or toll free at (800) 245-3022. Find out for yourself why PSpice has become the standard for circuit simulation.

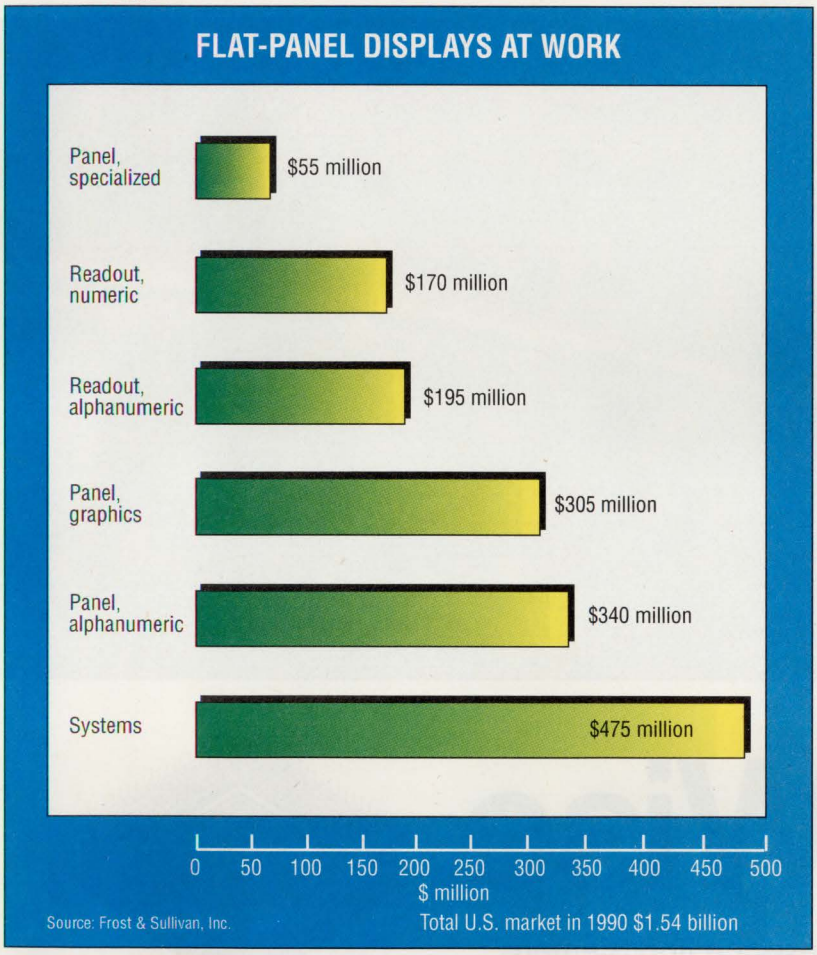
20 Fairbanks • Irvine, CA 92718 USA • FAX (714) 455-0554

CIRCLE 98

ELECTRONIC DESIGN

QUICK LOOK

EDITED BY SHERRIE VAN TYLE



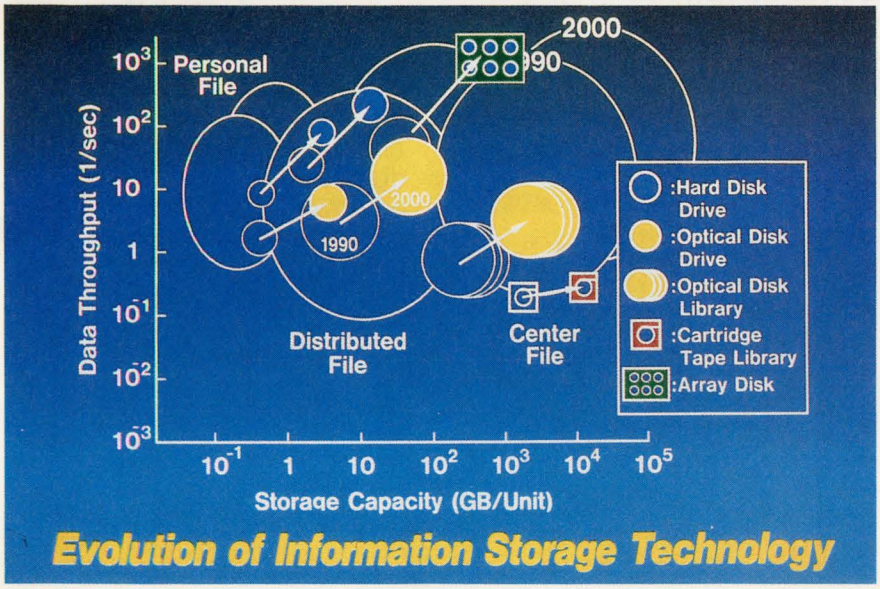
MARKET FACTS

Already entrenched in laptop computers, flat-panel displays are expected to become fixtures in automobile dashboards. As a result, the U. S. market for displays should expand from $1.54 billion in 1990 to $2.7 billion by 1994. So forecasts New York market researchers Frost & Sullivan Inc.

Flat-panel displays are an OEM market. Computer makers and others have a range of competing and improving technologies to pick from. Supertwist liquid-crystal displays are leading the market. Sales should more than double, from $325 million in 1989 to $680 million by 1994. Twisted-nematic type displays come in second, with $305 million in sales in 1989 predicted to grow to $625 million in 1994.

The fastest growing sector is the active-matrix LCD, which garnered a $22 million share of the market last year. The market for these LCDs is predicted to skyrocket, reaching $115 million by 1994. Other than LCDs, flat-panel displays include ac and dc plasma displays, vacuum fluorescent, and light-emitting diode displays—still the display of choice when fast response is required. Vendors are also looking into electrochromic, electrophoretic, and ferroelectric ceramic displays.

In most market segments, display vendors are bundling the drive and logic electronics. Adding electronics simplifies the addressing and driving of the panel elements.



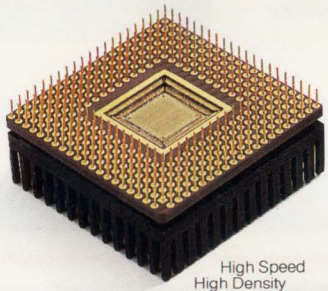
EVOLUTION OF INFORMATION STORAGE TECHNOLOGY

By the year 2000, hard-disk drives will improve in throughput and capacity by an order of magnitude. Array disk systems will replace larger hard disks, and optical disk drives will jump in capacity by an order of magnitude. (Data throughput is measured at one access per second.) These projections come from Yoshito Tsunoda, department manager for Hitachi Ltd.'s Central Research Laboratory in Tokyo. Tsunoda showed this slide at Hitachi's recent technology seminar in New York.

SIEMENS

World Wise.

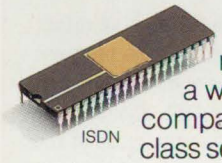
U.S. companies with a global presence find Siemens an expert, dependable source for advanced semiconductor products. From Smart Power to RISC. Santa Clara to Singapore.



High Speed
High Density
Gate Array

As the U.S. market becomes increasingly competitive, more and more companies find their domestic survival depends on how well they can capitalize on international opportunities in sales and manufacturing.

4MB
DRAM

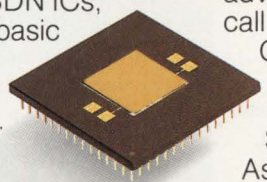


ISDN

To tap the world market, you need a world partner. A company with world class semiconductor technology and products, world wide service, support, and manufacturing capabilities, and unchallenged financial strength.

Siemens is that partner. With 173 manufacturing plants in 35 countries. 42,000 employees dedicated to R&D alone. And high performance, high quality semiconductor technology, ranging from the simplest components to the most advanced.

1MB and 4MB DRAMs. Smart Power. RISC processors. Microcontrollers. High-density CMOS gate array technology—soon to reach sub-micron dimensions. The most comprehensive line of ISDN ICs, from primary to basic rates. Chip-level solutions, for your application.



MIPS
High-Performance
RISC Processor

All that technology comes with the world class manufacturing, service and support that has made Siemens one of the world's largest electronics suppliers.

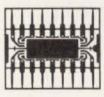
Wherever your company grows, we'll be there. From Detroit to Dublin. Or Santa Clara to Singapore.

Smart
Power

For details on our advanced products, call (800) 456-9229.

Or write:
Siemens Components, Inc.
2191 Laurelwood Road,
Santa Clara, CA 95054-1514.
Ask for literature package M51A001.

Find out how a world partnership with Siemens can help your company grow world wise.



Siemens...
Practical Solutions By Design.

QUICKLOOK

HOT PC PRODUCTS

On the market about six months, a low-cost version of the Unix operating system has captured about 5% of the PC-based Unix market. Coherent has a list price of $99. From Mark Williams Co., the operating system has System V features like shared memory, semaphores, interprocess communicators, and the Bourne shell. Coherent has a C compiler, assembler, debugger, linker, and archiver.

The operating system supports multiple users, coresides with DOS, and transfers files between DOS disks and hard disk partitions. It runs on IBM PC ATs and 286, 386, and 486 compatibles with 640k of RAM. Two drawbacks: Coherent doesn't support X Windows and, as a result, lacks support for Unix-based graphical user interfaces (GUIs). In addition, Coherent doesn't run on Micro Channel machines. Taking aim at a 20% share of the PC Unix market by the end of this year, the Northbrook, Ill., company plans to upgrade Coherent by adding TCP/IP, NFS, X Windows, an ANSI standard C compiler, graphics, and support for non-U. S. keyboards. For further information, contact the company at 60 Revere Dr., Northbrook IL 60062; (708) 291-6700; fax (708) 291-6750.

DID YOU KNOW?

. . . that in 1990, 2.5-in. disk drives accounted for just 1% of the drive market. By 1994, their market share will increase to 50%, with the other half held by 3.5-in. drives.

Electronic Trend Publications

. . . that 8-bit processors still lead the microprocessor industry in unit volume, with 10 to 12% growth a year. If microprocessors, not microcontrollers, are considered, the most popular 8-bit architecture is based on the Z80, introduced by Zilog in 1976.

Microprocessor Report

BEST SELLERS

Which technical books are the most popular in Silicon Valley?

ELECTRONICS:

1. *Art of Electronics*, 2nd ed. by Paul Horowitz and Winfield Hill. Cambridge University Press, 1989. ***$49.50.***
2. *SPICE: A Guide to Circuit Simulation and Analysis Using PSPICE* by Paul Tuinega. Prentice-Hall, 1988. ***$20.60***
3. *Noise Reduction Techniques in Electronic Systems*, 2nd ed. by Henry W. Ott. Wiley, 1988. ***$47.95.***
4. *Radargrammetric Image Processing* by Franz W. Leberl, Artec House, 1990. ***$88.***
5. *Vacuum Technology*, 3rd ed., by A. Roth. Elsevier, 1990. ***$95.***

COMPUTER SCIENCE:

1. *Object-oriented Design with Applications* by Grady Booch. Addison Wesley, 1990. ***$37.25.***
2. *Compiler Design in C* by Allen D. Holub. Prentice-Hall, 1990. ***$56.20.***
3. *Object-oriented Analysis*, 2nd ed., Peter Coad and Edward Yourdon. Prentice-Hall, 1990. ***$31.***
4. *Computer Architecture: A Quantitative Approach* by John Hennessy and David Patterson. Morgan Kaufman, 1990. ***$54.95.***
5. *Wicked Problems, Righteous Solutions: A Catalogue of Modern Software Engineering Paradigms* by Peter DeGrace and Leslie Hulet Stahl. Prentice-Hall, 1990.***$30.***
5. *Tex for the Impatient* by Paul Abraham. Addison-Wesley, 1990. ***$25.50.***

Compiled for *Electronic Design* by Stacey's Bookstore, Palo Alto, Calif; (415) 326-0681.

KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458

Once a product-development team has prepared a product definition, complete with estimates, the temptation is to begin development without a planning phase. Often, managers and key advisers, acting with the best of intentions, draft what they think is a reasonable top-down schedule and commit themselves and the development team to this rough, no-depth, plan. When this happens, the project's execution phase is mostly out of control. Only top-level scheduling information exists on the project. In effect, the project/program has milestones specified during its execution phase.

However, these milestones have been placed by guess and opportunistic thinking rather than by reason, logic, and cross-functional participation. With a plan of this type, progress can't be tracked and measured daily or weekly. Measuring performance at a group or individual level is out of the question. Time can be measured only at a milestone. Should milestone slip occur and it likely will, there is nowhere to turn to determine the cause of the problem other than to rely on the judgment of project participants.

Plans of this type are often revised at the top level. Of course, the revision's direction will lengthen the project and affect the product's time to market.

Many project/program managers find it easy to delay early milestones while keeping the product's introduction date fixed. I did this and most people involved in new product development have some experience with the phenomenon. At the time of a milestone slip, you can convince yourself that circumstances were unusual and that it's surely to get better between now and the next milestone. Somehow you figure out how you are going to regain lost ground without spending more money or adding more resources.

Besides creating a false sense of security for yourself, you'll probably come up with an argument so convincing that the management and development teams within your organization will go along with the flow. Nothing new will really have happened until you begin to approach the next major milestone and it too begins to slip.

Then, you'll develop a new superficial plan. This time around, slip and delay become a big issue. You'll have to move the product's introduction date. But to keep it from moving too far, money and staff need to be added.

With each tick of the clock, the project grows in complexity and starts to consume more of your precious resources. And, even with all this bad news, there is more bad news—time to market continues to elongate. Does any of this sound familiar?

In the next column, I'll start to look at ways to develop meaningful plans to steer clear of the obstacles just presented.

QUICKLOOK

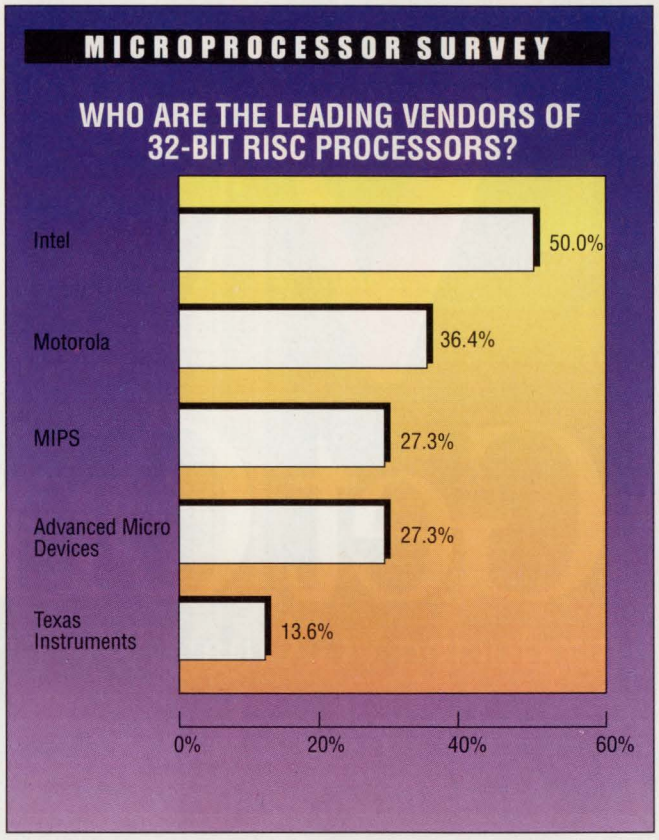
OFFERS YOU CAN'T REFUSE

Pairing a college textbook with related design software should speed up the learning curve. For engineers just getting started designing with programmable logic devices, PLDesigner Student Version from Minc Inc. teams up with *Modern Digital Design* by Richard Sandige (McGraw-Hill). The 700-page text covers basic and advanced logic design, including combinatorial and sequential logic design.

With the software, students can try out design examples from the text or other designs. Then they can implement a design in various solutions with a commercial version of Minc's PLDesigner, available in the university's design library. The Colorado Springs company offers a 40% discount if the design tools are used in a teaching environment. As a result, a student builds a circuit and proves out the design. For more information contact Karen Jackson, (212) 512-4179.

Along similar lines, Accel Technologies offers five educational versions of its DOS-based Tango design software. The Tango/e educational products differ from the professional counterparts by design size, library size, and output limitations. Each of the five programs is $100, about one-seventh of the retail price for the commercial software.

The programs are the Tango-Schematic/e schematic capture tool; Tango-PLD/e, a PLD design program; Tango-PCB PLUS/e, a pc-board layout tool; the Tango-Route PLUS/e autorouter; and the Susie Digilab II logic simulator. For further information, contact Accel, 6825 Flanders Dr., San Diego, CA 92121; (619) 554-1000; fax (619) 554-1019.



TIPS ON INVESTING

The biggest investment for engineers used to be buying a home. Today, the family home has a competitor: educating the kids. As higher education costs continue to outpace the nation's overall inflation rate, more engineers are wondering where the money's going to come from. To put this in perspective, let's say that Junior's freshman year at state U. costs $6,000. His freshman year, 18 years from now, is expected to cost $25,894.

Money for education usually comes from three sources:

- Cash flow. With this method, tuition bills are paid out of current income as a child attends school.
- Lump sum funding. Parents set aside money when children are small, then withdraw funds as children enter college.
- Student loans and grants. Loans for higher education are still available to many families, though the government is setting tougher income restrictions. Too, students with good grades may qualify for private scholarships and grants. Applying early and often is key.

An engineer should first get an idea of the amount of money to set aside. Will his children attend an Ivy League-caliber school, where costs are running at just over $20,000 per year or a state college? Next, consider a child's age, tax considerations, and risk tolerance—which is the most important. In general, the younger the child, the more growth- oriented investments should be. As the child approaches college age, safety and liquidity become more important. A caveat: This rule of thumb works only for people who are comfortable with a degree of risk. If you're the type who stays up nights worrying about your investments, stick to safe vehicles.

Various investment products are appropriate for education funds. If you favor a conservative approach, consider CDs, zero-coupon, government, and municipal bonds. More aggressive investors might place their education assets in corporate bonds, growth stocks, or mutual funds. Your financial consultant can help you review the options.

Despite changes to the tax law, there are still benefits to have investment income taxed at your child's rate. For a child under age 14, the first $500 is received tax-free because of the standard deduction. The next $500 is taxed at the child's rate (usually 15%), and amounts over $1,000 are taxed at the parent's rate. At age 14, all unearned income is taxable at the child's rate.

Should you transfer assets into your child's name? The answer depends on several things, including your tax bracket. Before you decide, consult your tax adviser. If you decide to transfer assets, two methods to consider are:

- A custodial account. Although it has no inherent tax advantages, placing assets in the child's name may permit unearned income to be taxed at a lower rate. The disadvantage: The transfer is irrevocable. And when the child attains majority (between 18 and 21, depending on state law), he or she gains full control of the assets. That means you have no guarantee that the money will be spent on college.
- Creating a trust. Trusts allow more flexibility regarding investment and asset control. A potential drawback is the often expensive attorney's few for setting up and maintaining trusts.

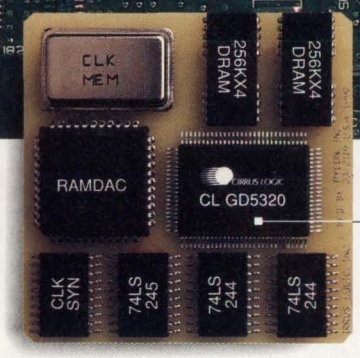
Whatever decisions you make, when it comes to educational funding, there's no replacement for early planning. Start saving today.

by Henry Wiesel, a financial consultant with Shearson Lehman Bros. Inc., 1040 Broad St., Shrewsbury, NJ 07702; (800) 221-0073. Wiesel invites questions and comments.

VGA

Get On Board.

Introducing VGA that fits your motherboard and your budget.



To put VGA graphics on your motherboard, you need a cost-efficient, highly integrated, powerful solution that uses minimal board space. You need the new CL-GD5320 Enhanced VGA-Compatible Graphics Chip from Cirrus Logic.

Use it to incorporate full 16-bit or 8-bit VGA into low-cost personal computers. You only need two industry standard 256K x 4 DRAMs and as few as five other ICs. Whatever memory speed you select — 80ns, 100ns, or 120ns — you'll get a complete VGA display system with greater performance than systems using a more expensive solution with 64K x 4 DRAMs.

You don't sacrifice features. You get 16-bit and 8-bit support for the VGA graphics standard, and full, register-level backwards compatibility. For maximum performance, it has an 8/16-bit CPU interface, independent video and DRAM clocks, internal FIFOs, and page mode DRAM access. And it will interface to both analog (PS/2 and multi-sync) and TTL monitors.

You can also pick a ready-to-use solution that's right for you. Anything from a chip with full BIOS, drivers, utilities, user's manual, and documentation — to a complete manufacturing kit including everything you need to quickly move into high-volume production.

Make your PC more competitive and save time, space, and money. Call Cirrus Logic today.

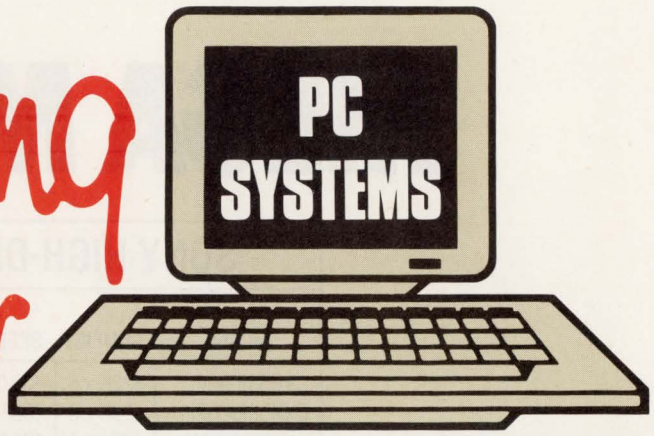
Get on board. Call today for more information on our motherboard VGA solutions.
Call 1-800-952-6300. Ask for dept. LM32.

This full 16-bit CL-GD5320 lets you implement 16-bit or 8-bit VGA capabilities on your motherboard with as few as 5 other chips and two 256K x 4 DRAMs. Get a complete solution that saves time, space, power, and expense. You still get all the speed, features and flexibility you're looking for.

CIRRUS LOGIC

CLOSING THE GAP

Designing For PC SYSTEMS



This is the first installment of a new section in Electronic Design focusing on the design of PC systems. The section, which will appear regularly throughout 1991, will comprise three parts: a newsletter with reports on late-breaking developments; a contributed technical article detailing a particular aspect of PC system or subsystem design; and a series of write-ups on recent products aimed at PCs.

Apple Desktop Bus Powers New Peripherals

THE SMALL CURRENT that can be supplied over the Apple Macintosh desktop bus (ADB) can, with careful design, supply power to a peripheral device. This saves an internal card slot or the "modem" serial port—a major benefit on the limited-expansion Macintosh systems. One of the first peripherals to use the ADB, a facsimile and modem combo, was developed by Global Village Communication Inc., Menlo Park, Calif. The TelePort/Fax modem is about 3-by-5-by-1 in. and includes MNP level-5 data compression for error-free data communications at up to 4800 baud. The data-modem mode has automatic baud-rate selection and is Hayes compatible. The transmission-only fax mode sends images at 4800 baud. Contact Leonard Lehmann, (415) 329-0700. CIRCLE 530

Graphics Chips Go Beyond VGA Standard

WITH HARDWARE ACceleration for many graphics operations, a three-chip set delivers 10 to 20 times the throughput of the VGA controller while delivering the 1024-by-768-pixel resolution of the 8514/A standard. Developed by IBM Corp., White Plains, N.Y., the extended graphics array (XGA) chip set has all the architectural features needed for a 4k-by-4k pixel image. However, initially, the chips will support the 1024-by-768-pixel interlaced 8514/A images with 256 colors, or VGA resolution (640 by 480) with 65k colors.

To achieve higher performance, the new controller chip employs a custom RISC-based core processor and uses on-chip hardware to accelerate many graphics operations. The trio's second chip handles the interface to the Micro Channel bus, making it possible for the controller to be a full 32-bit bus master. The third chip is a new palette digital-to-analog converter that supports VGA modes with 256 or 65k colors, or 8514/A modes with 16 or 256 colors. Software already written for the 8514/A application interface (AI) will run directly on the XGA chip set. That AI will provide a migration path for software currently being written for the 8514/A AI. The XGA hardware, though, isn't register-compatible with the 8514/A register set, and software written directly to the 8514/A registers will have to be redone.

The unanswered question about XGA is whether others will try to clone the chips, as was done with VGA and as a few did with 8514/A. With some VGA chip makers already including hardware cursor support or bitBLT operations, many feel that XGA offers too little, too late. However, the XGA chip set, with some 50,000 gates, does excel in applications that require multitasking.

IBM has published a technical specification, "The XGA Video Subsystem User Guide," which can be purchased from IBM's major U.S. field sales offices. And, because IBM is a member of the Video Electronics Standards Association (VESA), copies should also be available from VESA, 1330 South Bascom Ave., Suite D, San Jose, Calif. 95128-4502; (408) 971-7525.

Standards For Multimedia On PCs Released

A DEFINITION OF THE multimedia environment for the PC platform has been developed by Microsoft Corp., Redmond, Wash., with IBM Corp., White Plains, N.Y., and Tandy Corp., Ft. Worth, Texas. The software environment includes Windows 3.0 plus extensions to both Windows and IBM's OS/2. The extensions include device drivers and libraries that link applications and the hardware. The multimedia definition includes specifications for common data file formats and applications-programming interfaces to control media devices, and defines a minimum system configuration—a fast CPU (a 10-MHz or faster 80286 or 80386), 2 Mbytes of RAM, standard or enhanced VGA, a digital-audio subsystem, a minimum of 30 Mbytes of hard-disk storage, and a CD-ROM drive. To help create multimedia applications, Microsoft offers a developer's kit and Tandy has assembled specially configured systems for developers. Contact Microsoft at (206) 936-4877; Tandy at (817) 390-3549. CIRCLE 532

MEGA MEMORY.

SONY HIGH-DENSITY SRAMS				
MODEL	CONFIG.	SPEED (ns)	PACKAGING	DATA RETENTION
CXK581000P*	128K x 8	100/120	DIP 600 mil	L, LL
CXK581000M*	128K x 8	100/120	SOP 525 mil	L, LL
CXK581100TM*	128K x 8	100/120	TSOP	L, LL
CXK581100YM*	128K x 8	100/120	TSOP (reverse)	L, LL
CXK581001P	128K x 8	70/85	DIP 600 mil	L
CXK581001M	128K x 8	70/85	SOP 525 mil	L
CXK581020SP	128K x 8	35/45/55	SDIP 400 mil	
CXK581020J	128K x 8	35/45/55	SOJ 400 mil	

*Extended temperature range available.

L = Low power.
LL = Low, low power.

MEGA COMMITMENT.

As you can see, Sony's more committed than ever to meeting your high-density SRAM needs.

Just consider the enhancements we've made in a few short months: TSOP and TSOP-reverse packaging. Low data retention current. And extended temperature range.

All based on our unique 0.8-micron CMOS technology, and available in 32-pin DIP and surface-mount plastic packages.

Then consider our ever-increasing production capabilities. We've just added yet another SRAM facility in Japan. And acquired a large AMD facility in San Antonio, Texas.

So you can really count on us in a crunch.

Need more proof we're serious about your each and every SRAM need?

Call us. We've got more breakthroughs on the way. Well over 100 SRAM products spanning the performance spectrum. And the desire to meet—or exceed—your toughest performance spec.

Sony high-density SRAMS are shipping now, complete with competitive pricing. So call (714) 229-4190 today. Or write Sony Corporation Of America, Component Products Company, 10833 Valley View St., Cypress, CA 90630, Attention: Semiconductor sales. FAX (714) 229-4285.

SONY®

CIRCLE 174

Designing For PC SYSTEMS

Boost PC's Floating-Point Speed With An Add-On DSP Coprocessor Board

With A 96002-Based Coprocessor, IEEE-compatible Floating-point Math Runs At Supercomputer Speeds.

BY ZVI ROZENSHEIN

Motorola Semiconductor Israel Ltd., 147 Bialik St., Ramat-Gan, 52523 Israel; 972-3-7538-275.

There's a lot of attention being paid to floating-point math for analysis programs that run on personal computers. This type of math offers added precision over integer calculations. Unfortunately, though, math coprocessor chips offered by microprocessor suppliers and several other vendors are limited to just a few MFLOPs, which becomes a bottleneck to system throughput.

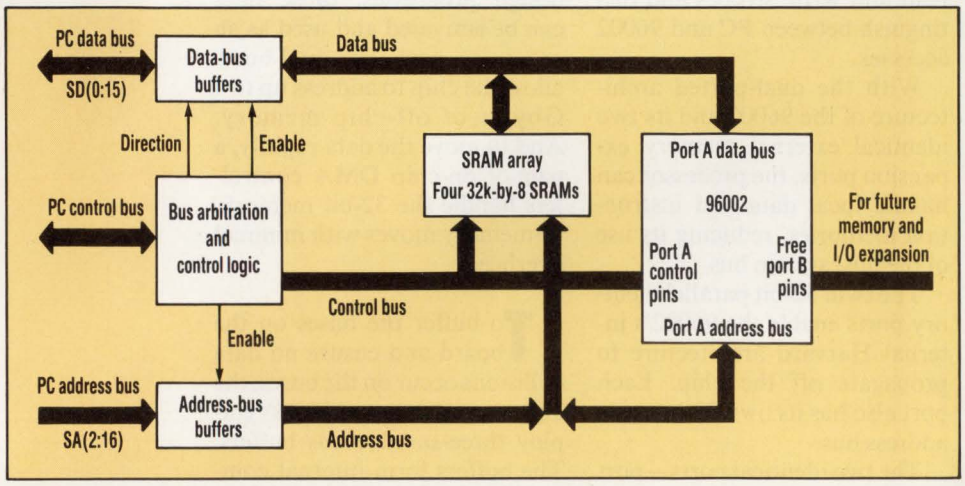
One solution to this problem is an accelerator card—based on Motorola's recently released 96002 media engine—that is easily built for the IBM PC/AT industry-standard architecture (ISA) bus. When running with a 40-MHz clock, the media engine can execute 60 MFLOPS (20 million floating-point additions, subtractions, and multiplications; and 20 million instructions/s). With an accelerator card in the system, numeric tasks that require extensive IEEE-compatible (both IEEE 754 single precision and single-extended precision) floating-point calculations can be transferred to the 96002 by the host system. Then the results can then be transferred back to the host processor.

To evaluate the performance-enhancement factor achieved by using a 96002 as an attached processor, a Fractal program, based on one of Dr. Benoit Mandelbrot's functions, was written. It was first written in C and run on an 8-MHz IBM PC/AT. It took the PC about 4 hours to finish calculating and drawing the picture. The same example was run on an IBM PC/AT (80386 + 80387) running at 20 MHz. That combination created that image in about 4.8 minutes. Lastly, the same equation was implemented in the 96002's assembler and run at a 40- MHz clock speed, transferring the results to the PC's video memory. Just 6 seconds were needed by the coprocessor board to do the computations—a 48-fold improvement over the 80386 and floating-point 80387 coprocessor combination.

When building a board with the 96002, there should be a sufficiently large local memory, say, 128 kbytes of RAM to hold the incoming data and the outgoing results. Furthermore, the 96002 can appear as a host processor to the PC's CPU—the 80286 in the case of a PC/AT, or any 80386/486 processor. Four main sub-blocks of control logic must be implemented to make the coprocessor card practical—the CPU, Memory, Data and Address Bus Logic, and Arbitration Logic *(Fig. 1)*. Tying the board into the ISA bus also requires a little familiarity with the ISA signals, which are reasonably well defined in many documents (ELECTRONIC DESIGN, *Oct. 11, 1990, p. 86)*.

The heart of the board is the CPU block, which contains the 96002, the 40-MHz clock generator, and some additional logic to generate the RESET signal. The RESET signal is needed by the 96002 during power-up, when the on-chip emulator (OnCE) is activated, or when a program requests a signal to be generated. The extra logic also generates the mode signals required by the 96002 for configuration during power-up. In addition, external interrupt requests are handled through the same logic block.

A quartet of 32-kword-by-8-bit static RAM chips form the



1. With the high integration level of Motorola's 96002 media engine, a coprocessor card can be assembled with a small amount of support logic and a bank of four 32-kword-by-8-bit static RAMs.

TABLE 1. IMPORTANT 96002 CONTROL SIGNALS

$\overline{\text{RESET}}$	Assertion of this signal places the 96002 in the reset state.
MODA/$\overline{\text{IRQA}}$	Mode Select A/External Interrupt Request A. This signal selects the initial 96002 operating mode during hardware reset and becomes a maskable interrupt request input during normal instruction processing.
MODB/$\overline{\text{IRQB}}$	Mode Select B/External Interrupt Request B. This signal selects the initial 96002 operating mode during hardware reset and becomes a maskable interrupt request input during normal instruction processing.
MODC/$\overline{\text{IRQC}}$	Mode Select C/External Interrupt Request C. This signal selects the initial 96002 operating mode during hardware reset and becomes a maskable interrupt request input during normal instruction processing.
$\overline{\text{DR}}$	Debug Request. This input provides a means of entering the debug mode of operation from the external command converter.
DSCK/OS1	Debug Serial Input/Chip Status 1. When this pin is configured as an input, it provides serial clock to the OnCE. When an output, this pin provides chip status information.
DSI/OS0	Debug Serial Input/Chip Status 0. This pin can be configured as an input through which serial data or commands are provided to the OnCE. When an output, this pin provides information about the chip status.
DSO	Debug Serial Output. This pin provides the data contained in the OnCE registers to the external command converter.
aA(0:31)	These signals are the 32 port A address lines.
aD(0:31)	These signals are the 32 port A data lines.
aR/$\overline{\text{W}}$	Read/$\overline{\text{Write}}$ for port A. This signal is high for the read cycle and low for the write cycle.
a$\overline{\text{TS}}$	Transfer Strobe for port A. This signal is asserted to indicate that the port A address and control lines are stable and that a bus read or write is taking place.
a$\overline{\text{HS}}$	Host Select input for port A. This signal is asserted to enable selection of the Host Interface functions.
a$\overline{\text{HA}}$	Host Acknowledge for port A. This signal is used to acknowledge a request to the Host Interface.
a$\overline{\text{BG}}$	Bus Grant input for port A. This signal is asserted by an external bus arbiter when the 96002 may become the next bus master.
a$\overline{\text{BA}}$	Bus Acknowledge output for port A. This signal is asserted when the 96002 has taken the bus and is the bus master.

32-bit-wide array in the memory sub-block. The block also contains the control circuits that provide the memory array with read and write strobes and distinguish between PC and 96002 accesses.

With the dual-ported architecture of the 96002 and its two identical external memory expansion ports, the processor can handle local data and instruction memories, reducing its use of the host system bus.

The twin 32-bit parallel memory ports enable the 96002's internal Harvard architecture to propagate off the chip. Each port also has its own 32-bit wide address bus.

The two identical ports—port A and port B—will be used. Port A will serve as the host interface, while port B will initially be left in the non-active state. As the design progresses, those lines can be activated and used as an expansion port. The dual buses allow the chip to address up to 4 Gbytes of off-chip memory. And to move the data rapidly, a pair of on-chip DMA controllers handle the 32-bit memory-to-memory moves with minimal overhead.

To buffer the buses on the board and ensure no data collisions occur on the buses, the address and data sub-blocks employ three-statable bus buffers. The buffers form internal common data buses and address buses that are shared between the 96002 and PC.

Built-in hardware improves such key operations as nested Do Loops.

Each buffer is activated when the PC accesses the memory array or the 96002's host port. The direction of the data-bus buffers is determined by whether the access is a read or a write. When the 96002 is the master of this internal bus, the bus buffers are three-stated.

The fourth sub-block contains the logic that generates all control signals required to maintain a bus-sharing mechanism. That allows either the 96002 or the PC access to the board's internal common-bus resources (memory and host port). This logic also generates the 96002's a$\overline{\text{BG}}$, which tells the 96002 when it can be the bus master; and the PC's IO_CH_RDY, which tells the PC to lengthen its bus cycle until the 96002 releases the bus.

With the four basic sections of the board loosely defined, let's zero in on each section for a more detailed view of what's really needed. For starters, to build the CPU block, some of the resources already included on the processor should be reviewed.

A number of on-chip features help simplify the design of a coprocessor card because less off-chip circuitry will be required. Some of those resources include a pair of independent 512-word by 32-bit data RAMs, two independent 1024-by-32 data ROMs, a 1024-by-32 program RAM, and a small, 64-by-32 bootstrap ROM.

Low overheads, thanks to built-in hardware, improve such key operations as nested Do Loops and reduce the time for the processor to return from interrupts. Furthermore, the chip's highly parallel instruction set has unique DSP addressing modes and dual 32-bit parallel host microprocessor/DMA slave interfaces that give the chip one of the best throughput's available.

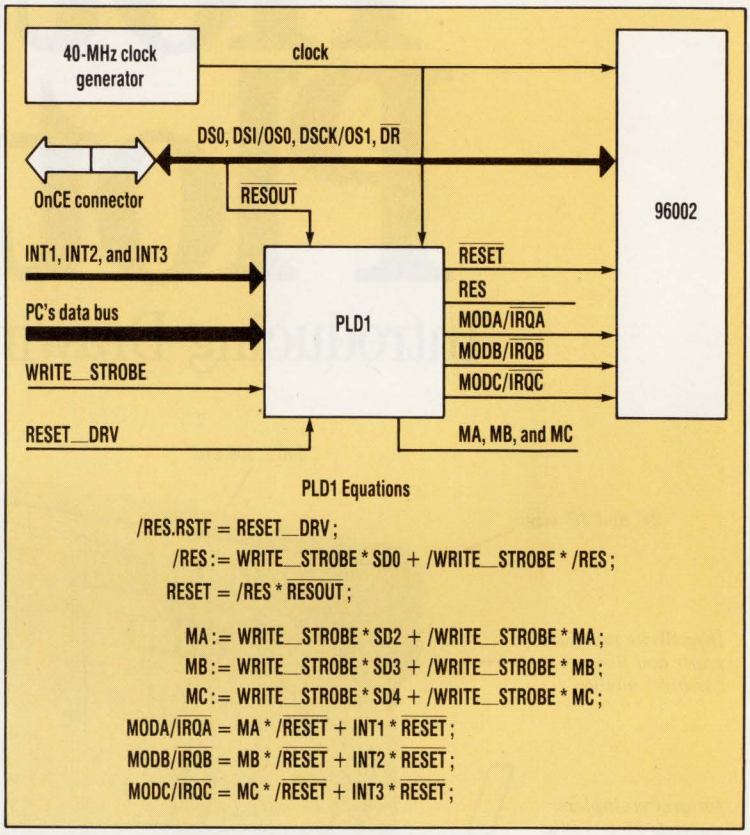
To use the processor, the chip's Port A data and address buses along with a number of control signals must, of course, be tied to the various sub-blocks and to the host system's ISA bus. The control signals of the 96002 that must be used consist of the RESET line as well as the three Mode Select/Interrupt Request lines, the Read/Write strobe, Transfer strobe, Bus Grant and Acknowledge, Host Select and Acknowledge, and the Debug Request signal, along with the related OnCE port signals *(Table 1)*.

In the CPU section, a separate connector gives an external command converter access to the 96002's OnCE port. With this facility, users can then debug the chip's software and onboard hardware.

The connector brings out the Debug Serial Input (DSI), Debug Serial Output (DSO), Debug Serial Clock (DSCK), and Debug Request (DR) which control the OnCE port, and Reset Output (RESOUT), which can assert RESET on the 96002. The RESET signal drives the 96002's RESET pin and can be asserted by one of three sources:

- The RESET_DRV signal, which indicates a power-up sequence in the PC.
- The RESOUT signal, which is generated by the external command converter.
- A write operation from the PC to a PLD that serves as an output port for the PC.

Each is fed into a programmable logic device (PLD1) that determines the ensuing action *(Fig. 2)*. PLD1 collects the three sources and drives the RESET signal according to the first three equations that are listed in Figure 2.



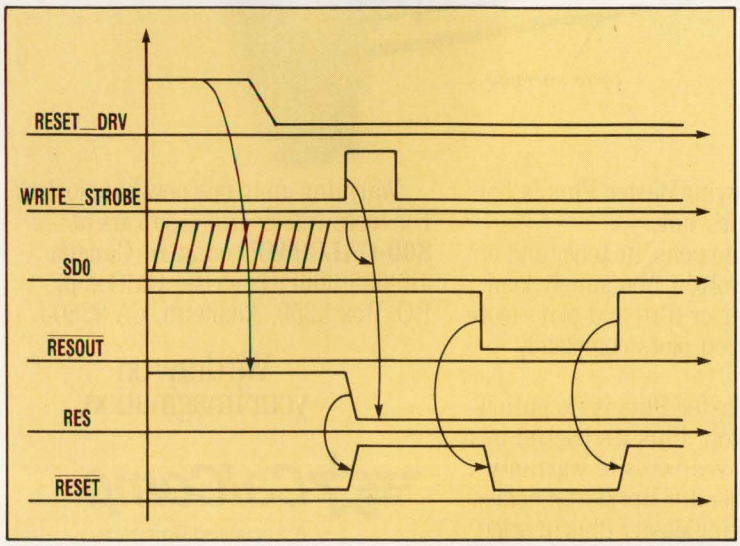
2. By accepting various inputs, the programmable logic chip (PLD1) generates the mode control and reset signals required by the 96002 when the board powers up.

The RES signal is an internal signal generated by the PLD, which causes the PLD to appear to the 80286 as a write-only latch. The WRITE_STROBE signal is generated by the control logic on the board and is a result of decoding the PC address and control buses. It's produced when the PC writes to this one-bit output port.

When the PC writes to the port, bit SD0 of the PC's data bus is written to the PLD, changing the RES signal. The RES signal is cleared by the RESET_DRV signal.

That RESET signal is the logical AND between /RES (which indicates a reset request from the PC), and RESOUT (indicating a reset request from the external command converter).

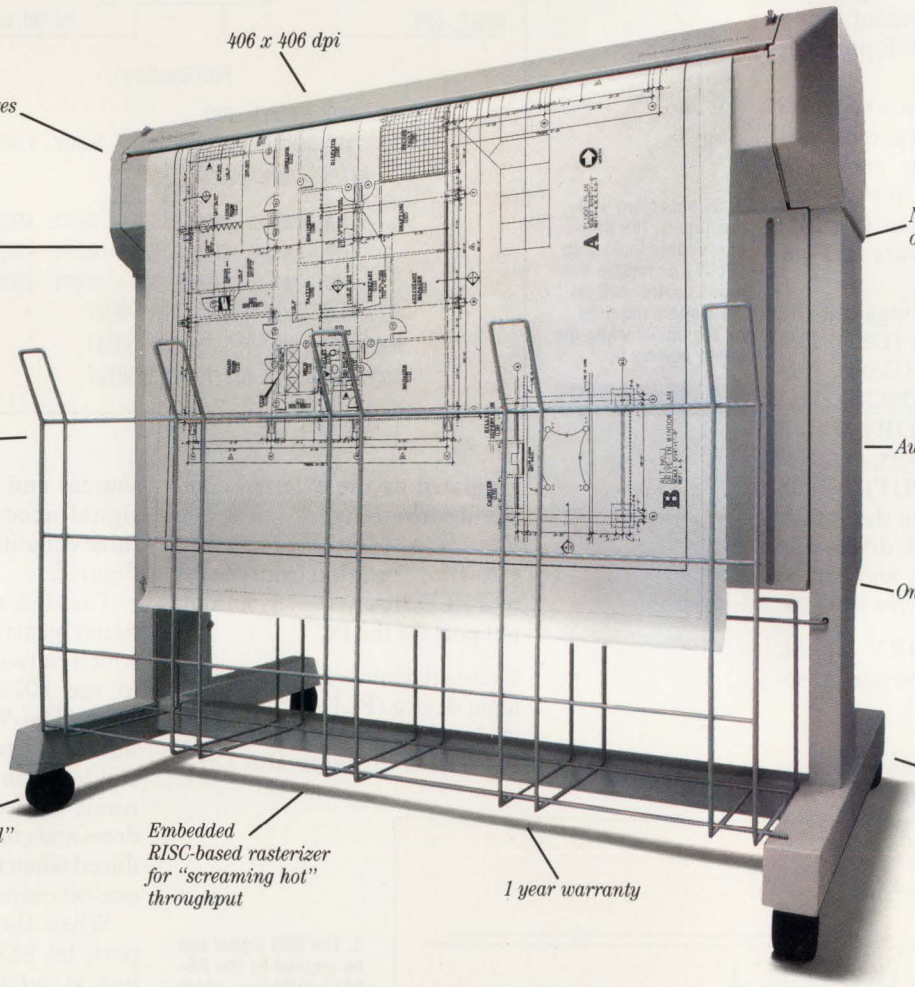
The 96002 has three interrupt inputs that also serve as mode programming inputs when the



3. The RES signal can be cleared by the RESET_DRV line, which goes low to indicate that the PC is going through a power-up sequence. RESET is the logical AND between the active-low state of the RES signal, which indicates a reset request from the PC, and RESOUT, which provides a reset request originating from an external command converter.

Hotter Plotter.

Introducing DrawingMaster Plus



CADALYST MAGAZINE HIGHLY RECOMMENDED 1990

DrawingMaster® Plus is hot to plot.

In fact, it was specifically designed to run with the fastest CAD systems–taking just minutes to do jobs that take pen plotters hours.

And high throughput doesn't mean low resolution. At 406 X 406 dpi, you get exceptionally clean lines that rival laser and electrostatic plotters.

For fast checkplots, select QuikPlot® mode and cut plotting time almost in half.

While DrawingMaster Plus is hot, complicated it's not.

There are no pens, no toner and no chemicals involved. You simply load a roll of paper or film and plot–more than 50 E-sized plots completely unattended.

DrawingMaster Plus is exceptionally reliable too. Plus it's backed by a standard one year on-site warranty.

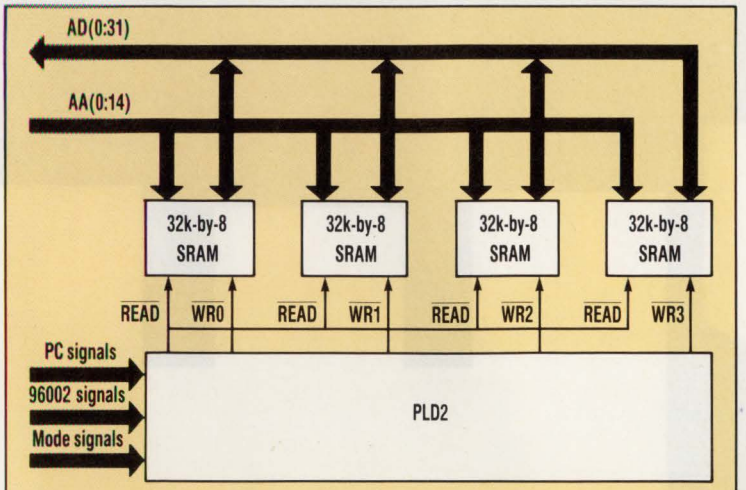
And no other 406 dpi plotter comes close to DrawingMaster Plus in price.

Warming up to our new hot plotter? For more information, call us at **800-CALCOMP** today. In Canada, 416-635-9010. Or write: CalComp, P.O. Box 3250, Anaheim, CA 92803.

We draw on your imagination.™

CalComp
A Lockheed Company

CIRCLE 90



PLD2 Equations

/READ = ADD_EN * /aBA * aR/W * /aTS
+ /ADD_EN * aBA * /OFF_RAM * MEMORY * /LAEN * /SMEMR;

/WR0 = ADD_EN * /aBA * /aR/W * /aTS
+ /ADD_EN * aBA * /OFF_RAM * MEMORY * /LAEN * /SMEMW * /SA1 * /SA0;

/WR1 = ADD_EN * /aBA * /aR/W * /aTS
+ /ADD_EN * aBA * /OFF_RAM * MEMORY * /LAEN * /SMEMW * /SA1 * /SBHE;

/WR2 = ADD_EN * /aBA * /aR/W * /aTS
+ /ADD_EN * aBA * /OFF_RAM * MEMORY * /LAEN * /SMEMW * SA1 * /SA0;

/WR3 = ADD_EN * /aBA * /aR/W * /aTS
+ /ADD_EN * aBA * /OFF_RAM * MEMORY * /LAEN * /SMEMW * SA1 * /SBHE;

4. By using a PLD to implement most of the control logic, the off-chip memory subsystem for the coprocessor can be built with four SRAMs and one PLD. Control signals feeding into the PLD can be grouped into three loose categories: PC signals, 96002 control signals, and mode configuration lines.

RESET line is asserted. The inputs revert back to interrupt inputs after the RESET line is negated.

The PC programs the 96002's operation mode by writing to what it thinks is a three-bit output port. That port is simulated by another section of PLD1 that also generates the RES timing *(Fig. 3)*. The remaining equations in Figure 2 configure that portion of PLD1.

The signals MA, MB, and MC appear as a three-bit output latch to the PC and determine the mode of operation that the 96002 will enter when RESET is negated. The PC's software can change the state of MA, MB, and MC by writing to this output port and asserting the WRITE_STROBE signal. The last three equations describe a simple multiplexer that routes either the MA, MB, or MC signals to the MODA/IRQA, MODB/IRQB, or MODC/IRQC input pins (when RESET is asserted), or the INT1, INT2, and INT3 external signals that serve as external interrupt requests (when RESET is negated).

To allow both the host CPU and the 96002 to read from or write to the memory array, the array must appear to the host processor as either an 8- or 16-bit wide array. The 96002 must appear as a 32-bit wide memory. Four byte-wide 256-kbit SRAMs can be used for the dual-ported memory and another PLD (PLD2) can be used to generate the Read strobe that controls all of the chips and the individual Write strobes (WR0...WR3) that control the write operation to each of the memory chips *(Fig. 4)*.

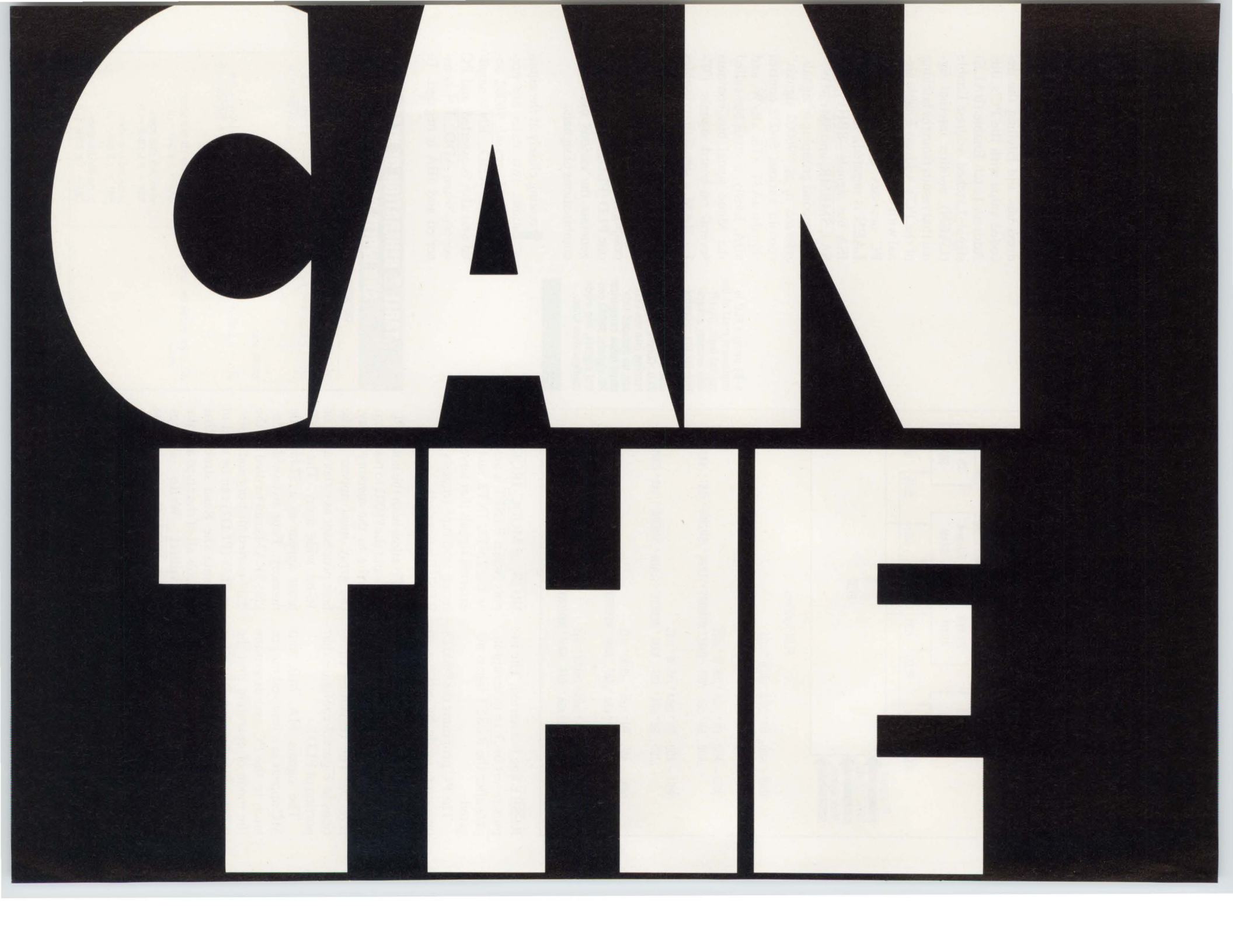
The bus labeled "PC signals" contains various control signals that develop from gating several signals together. Those control signals include: Memory, an internal on-board signal that's the result of decoding the PC's address bus and latching the decoded value with the PC's Bus Address Latch Enable (BALE) signal; Latched Address Enable (LAEN), another internal signal that results from the latching of the PC's Address Enable signal with the BALE signal (valid PC accesses are those when LAEN is negated); and several ISA bus signals—SBHE, SA0, SA1, SMEMR, and SMEMW.

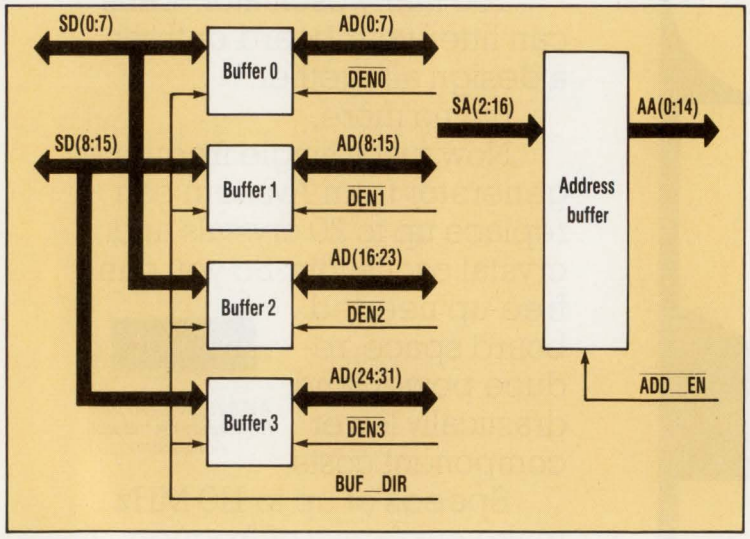
A second grouping of signals, referred to as "96002 signals" contain various 96002 control signals: aA31, aTS, aR/W, and aBA. Lastly, a small bus called the Mode signal bus contains several on-board signals: OFF_RAM, a signal that disables the PC from accessing the RAM array; and ADD_EN, a signal that disables the 96002 from accessing the RAM array. Again, one PLD (PLD2) can be used to generate the various signals or combinations of signals.

Looking closely at the equations, two states are present *(Fig. 4, again)*: 96002 access, when ADD_EN is negated and aBA is asserted; and PC access, when ADD_EN is asserted and aBA is negated. To

TABLE 2. GENERATION OF READ AND WRITE SIGNALS

DSP96002	PC access
READ when:	READ when
aTS = 0 & aR/W = 1;	MEMORY = 1 & LAEN = 0 & OFF_RAM = 0 & SMEMR = 0;
WRITE when:	WRITE when:
aTS = 0 & aR/W = 0;	MEMORY = 1 & LAEN = 0 & OFF_RAM = 0 & SMEMW = 0;
ALL chips receive the same write strobe.	and, to the 1st chip when: SA1 = 0 & SA0 = 0;
	to the 2nd chip when: SA1 = 0 & SBHE = 0;
	to the 3rd chip when: SA1 = 1 & SA0 = 0;
	to the 4th chip when: SA1 = 1 & SBHE = 0;


CAN
THE



5. The address and data buffer section connects the internal common bus to the PC data and address buses. Each slice of the data buffer handles one byte of the 96002's 32-bit data bus.

generate the read and write signals for the memory, several conditions must be met to ensure that each processor properly transfers the right size data *(Table 2)*.

Although the 96002 accesses 32-bit words, the PC can only access 8-bit bytes or 16-bit words. When the PC reads data from memory, all memory chips receive a read signal, although the PC accesses only one or two of the memory chips. However, bus arbitration logic enables only the appropriate data-bus buffers, putting only 8- or 16-bit data on the bus. When the PC writes data to the memory, only the memory chips that should be written receive the write strobe. This prevents data from being written to the wrong memory cells and allowing the PC to pack more than one byte into a 96002 word.

The OFF_RAM signal is used primarily during PC power-up to disable the PC from accessing memory. During PC power-up, the OFF_RAM signal is set by circuitry on the card, preventing PC-DOS from recognizing the memory as part of the system's free memory. The LAEN signal, which also disables the PC from accessing the 96002's external memory, indicates that the PC is performing DMA transfers so the 96002 memory can't be accessed by the PC using it's own DMA capability.

Ensuring the data is properly routed and buffered, the address and data buffer sub-block connects the PC data and address buses to the internal common bus *(Fig. 5)*. Because the PC's data bus is 16 bits wide and the 96002's internal bus is 32 bits wide, multiplexers let the PC transfer data onto either the low portion (bits 0-15) or the high portion (bits 16-31) of the 96002's data bus in any one access.

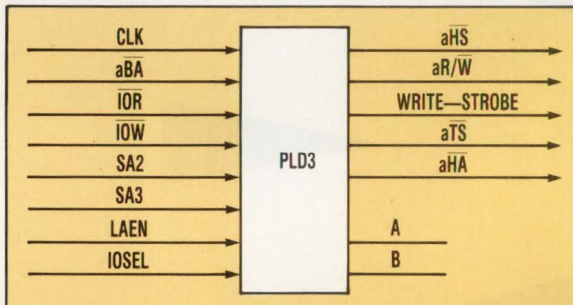
If the PC transfers data on its byte-wide bus, it can put the low byte (bits SD0-7) or the high byte (bits SD8-15) of its 16-bit word on the data bus. Therefore, the data-bus buffer is organized as four slices, each handling one byte of the 96002's 32-bit data bus. Each slice of the buffer is controlled by a separate enable signal—$\overline{\text{DEN0}}$, $\overline{\text{DEN1}}$, $\overline{\text{DEN2}}$ and $\overline{\text{DEN3}}$.

The BUF_DIR signal controls the buffer's direction, which is determined by the type of operation—read or write. The address-bus buffer drives the 96002's address bus, creating an internal address bus that's shared between the PC and the 96002. The buffer is controlled by the ADD_EN signal. That signal is asserted when the PC wants to access the internal bus resources and the 96002 isn't the bus master. Note that PC addresses SA(2:16) drive the 96002's address lines AA(0:14), while the PC's SA(0:1) addresses are used in the control logic to detect the nature of the PC access.

Some simple bus arbitration logic rounds out the coprocessor board's design to ensure that only one of the two chips controls the ISA bus at any one point in time. The logic must handle several aspects of control—the host interface between the PC and the 96002's host port; decoding the PC's address lines to identify PC accesses; control of the buffers that connect the PC and 96002 buses; and bus arbitration between the PC and the 96002 buses.

Once again, programmable logic can easily handle the design of the bus buffer and arbitration logic. PLD3, which is the first of a few PLDs for the arbitration block, generates some

6. Building the host interface that generates the control signals for the 96002 requires one PLD. That PLD controls the A port of the 96002 and supplies most of the 96002's control signals.



PLD3 Equations

aR/W.TRST = aBA;

a/TS.TRST = aBA;

aHA.TRST = aBA;

WRITE—STROBE = /LAEN * IOSEL * /SIOW * SA3 * /SA2;

/aHS = aBA * (/SIOR + /SIOW) * /SA3 * /SA2 * /LAEN * IOSEL;

aR/W = /SIOR * /LAEN * IOSEL;

/aHA = aBA * (/SIOR + /SIOW) * /SA3 * SA2 * IOSEL * /LAEN;

A := aBA * (/SIOR + /SIOW) * /SA3 * /SA2 * IOSEL * /LAEN;

B := A;

/aTS = aBA * (/SIOR + /SIOW) * /SA3 * /SA2 * B * IOSEL * /LAEN;

control signals for the 96002 when the PC is accessing the 96002 host port *(Fig. 6)*. The WRITE_STROBE signal is also generated by PLD3 when the PC accesses some output ports, like the previously described 3-bit port used to program the mode bits. The CLK signal is the same timing signal used by the 96002. The equations required to configure the PLD are relatively simple.

The first three equations indicate that aR/$\overline{W}$, a$\overline{TS}$, and a$\overline{HA}$ are three-stated when the a$\overline{BA}$ is asserted. This happens if the 96002 is the bus master and it generates those signals. The IOSEL signal, which is an input to the PLD, is generated in another section of the control logic, and is a product of decoding the PC's address bus. It is generated when the PC is accessing addresses in the $F100 - $F1EF range. In this address range, the PC has the following I/O ports on board:

SA3=1 and SA2=0: generating WRITE_STROBE for some output ports in the card.

S$\overline{A3}$=0 and S$\overline{A2}$=0: generating a$\overline{HS}$ and a$\overline{TS}$ when selecting the 96002's host port.

S$\overline{A3}$=0 and SA2=1: generating a$\overline{HA}$ when selecting the 96002's host port.

Signals A and $\overline{B}$ delay the generation of a$\overline{TS}$ to satisfy the 96002's timing requirements.

Another PLD (PLD4) handles the address decoding for the coprocessor card *(Fig. 7)*. It decodes the addresses coming from the PC for some of the common bus resources, such as one of the memory locations or the 96002's host port. The PLD generates two signals—Memory Selection (MEMSEL) and I/O Selection (IOSEL)—and has just two simple equations for configuration.

As previously mentioned, the PC can access I/O addresses $F100 - $F1EF and has a permitted memory-access range of $80000 - $9FFFF, which is a total of 128 kbytes. The signals MEMSEL and AEN are latched by BALE, which make it possible to generate the Memory signal used by the SRAM array.

Controlling the data-bus buffers, another PLD (PLD5) distributes the $\overline{DEN0}$...$\overline{DEN3}$ signals that enable the buffers when the PC accesses the internal common bus and the 96002 is no longer the bus master *(Fig. 8)*. The BUF_DIR signal controls the data-bus buffer direction, depending upon the nature of the PC access, such as read or write. The bus controller also

The software developer must write the code for both the PC and the 96002.

TABLE 3. SAMPLE APPLICATION: DATA DOWNLOAD THROUGH COMMON MEMORY:

The 'C' Program

```
#define     READY   0×80000800     /*status handshake word     */
#define     DATA    0×80000820     /*data handshake word       */

main()
{
unsigned far *i,*j;
int n;

i = READY;
j = DATA;

for (n=0;n<0×200;n++)
      /*this loop will transfer 0×200 16-bit words to the 96002's internal
        memory through the boards's common memory.*/
      {
      /*first the PC waits until the 96002 is ready to receive
        a new word by checking the READY word in the common                memory.*/
      while (*i!=0);

      /*now the PC will transfer the data to common memory */
      *j=n;

      /*now the PC signals the 96002 that the transfer is READY */
      *i=0×FFFFFFFF;
      }
}
```

The 96002 Assembler Program

```
                opt         mu,cre,cex,mex
                page        132,66,0,3,1

READY           equ         $200                ; READY handshake word
DATA            equ         $208                ; DATA handshake word

                org         P:0

start           movep       #$00000000,×:$ffffff ; bcra programming for
                                                   0 wait states

                move        #$0000ffff,d2.l     ; set mask
                move        #0,r0               ; init pointer
                move        r0,r7
                move        #READY,r3           ; init pointer
                do          #$100,endloop       ; read 0×100 words from
                                                   the Host
                move        r7,×:(r3)           ; clear READY flag
loop1           jclr        #0,×:(r3),loop1     ; wait until READY is set
                move        ×:DATA,d0.l         ; read Data handshake word
                move        r7,×:(r3)           ; clear READY flag
Loop2           jclr        #0,×:(r3),loop2     ; wait until READY is set
                move        ×:DATA,d1.l         ; read Data handshake word
                asl         #16,d1              ; the 2nd word holds the
                                                   16 MSBits.
                and         d2,d0               ; get only 16 LSBits
                or          d0,d1               ; get the complete word
                move        d1.l,×:(r0)+        ; store in memory
endloop         nop                             ; end of transfer
                nop
                nop
endp            jmp         endp
```

has a simple set of configuration equations.

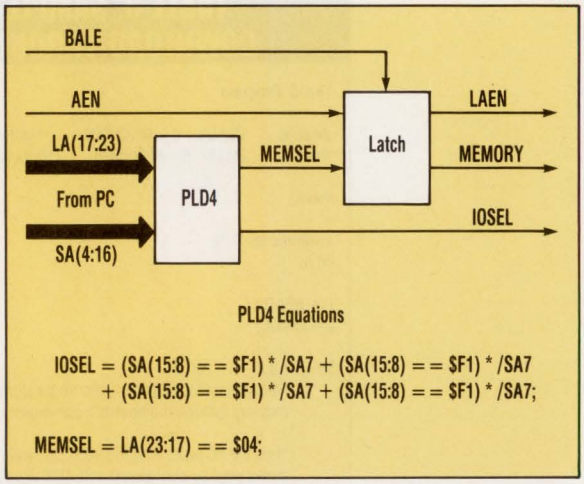
The ACC signal is generated by another section of the control logic, which indicates that the PC is in the middle of an access while the 96002 is no longer the bus master.

The data-bus buffer direction is controlled by BUF_DIR, which is asserted when both SMEMR and SIOR are negated. The PC then executes a write cycle. In this case, the data-bus buffers are directed to route data from the PC to the 96002.

Perhaps the most complex block of logic that must be implemented on the coprocessor card is the bus arbitration circuitry (implemented in PLD6), because it must perform at least a half-dozen functions *(Fig. 9a)*:

- It must assert the ACC signal when the PC executes an access to the common bus while the 96002 is not the bus master
- It has to assert ADD_EN when the PC accesses the common bus and the address bus can be driven by the PC.
- It must pull the MEMCS16 signal low, telling the PC that it accessed a 16-bit-wide memory port.
- It must pull the IOCS16 signal low, telling the PC that it accessed a 16-bit-wide I/O port.
- It has to pull the I/O_CH_RDY signal low when the PC accesses the common bus while the 96002 is still the bus master.
- And, it must assert the aBG signal when the PC doesn't access the common bus, or to negate aBG when the PC tries to access the common bus.

The ISA bus signals MEMCS16, IOCS16, and I/O_CH_RDY are driven by three-state buffers so that other ISA-bus boards can drive these signals if needed. The PLD's clock is an inverted copy of the 96002's clock, which ensures both the setup and hold-time requirements for aBG. These functions are accomplished by the PLD equations *(Fig. 9a, again)*.



7. PLD4 handles the address decoding for the coprocessor card. Two simple equations configure the PLD for generating the MEMSEL and IOSEL signals.

The first equation is a macro (not an output definition) that defines the state when the PC accesses the internal common bus resources. It is true when LAEN is low, indicating a valid address-bus value driven by the 80286. It's also true either when Memory is high—indicating that the PC is accessing the on-board memory—or whenever 'IOSEL*(/SIOR+/SIOW)' is high—indicating that the PC is accessing the on-board I/O space *(Fig. 9b)*.

The ADD_EN signal is used by the address-bus buffers and is asserted when aBA, aBG, and PC_ACC are high. This indicates that the coprocessor card is no longer the bus master and the PC is in the middle of a transfer cycle to the on-board common resources.

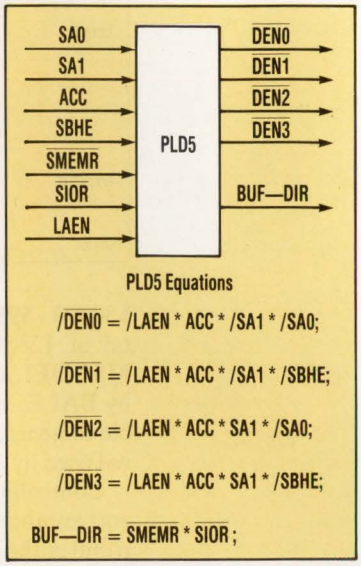
The RDY_TRST signal, when asserted, pulls the ISA bus I/O_CH_RDY pin low, indicating to the PC that the present cycle should be lengthened by extra CPU cycles until the 96002 releases the bus. The signal is high as long as PC_ACC and ADD_EN are both high. During a PC access, when the 96002 releases the bus, the ADD_EN signal will be asserted, causing RDY_TRST to be negated and the PC to end its transfer cycle.

Signals T1 and T2 synchronize the generation of aBG, which is a 96002 input signal that must be synchronized with the 96002's clock input. The purpose of this three-stage shift register (T1, T2, and aBG) is to negate aBG when the PC tries to access the common bus while the 96002 is the bus master. First, the T1 signal goes high if and only if aBG, T1, and T2 are low.

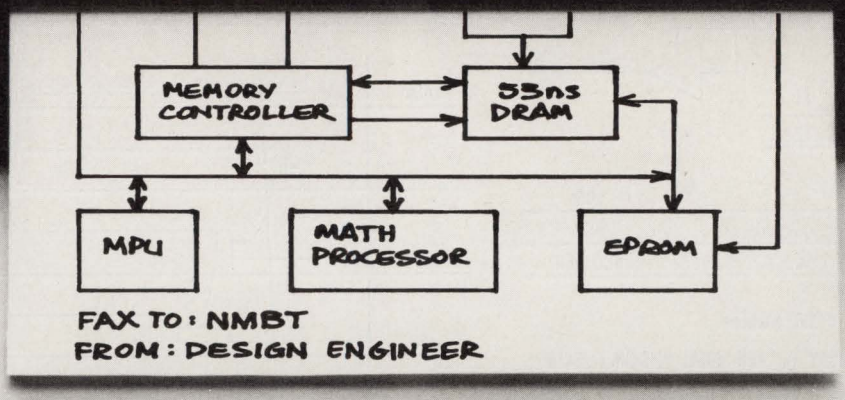
If one of these signals is still high from a previous PC transfer, then T1 will be asserted only when all three stages are cleared. After 2 clocks, aBG will be negated, causing the 96002 to release the bus. Consequently, the PC can gain bus control and accomplish its transfer. Finally, the ACC signal is generated by the same PLD when PC_ACC and ADD_EN are asserted to indicate to other parts of the board's control logic that the PC is in the middle of a board access and it is the bus master.

That basically completes the physical design of the coprocessor card. However, the card won't do anyone any good without some software that loads and unloads the math problems and results for the card. The starting point in any use of a co-

8. Looking like the proverbial black box, PLD5 serves as the buffer controller and provides the four enable signals, one for each of the 8-bit buffer slices and the Buffer Direction control line. Inputs to the PLD are various control lines from the PC's bus that define the nature of the access.



53ns FREE*



Now you don't have to compromise the performance of your 16 MHz and 20 MHz systems. Now you can create **true zero** wait-state 16 MHz and 20 MHz systems. Not close to zero; but **true zero** wait-state designs. Eliminate "patchwork" solutions requiring complex, expensive interleaving, page mode designs, or costly cache schemes.

Upgrade your systems to direct memory access — and get the benefits of higher performance **and** lower cost. The perfect mid-life "kicker" for your current designs; stake out a strong competitive position for new designs.

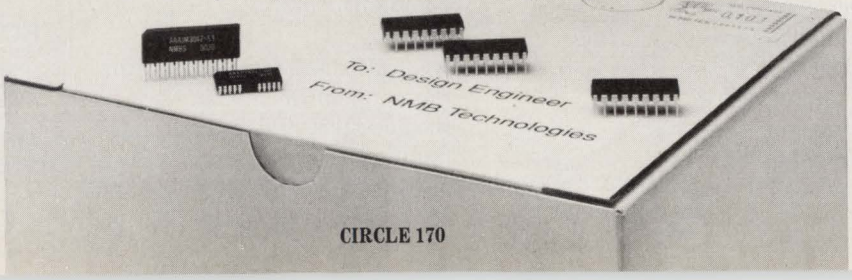
* **See for yourself . . .** We'll send you **Free** samples (up to 1MB) to evaluate in your designs. Just fax us your rough block diagrams for review — we'll be in touch ASAP! Only one qualification: It must be a company funded/scheduled project.

Don't put it off. Your free samples are available now from NMB — the high-speed DRAM specialists. Fax us your design sketches today. Or give us a call at (800) 662-8321 for further information.

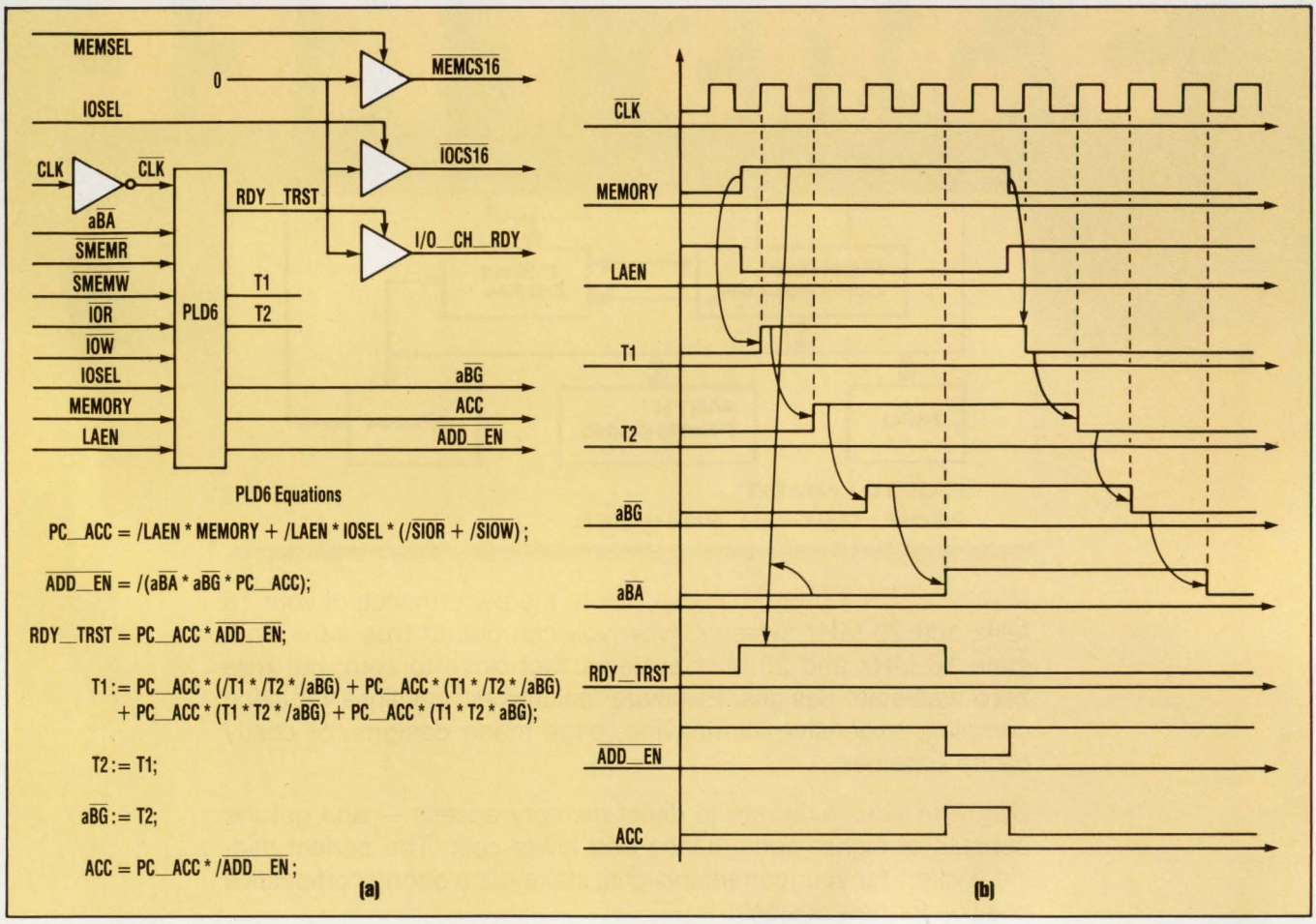
NOW!

NMB || **NMB TECHNOLOGIES INCORPORATED**

NMB TECHNOLOGIES INCORPORATED
9730 Independence Avenue, Chatsworth, CA 91311
Phone: (818) 341-3355 Fax: (818) 341-8207



CIRCLE 170



9. Perhaps the most complex subsection, the bus arbitration logic uses most of the ISA bus' control signals to exert control over the 96002 (a). The bus arbitration uses timing signals T1 and T2 to synchronize the generation of the A port Bus Grant (aBG) signal, an input to the 96002 that must be synchronized with the 96002's clock input (b).

processor is to get it the data that it must process. This can be accomplished with a simple program, written so that it takes advantage of the shared memory by using a portion as semaphore and data registers, even though data will still be transferred into the 96002's on-board data RAM *(Table 3)*.

Before actually building the coprocessor card, a commercially available development board for the 96002 can be used to debug the software. To get the coprocessor to run properly, software must be written for both the 96002 and the PC. One way to set up the software is to use the common memory to pass data as well as messages in both directions. An alternative approach uses the common memory to pass data and the 96002's host port to pass messages in both directions.

A typical software application, which contains the mathematical processing by the 96002 of data given by the PC, follows these steps:

- First, load the 96002's object code into the common memory or into the 96002's internal memory by using the 96002's host port or a direct write to the common memory.
- Next, supply the input data to the common memory by using a direct write to this memory by the PC.
- Supply the message 'go' to the 96002 by using the host port or by using a semaphore in the common memory.
- Check another semaphore in the common memory to see if the 96002 has finished the computation.
- Read the results from the common memory.

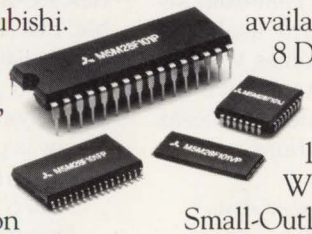
The software developer must write the software that will be run on both the PC and the 96002. Many of the routines for the 96002, though, will be available as part of the software application library being compiled for the 96002.

Zvi Rozenshein, 96002 senior system design engineer for Motorola Semiconductor Israel Ltd., holds a BS in computer and electrical engineering from the Technion, Haifa, Israel Institute for Technology.

Another FLASH Of Brilliance From Mitsubishi.

From the people who brought you ZIP packaging and the first TSOPs, another great idea – Flash EEPROMs from Mitsubishi.

Lower the cost of your system upgrades with Flash EEPROMs' on-board reprogramming. In workstations, office automation equipment and telecommunications systems, our 10K erase/write cycles ensure the reliability of your product.



Mitsubishi Flash EEPROMs are available in 1 Mb, 128K x 8 DIP packages, as fast as 100ns. Flash will also be available in 64K x 16, and higher densities. Watch for TSOP (Thin-Small-Outline-Package), SOP and PLCC versions in the future.

Here's another brilliant idea:

VISION[SM] ACTION REALITY call us now at **1-800-624-8999, ext. 178D** and set your vision into action with Mitsubishi Flash EEPROMs. They can make your new design a reality.

MITSUBISHI
ELECTRONIC DEVICE GROUP

CIRCLE 212

▼ CHIP SET ACCELERATES PC GRAPHICS

Accelerating complex graphics operations in the VGA and 8514A environments by three to ten times, a two-chip set developed by Chips and Technologies functions as a coprocessor inside a PC. The programmable, universal micro accelerator (PUMA) chip set consists of a processor and an interface chip. The processor executes commands from a 64-bit-wide microcode memory. The interface chip connects the processor to the ISA or EISA bus and can serve as a bus master or slave interface.

The 94C2001 processor operates from a 50-MHz clock and can execute several operations in parallel in two to five clock cycles—the time required to complete one microcode instruction. The wide internal microcode word improves overall instruction efficiency. The chip has a four-bus architecture to maximize data transfers between the system and the display. The chip includes a 16-bit ALU and shifter, a 16-word-by-16-bit register file, and a 16-bit hardware multiplier.

With the 94C2002 interface chip, the processor IC can take full advantage of the host system's memory and I/O resources over the ISA or EISA buses. On-chip FIFO buffers enable the interface circuit to work in parallel with the processor. The interface chip's output can also directly drive the engine of a laser printer. Consequently, a graphics subsystem can be built with the PUMA chip set without requiring a frame buffer. The chips can simply communicate over the bus and use the system's standard display adapter. Boards employing the PUMA chip set can be dynamically programmable so that the chips can accelerate different functions. The chips can also be incorporated into a graphics adapter card rather than as a separate card.

Samples of the Puma chip set will be ready in February. The chip set will sell for about $90 in quantities of 10,000. The first microcode software release will offer acceleration for CAD and Windows 3.0 environments.

Chips and Technologies Inc.,
3050 Zanker Road,
San Jose, CA 95134;
Steven Chan,
(408) 434-0600.
▶ **CIRCLE 301**

▼ TOUCH-SCREEN DISPLAY GOES ANYWHERE

The latest electroluminescent technology now appears in a front-panel-mounted touch-screen terminal that can withstand the most demanding industrial environments. The Seal-Touch Terminal ST2400 is small, thin, and resistive to everything except the touch of a finger. Weighing less than 12 lbs. and measuring 10.5 by 11.5 by 3 in., the ST2400 can be mounted almost anywhere using just two bolts. It's cased in rugged cast aluminum, and has no fans or filters. With the touch-screen interface, developers can design menu-driven applications for any user. Display resolution is 640-by-200 pixels. The operating environment can range from 0 to 45°C. The ST2400 is priced at $3750, with large-quantity discounts available.

Digital Electronics Corp.
31047 Genstar Rd.
Hayward, CA 94544
(415) 471-4700
▶ **CIRCLE 302**

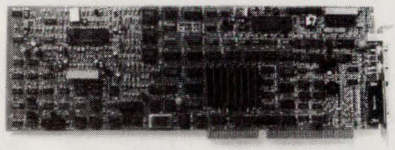
▼ KEEP PCS TUNED TO CORRECT TIME

For just $350, the CTS-10 board keeps your PC precisely tuned to the correct time. The IBM PC/XT/AT compatible plug-in board links the system to station WWV, which transmits the world atomic time standard. The National Institute of Standards and Technology broadcasts the correct time throughout North America, and it gets transmitted on radio. The CTS-10 receives and decodes the digital time information and supplies the time (month, day, hour, minute, second, and tenth of second) directly to the PC clock. Accuracy is within 50 ms. Time-zone selection makes the board usable in any area. The board comes with all the hardware needed to receive the radio signal. It's suitable for process control and communications.

Odetics
1515 South Manchester Ave.
Anaheim, CA 92802
(714) 758-0400
▶ **CIRCLE 303**

▼ LIVE VIDEO APPEARS ON PC DISPLAY

Working with a PC's VGA display card, the Spectrum-XGA video overlay controller places multiple live or frozen full-color video windows on



the system's display. The controller board has a palette of 16.8 million colors. The window size, position, and chroma-key color are completely programmable. Up to 256 windows can display video using 2 Mbytes of memory. Advanced VGA resolutions of up to 1024 by 768 by 8 pixels are possible at a screen update rate of 60 Hz, noninterlaced. The Spectrum-XGA comes with a complete package of development software, including a library of C callable routines, a DOS interactive application program, and a Windows 3.0 dynamic-link library. Available now, the controller board costs $3200.

Redlake Corp.
15005 Concord Cir.
Morgan Hill, CA 95037
(408) 779-6464
▶ **CIRCLE 304**

▼ RUN X-WINDOWS ON A PC

Using PC-Xview, users can run X-Windows on their PCs. PC-Xview is a DOS application that supplies X-Window terminal emulation. With the software and a local-area-network connection, users can access X-Windows applications running on remote X hosts without sacrificing the advantage of local computing power. The system, however, retains access to local peripherals and DOS utilities. PC-Xview runs on IBM-compatible PC/ATs and PS/2s. It only requires 640 kbytes of memory. Users can also get TCP/IP and Network File System (NFS) options. PC-Xview is priced at $449.

Graphic Software Systems
9590 SW Gemini Dr.
Beaverton, OR 97005
(503) 641-2200
▶ **CIRCLE 305**

Pick The Friendly Face For Your Meanest Problem.

Custom configurations by the thousands with standard components.

64 anti-alias channels. Gain, cal, monitor, 1° match.

32 ch.-130 dB/octave. 204.7 kHz, 1° match, gain, cal, monitor.

32 band-pass channels. 80 dB/octave, 25 kHz, gain, cal, monitor.

16 ch.-2 MHz filter/amps. 80 dB/octave, amplitude & phase matched.

28 ch. Gain Ranger® amps. Low noise, 78 dB gain, 200 kHz, MX/DMX, monitor.

Band-pass arrays. DF receivers, towed array, I&Q, 1° & 1% match.

8 super band-pass ch. Programmable F_0 & B. $Q > 10{,}000$.

64 prog. notch filters. 10% BW, 60 dB notch depth, gain, cal, monitor.

Programmable switch matrix. 4x4, 8x8, 16x16, 32x32 plus bank switches.

You get the idea. The friendly face of Precision 6000 helps you have it your way. The density. The extra functions. Easy to change and upgrade later. That's system friendly.

Friendly High Density

- 64 prog. filter amp. channels.
- 32 band-pass channels.
- 64 prog. amp. channels.
- Diff. input, gain, cal, monitor, and other options, of course.
- Zero suppress.

Friendly Performance

- Band-pass with $Q > 10{,}000$.
- 2 MHz prog. filters, 80 dB/octave.
- 204.7 kHz prog. filters, 130 dB/octave.
- Filter match 0.25° and 0.25% typical.

Friendly Functions

- Cal subsystem for go/no-go cal, end-to-end cal, plus diagnostics.
- Group configuration for easy control.
- Up-load and down-load for easy setup.
- System status, other reports.

Friendly Choice

- Prog. filters—HP, LP, BP, notch, anti-alias.
- Prog. amps—pre, post, gain ranging.
- Prog. frequency-band translators.
- Switch matrix.
- Buffered I/O to sense/control other devices.
- Proto-cards for custom circuitry.
- Custom systems from standard proven hardware that's economical and available.
- Buy only what you need now, add and change as needs change.

Meet Us On The New Frontiers Of Precision

Look at our tradition of pushing technology since we began in 1975.

- Slopes from 80 dB/octave to 130 dB.
- Match from 1° and 1% to 0.03° and 0.03%.
- Cutoffs from 100 kHz to 1 MHz to 6.4 MHz.
- Mainframe channels from 16 to 32 to 64.

Call. Fax. Or write. Let us provide details in terms of your requirements.

PRECISION FILTERS, INC.
240 Cherry Street, Ithaca, New York 14850
607-277-3550 Fax: 607-277-4466

CIRCLE 216

▼ MONOCHROME MONITOR SHOWS SUPER VGA

The Model 1405 flat-screen monochrome monitor measures 14 in. diagonally. The nonglare paper-white display is compatible with Super VGA, VGA, and Macintosh II systems. Resolutions supported are 640- or 720-by-350, 720-by-400, 640-by-480, and 800-by-600 pixels. The monitor accepts an analog RGB input signal. The tilt-swivel base display has its controls on the front panel for easy accessibility. The monitor, which costs $299, is available now.

GoldStar Technology Inc.
3003 N. 1st St.
San Jose, CA 95134
(408) 432-1331
▶ CIRCLE 306

▼ REMOVABLE HARD DRIVES ENSURE FILE SECURITY

Improve file security by using the SecureStor removable hard-disk drives. In capacities ranging from 20 to 400 Mbytes, the drives simply slide in and out of their metal housing. They fit in standard 5.25-in. half-height drive slots. The drives feature access times ranging from 40 to 11.5 ms. A second advantage of this type of drive is the transportability of software. Users can take their files with them wherever they go and use them in any computer employing the same controller. And each SecureStor drive comes with a foam-lined, shock-resistant carrying case and all necessary cables. The drives are compatible with almost all standard interfaces, including IBM PC/XT/AT, PS/2, Macintosh, and their compatibles, plus SCSI, ESDI, and Integrated Device Electronics (IDE). The drives range in price from $528 to $2720.

Rotating Memory Services
5090 Robert J. Mathews Pkwy., Suite 2
El Dorado Hills, CA 95630
(916) 939-7500
▶ CIRCLE 307

▼ IMPROVE RESOLUTION OF HP LASERJET

By combining an existing HP LaserJet Series II, III, or similar laser printer with the LaserMaster Series III Professional printer controller, users can get fast, high-resolution output. The board uses 800-by-800 TurboRes, LaserMaster's resolution-enhancement technology. This feature eliminates all jagged edges and poorly formed letters on plain paper. And it can be used in portrait or landscape mode. The board's 2 Mbytes of memory can produce up to 135 different typefaces. The LaserMaster Series III Professional also adds special effects, such as shadowing, rotating, obliquing, squeezing, stretching, and shearing, among others. The board works with any IBM PC/XT/AT, PS/2, or compatible computer. Prices start at $1495.

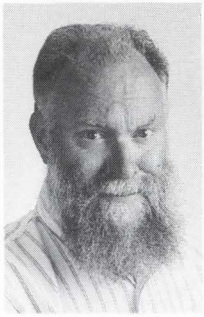
LaserMaster Corp.
7156 Shady Oak Rd.
Eden Prairie, MN 55344
(612) 944-9330
▶ CIRCLE 308

PEASE PORRIDGE

WHAT'S ALL THIS TESTING STUFF, ANYHOW?

The other day, Graham Baskerville, my boss' boss, and I got into a screaming contest. But we weren't in disagreement. We were in complete agreement that there was a problem, and we were thinking of examples to illustrate the problem.

One of the first examples was "The Noise Test." Many years ago, in a quarterly report, a manager glowingly explained that on the model XYZ, the yield loss due to noise had been cut to a trivially negligible level for the last quarter. Graham said that he inquired politely how this was accomplished. After a little investigation, he found that the "yield" was excellent because the test circuit was broken. To restore sanity, he made sure that the noise test now had a lower limit, so if the tester was broken, nothing would pass, and the tester would have to be repaired. Now, that was many years ago, but the general problem of ensuring that your tester makes sense never goes away completely.



BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

I countered with the story of the reference circuit that had a yield problem. The marketing manager wanted to take a big contract for 1% trimmed parts, but the yield wasn't very good for parts with a 1% tolerance. I got some data from the product engineer and studied it. That's strange—the yield for 1% parts was *okay* before trimming the output.

The problem turned out to be a false algorithm. (What *is* an algorithm? Isn't it just a logarithm that got twisted around? When I was a kid, we had lots of logarithms, and I think it's kind of suspicious that you don't see them any more....) And when we went back and corrected the trim scheme, the yield was, of course, quite adequate.

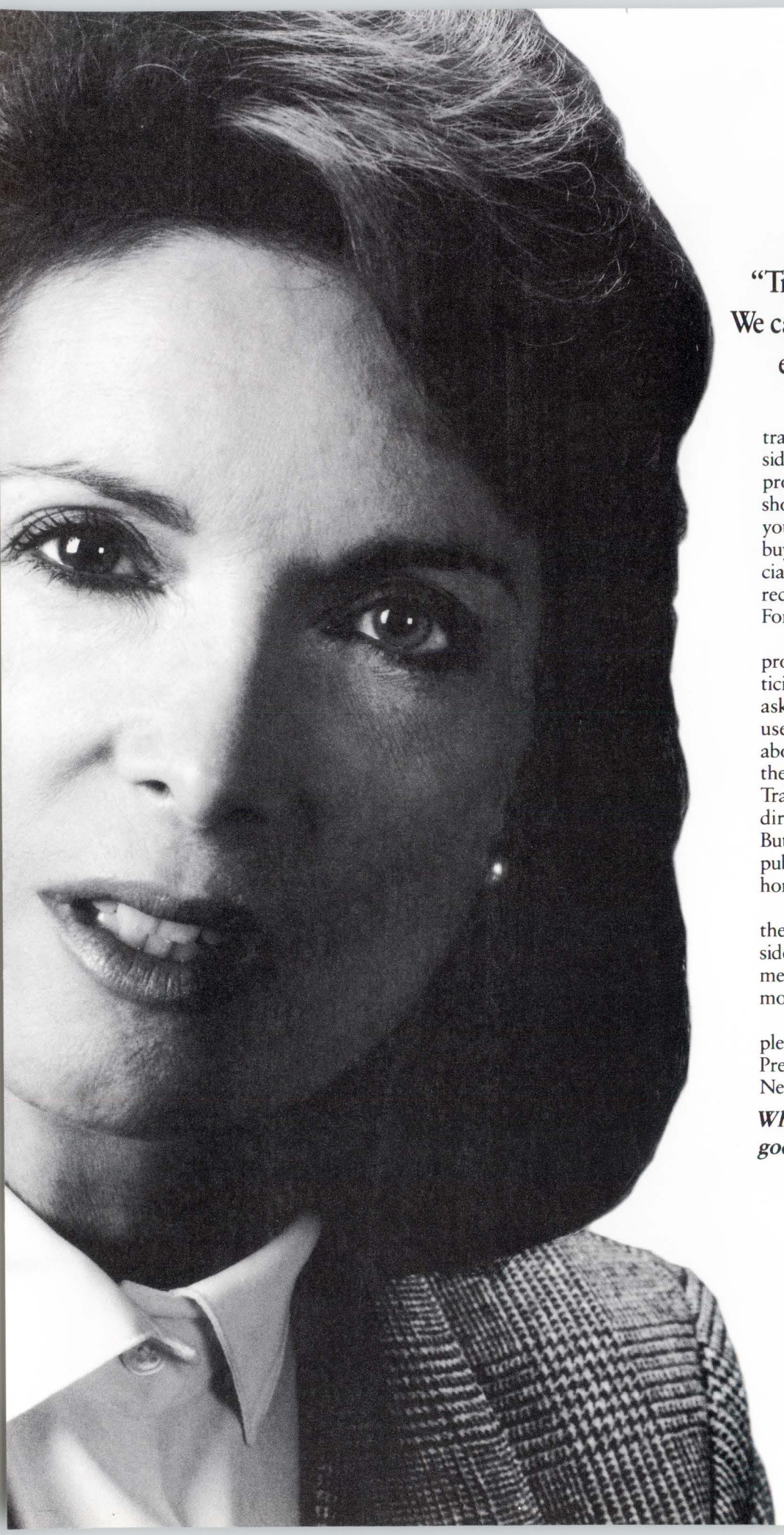
I guess the moral of the story is that there are plenty of things that we shouldn't trust blindly. I tell the test engineers that I'm going to check to see that things make sense when we're all done. And *they* had darned well better check on *me*, because nobody is immune from screwups. Certainly not me.

Specifically, when you create a test, you have to make sure that the results make sense. If the answer is zero, and that doesn't make any sense, then you should probably set a minimum limit. What if a part normally has a power drain of 2 mA, and 3.0 mA maximum? What if you saw a batch of parts with less than 1/2-mA current drain? Wouldn't you tend to get suspicious?

What if we assumed the slew rate could be guaranteed by correlation with the power-supply current but there was no minimum limit on the test for current drain? A sanity check is in order! Some other time, we can think about other interesting cases that deal with "minimum limits."

All for now. / Comments invited! / RAP / Robert A. Pease / Engineer

ADDRESS:
Mail Stop C2500A
National Semiconductor
P.O. Box 58090
Santa Clara, CA 95052-8090



"Trade shows are a luxury. We can't afford to send everyone who wants to go."

If money were no object, travel no hassle and time no consideration, all your customers and prospects would attend trade shows. But in the real world, you're more likely to reach more buying influences through specialized business publications. A recent study, conducted by the Forsyth Group, proves it.

Almost 10,000 business and professional decision makers participated in the study. They were asked what sources they find most useful in providing information about the products and services they buy for their companies. Trade shows, salespeople and direct mail were all well regarded. But overall, specialized business publications clearly took top honors.

Trade magazines are also at the top of the list when you consider cost per contact. No other medium is more efficient. Or has more credibility.

For a free copy of the study, please write to American Business Press, 675 Third Avenue, Suite 400, New York, NY 10017.

Where business goes shopping. **ABP**

CIRCLE 521

DECODER RETAINS ACCESS TIME

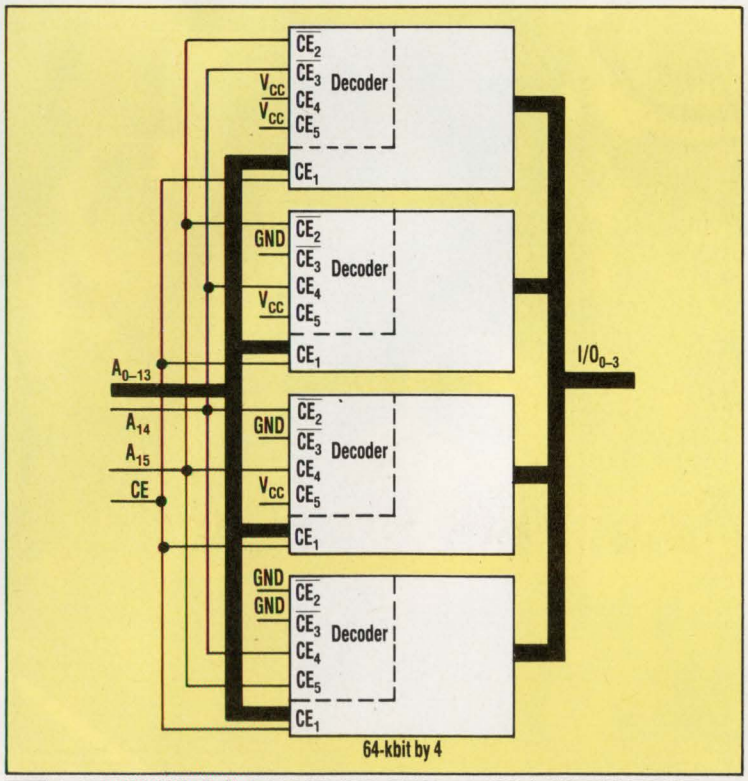
TOM DELURIO
Aspen Semiconductor, a subsidiary of Cypress Semiconductor, 4001 N. 1st St., San Jose, CA 95134; (408) 456-1800.

An internal decoder with four chip-enable inputs helps designers retain the 10-ns access time of the Cypress CY7C160 16-kbit by 4 biCMOS static RAM in multiple memory-chip configurations. Without this capability, denser memory arrays would require external logic, which adds 3 ns or more to the access time.

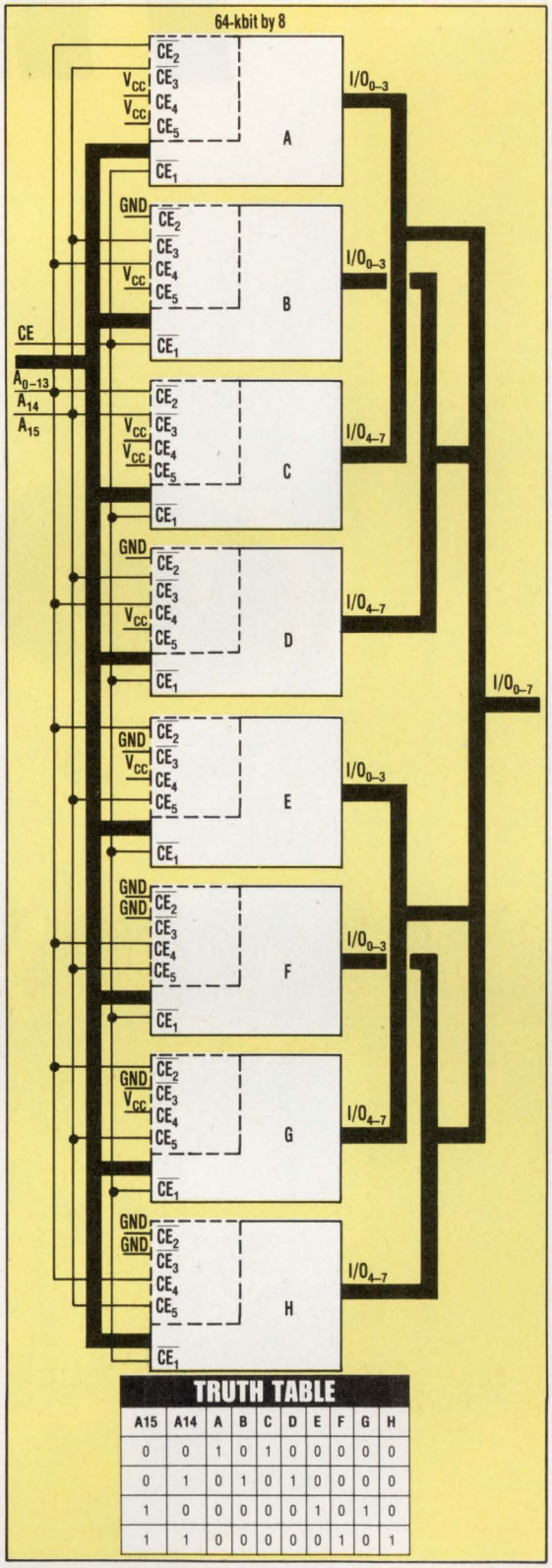
In the "by-4" configuration, only one CY7C160 is active at a time, while in the by-8 configuration, two chips are active at once *(Fig. 1)*. Devices that are deselected will power down to a standby current of less than 40 mA. Maximum operating current is 120 mA per device.

Two additional address lines must be connected to the memories' Chip Enable (CE) inputs in the 64-kbit-by-4 or -by-8 configurations *(Fig. 2)*. A fifth CE input can power down all devices.

The decoder works without external logic because two of the CE inputs, $\overline{CE_2}$ and $\overline{CE_3}$, are active low, and CE_4 and CE_5 are active high. When any CE pin is pulled out of its active state, the chip is deselected. Any CE pin can deselect and power down the device independently of the other CE pins.□



1. DESIGNERS CAN KEEP THE 10-NS ACCESS TIME of the static RAM chips with this circuit. In the "by-4" configuration, only one memory chip is active at a time.



TRUTH TABLE

A15	A14	A	B	C	D	E	F	G	H
0	0	1	0	1	0	0	0	0	0
0	1	0	1	0	1	0	0	0	0
1	0	0	0	0	0	1	0	1	0
1	1	0	0	0	0	0	1	0	1

2. WHEN USED IN THE BY-8 configuration, two chips are active at one time. In either the by-4 or by-8 configurations, two extra address lines (A_{14} and A_{15}) are connected to the chips' CE inputs. A fifth CE input powers down all the devices.

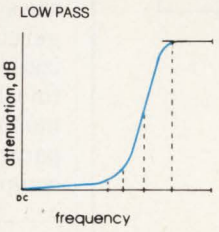
FILTERS

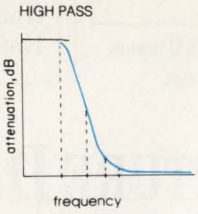
F132-1 REV. ORIG.

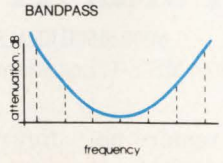
dc to 3GHz from $11.45

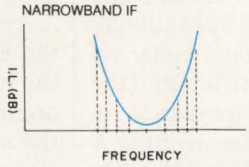
lowpass, highpass, bandpass, narrowband IF

- less than 1dB insertion loss • greater than 40dB stopband rejection
- 5-section, 30dB/octave rolloff • VSWR less than 1.7 (typ) • meets MIL-STD-202 tests
- rugged hermetically-sealed pin models • BNC, Type N; SMA available
- surface-mount • over 100 off-the-shelf models • immediate delivery









low pass dc to 1200MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Max.	STOP BAND, MHz (loss>40dB) Max.	STOP BAND, MHz (loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45

high pass dc to 2500MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Min.	STOP BAND, MHz (loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95

bandpass 20 to 70MHz

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB) Max. F1	PASS BAND, MHz (loss <1dB) Min. F2	STOP BAND, MHz (loss > 10 dB) Min. F3	STOP BAND, MHz (loss > 10 dB) Max. F4	STOP BAND, MHz (loss > 20 dB) Min. F5	STOP BAND, MHz (loss > 20 dB) Max. F6	VSWR 1.3:1 typ. total band MHz	PRICE $ Qty. (1-9)
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95

narrowband IF

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB F5	STOP BAND, MHz I.L. > 20dB F6	STOP BAND, MHz I.L. > 35dB F7	STOP BAND, MHz I.L. > 35dB F8-F9	PASS-BAND VSWR Max.	PRICE $ Qty. (1-9)
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95

Mini-Circuits

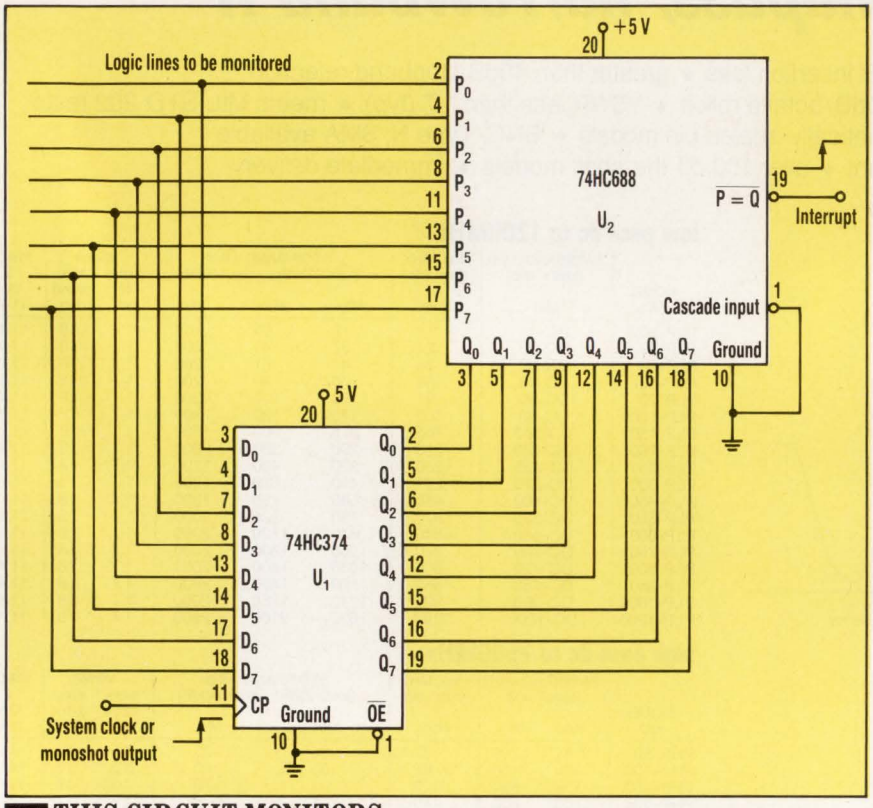
P.O. BOX 350166, Brooklyn, New York 11235-0003 (718) 934-4500 FAX (718) 332-4661 TELEX 6852844 or 620156 **WE ACCEPT AMERICAN EXPRESS**

F132-2 REV. ORIG.

CIRCLE 135

CIRCLE 522 MONITOR LOGIC-LINE STATE

SHANKER. C
Indian Telephone Industries, Bangalore 560038, India.



THIS CIRCUIT MONITORS the state of the logic lines. When any of U_2's Q inputs don't equal their P counterparts, the P = Q signal will go high, causing an interrupt.

Some process-control applications require their logic lines to be monitored constantly for state changes. This circuit does that independently and interrupts the microprocessor when a change occurs *(see the figure)*.

At the low-to-high clock transition, the eight flip-flops in U_1 (octal three-state D flip-flop) will store the state of their individual D inputs, which also form the P input to U_2 (8-bit magnitude comparator). Because U_1's Output Enable signal is low, the contents of the eight flip-flops are available at the outputs. These outputs form U_2's eight Q inputs. Now, if the logic state of any of U_2's P inputs changes, the P = Q output will go high, causing an interrupt.

The circuit operates from either the system clock or a monoshot triggered by the processor during initialization, or at the end of a service routine. If more than eight lines are to be monitored, the latches and the comparators should be cascaded and the comparators' outputs ORed.□

Send in Your Ideas for Design

Address your Ideas-for-Design submissions to Richard Nass, Ideas-for-Design Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604.

IFD WINNER

IFD Winner for September 13

Elias Eliopoulos, 117 Konstantinoupoleos, GR-132 31 Petroupoli, Greece. His idea: *"Get Pulse Train From One Pulse."*

VOTE!

Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $150 Best-of-Issue award and becomes eligible for a $1,500 Idea-of-the-Year award.

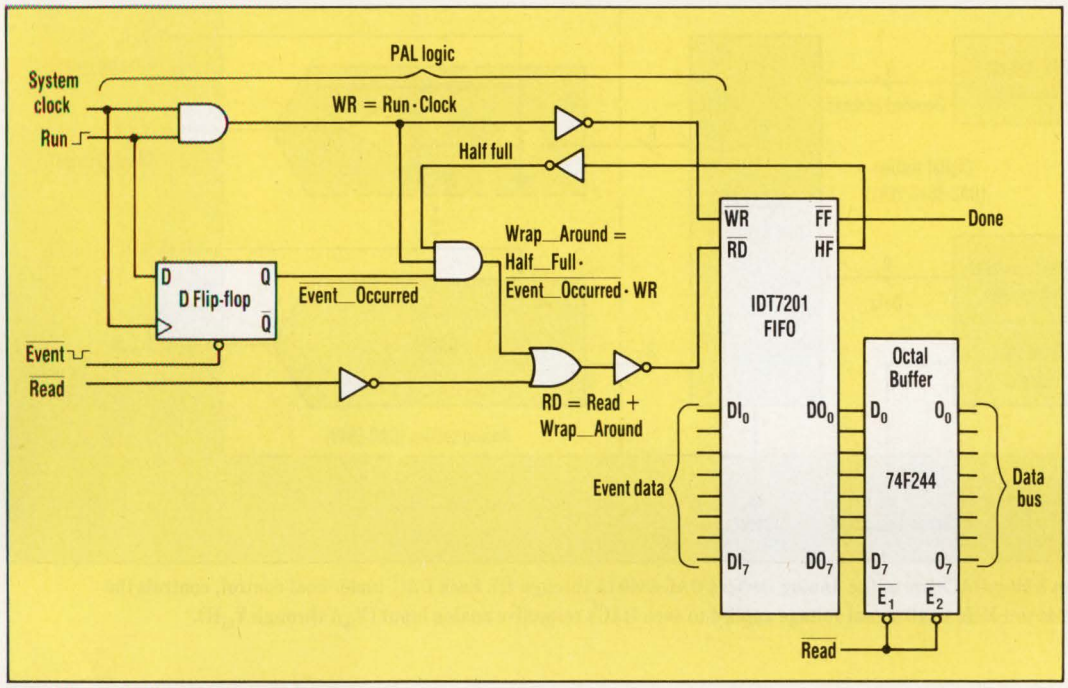
CIRCLE 523 CAPTURE DATA BEFORE, AFTER EVENT

NOOR SINGH KHALSA
EG&G Inc., P.O. Box 809, MS E-1, Los Alamos, NM 87544; (505) 667-0200.

Some applications require users to capture data before and after an event. This task can be accomplished by continually feeding the data that's being recorded into a circular buffer until the event occurs. Then, more data is recorded until the buffer is full. A FIFO buffer with a half-full flag fits the bill for this chore.

A start signal causes the FIFO buffer to collect data initially *(see the figure)*. When the buffer's half-full flag becomes active and a trigger hasn't yet been received, the Wrap_Around signal becomes active and the FIFO's Write signal is gated to the Read signal. When this situation occurs, the FIFO buffer is emptied at the same rate that it's being filled. Hence, the buffer remains in a half-full state.

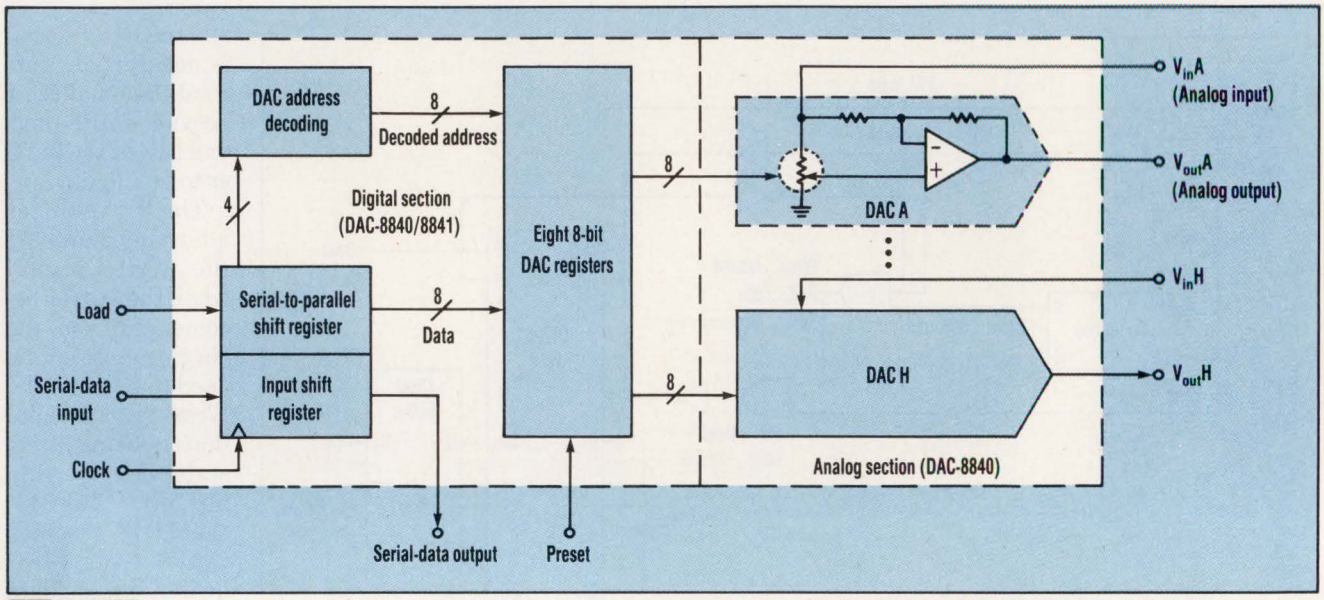
When a trigger signal is received, Event_Occurred becomes active



TO CAPTURE DATA before and after an event, use a FIFO with a half-full flag. Initially, the half-full FIFO is emptied as fast as it's filled. Asserting Event_Occurred and removing Read fills the rest of the FIFO.

and the Read signal is deasserted. This condition makes it possible for the second half of the buffer to be filled.

The FIFO buffer internally shuts off the Write signal when the buffer becomes full, so the flag needn't be used to gate off the Write signal. Note that an octal three-state noninverting buffer (74F244) should be inserted between the FIFO buffer and the data bus. Data appears on the FIFO's output lines when the buffer reads and writes simultaneously.□



EIGHT voltage-output 8-bit mDACS are in the Analog Devices DAC-8840 (A through H). Each DAC, under host control, controls the amplitude of a separate dc-to-1-MHz small-signal voltage applied to each DAC's respective analog input ($V_{in}A$ through $V_{in}H$).

EIGHT, 8-BIT DACS ON AN IC SET DC LEVELS, CONTROL GAIN AND PHASE, AND PERFORM MODULATION UNDER THE AEGIS OF A HOST.

1-MHz MDACs REPLACE GAIN-SETTING TRIMMERS

FRANK GOODENOUGH

The ubiquitous trimming potentiometer (trimmer pot) may soon become obsolete. That's if Analog Devices has its way, whereby TrimDACs would replace trimmer pots in a number of wide-ranging applications. TrimDACs are octal 8-bit digital-to-analog converters (DACs) that connect through a serial link with a host microprocessor.

The first TrimDAC, the DAC-8800, was limited to setting dc voltage levels. For example, it trimmed the offset voltage of three op amps while providing the reference for three comparators and two additional DACs. But now, Analog Devices' recently acquired PMI division added a pair of second-generation 8-bit CMOS DACs to the family, the DAC-8840 and DAC-8841. The DACs not only set dc levels, but can also control gain/phase or modulate a carrier. And the DACs offer a small-signal bandwidth of 1 MHz—enough for many video applications.

EIGHT-BIT-DAC POTENTIOMETERS

The DAC-8840 and DAC-8841 are true multiplying DACs (MDACs), each with its own analog input and an additional output op amp. The DAC-8840 runs off ±5-V supply rails, can provide an output of ±3 V across 2000 Ω, and performs four-quadrant multiplication. Its cohort runs off a 5-V supply rail and puts out 3 V across 2000 Ω, but is limited to two-quadrant multiplication.

Replacing the multiple trimmer pots in high-volume products, such as color monitors with 1000-line (or greater) resolution, is a major application. These potentiometers are now adjusted at the factory by robot-controlled screwdrivers.

The analog input of the eight four-quadrant MDACs (A through H) on the 8840 looks like the top of a potentiometer connected between the feedback resistors of an op amp and ground *(see the figure)*. The potentiometer's wiper connects to the plus input of the op amp. When the wiper is at the top (an input code of all ones), the DAC's output equals the analog input multiplied by 127/128. In this circuit, the op amp operates as a unity-gain follower.

As the wiper is run down the potentiometer by decreasing the value of the digital input word, the analog output is attenuated, relative to the input, in increments of 1 part in 127 per least-significant-bit (LSB) drop in the value of the binary input word. With the wiper at the midpoint of the potentiometer (an input word of all zeros), the op amp's output will be 0 V. As the wiper moves further down the potentiometer (the code decreasing toward all zeros), the polarity and phase of the output voltage reverse and the voltage's amplitude starts increasing, reaching a value of minus the full-scale input (at an input code of all zeros). The op amp now operates as a unity-gain inverter.

TEA FOR TWO

These DACs not only control the amplitude of an ac signal, such as a sine wave, they also phase-shift the signal 180° between input and output while passing through mid-scale. Thus they can be perceived as modulators capable of amplitude and/or phase modulating a carrier by a host.

The analog circuits of the two-quadrant DAC-8841s are similar to, but simpler than, those of the 8840. The DAC itself still appears as a potentiometer, with the analog input applied to its top and the plus input of the op amp tied to the wiper. However, feedback is connected to the bottom of the potentiometer, either to ground or an offset reference. It operates as a "follower with gain" fixed at a gain of two. Thus the output is two times the analog input—multiplied by the zero-to-100% attenuation defined by the digital input

EIGHT-BIT-DAC POTENTIOMETERS

word. The bottom of the potentiometer, though typically connected to ground, can be run to a positive reference voltage (for example, half the maximum input) so that an ac input signal can be handled. In other words, a dc offset of 1 V is used with an ac input of 1 V pk-pk. The full-scale output is then 2 V pk-pk with an input code of all ones.

Minimum/maximum analog specifications over the extended-industrial-temperature range include integral and differential nonlinearities of ±1 LSB, code-dependent analog input resistance of 4000 Ω, and a slew rate of 1.5 V/μs. Total harmonic distortion is 0.01% at 1 kHz with 4 V pk-pk and 1 V pk-pk into the 8840 and 8841, respectively. Outputs settle in 6 μs to within 1 LSB, and DAC-to-DAC crosstalk is –60 dB. Typical full-power 3-dB bandwidth is 100 kHz.

For ease of use with a host microprocessor, there's a simple, layout-efficient, three-wire, serial-data interface *(see the figure, again)*. All that's needed are a clock, a serial-data input, and a load-strobe input. Each DAC has its own register that holds the output state. These registers are updated from an internal serial-to-parallel shift register that's loaded from the serial input. Twelve-bit data words from the host are clocked into the serial-input register. The first four bits contain the address for the DAC register into which the next eight bits are to be loaded. These 4-bit addresses and the data word allow any DAC register (and thus any DAC's output) to be updated at any time without disturbing the other DACs on the chip. The strobe pulse to the load input updates just the DACs addressed.

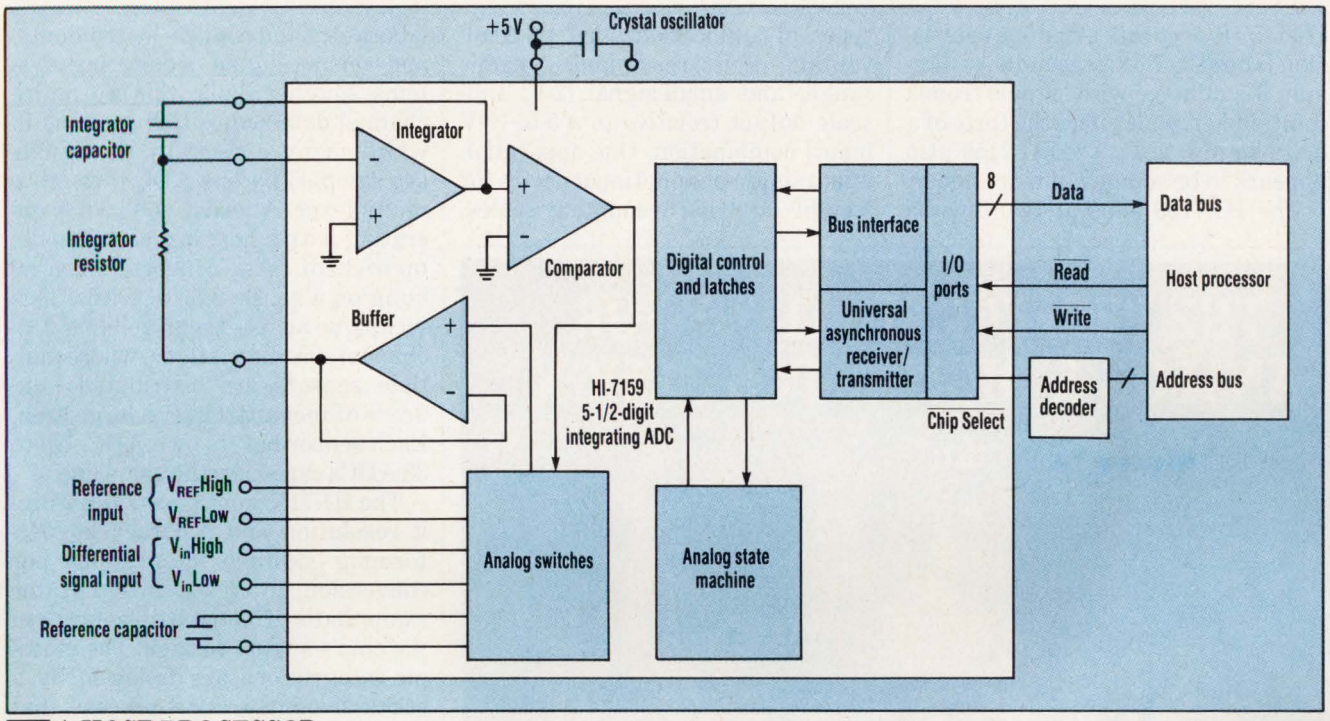
Since many systems will need several or even tens of 8840s or 8841s, a serial-data output-pin at the end of the serial input register allows numerous octal DACs to be daisy-chained on one serial bus. When the preset pin (an additional digital input found on both ICs) is brought to logic low, the output of all eight DACs is brought to zero. This is a particularly useful state to start a system at power-up or the onset of a calibration. The DAC-8840 takes 26 mA from ±5 V. The DAC-8841 draws similar current from 5 V.□

PRICE AND AVAILABILTY

The DAC-8840 and DAC-8841 come in 24-pin plastic and ceramic DIPs and plastic SOICs. Cost starts at $9.95 each in 100s. Availability is from stock.

Analog Devices, PMI Div., 1500 Space Park Dr., Santa Clara, CA 95052-8020; (408) 562-7513. **CIRCLE 513**

HOW VALUABLE?	CIRCLE
HIGHLY	562
MODERATELY	563
SLIGHTLY	564



A HOST PROCESSOR sets the operating modes of the HI-7159, a 5-1/2-digit integrating ADC. The host reads the ADC's data via a parallel bus, or alternatively over a two-line standard serial interface.

5-1/2-DIGIT INTEGRATING ADC RUNS 15 CONVERSIONS/S

FRANK GOODENOUGH

Today, to get high resolution from an IC analog-to-digital converter, delta-sigma types are almost certainly your first choice. But don't give up on the old-fashioned multislope integrating ADC. The 5-1/2-digit HI-7159 from Harris (formerly Intersil) offers 10 times the resolution of any other multislope integrating IC ADC. It performs fifteen 200,000-count conversions per second, resolving 10 μV out of a 2-V full-scale input. In its high-speed mode, it performs sixty 20,000-count conversions each second on a similar-sized signal. The host can change this mode/word rate at will. The chip has its own universal asynchronous receiver/transmitter (UART) which simplifies the interface with a host processor through serial or parallel buses *(see the figure)*.

The chip offers several significant advantages over delta-sigma ADCs, particularly lower system cost. At $15 in 100-lot quantities, system cost will run under $21 with the integrator, while system cost for comparable delta-sigma converters could run over $25.

The converter's serial and parallel digital outputs connect easily with standard microprocessors. In addition, unlike instrumentation-type 16- and 20-bit delta-sigma converters that can take as much as a second to settle to a correct answer, the

5-1/2-DIGIT INTEGRATING ANALOG-TO-DIGITAL CONVERTER

HI-7159 is accurate after one conversion (about 1/7 of a second). As a result, it's at home with signals from a multiplexer, which isn't the forte of a delta-sigma ADC. The HI-7159 also appears to be somewhat more linear.

The HI-7159 aims at two diverse types of applications that take advantage of its resolution, dynamic range, and small-signal (2-V) full-scale output (relative to a 5-to-10-V input) combination. One application is as a single-channel input device for weight- and parts-counting scales, laboratory and medical instruments, and seismic-signal monitoring systems. Another application is in multichannel data-acquisition systems in which many essentially dc signals are sampled by one ADC through a multiplexer. Alternatively, while operating with a host in a serial mode, up to 32 of these converters can be hung on a single pair of wires. This technique adapts them well to multichannel seismic systems, where multiple sensors are distributed hundreds of feet apart over a large area. Each sensor has its own ADC. Up to 32 ADCs can share the same line.

The HI-7159 achieves its 5-1/2-digit resolution and accuracy by performing multiple integrations per conversion, to create an integrator ramp that's effectively greater than the chip's supply voltage. The multiple integrations are followed by a successive-integration process that measures the voltage remaining on the integrator capacitor (called the residue voltage) to the 5-1/2-digit accuracy of the ADC.

In the 5-1/2-digit mode, the input voltage is integrated and then de-integrated against the reference four times. The resulting count achieves the same resolution as one integration, but with a maximum ramp voltage effectively four times as great. That is, the signal thinks a $\pm$12-V ramp was created from $\pm$5-V supply rails (in the 4-1/2-digit mode, the circuit integrates just once).

At any given time, the host chooses between one of three types of conversions. The host may direct the ADC to measure its own internal offset voltage, or measure the input voltage—including the offset voltage—or operate in the default mode. In the default mode, the ADC measures the internal offset and input voltages, and subtracts the offset voltage from the input voltage.

INS AND OUTS

The HI-7159 receives instructions from, and transmits data to, its host processor through one of three communications modes: parallel microprocessor, and serial non-addressed and serial-addressed modes. The first mode connects the chip directly

5-1/2-DIGIT INTEGRATING ANALOG-TO-DIGITAL CONVERTER

to the host's parallel data bus. Data is read in and out under control of the host's Chip Select, Write, and Read lines. Serial-mode 1 reads and writes serial data packets at one of four selectable baud rates: 300, 1200, 9600, or 19,200. Serial-mode 2 is identical to serial-mode 1 except for additional addressing abilities, which make it possible for 32 of these ADCs to share the same line.

The ADC can run in a single-conversion mode, in which the host defines conversion modes, asks for a conversion, waits for completion, and reads the results. Alternatively, in the continuous-conversion mode, the ADC runs continuously, updating the data registers after each reading for the I/O ports.

The analog portion of this bipolar-MOS IC requires just four external components: a crystal oscillator, an integrator resistor, and reference and integrator capacitors. The integrator capacitor is critical. It must be a polypropylene, polystyrene, or Teflon type, having minimum leakage and dielectric absorption. If typical Mylar or other ceramic capacitors are used, significant linearity errors will occur. In typical applications, the integrator capacitor's value will run between 0.1 and 0.47 μF.

As with most integrating ADCs, the full-scale input-voltage span at the converter's differential input is ± 2 V. That's when the converter is used with a 1-V reference tied to V_{REF}High, and V_{REF}Low is connected to ground. Integral linearity error runs a maximum of ± 3 counts. Because the converter input looks at the gates of MOS transistors, input resistance is virtually infinite. In both unipolar and bipolar operation, zero-error is a maximum of ± 1 count. Gain error for full-scale positive inputs is zero counts, 18 counts for negative full scale signals. Like most integrating ADCs, the HI-7159 has a differential input, giving the device a common-mode rejection error of ± 3 counts (96 dB) for ± 3 V of common-mode voltage. Zero drift with temperature runs 0 counts/°C, and full-scale error is ± 0.1 count/°C. The HI-7159 needs 10 mA from a +5-V rail, and 4.5 mA from a –5-V rail.

PRICE AND AVAILABILTY

The HI-7159, 5-1/2-digit ADC comes in a 28-pin plastic DIP. It operates from 0 to 75°C. In quantities of 100, it goes for $15 each. Small quantities are available from stock.

Harris Corp., Semiconductor Sector, 2450 Walsh Ave., Santa Clara, CA 95051; Swapan Banerjee, 1-800-4HARRIS, ext. 1098.

CIRCLE 512

HOW VALUABLE?	CIRCLE
HIGHLY	559
MODERATELY	560
SLIGHTLY	561

Optocoupler With Two Diodes Sports Linear Isolation Approaching 0.01%.

Linear Isolator Stands Off 7500 V For 1 Second

Frank Goodenough

Adding a couple of 741 class op amps to Siemens' low-cost IL300 linear optocoupler can give you an isolation amplifier that offers a typical linearity to within better than 0.1%. If OP-07 class op amps are used, linearity can approach 12 bits (0.01%). And using chopper-stabilized op amps should provide performance that goes well beyond 12 bits. Couple this accuracy with the ability to withstand 7500 V ac peak (5300 V ac rms) for 1 second, or 6250 V ac peak (4420 V ac rms) for 1 minute—at 60 Hz—and you've got impressive isolation performance. Though not blindingly fast (rise and fall times typically run 1.75 μs each), this inexpensive optocoupler costs less than $2 each in quantities of 5000, and under $3 each in 100-lot quantities.

Until the IL300 came along, optocouplers were limited virtually to isolating digital signals. The IL300 is a horse of a different color. In addition to its aluminum gallium arsenide infrared LED, it hosts two p-i-n photodiodes galvanically isolated from each other and from the LED *(see the figure)*. The LED irradiates both diodes, one of which—D_O—supplies the output. The second diode—D_f—provides negative feedback. D_f captures part of the LED's flux (light output) and generates a control signal, K_1, that can be used to servo the LED's drive current. This technique compensates for nonlinearities in the LED's flux with drive current, as well as flux changes with time and temperature. The output p-i-n photodiode produces an output signal, K_2, that's linearly related to the servoed, optical flux created by the LED.

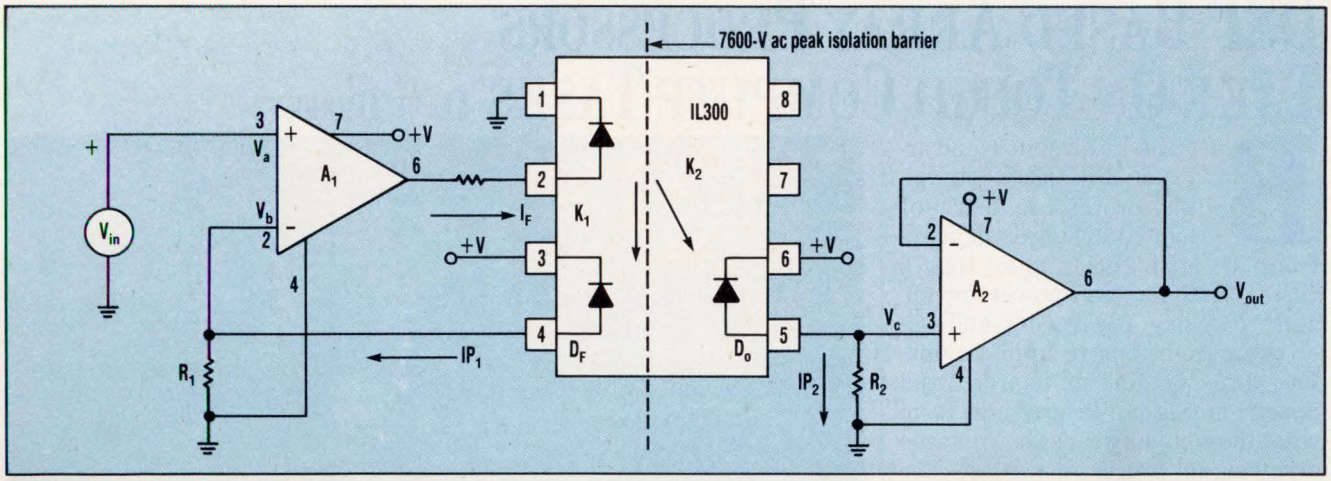
A typical isolation application includes the ability to supply linear feedback from the output of a switching power supply to the switcher's control circuitry. Other applications include medical and industrial data-acquisition systems, and the measurement of currents in the hot side of a high-voltage line.

In medical applications, the IC is used between sensors such as EKG probes and patient-monitoring systems. It isolates the patient from ac power-line faults, either within the instrument or external to it—such as the frame of an electrically-operated bed. Industrial applications include monitoring the voltage- and current-switching waveforms that drive large ac and dc motors which employ solid-state motor-control systems.

The isolator can also be used to handle digital signals—particularly in industrial applications, such as programmable controllers. Unlike the typical optocouplers employed for logic, there's no degradation over time and temperature for signal level, propagation delay, or waveform when using the IL300.

A typical application requires two op amps—A_1 and A_2—which must lie on separate silicon die to provide isolation *(see the figure, again)*. Op amp A_1 drives the LED with the input signal. The feedback photodiode sources current to resistor R_1, which is connected to the inverting input of op amp A_1. The photocurrent from the diode IP_1 is forced by negative feedback to a value that satis-

LINEAR OPTOCOUPLER IC



THIS LINEAR OPTOCOUPLER, the IL300 from Siemens, with a couple of op amps added, builds a highly linear isolation amplifier that can stand off 7600 V ac peak. Despite its impressive isolation performance, the IL300 linear optocoupler can be purchased for less than $2 each in 5000-lot quantities.

fies the relationship:

$$-IP_1 = V_{in}/R_1$$

The magnitude of this current is directly proportional to the feedback-transfer, or servo, gain (K_1), multiplied by the LED drive current I_F, or:

$$-V_{in}/R_1 = (K_1)(I_F)$$

where $K_1 = IP_1/I_F$.

An electron-photon-electron negative-feedback loop from the output of op amp A_1, through the LED, through diode D_F, to the minus input of op amp A_1. This in turn forces the op amp to supply enough output current I_F to produce sufficient photocurrent, IP_1, to force voltage V_b to equal voltage V_a.

The output photodiode connects to op amp A_2, which is connected as a simple follower. The diode's load resistor, R_2, performs the current-to-voltage conversion. The output voltage of op amp A_2 is the product of the output forward gain K_2, the LED current, and the diode's load, or:

$$-V_{out} = (I_F)(K_2)(R_2)$$

Input-To-Output

The overall transfer gain of circuit V_{out}/V_{in} (or K_3) now becomes the ratio of the output forward gain K_2 multiplied by the photodiode load, to the product of the feedback transfer gain K_1 multiplied by the value of the input resistor R_1. This ratio reduces to:

$$K_3 = V_{out}/V_{in} = (K_2)(R_2)/(K_1)(R_1)$$

This equation indicates that the overall transfer gain K_3 is completely independent of the LED's forward current. The overall transfer gain parameter is expressed as the ratio of the output gain K_2 to the feedback gain K_1, or:

$$V_{out}/V_{in} = (K_3)(R_2)/(R_1)$$

While the circuit shown provides noninverting operation, either op amp can also be used in an inverting circuit. In addition, the circuit only handles unipolar, positive, input voltages. But both input and/or output op amps may be given offset voltages from a reference (or supply rail) so that bipolar signals can be handled (or produced).

From one IL300 to another, transfer gain K_3 ranges from a minimum of 0.56 to a maximum of 1.65. Servo gain K_1 runs between 0.0036 and 0.011. This wide range of values may seem to rule out the IL300 linear optocoupler as an easy-to-use drop-in part for high-volume production. However, the isolators are sorted into bins as they come off the production line.

The first sorting divides the isolators into two categories based on servo gain. Then each group is sorted into one of ten categories based on transfer gain.

Each of the 20 categories represents a transfer-gain spread of ±5% (for example, a typical category contains IL300s with transfer-gain values that range between 1.056 and 1.175). The ICs are delivered in tubes of 50, all of which fall in the same category.

Other specifications of the IL300 linear optcocoupler include a typical open-loop transfer-gain linearity within ±0.25%. Its open-loop transfer-gain linearity temperature coefficient is within ±0.005%/°C.

The optocoupler's small-signal 3-dB bandwidth is 200 kHz, and its input-to-output capacitance at 1 MHz is just 1 pF. The device's common-mode rejection ratio is 130 dB at 60 Hz. Power consumption is just 15 mW.□

Price And Availabilty

The IL300, which is UL recognized, comes in an 8-pin plastic miniDIP and goes for $2.95 each in 100s and $1.95 each in quantities of 5000. VDE 0884 approvals are being applied for. The device is also available as the IL300G with the VDE lead bend that assures 0.4-in. spacing across the package for $3.20 each in 100s, and $2.10 each in quantities of 5000. A wide-band version is expected by the middle of the year.

Siemens Components Inc., 19000 Homestead Rd., Cupertino, CA 95054; Bob Krause, (408) 725-3543. **CIRCLE 511**

How Valuable?	Circle
Highly	556
Moderately	557
Slightly	558

DSP-Based Array Processors Take On Tough Compute Tasks

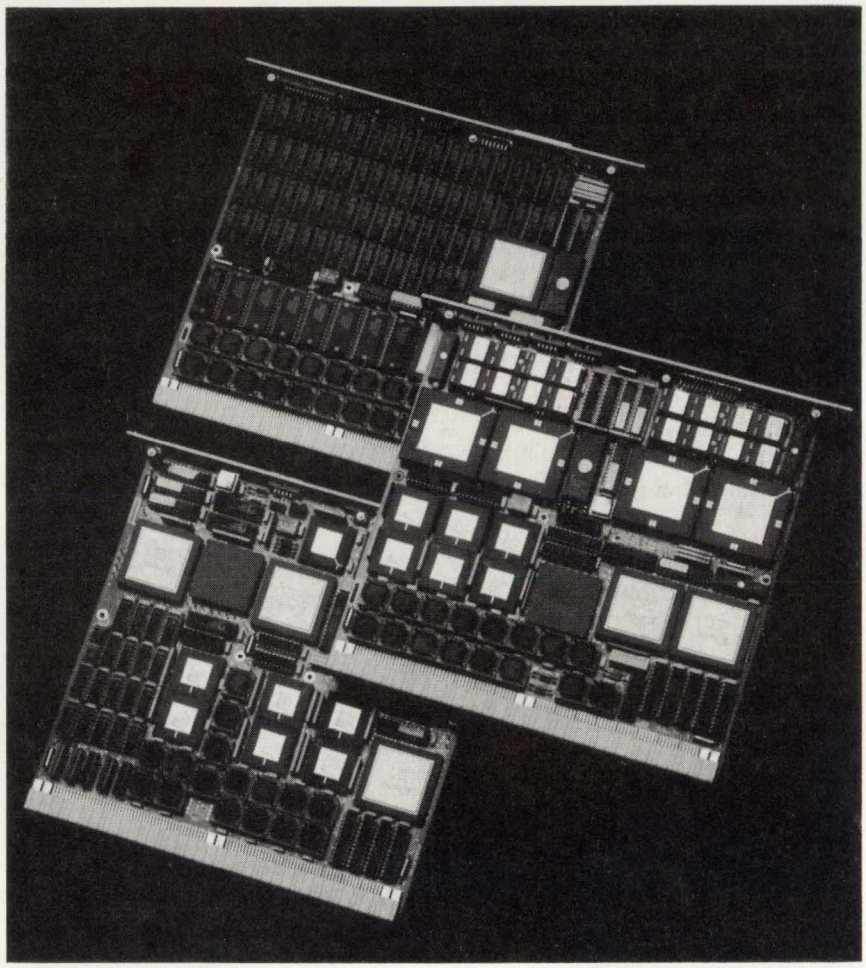
DAVE BURSKY

Based on Futurebus+ and arrays of DSP96002 digital-signal processors, a trio of expandable boards delivers from 200 MFLOPS to more than 5 GFLOPS of compute power for image processing, ray tracing, and other compute-intensive applications. The three 6U-format boards from Spectrum Signal Processing form what the company calls the versatile array signal processor (VASP). The boards consist of an I/O processor card, a general signal processor, and a two-port memory board.

A proprietary high-bandwidth signal bus along with pipeline memories make it possible for rapid transfers of large data arrays. The bus operates in either a programmed I/O mode with transfers up to 100 Mbytes/s, or in a DMA-controlled mode with 50-Mbyte/s transfers. The bus has a 64-bit data path and a 32-bit address range.

The I/O card supplies data from memory to the array of processors and then transfers results from the array back to memory. A 96002 DSP chip on the card allows the board to serve as a 40-MFLOPS standalone DSP card by using the local resources—a 32-kword (32-bit) data memory, a 32-kword nonvolatile memory for program storage, various control resources, and three independent, bidirectional data ports. The three ports include a synchronous 16-bit parallel I/O port that runs at 10 MHz, a VMEbus interface running at 10 Mbytes/s, and the proprietary signal bus that can run at 50 Mbytes/s (under programmed I/O).

Packing up to four DSP chips, each with its own local 64-kword-by-32-bit RAM, the signal-processor array card delivers a peak throughput of 160 MFLOPS with all four DSP chips installed. Multiple signal processor cards can be installed in a system to provide the desired system throughput. The board overlaps the input. Output tasks are normally overlapped with data processing and therefore don't cause any performance degradation. Processing from local memory releases a particular DSP chip from the global bus and permits the connection of multiple boards to a common bus.



The third card in the trio consists of a large data memory array—4 Mwords-by-64-bits—and the control logic to turn the array into a dual-port subsystem for bus-to-bus data transfers. Access time through either port is 75 ns, and data can be simultaneously read or written through both ports.

To control the boards, users must develop two software routines. One is the executive control software to coordinate the operation of the boards. The other routine is the actual application program that includes the algorithms the DSP chips must execute. A typical development scenario might include the use of a Sun workstation for application-code development, simulation, and debugging, using software tools from Motorola, Intermetrics, Comdisco, and others. Resident firmware on the cards consists of rudimentary routines for initialization, bus control and communication, diagnostics, board-resource configuration, and application program downloading.

Actual system availability will be in the second quarter; price will be in the $160/MFLOP range.

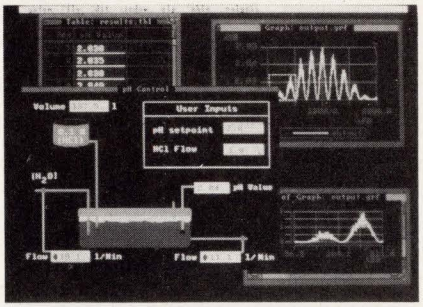
Spectrum Signal Processing Inc., 3700 Gilmore Way, Suite 301, Burnaby, British Columbia, Canada V5G 4M1; Barry Jinks, (604) 438-7266. **CIRCLE 310**

DATA-ACQUISITION PACKAGE WORKS WITH 386, 486 PCS

The Viewdac data-acquisition, analysis, and graphics software package takes full advantage of 80386- and 80486-based personal computers. The software combines the simplicity of a package solution and the flexibility of a programming language. A windowing environment makes the software easy to use and increases the operator's efficiency.

With Viewdac's multitasking capabilities, the user can switch from one application to another quickly and efficiently. Users can acquire, graph, tabulate, manipulate, or create data while other applications are running. Post-acquisition processing can be handled by the built-in interactive data-analysis and graphics functions.

To develop new applications, users can quickly set up customized virtual front panels by selecting menu items in a window. No programming experience is needed. The panels can then be used to control an experiment and supply graphical or numerical feedback on the results. The user can change panels or application parameters while a task is being performed without stopping the experiment.



The software runs on IBM-compatible 386- or 486-based computers running DOS 3.0 or above. Numerous data-acquisition boards are supported, including those from Keithley DAC, Keithley MetraByte, Analog Devices, Burr-Brown, Data Translation, and Markenrich.

Viewdac costs $2495, which includes a 30-day money-back guarantee, one day of training, and 1 year of extended support with software upgrades. Runtime licenses are also available.

Keithley Asyst, *100 Corporate Woods, Rochester, NY 14623; (800) 348-0033 or (716) 272-0070.* **CIRCLE 311**

■ *JOHN NOVELLINO*

PORTABLE DSO FEATURES 10-BIT RESOLUTION

With its dual 10-bit, 100-Msample/s ADCs, the LeCroy 9430 portable oscilloscope is suitable for a wide range of precision measurement applications. Using the scope's filtering and averaging capabilities, operators can increase resolution by eight times (from 10 to 13 bits). And dc accuracy is within a state-of-the-art 1%.

Each of the 9430's two channels has a nonvolatile, 50k acquisition memory. These very long memories permit high sample rates on slow time-base settings, as well as horizontal expansion of up to 1000 times. As a result, users can closely examine short-duration glitches.

Menus help users call up standard waveform-processing routines, including arithmetic functions and summation averaging. The 9430 also performs 10 standard pulse-parameter measurements. In addition, optional firmware can be installed to transform the scope into an FFT spectrum analyzer with a dynamic range of 80 dB.

Standard trigger functions include pre- and post-triggering, level, slope, mode, and coupling. The 9430 also features LeCroy's advanced Smart trigger capabilities. These include hold-off by time or event, delay by time or event, and TV, pattern, state-qualified, interval, or glitch triggering. In the Fastglitch mode, the scope triggers on pulses as narrow as 2.5 ns on all time-base settings. To make the 9430 easier to use, LeCroy employed familiar analog-type controls.

The Model 9430 costs $16,990 and is available for delivery within 10 weeks.

LeCroy Corp., ITI Div., *700 Chestnut Ridge Rd., Chestnut Ridge, NY 10977-6499; (914) 578-6097.*

CIRCLE 312

■ *JOHN NOVELLINO*

IC STORES ITS SYSTEM'S HISTORY FOR DIAGNOSIS

The TMS29F816 Scope Diary memory IC stores diagnostic information automatically for pc boards or systems where testability is an important issue. The memory, which is compatible with the IEEE-1149.1 (JTAG) boundary-scan standard, is a one-chip solution for retaining a board's operating history. The core of the chip is an IEEE-1149.1 interface controller with an embedded 5-V, 16-kbit flash EPROM. Basic board information and key data can be stored a protected area. Using the 1149.1 four-wire interface and serial data protocol, the memory works with other chips in the Scope (System Controllability/Observability Partitioning Environment) line. Sample quantities of the Scope Diary memory are available now, and production quantities are scheduled for availability in the second half of 1991.

Texas Instruments, Semiconductor Group, SC-9067, P.O. Box 809066, (800) 336-5236 ext. 700 or (214) 995-6611, ext. 700. **CIRCLE 313**

VXI CARD HOLDS 12-BIT DIGITIZER/ANALYZER

A 12-bit, 10-MHz ADC with a state-of-the-art RISC transputer gives the VX4240 waveform digitizer/analyzer module sophisticated measurement and analysis functions. The C-size VXI-bus module captures waveforms to 5 MHz and features extensive on-card signal-analysis and conditioning routines. Users can program all key parameters, and calibration is simplified by semi-automatic calibration-alignment software. The VX4240 has 256 ksamples of memory, with an optional capacity of 1 Msample. More than 40 analysis routines include fast Fourier transforms; signal-to-noise ratio; total harmonic distortion; maximum, minimum, average, and rms values; and rise and fall times. Eight voltage ranges are calibrated, but users can directly set any range of less than 100 V. The VX4240 costs $8000 and is available within 6 weeks.

Tektronix/Colorado Data Systems Inc., 3301 W. Hampden, Englewood, CO 80110; (800) 237-2831 or (303) 762-1640. CIRCLE 314

ATVG SOFTWARE HANDLES ADDITIONAL DEVICES

PLDtest Plus version 2.0 features added device support, a new intuitive user interface with a windowed environment, in-circuit test capability, hard- and soft-fault grading, and an enhanced design-analysis report file. The software is an automatic test-vector-generation package for both non-preloadable and preloadable registered and combinatorial devices. Added device support includes the Altera family of EPLDs, the 20RA10, and 20 other unique architectures. Also available as an option is TesterLink, a test-vector-to-in-circuit-tester translator. With TesterLink, which currently works with GenRad 227X, 228X, and 2750 testers, users can functionally test programmable-logic devices at the board level. PLDtest Plus 2.0 prices range from $1995 to $7995, depending on devices supported and workstation compatibility. Availability is 2 to 4 weeks. TesterLink starts at $1395.

Data I/O Corp., 10525 Willows Rd. N.E., Redmond, WA 98073-97460; (206) 881-6444. CIRCLE 315

UPGRADED DMMS BOAST HIGH ACCURACY

Two new digital multimeters (DMMs) improvement on their earlier versions. The 5-1/2-digit 197A and 4-1/2-digit 175A feature a backlit electroluminescent display, a CMOS memory for longer battery life, and an extended storage temperature range of –40 to +70°C. The 197A also adds six dB reference impedance levels (50, 75, 93, 135, 300, and 600 Ω) for more flexibility in ac measurements, and an improved accuracy within 0.5% on the highest-current range of 10 A. Both meters specify an accuracy within 1% on the lowest ac-voltage range and are IEEE-488 compatible. The Model 175A costs $495 and the Model 197A goes for $659. Both are available 4 weeks after receipt of order.

Keithley Instruments Inc., 28775 Aurora Rd., Cleveland, OH 44139; (800) 552-1115 or (216) 248-0400. CIRCLE 316

WIDEBAND METERS MEASURE POWER FACTOR

Dual displays allow a pair of digital power-factor/wattmeters to simultaneously track a circuit's true power or power factor and true-rms voltage or true-rms current levels. The 2111A has three voltage ranges (to 300 V) and nine power ranges (to 6000 W). The 2110A also features three voltage ranges (to 600 V) and nine power ranges (to 12,000 W). Both have three current ranges (to 20 A). The 2110A and 2111A are available from stock at an introductory price of $1795.

Valhalla Scientific, 9955 Mesa Rim Rd., San Diego, CA 92121; (800) 548-9806 or (619) 457-5576. CIRCLE 317

BIPOLAR POWER SUPPLIES SINK OR SOURCE CURRENT

The POW Series of single-output, bipolar power supplies can be used as variable-output power supplies or as power amplifiers with frequency characteristics to 35 kHz. Without switching polarity, users can continuously vary both gain and positive/negative voltage. Three voltage ranges are available: +70 to –70 V dc, with about 0 V or ground at +2 to –2 A; +35 to –35 V dc, with 0 V or ground at +1 to –1 A; and +35 to –35 V dc, with 0 V or ground at +5 to –5 A. Prices start at $925. Most units are available from stock.

Kikusui International Corp., 19601 Mariner Ave., Torrance, CA 90503; (213) 371-4662. CIRCLE 318

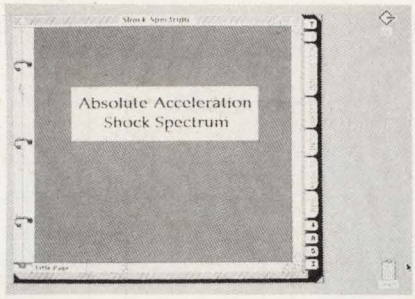
MATH SOFTWARE SOLVES SCIENTIFIC AND ENGINEERING PROBLEMS

The HiQ software system is a tool that solves engineering and scientific problems. It's intended for engineers, physical scientists, university educators, and students. Applications range from simple engineering problems, such as computing responses to suspension-bridge loading, to extremely complex projects like space-shuttle launches. In addition, HiQ is easy to learn and use.

The core of HiQ is a suite of mathematical algorithms covering over 500 functions. Using an icon-driven language called Q-Script, engineers can solve problems by generating high-level script functions that invoke various HiQ tools. Once the problem is solved, the HiQ package delivers interactive 2D and 3D graphical representations of the solution with the press of a button.

HiQ's programming language, called QScript, helps users construct tools. Users can also employ Problem Solvers to create tools. Problem Solvers are built-in procedures with a graphical interface that generate a script that solves a particular problem.

Solutions are automatically organized and presented in the desired format by a project notebook. The notebook function is updated throughout a project, and can be used as a final, compiled presentation.



The initial version of the HiQ software will run on Macintosh computers. It will be available in April for an introductory price of $495. After that, the list price will be $695. A Unix version, planned for June, will have the same graphical interface as the Macintosh version. It will cost $1495 for the introductory version and have a $1995 list price.

Bimillennium Corp., *101 Albright Way, Los Gatos, CA 95030; (408) 866-2010.* **CIRCLE 320**

■ *LISA MALINIAK*

NETWORK SOFTWARE MANAGES CONCURRENT ENGINEERING

TeamNet 2.0 is a software system that supports distributed, concurrent product development across heterogeneous networks. The software supplies designers and project managers with the real-time information and control they need to manage a concurrent design project. It synchronizes inputs from multiple disciplines, such as engineering, marketing, manufacturing, and testing, during all stages of the product life cycle.

The TeamNet 2.0 software is a Unix-based product that can be hosted on any Sun Microsystems workstation or server. TeamNet can transparently track product development using any tool on the network without modifying the tool. The tools may run on Unix-based systems, Macintosh systems, DOS- and OS/2-based PCs, and any computer that runs Sun Microsystems' Network File System. TeamNet plugs into the Unix virtual-file layer and gains access to information at the operating-system level.

The point-and-click user interface is the same across the entire range of supported systems. The graphical interface is based on the X-Windows and Motif standards.

A distributed, object-oriented database stores information on all files and directories managed by the system. The database performs four integrated functions: a distributed-project repository, configuration management, change management and version control, and a database query system for reports. In addition, TeamNet uses data compression so that large amounts of data are easily managed.

TeamNet 2.0 is available now. It costs between $100,000 and $175,000 for 50 to 100 seats. The price includes maintenance, training, and consulting services.

TeamOne Systems Inc., *2700 Augustine Dr., Santa Clara, CA 95054; (408) 986-9191.* **CIRCLE 321**

■ *LISA MALINIAK*

ASIC ANALYSIS TOOL PREDICTS POWER USAGE

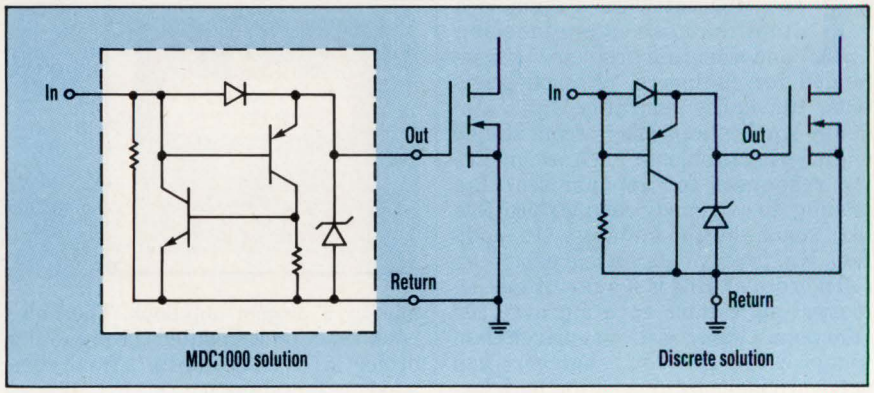
Powertool is an ASIC analysis tool that collects data to calculate dynamic and dc power consumption. It can be used to guide the placement of functional circuit blocks in the layout phase of ASIC design, and to calculate power consumption after the initial layout is complete. Powertool is driven by gate-level net lists and a stimulus file. Three ASCII data files are generated for power-consumption calculation. One file lists each cell's output in one column and total capacitance in another column. A second file lists all cells and their dc power dissipation. The third file lists the total number of transitions per net. Ikos Systems supports the libraries of twelve major ASIC vendors. They will incorporate the power information used in Powertool calculations into their libraries. The Powertool software is available now for a license fee of $20,000 per node.

Ikos Systems Inc., 145 N. Wolfe Rd., Sunnyvale, CA 94086; (408) 245-1900 **CIRCLE 322**

Low-Cost IC Protects DMOSFETs And IGBTs, And Turns Both Off Fast

Frank Goodenough

The gates of power MOSFETs and IGBTs look like capacitors that must be charged to between 5 and 10 V to turn them on, and discharged to turn them off. With high-speed active turn-off of FET gates becoming more vital, Motorola has developed a tiny low-cost IC, the MDC1000, that actively turns off n-channel power MOSFETs and IGBTs *(see the figure, left)*. The IC replaces a typical circuit of three discrete devices *(see the figure, right)*. A fourth component, a Zener diode typically used for overvoltage protection, is included in the IC.



The need for active turn-off is increasing because pulse-width-modulated (PWM) switching frequencies are getting higher while at the same time FETs are sporting larger die sizes. The higher PWM switching frequencies combined with the larger FET die sizes are resulting in larger FET gate capacitances to charge and discharge.

While parts cost for the discrete approach is about $0.70 per FET in 1000-unit quantities, the IC goes for a lower price in the same quantities. The SOT-23, TO-92, and SOT-223 go for $0.35, $0.40, and $0.70 each, respectively, in 1000-unit quantities. There's also the more subtle cost reduction of less board space per FET. Further savings accrue due to reduced purchasing, handling, and assembly costs, and even slightly less design time.

In the discrete solution, the 5-to-10-V positive-going PWM pulse is applied to the FET's gate through a diode, such as a 1N4148. Although the pulse is also applied to a small-signal pnp transistor, it's biased off by the voltage drop across the diode. The FET's gate capacitance charges to the peak voltage of the drive pulse minus the voltage drop across the diode.

When the drive pulse goes low to turn off the MOSFET, it back-biases the diode and the pnp transistor turns on, discharging the gate capacitance quickly through the transistor's low impedance. The Zener diode protects the gate from voltages above 10 V, which can occur when driven from the current source used in many applications.

The MDC1000's circuit is very similar to the discrete implementation of the turn-off function. Like the IC, PWM pulses applied to the IC's input pin drive the FET's gate through a diode; the emitter of a pnp transistor connects to the gate, and a protective 10.4-V Zener connects the FET's gate and source. However, an added npn transistor connects with the pnp to form a silicon controlled rectifier (SCR).

When the drive pulse is removed and the pnp transistor starts to conduct, the regenerative turn-on action of the SCR further speeds up the process of discharging the FET's gate capacitance.

When the residual charge on the gate is too small to provide holding current for the SCR, it turns itself off. At this point, the gate-to-source voltage has dropped below 1 V, well below the threshold voltage of most MOSFETs.

The MDC1000 can continuously supply up to 50 mA of charging current along with peaks of 500 mA (for 20 μs at a 2% duty cycle). Under test conditions, the IC typically discharges a 1000-pF capacitor from 9 V to 1 V in 15 ns, following a storage time of typically 60 ns. Even if it's discharging a 1-μF capacitor, the MDC1000's discharge time is less than 250 ns.

The MOSFET's turn-on time is a function of its input capacitance and the essentially constant current drive from the IC. While this current is a continuous maximum of 50 mA when operating with narrow pulses at low duty cycles, higher currents can be used to charge the capacitance faster. Power dissipation of the MDC1000 actually limits charging current.

The chip isn't limited to driving single, n-channel MOSFETs in switching power supplies. It can drive a FET used as the horizontal output transistor in a video monitor circuit.

Or a pair of MDC1000s can provide fast turn-off for the high-side switches in a full-bridge circuit controlling both the speed and direction of a dc motor. And MDC1000s can be driven by optoisolated level-shifters in high-side drive applications, like the control of three-phase brushless dc motors.

The MDC1000 is rated over an operating-temperature range of –65 to +150°C. However, current rating drops linearly to zero between 25 and 150°C. The MDC1000A, MDC1000B, and MDC1000C are available in TO-92, SOT-23, and SOT-223 packages, respectively.

Motorola Inc., Z301, 5005 E. Mc Dowell Rd., Phoenix, AZ 85008; Mike Lissy (602) 244-5504. **CIRCLE 323**

GaAs Chip Family Drives UHF Communications

A family of GaAs MMICs from Oki Semiconductor covers a range of portable UHF communications applications. Eight parts with KGF prefixes come in 4-pin minimold packages. The unit prices given for all devices are for quantities of 10,000 pieces, and device specifications are for 850-MHz operation.

The KGF-1145 dual-gate buffer amplifier ($1.32) has a 3-dB noise figure, a 2-dBm power output, and draws 4 mA. The KGF-1146 2-stage buffer amplifier ($1.40) has a 4.2-dBm power output, a 2-dB gain, and operates on 2.5 mA. With a noise figure of 3 dB, the KGF-1155 dual-gate mixer amplifier ($1.32) has a gain of 12 dB and runs on 2.5 mA. The KGF-1165 feedback wideband amplifier ($1.40) offers a 4-dB noise figure, a 7-dBm output, and draws under 25 mA of current.

For front-end applications, the KGF-1175 dual-gate head amplifier ($1.40) has a 2-dB noise figure, a 3-dBm power output, and a 2.5-mA operating current. The KGF-1255 single-gate driver amplifier ($1.40) has a 2.5-dB noise figure, a 17-dBm power output, and draws 80 mA. The KGF-1254 amplifier ($1.40) delivers 20 dBm minimum with a gain of 13 dB while operating on 80 mA. Running on 40 mA, the KGF-1256 medium power amplifier ($1.40) has a 15-dBm minimum power output and a 13-dB gain.

The KGA-1305 single-gate power amplifier ($9.82) is available in a 4-pin ceramic package. Also available in chip form, it has a 31.5-dBm output and runs on 400 mA. The family's digital part is the KGL-2115 two-modulus prescaler ($3.08). Housed in an 8-pin flat pack, this device draws 6 mA of current, has a toggle frequency of 0.7 to 1.0 GHz, dividing ratios of 1/128 and 1/129, and operates over a temperature range that spans –30 to +85 C.

Oki Semiconductor, *785 N. Mary Ave., Sunnyvale, CA 94086-2909; Jerry Gora, (408) 737-6361.*

CIRCLE 324

■ *MILT LEONARD*

VME Board Emulates Military Peripherals

The Hawke circuit board offers a 32-bit interface between VME bus systems and Navy Tactical Data System (NTDS) computers. With on-board 1 Mbyte of user EPROM, the board can emulate costly peripheral devices, such as reel-to-reel magnetic-tape drives, teletypes, and paper-tape readers and punches.

Supporting VME revision C (IEEE standard P1014), the board occupies one 6U-size slot and includes a 512-kbyte triple-ported RAM that connects the resident 68020 microprocessor to the VME bus and the host NTDS system. The Hawke circuit board also has a 7-level vectored interrupt handler, a real-time clock circuit, and a built-in test feature.

The front panel of the Hawke circuit board has LEDs that indicate handshake-line status, and a hexadecimal display that indicates board-address and system status. Priced at $4295 each, the Hawke circuit board is available from stock to four weeks.

Sabtech Industries Inc., 5411 E. La Palma Ave., Anaheim, CA 92807; (714) 970-5311. CIRCLE 325

Ethernet Transceiver Targets Bipolar ICs

A CMOS Ethernet/Cheapernet transceiver for 10Base-5 or 10Base-2 LAN media runs on 30% less current than bipolar 8392 bipolar devices. The 83C92A from Seeq Technology is a pin-for-pin replacement for the bipolar part and draws 120 mA.

Combining the transceiver with prior members of the chip set, Seeq's 8005 data-link controller and 8023 Manchester-code converter reduce by half the number of support chips required by other solutions. A complete Ethernet circuit node needs just nine devices to operate.

The 83C92A is available in a 16-pin DIP and a 28-pin plastic leaded chip carrier. Samples are available now, and production quantities are scheduled to be available for the first quarter 1991. Unit pricing will be from $10 to $11. Crystal Semiconductor second-sources Seeq's Ethernet chips.

Seeq Technology Inc., 1849 Fortune Dr., San Jose, CA 95131; (408) 432-7400.

Crystal Semiconductor Corp., 4210 S. Industrial Dr., Austin, TX; (512) 445-7222. CIRCLE 326

Ethernet Controller Drops Parts Count

An Ethernet controller, a buffer-management unit, and a 10-Mbit/s Manchester encoder-decoder are combined in the MB86960 NICE device. When used with Fujitsu's MBL8392A coaxial transceiver or its forthcoming MB86962 10BASE-T transceiver, the device gives local-area-network designers a two-chip Ethernet system. Key features of the MB86960 device are a data-bus transfer rate of 20 Mbytes/s, configurable transmit and receive buffers, address filtering, and a low-power standby mode.

The device is available in 100-pin plastic quad flat packages and will be priced to start at about $25 in low volumes. Samples are available now; volume production is scheduled for the first quarter of 1991.

Fujitsu Microelectronics Inc., Advanced Products Div., 50 Rio Robles, San Jose, CA 95134-1806; (408) 922-9000. CIRCLE 327

8-×-8 VIDEO SWITCH BUFFERS ALL 8 OUTPUT CHANNELS

Under the aegis of a host processor, Maxim's 8-×-8 video crosspoint switch, the MAX456, connects any combination of its 8 video inputs to any combination of its 8 video outputs. Applications include studio equipment, plus video-surveillance, automated-visual-assembly and inspection, and medical-imaging systems.

The switch matrix consists of 64 make-before-break "contacts," each built from 3 MOS analog switches connected in a T-configuration. Between the matrix and each output pin lies a unity-gain buffer amplifier. True op amps, the switches slew at 250 V/μs and sport a minimum 3-dB bandwidth of 25 MHz. These specifications hold while putting 2 V pk-pk across internal 400-Ω dynamic loads. When an output isn't selected, the output pin looks like a high impedance, letting multiple MAX456s be paralleled to form larger switching networks. The host can choose any one of three methods to set up the matrix: a 7-bit parallel word, a 7-bit serial word, or a 32-bit serial word.

At 5 MHz, maximum single-channel crosstalk is 60 dB, typical all-channel crosstalk is 57 dB, and typical all-channel off isolation is 80 dB. Differential phase and gain error at 3.58 MHz typically run 1.5 and 0.5%, respectively. With all buffers on, the IC draws 45 mA maximum from ±5 V. With all buffers off, supply current drops to 2 mA. The chip also has a power-on reset (POR) that remains low for 5 μs when power is applied—or if the total supply voltage drops below 4 V. In the serial interface modes, POR clears all address and data latches and disables all buffer outputs at power-up. Packages include 40-pin plastic and ceramic DIPs, and 44-pin PLCCs. The MAX456, in quantities of 1000, starts at $19.97 each.

Maxim Integrated Products Inc., *120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600.* **CIRCLE 328**

■ *FRANK GOODENOUGH*

DG201 ANALOG QUAD SWITCH GETS BETTER

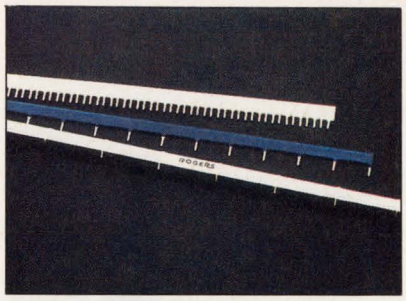
The LTC201A is an improved, drop-in version of the multiply-sourced, industry workhorse DG201 analog quad switch. This quad single-pole, single-throw CMOS switch draws 1/500 as much quiescent current as earlier versions (40 μA vs. 2 mA) and operates from a single 5-V supply (vs. ±15-V rails). The signal voltage can equal the supply rails. Make-before-break switching is guaranteed. On-resistance is 110 rather than 175 Ω. Charge injection, critical for sampling amplifiers, is typically 2 pC and a maximum of 25 pC; that of the standard device typically runs 25 pC and 100 pC maximum. The switch comes in 16-pin ceramic and plastic DIPs and 16-pin SOICs. Pricing in 100s starts at $3.45 each.

Linear Technology Corp. 1630 McCarthy Blvd., Milpitas, CA 95035-7487; (800) 637-5545. **CIRCLE 329**

ELECTRONIC DESIGN

DIRECT CONNECTION ADS

New Products/Services Presented By The Manufacturer.
To Advertise, Call JEANIE GRIFFIN At 201/393-6080



SAVE SPACE WITH MINI/BUS® BARS

- Improve power distribution
- Reduce required board layers
- Eliminate up to half the decoupling capacitors
- Fit between or beneath IC's
- Also available in surface mount

Send for Rogers Mini/Bus® Bars Application Bulletin.

ROGERS CORP., 2400 S. Roosevelt St.
Tempe, AZ 85282 602/967-0624

MINI/BUS®BARS CIRCLE 256

AT BUS DESIGN

At last, here is the **timing book** for the XT and AT Bus. Detailed text, tables and diagrams tell you what each signal line is for, what it does and when it does it. All the information is compatible with the IEEE P996 Specification for the **ISA** (AT) Bus. In addition, the 8 and 16 bit parts of the **EISA** Bus are included. **AT Bus Design,** by Ed Solari, has over 200 pages, with more than 100 figures and tables. Handy 7" x 9" format, soft cover, $69.95.

FREE We'll include a free copy of the pocket-sized **XT-AT Handbook by Choisser and Foster** with each AT Bus Design book if you tell us where you saw this ad. Of course, this $9.95 value is also available by itself. Or buy five or more for only $5.00 each.

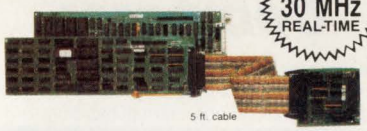
VISA 800-462-1042 MasterCard
619-271-9526

Annabooks
12145 Alta Carmel Ct., Suite 250
San Diego, CA 92128
FAX 619-592-0061
Money-back guarantee

ANNABOOKS CIRCLE 264

☆ ☆ ☆ ☆ *"The Best 8051 Emulator"*

NEW 30 MHz REAL-TIME



8051 *SEE EEM 90/91 PAGES D 1320-1323*

PC based emulators for the 8051 family

8031, 8032, 8051, 8052, 80C152/154/321/451/452/51FA/51GB/515/517/535/537/552/562/652/851, 80532, 83C451/552/652/751/752/851, 8344, 87C451/552/751/752, 8751, 8752, DS5000 + CMOS . . . more.

- PC plug-in boards or RS-232 box.
- Up to 30 MHz real-time emulation.
- Full Source-level Debugger w/*complete* C-variable support.
- 48 bit wide, 16K deep trace, with "source line trace."
- "Bond-out" pods for 8051, 83C552, 83C451, 83C652, 83C751, 80C515/80C517, 83C752.

Prices: 32K Emulator 8031 $1790; 4K Trace $1495*

CALL OR WRITE FOR FREE DEMO DISK!
Ask about our demo VIDEO

nohau CORPORATION
51 E. Campbell Avenue
Campbell, CA 95008
FAX (408) 378-7869
(408) 866-1820
*US only

NOHAU CIRCLE 258

NEW, POWERFUL, UNIVERSAL

PILOT-U40 is our second generation 40-pin universal programmer, following the very successful and popular Sailor-PAL line of programmers. Programs PALs, GALs, PROMs, E/EPROMs, micros, AMD MACH-110, etc, etc. 28-pin and 32-pin versions also available. Industrial quality. $1,095 to $2,495. Satisfaction guaranteed.

408-243-7000, 800-627-2456, Fax 408-736-2503

ADVIN SYSTEMS INC.
1050-L E. Duane Ave., Sunnyvale, CA 94086

ADVIN SYSTEMS CIRCLE 253

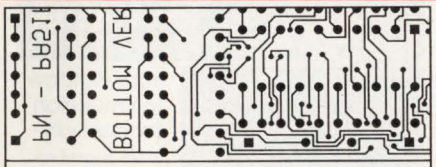
'488 CONTROL FOR YOUR MACINTOSH II

- Control any instrument in minutes.
- Supports BASIC, Pascal, C and Hypertalk.
- HyperCard utilities included.
- Software library. Risk free guarantee.

cec Capital Equipment Corp.
Burlington, MA. 01803

Informative catalog 800-234-4232
Applications help (617) 273-1818

CAPITAL EQUIPMENT CIRCLE 272



GerberJet V1.2 $199
NEW! Multilayer and Preview

Plot Gerber data files on HP LaserJet-II compatible printers at 300 dots per inch. With GerberJet you will be sure your files are correct **BEFORE EXPENSIVE PHOTOPLOTTING.**

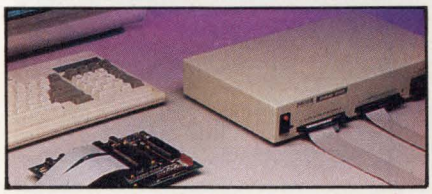
- ☐ Multi-layer- positive/negative overlays.
- ☐ Preview- VGA display of page before printing.
- ☐ Auto Scaling- shrink to fit on one page.
- ☐ Auto Tiling- large plots on several pages.
- ☐ EMS support- plots fast.
- ☐ Plot AT card on one legal size sheet.
- ☐ 260 Apertures per layer.
- ☐ **Free demo on BBS, download GJD.EXE**

CALL (315) 478-0722 FAX (315) 475-8460
BBS (315) 471-3961 (2400/1200,8,N,1)
Logical Systems Corporation
P.O. Box 6184, Syracuse, NY 13217 USA

LOGICAL SYSTEMS CIRCLE 263

How To Get More Emulation for Less

ORION 8620 ANALYZER-EMULATOR



■ High-Level language/Symbolic debug support ■ Over 170 processors supported with the same base hardware and software environment ■ Easy-to-use, powerful triggering ■ Extensive MACRO capabilities ■ Program Performance Analyzer ■ Built-In EPROM programmer

Go ahead and compare. The 8620 Analyzer-Emulator gets your product to market faster and costs less. Base prices start at $5080. Send for more information and free demo disk.

Toll Free 800/729/7700 or 415/327/8800

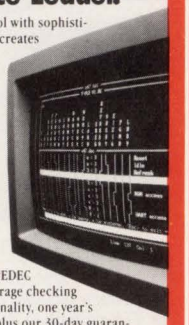
ORION INSTRUMENTS

180 Independence Dr., Menlo Park, CA 94025

ORION INSTRUMENTS CIRCLE 278

Tango-PLD. The New Price/Performance Leader.

Tango-PLD, a universal PLD design tool with sophisticated features at an affordable price, creates complex designs with multiple PALs and GALs. Our top-down approach, emphasizing logic description first and part selection second, along with a "C-like" design language, makes Tango-PLD easy to use.



Tango™

Describe designs with Boolean equations, truth tables, state machines, high-level C expressions, or existing JEDEC files. Simulation with test-vector coverage checking guarantees no surprises. Rich functionality, one year's updates, free tech support and BBS, plus our 30-day guarantee. All this for **just $495**. Call today.

Now with Schematic Entry

FREE EVALUATION PACKAGE
800 433-7801 619 554-1000 619 554-1019 Fax

ACCEL™ Technologies ■ 6825 Flanders Drive ■ San Diego, CA 92121 USA
International prices may vary. Contact us for the distributor nearest you.

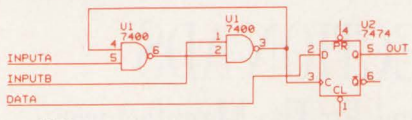
ACCEL TECHNOLOGIES **CIRCLE 290**

FREE Demo Disk

SCHEMA III

MOST POWER OF ANY PC SCHEMATIC CAPTURE PACKAGE

Unlimited hierarchies, ASCII input, 7000+ unique parts, library customization, user defined manager, color selections, online HELP, many netlist formats, TIFF, AutoCAD block, & PostScript outputs and much more!
ONLY $495



SCHEMA FROM OMATION

1-800-553-9119

Free 800 Support
30 Day Guarantee

FAX: (214)783-9072 BBS# (214) 231-135X

OMATION **CIRCLE 285**

CHIPSAFE™

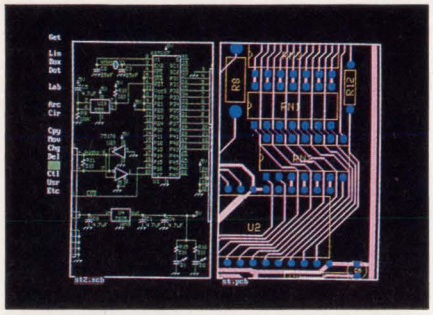
For Safely Storing, Organizing, Archiving and Transporting Your IC Components

Our handsome, Crushproof, Dust-Tight, Snap-fastened IC Storage albums with ESD protection are the perfect solution for physically and electrically protecting your library of IC MASTERS, MODS, REVS and samples. In stock for immediate delivery.

Product	Model	Size	Chip Capacity (DIP) 8 pin	16 pin	28 pin	40 pin	Features	Prices (1-4)
ChipSafe™	100	7" x 10"	528	264	76	56	Maximum IC storage	$ 16.95
ChipStore™	200	7" x 10"	264	132	38	28	Combination IC & diskette storage	$ 16.95
			5	5 1/4" diskettes				
ChipCarry™	300	5" x 6"	120	70	19	12	Briefcase size IC storage	$ 12.95
ChipPocket™	400	3" x 4"	25	26	7	5	Shirt pocket size	$ 6.95

*i*TOI ENTERPRISES P.O. Box 59, Newton Highlands, MA 02161
TEL: (617) 332-1010

iTOI **CIRCLE 292**



NEW SCHEMATIC AND PCB SOFTWARE

With support for extended and expanded memory, HiWIRE II can handle your most demanding schematic and PCB designs quickly and easily. The unique HiWIRE editor allows you to display and edit schematics and PCBs simultaneously, using the same commands for each. HiWIRE II is $995, and is guaranteed.

WINTEK CORPORATION,
1801 South Street, Lafayette, IN 47904
(800) 742-6809 or (317) 448-1903

WINTEK **CIRCLE 282**

C for the 8051 Compare:

Benchmark Results—Sample program: Eratosthenes Sieve Program from BYTE (1/83), expanded with I/O and interrupt handling.

	FRANKLIN SOFTWARE C-51 v2.1	MCC51 v1.2	Archimedes ICC51 v2.20A
Linkage time	*6 sec*	*9*	*29*
Execution time	*0.88 sec*	*9.00*	*11.45*
Total code size	*1726 bytes*	*3798*	*5318*
Compilation time	*17 sec*	*18*	*12*
Sieve module size	*541 bytes*	*1021*	*736*

Call now for your free DEMO disk.

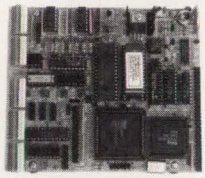
FRANKLIN SOFTWARE, INC.

888 Saratoga Ave. #2 • San Jose, CA 95129
(408) 296-*8051* • FAX (408) 296-8061

FRANKLIN SOFTWARE **CIRCLE 260**

Little Giant™

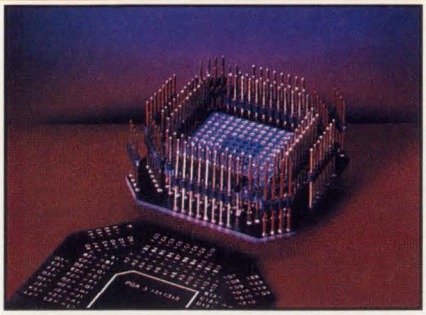
C Programmable Controller



This shirt pocket sized computer interfaces directly to the outside world. Use it to control anything. Instantly programmable using your PC with Dynamic C. ROM and battery backed RAM to 1024k bytes. 8 Channel, 10/12 bit, A/D with conditioning. High voltage and current drivers. Battery backed time and date clock. Watchdog and power fail. 4 serial channels. 24 parallel I/O lines. Timers. Integral power supply. Terminations for field wiring. Expansion connector. Plastic or metal field packaging available. OEM versions from $199.00.

Z-World Engineering
1340 Covell Blvd., Davis, CA 95616
(916) 753-3722
Fax: (916) 753-5141

Z-WORLD ENGINEERING **CIRCLE 291**



Complete Line of Debug Tools

- **Famous Bug Katcher™ makes it easy to attach test leads to ICs in LCC, PLCC, PGA, PQFP, and DIP packages.**
- **Eliminates need for noisy cables; reduces capacitance and inductance in your test set-up.**
- **You can also quickly isolate and reconnect sections of your socketed IC with our Bug Isolator.™ (All packages.)**
- **Quick turnaround on custom engineering services, if needed. For a free catalog, contact:**

Emulation Technology, Inc.
2368-B Walsh Ave. Santa Clara, CA 95051
Phone: 408-982-0660 FAX: 408-982-0664

EMULATION TECH **CIRCLE 293**

NEW! **iceMASTER** 8051 68HC11

Your Window to Emulation Productivity

- **Easy to learn & use**
- **Windowed interface – user configurable**
- **FAST! Download – < 3 sec. typ. at 115KB**
- **Source Level debug**

- **A 4K frame trace buffer** with advanced searching capabilities.
- **Hyperlinked On-line help** guides you through the emulation process.
- **Best Performance Analyzer** in the industry.
- **iceMASTER** connects easily to your PC, requires no disassembly, or expansion slots. Works on any PC (DOS or OS/2), MicroChannel or EISA. Even laptops!
- **Supports more than 50 different 8051 family derivatives.** M68HC11 support will be available early in 1991.
- **Try iceMASTER risk free!** Satisfaction Guaranteed or return for a full refund!*
- **RENTALS AVAILABLE!** Ideal for consultants and researchers!
- **Call today for free demo disk and ask about a free 8051 Macro Assembler! (800)638-2423**

MetaLink Corporation

FREE ASSEMBLER

MetaLink Corporation P.O. Box 1329 Chandler, AZ 85244-1329
(602) 926-0797 FAX (602)926-1198 TELEX 4998050MTLNK

METALINK **CIRCLE 265**

RELIABILITY PREDICTION SOFTWARE

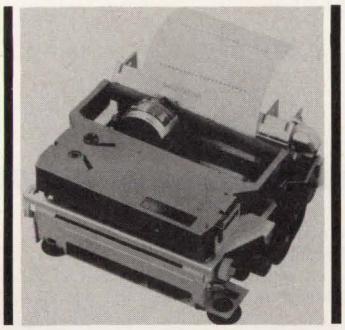
ARE YOUR PRODUCTS RELIABLE?

The RelCalc 2 Software Package predicts the reliability of your system using the part stress procedure of MIL-HDBK-217E, and runs on the IBM PC and full compatibles. Say goodbye to tedious, time consuming, and error prone manual methods! RelCalc 2 is very easy to use, and features menu windows, library functions, global editing for what-if? trials, and clear report formats. Try our Demo Package for $25.

T-CUBED SYSTEMS, 31220 La Baya Drive # 110, Westlake Village, CA 91362. (818) 991-0057 • FAX: (818) 991-1281

T-CUBED SYSTEMS **CIRCLE 286**

DIRECT CONNECTION ADS

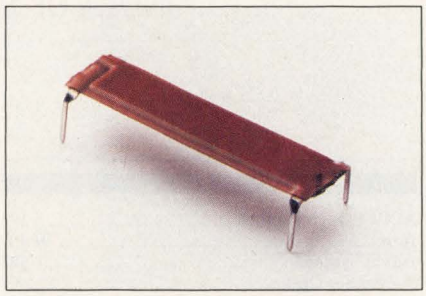


PRINTERS WITH IMPACT

Citizen dot matrix impact printer mechanisms provide for the perfect low-cost solution for point-of-sale, data logging, etc. Avail. in 23, 28 or 40 columns, serial or parallel, w/sprocket feed, auto-cutter & journal winder options. Fast (120 cps) & reliable (over 50 million char. head life). Also avail. in stand-alone versions.

MELFESS FIVE, INC.
12304 Santa Monica Blvd., #121, Los Angeles
CA 90025, 800/533-2297

MELFESS FIVE — CIRCLE 262



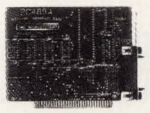
SIMPLIFY BOARD LAYOUT

MICRO/Q 1000 ceramic decoupling capacitors share board mounting holes with IC pins to simplify board design. Now add more active devices with increased density in the same space, or design the same package on a smaller board.

Send for your free information.

ROGERS CORPORATION
2400 S. Roosevelt St.
Tempe, AZ 85282. Phone: (602) 967-0624

ROGERS CORP. — CIRCLE 289



LOW COST INTERFACE CARDS FOR PC/XT/AT

RS-485/422 Card [PC485] $95/125
- Serial Async. Communication up to 4,000ft; 2 or 4 wires; NS16450 UART;
- COM1-4; Max. Baud Rate 56KB. **High speed version (256KB) - $165.**
- **Dual drivers/receivers;Handles 64 devices;**Compatible with most comm. S/W.
- DB9 or phonejack. **Sample programs included.**Optional S/W (w/ source)-$150

IEEE-488 Card [PC488A] $145
- Includes **DOS Device Driver** and sample Communication program in **BASIC.**
- Additional sample programs in **C, Pascal & Assembly - $50.**
- **Selectable IRQ (1-6). DMA** channel 1 or **2.** Up to **four boards** per computer.
- Compatible with most **IEEE-488 Software packages** for IBM-PC.
- I/O Addresses and Control registers compatible with **NI's GPIB-PCIIA.**

IEEE- 488 Card [PC488C] With Built-In Bus Analyzer $445
- Software Support for BASICA, QuickBASIC and GWBASIC.
- Additional libraries for **C, Pascal, FORTRAN, Assembly** available - **$50 (all)**
- **Powerful menu-driven BUS ANALYZER** runs in the background while 488 programs or commands are executed; Features **Program Stepping, Break points,** real time **bus data capture** (4K buffer), **instant screen toggling.**
- **Complete Controller / Talker / Listener** capability. Based on NEC-7210.
- Compatible with **NI's GPIB-PCII** card. **(TMS-9914** based card - **$345).**

Stepper Motor Card [PCL738] $395
- Capable of independent and simultaneous control of up to 3 **stepper motors.**
- **Programmable speed** from **3.3 PPS** to **3410 PPS;** Built-in acceleration control.
- Step Position Read-back; **Opto-isolated outputs;** Crystal based timing.
- **Pulse/Direction** or CW/CCW pulse output. Includes **8 bit digital I/O port.**

MC / VISA / AMEX *Call today for datasheets!*

B&C MICROSYSTEMS INC.
750 N. Pastoria Ave., Sunnyvale, CA 94086 USA
TEL: (408)730-5511 FAX: (408)730-5521

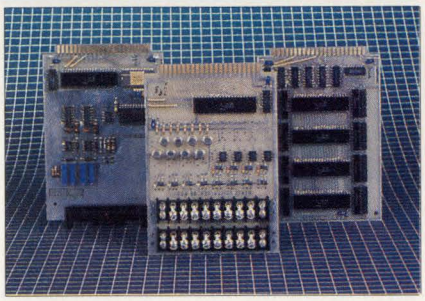
B&C MICROSYSTEMS — CIRCLE 274

FREE! 120 Page Catalog

"Optics for Industry"

ROLYN OPTICS supplies all types of "Off-the-Shelf" optical components. Lenses, prisms, mirrors, irises, microscope objectives & eyepieces plus hundreds of others. All from stock. Rolyn also supplies custom products & coatings in prototype or production quantities. Write or call for our free 120 page catalog describing products & listing off-the-shelf prices. **ROLYN OPTICS CO.**, 706 Arrowgrand Circle, Covina, CA 91722, (818) 915-5707 & (818) 915-5717. TELEX: 67-0380. FAX: (818) 915-1379.

ROLYN OPTICS — CIRCLE 284

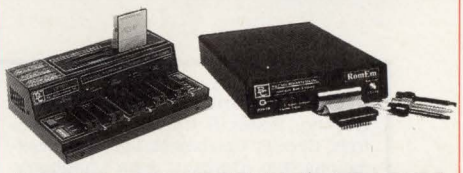


6800/6809 MICRO MODULES.

OEM 6800/6809 MICRO COMPUTER MODULES for dedicated control and monitoring. Interfaces for sensors, transducers, analog signals, solenoids, relays lamps, pumps, motors, keyboards, displays, IEEE-488, Serial I/O, floppy disks.

WINTEK CORPORATION,
1801 South Street. Lafayette, IN 47904-2993.
(317) 742-8428 or (800) 742-6809

MICRO MODULES — CIRCLE 259



RS232 EE/EPROM, MICRO & MEMORY CARD PROGRAMMER $345/495

- Programs **EE/EProms, Flash Eproms, ZPRams, Intel Micros, Memory Cards.**
- **Stand-Alone Mode** for EE/EProms and Memory Card Duplication / Verify.
- All 24/28/32 pin EE/EProms to **8 MBits** (upgradeable to **32 Megabits**). Micros:8741/A,-2/A,-4,-8,-9,-51,-C51,-C51FA/B,-52,-53,-55,-C521,-C541,9761.
- Accepts dedicated modules: **Memory Card Programming Module** (Seiko, Fujitsu) - $145, **Eraser/Timer Module** - $50, **Gang Module** (4 sockets) - $145. Simultaneously duplicates up to 5 devices in stand-alone mode (with Gang).
- Can be operated with any computer containing an **RS-232 serial port.**
- **User friendly Menu-Driven Interface Program for IBM-PC** or **Macintosh.**
- **Full 1 year warranty.** Customer support via voice line, fax or **dedicated BBS.**

INTELLIGENT ROM EMULATOR $395

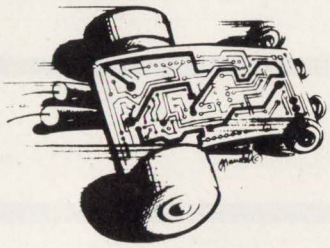
- Emulates **2716** through **27512** EProms with a single unit. **Access time 120ns.**
- Connects to the **standard parallel printer port** via a standard printer cable.
- User friendly software. Command set includes: **Load**(data), **Write**(data), **Display**(memory),**Type**(of EProm),**Edit**(memory),**Fill**(memory),**Calculator, Reset**(target system),**Activate**(debugging feature),**Monitor**(selected feature).
- **Address Compare with Halt output, Address Snapshot, Trigger input.**
- **Fast data loading via parallel printer port (64k bytes in less than 10 sec).**
- **Cascadable up to 8 units.**Includes target cable with Trigger/Reset/Halt clips.
- CMOS (stand-alone) model with rechargeable NiCad battery backup: **$495**

MC / VISA / AMEX *Call today for datasheets!*

B&C MICROSYSTEMS INC.
750 N. Pastoria Ave., Sunnyvale, CA 94086 USA
TEL:(408)730-5511 FAX: (408)730-5521

B&C MICROSYSTEMS — CIRCLE 275

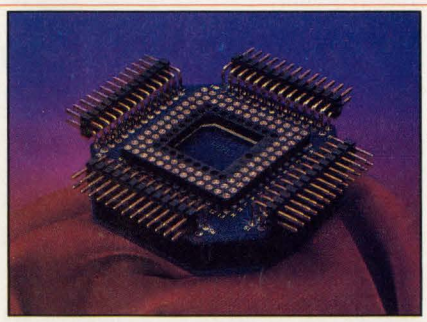
FASTEST PCB PROTOTYPE!



$199 Investment
One day turn In-house

With the **Fast-Proto PCB Kit**, your CAD system and pen plotter, you can prototype PCB's and avoid delays of photoplotting and vendor fabrications. This new process offers a fast and reliable alternative to costly quick-turn prototypes.

For more information call, FAX or write:
GENERAL CONSULTING
12856 Inglewood Avenue
Hawthorne, CA 90250
(213) 679-1405 FAX (213) 679-2995



Full Line of PQFP Adapters

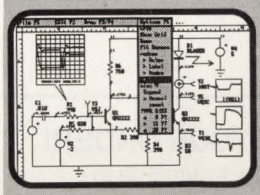
- At the prototyping stage, use a PQFP Adapt-A-Board.™ Extends leads for easy wire wrapping.
- For emulation, use an Adapt-A-Pod,™ like the one shown here for an 80386 PQFP package. Just plug and play.
- For production testing, a Bug Katcher™ turns your PQFP into an IC so you can start testing—ASAP.
- We stock all types of PQFP adapters. Quick turnaround on custom orders. Free catalog.

Emulation Technology, Inc.
2368-B Walsh Ave. Santa Clara, CA 95051
Phone: 408-982-0660 FAX: 408-982-0664

EMULATION TECH — CIRCLE 280

Analog Circuit Simulation

Completely Integrated CAE from $95



From Schematic Entry through SPICE Simulation to Post Processing

IsSPICE $95, the complete SPICE program, runs on all PC's.

IsSPICE/386 $386, The fastest PC based SPICE program available. Has virtually no circuit size limitations.

SPICENET $295, a schematic editor for any SPICE simulator. Generates a complete SPICE netlist.

INTUSCOPE $250, a graphics post processor that performs all the functions of a digital oscilloscope.

PRESPICE $200, extensive model libraries, Monte Carlo analysis, and parameter sweeping.

Please Write or Call
P.O. Box 6607 (213) 833-0710
San Pedro, CA 30 Day Money
90734-6607 Back Guarantee

intusoft

INTUSOFT — CIRCLE 261

CLASSIFIEDS

COMPUTER SOFTWARE

EMPLOYMENT OPPORTUNITIES

BUSINESS SERVICES

INDEX OF ADVERTISERS

The advertisers index is prepared as an extra service. Electronic Design does not assume any liability for omissions or errors.

incredible!

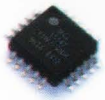
SPDT switch dc to 5GHz with built-in driver

Truly incredible...a superfast 3nsec GaAs SPDT reflective switch with a built-in driver for only $19.95. So why bother designing and building a driver interface to further complicate your subsystem and take added space when you can specify Mini-Circuits' YSW-2-50DR?

Check the outstanding performance specs of the rugged device, housed in a tiny plastic case, over a -55° to +85° C span. Unit-to-unit repeatability for insertion loss is 3-sigma guaranteed, which means less than 15 of a 10,000-unit production run will come close to the spec limit. Available for immediate delivery in tape-and-reel format for automatic placement equipment.

SPECIFICATIONS
YSW-2-50DR

	dc-500MHz	500-2000MHz	2000-5000MHz
Insertion loss, typ (dB)	0.9	1.3	1.4
Isolation, typ(dB)*	50	40	28
1dB compression, typ (dBm @ in port)	20	20	24
RF input, max dBm (no damage)	22	22	26
VSWR (on), typ		1.4	
Video breakthrough to RF, typ (mV p-p)		30	
Rise/Fall time, typ (nsec)		3.0	



*typ isolation at 5MHz is 80dB and decreases 5dB/octave from 5-1000 MHz

finding new ways...
setting higher standards

Mini-Circuits WE ACCEPT AMERICAN EXPRESS

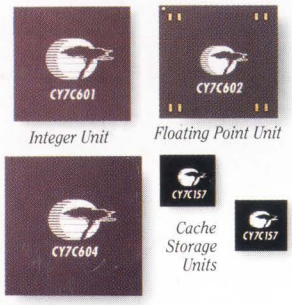
P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500 Fax (718) 332-4661 Telexes: 6852844 or 620156

CIRCLE 134

THE SPARC OF A NEW GENERATION.

A new generation of performance.

The new SPARCstation™2 from Sun Microsystems delivers almost twice the CPU performance of previous generations – the highest performance in its class.



Integer Unit *Floating Point Unit*

Cache Storage Units

Cache Controller and Memory Management Unit

The complete SPARC chipset, designed by our ROSS Technology subsidiary, is now available for high-volume applications.

The reason for this blazing speed: The highest-performance CMOS SPARC® available. The CY7C601, 32-bit SPARC microprocessor and CY7C157 16K x 16 Cache Storage Units from Cypress Semiconductor. Cypress 0.8 micron CMOS gives the CY7C601 SPARC RISC microprocessor 40 MHz clock rates and a sustained throughput of 29 MIPS.

Next generation compatibility.

Because they're SPARC chips, they're completely compatible with over 2100 SPARCware™ products. They offer true scalability into a wide spectrum of applications. And a growth path for future high-performance products.

Get this level of performance, potential, and compatibility for your next-generation products.

The Cypress SPARC.

For the whole story on RISC, call the Cypress Hotline at 1-800-952-6300.* Ask for dept. C3M.

CYPRESS SEMICONDUCTOR