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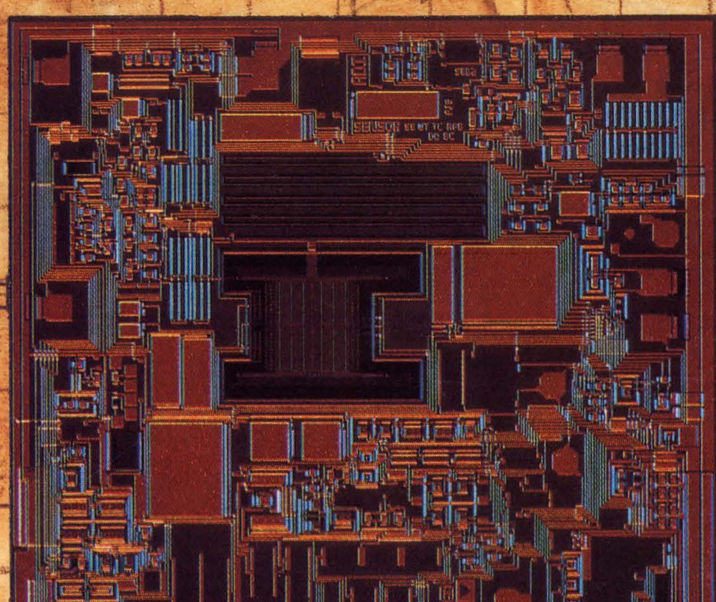

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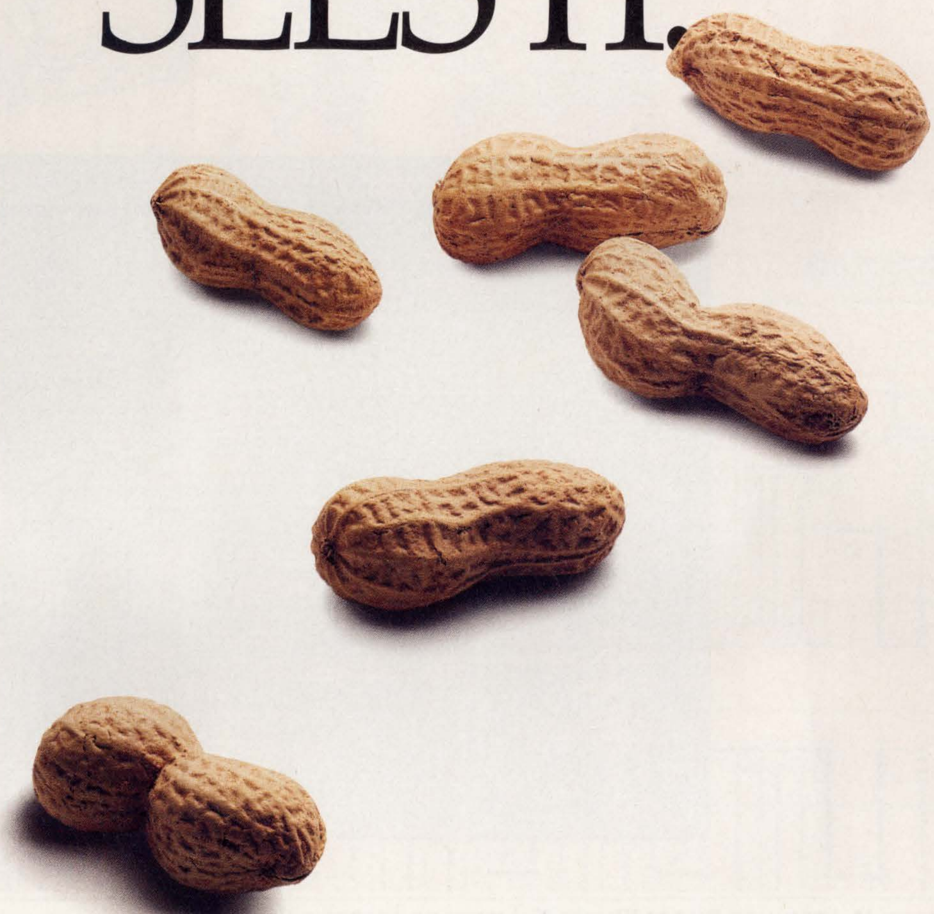

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MOTOROLA

AUGUST 8, 1991 VOL. 39, NO. 15

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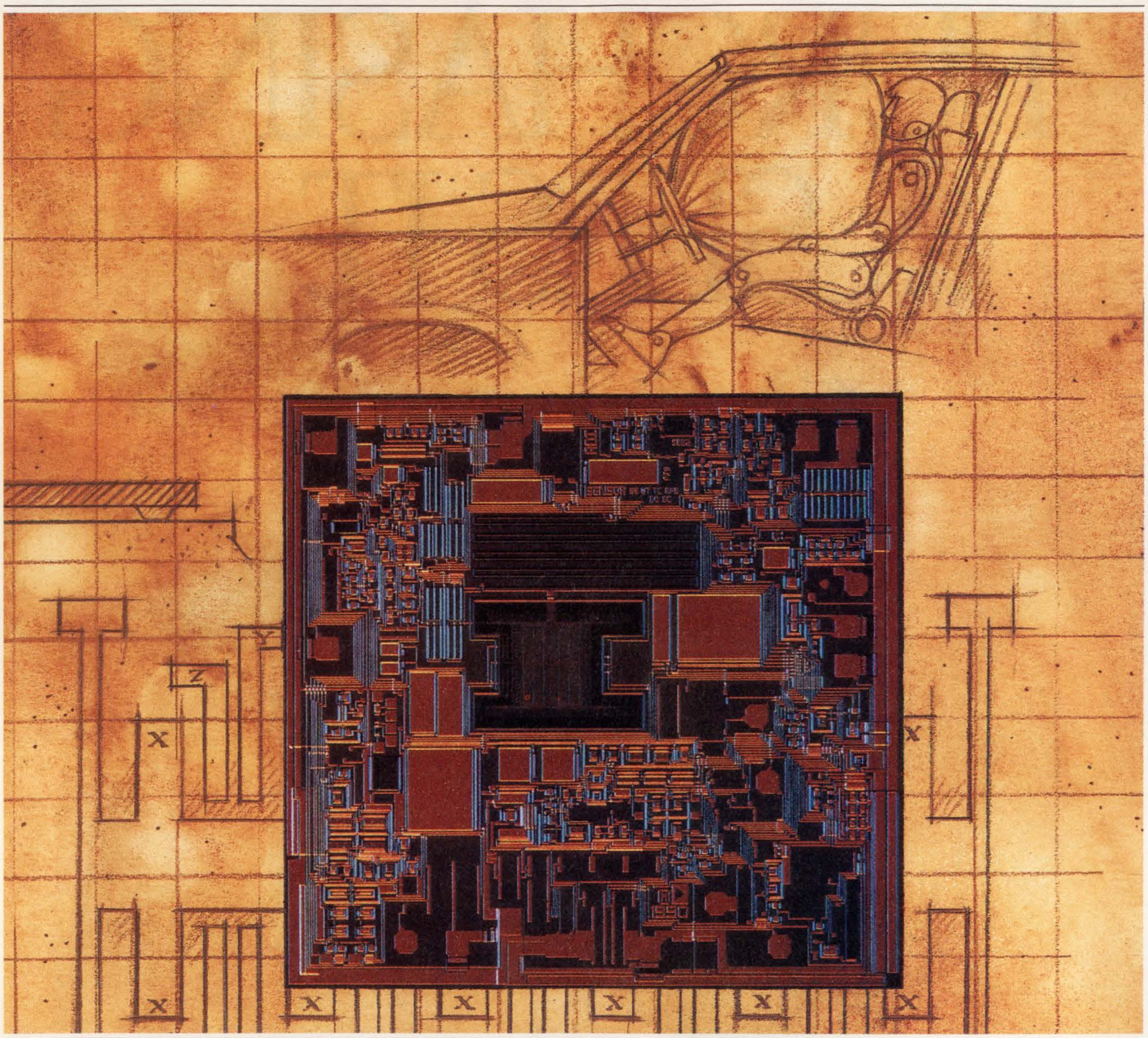

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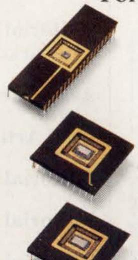

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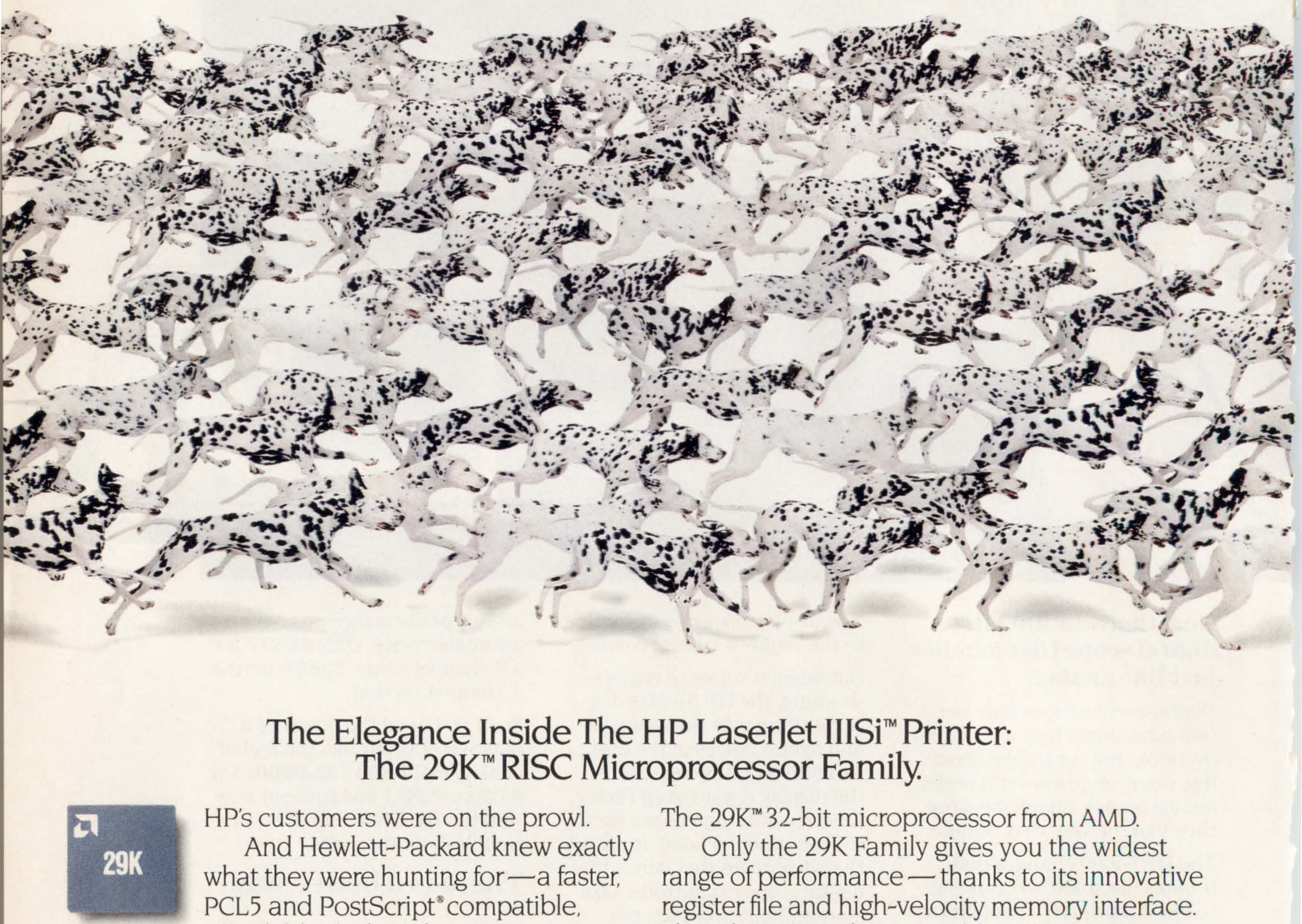
How AMD Keep Up With



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EDITORIAL

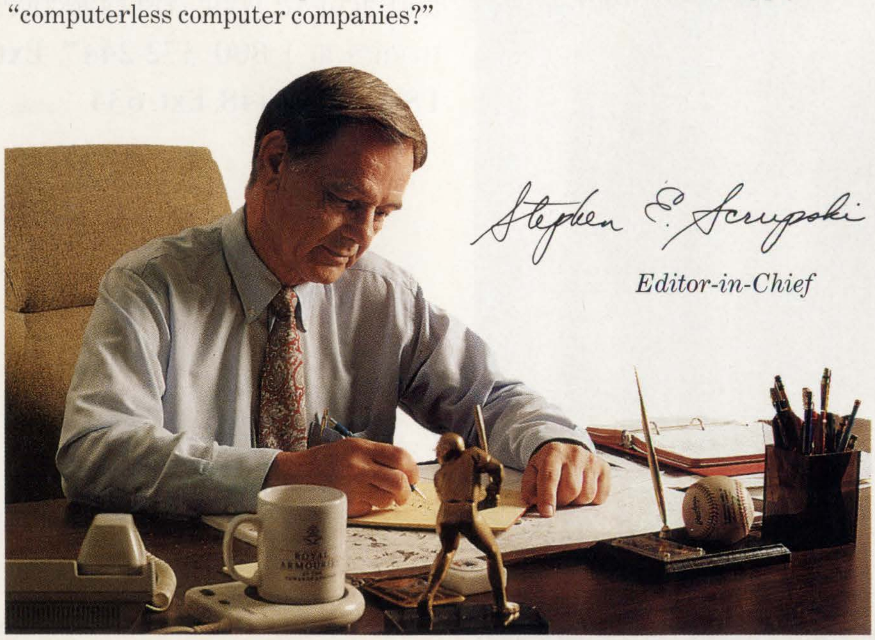
Insights On The Computer Industry

An interesting article appears in the most recent (July-August) issue of the Harvard Business Review: "The Computerless Computer Company," by Andrew Rappaport and Shmuel Halevi, president and vice president, respectively, of the Technology Research Group, a Boston-based consulting organization. The article's central point is that "Computer companies shouldn't aim to build computers. They should aim to create persistent value in computing." According to the article's authors, such companies already have a wealth of hardware available. And only when they're large enough should they consider adding their own manufacturing facility. Thus, manufacturing, rather than a fundamental necessity for business, should be considered a "perk" of success that reduces costs–a perk that's earned by first building a business which successfully satisfies customers' computing needs.

This thought also is interesting in relation to the total-quality programs currently permeating the electronics industry. Total quality, in Malcolm Baldrige award terms, is achieving total customer satisfaction. Implicit in the total-quality concept is the idea that ultimate success hinges on customer satisfaction by concentrating only on those aspects of the business contributing to that goal. A total-quality program also needs a cold, completely objective view of company operations.

This viewpoint might also take some of the sting out of the recent report by the Council on Competitiveness *(April 25, p. 14)*, which noted the United States' weaknesses in memory chips, flat-panel displays, and semiconductor-chip packaging. In addition, the report remarked on the U.S.'s strength in such customer-oriented technologies as applications software, high-level languages, computer architectures, database systems, and user interfaces. These strengths, as Rappaport and Halevi so ably point out, are exactly what's needed to take the lead in supplying computer systems that solve customer problems (of course, this is why many Japanese computer firms have established computer-systems research centers in the U.S.).

However, this shouldn't lead anyone to believe that advances in hardware technology are no longer important in the U.S. Continual improvements in RISC, as well as CISC, machines must proceed. But the sheer difficulty of developing next-generation hardware could very well be enough of a goal for those companies whose expertise lies in that area. Who else will supply those "computerless computer companies?"



Stephen E. Scrupski
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You have to build a to build just

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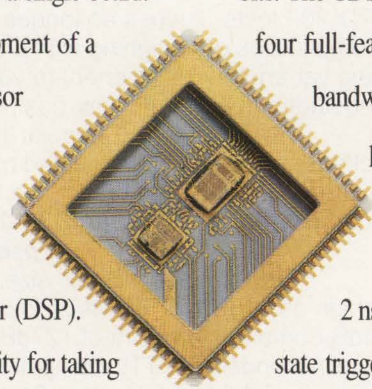

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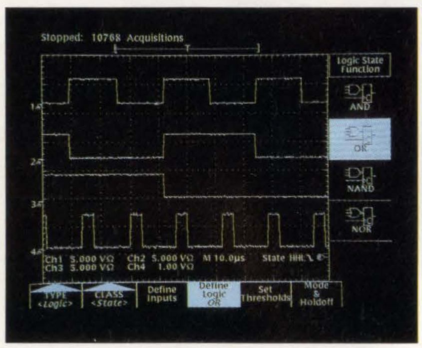

time DSP lets you perform single-shot averaging and extend resolution to 12 bits. The TDS Series arms you with up to four full-featured channels. 500 MHz bandwidth. Up to 1 GS/s sampling and 4 ns peak detect. Up to 50K record lengths. Time interval, 2 ns glitch, runt, pattern and state triggers. With acquisition sensitivity and fast overdrive recovery bringing greater waveform detail within your grasp.

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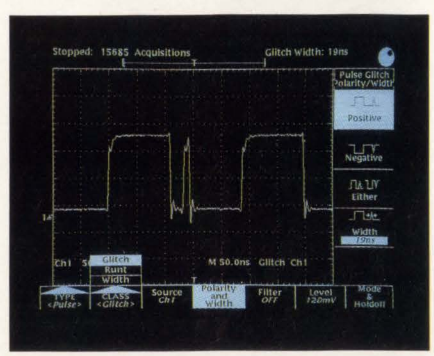

DIVIDING PCs AND WORKSTATIONS

RICHARD NASS
COMPUTER SYSTEMS

Not too long ago, the distinction between a personal computer and a workstation was clear: PCs ran DOS on an Intel-based CISC microprocessor with 640 kbytes of RAM, while workstations ran Unix on a Motorola 68000-family or RISC microprocessor with 2 to 8 Mbytes of system memory, and had excellent networking capabilities. Now, the lines between the two types of systems are somewhat obscured, and perhaps that's not so bad.

DEC's introduction of the DECpc 433, for example, appears to close the PC-workstation gap. In the computer's product description, the company says, "the DECpc 433 workstation is a high performance personal computer..." The machine's specifications go as follows: Intel 486 33-MHz processor; 8 Mbytes of system memory; 64 kbytes of cache memory; display resolutions up to 1280 by 1024 pixels, two LAN connectors; and an external SCSI adapter. Its operating-system compatibility includes MS-DOS, OS/2, and Unix.

It would be difficult to put this system wholly into either the PC or workstation category. And, as for the RISC versus CISC issue, DEC says, "The Intel 486 processor offers all the performance associated with 32-bit RISC microprocessors while remaining 100% binary compatible with the earlier Intel 386 architecture." By DEC's definition, there isn't any clear-cut advantage to employing a RISC processor over a CISC counterpart.

The formation of the Advanced Computing Environment (ACE) consortium has helped blur the lines of distinction even further. ACE promotes a broadly supported, standards-based, open-computing environment for what it calls "advanced computing systems." The consortium, which started with 21 members that were mostly high-powered companies selling either hardware or software, now has over 60 participants. Key elements of the initiative include two hardware platforms, RISC and CISC, as well as two operating systems, OS/2 version 3.0 and Unix.

ACE's RISC-compliant system requires a MIPS microprocessor (either R3000 or R4000); CD-ROM and/or other media interchange; 8 Mbytes of memory; IEEE 802.3 interfaces; SCSI, serial, and parallel ports; and a 1024-by-768-pixel display. On the CISC side, the systems will be developed around 386, 486, and future X86 microprocessors.

Another definition of the boundary line is that a workstation comes bundled with everything users need to do their tasks, whereas a PC is a base system that users stuff with add-in cards or drives to suit their needs. "There's a lot of ambiguity about whether an Intel-based system should be a PC or a workstation," says Heidi Sodos, director of marketing at Falco Data Products Inc., Sunnyvale, Calif. "But there's more to it than the processor. The workstation is up and running right out of the box." Falco recently released a 486-based system, the GT486/40, which the company calls a workstation. It comes with high-end graphics and a high-capacity hard drive, and takes full advantage of the 486's power.

Many people in the industry feel that the dividing line comes from how the system is used–applications determine the system's label. But, as the DECpc 433 shows, high-end PCs can handle most of the applications that were considered "workstation applications." Deviating from this rule are the processor-specific applications, such as the many Sparc applications. In this case, either a Sparc-based machine or some type of Sparc-based add-in card would be required. Most users would agree that the Sparc-based systems are considered workstations. But, if the rule was that all Sparc-based systems are workstations, then there's at least one exception. Last year, Mars Microsystems, Mars, Pa., released the Mariner 4i that could run both DOS and Sparc applications. This system could easily fall on either side of the boundary line. So, in the future, we may just have to drop the labels, or simply group them all together and look for the right system for the right job at the right price.

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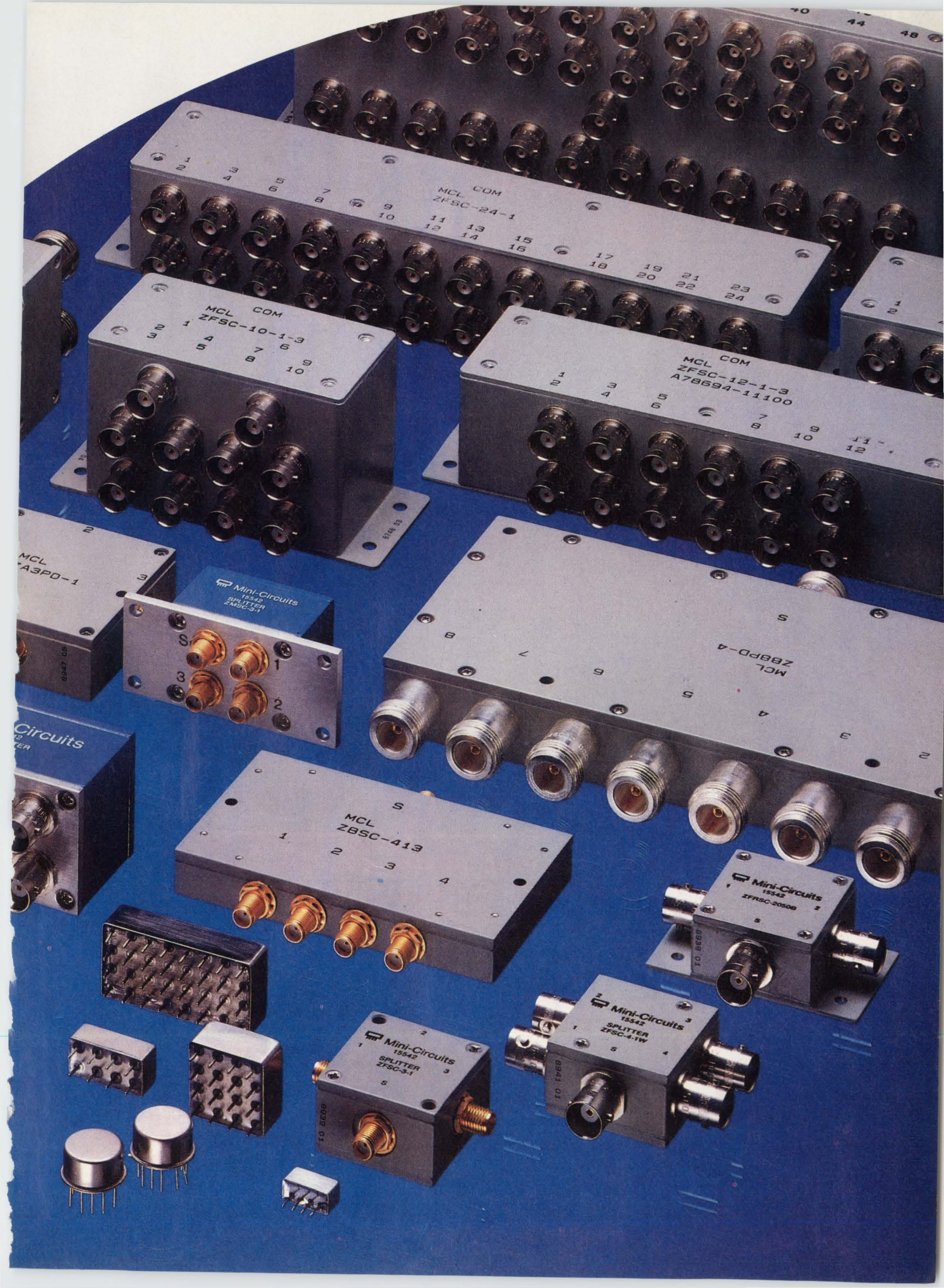
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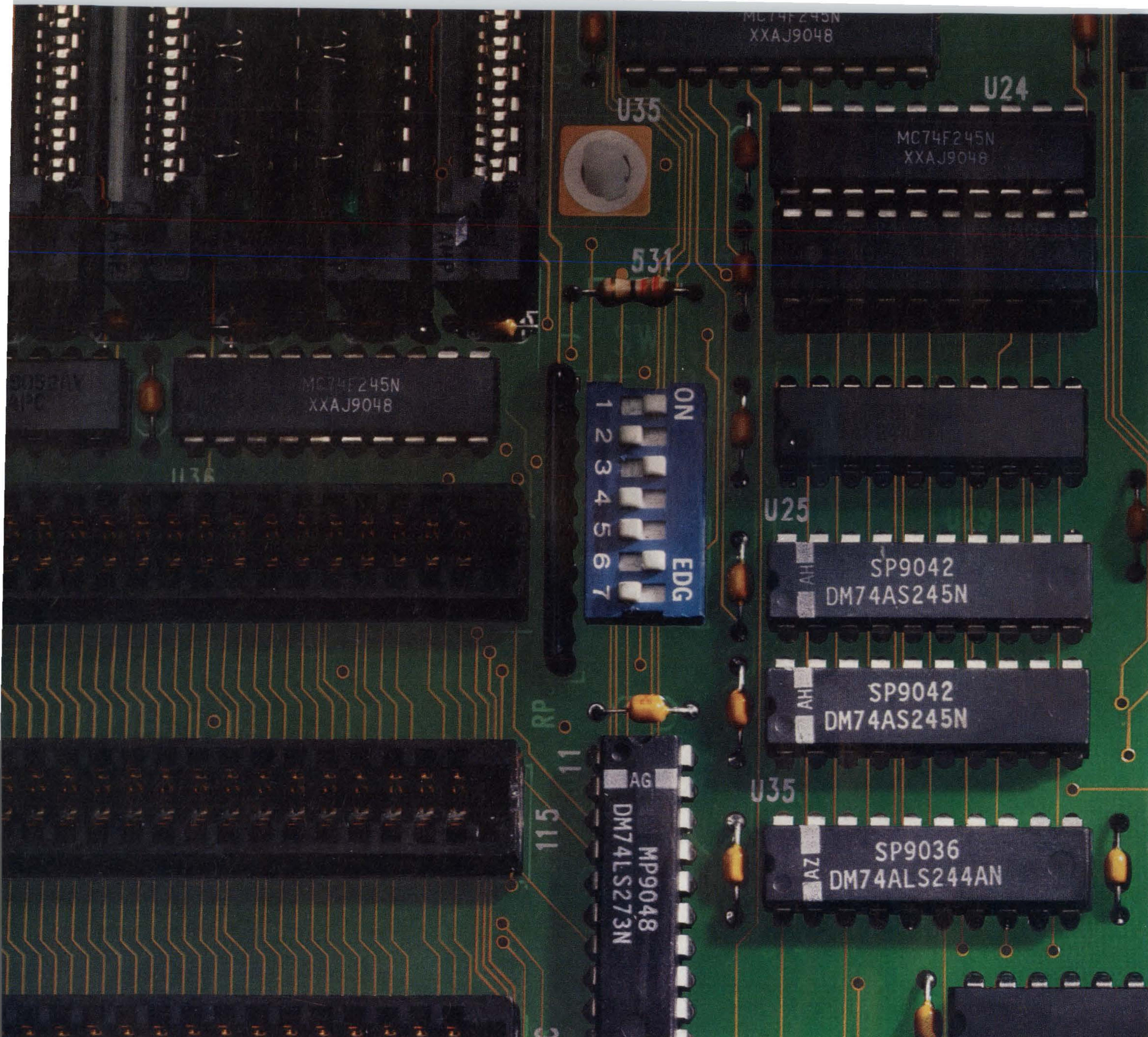

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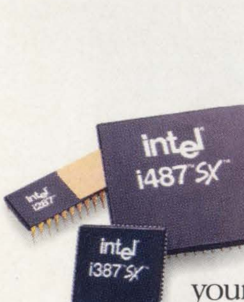

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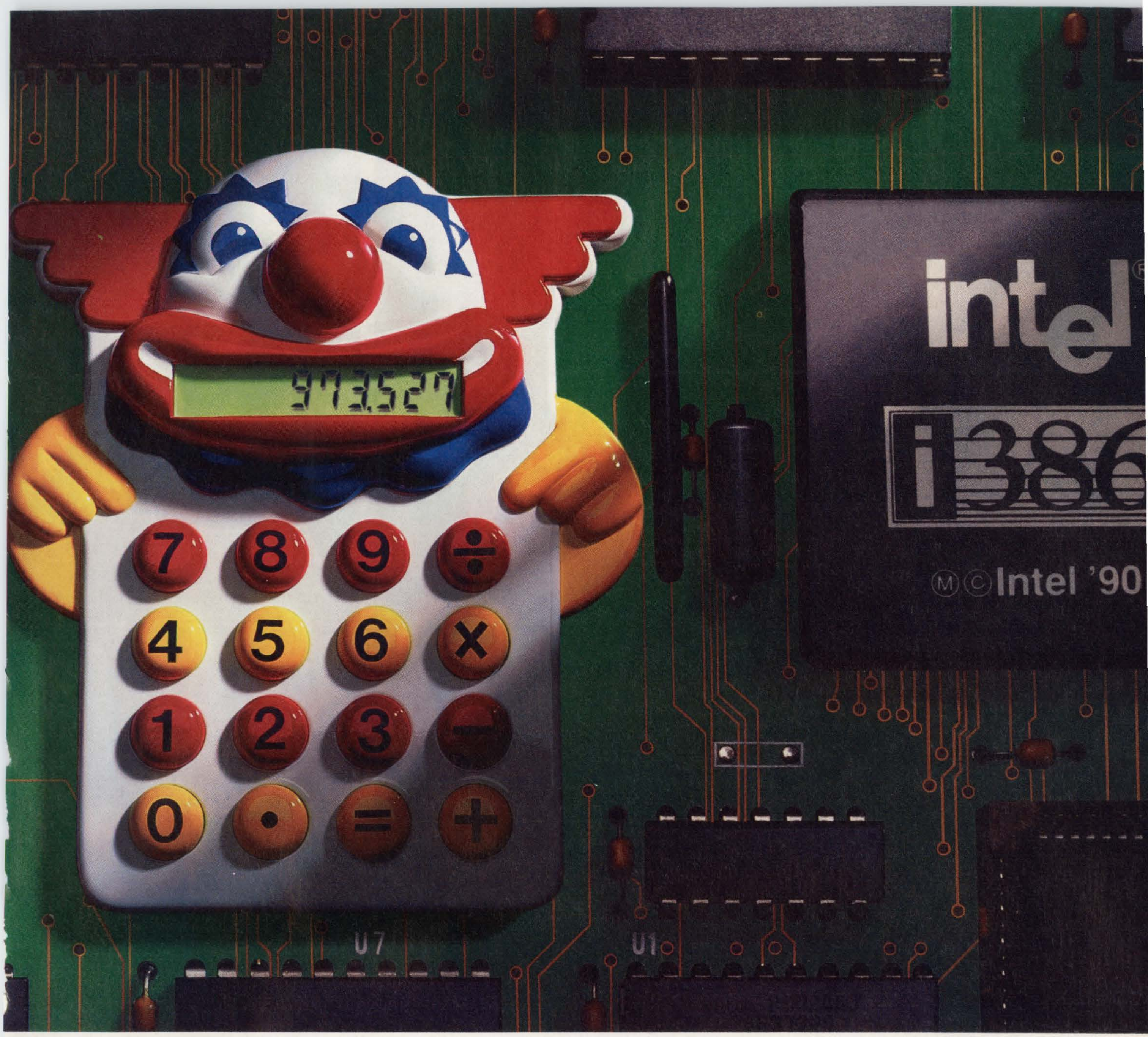
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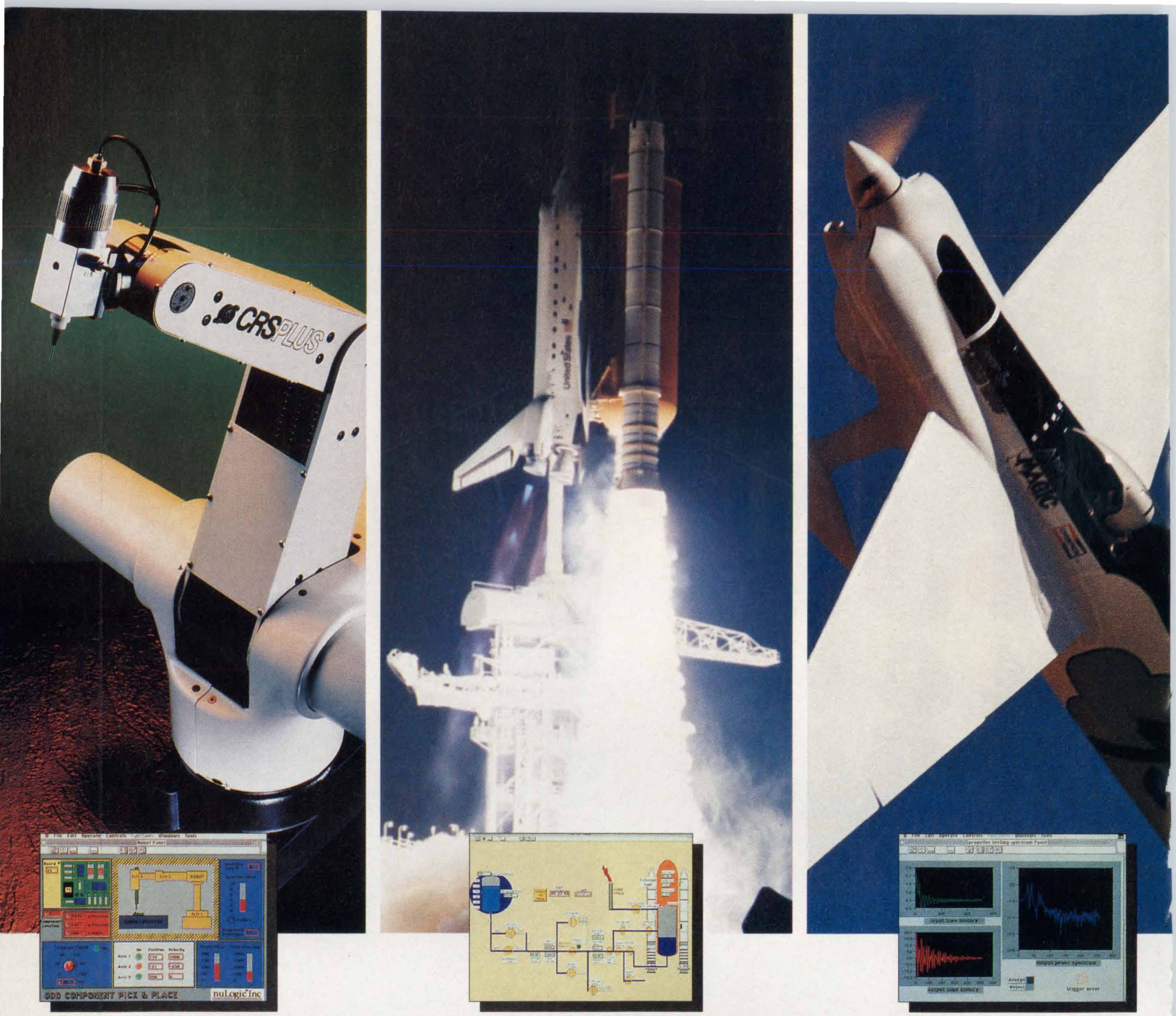

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OPTICAL FIBER TRANSMITS ANALOG/DIGITAL SIGNALS

Researchers at Standard Elektrik Lorenz (SEL) in Stuttgart, Germany, have demonstrated that it's possible to transmit analog cable-TV signals and digital high-definition TV signals simultaneously over a glass fiber network fitted with optical amplifiers. The standard analog CATV signal, for whose distribution coax cables are typically employed, was transmitted at a 1550-nm wavelength, while a 1536-nm wavelength was used for the 2.488-Gbit/s digital signal. Both types of signals were amplified in erbium-doped optical amplifiers. No intermodulation or crosstalk, nor any degradation of bit-error rate or signal-to-noise ratio were measured. SEL, a subsidiary of France's Alcatel N.V., says the laboratory demonstrations proved that fiber-optic analog TV distribution networks with erbium-doped optical amplifiers can easily be upgraded with digital multigigabit/s channels, without the need to modify the networks or their components. *JG*

JOINT ASIC DEVELOPMENT YIELDS DUAL SOURCES

GEC Plessey Semiconductors, Northants, U.K., and SGS-Thomson Microelectronics, Agrate, Italy, have inked a deal to codevelop a 0.7-μm CMOS technology and a standardized cell library, allowing them to directly alternate-source each other. This development, which will commence by early 1992, will allow chip designs to be interchanged at the mask database level and will allay the single-supplier fears of designers of standard-cell-based ASICs. Such fears center on sole-supplier deals and potential price gouging, as well as fabrication failure that could negatively affect the end product. Many ASIC suppliers have signed alternate-sourcing deals with other suppliers, opening the door for other companies to accept the circuit net list. However, that might still require considerable engineering time to resimulate and verify that the other company's results are identical to the original. GEC Plessey will adopt the SGS-Thomson design rules and will align their 0.7-μm process to be electrically compatible with the SGS-Thomson process. Both companies will also codevelop the cell library. Future areas of cooperation will extend into the area of field-programmable gate arrays and a possible 0.5-μm sea-of-gates array family. *DB*

KITS PAVE WAY FOR TECHNOLOGY EVALUATIONS

Designers can test out the latest technology with three evaluation kits concerning the 386SL microprocessor, SCSI devices, and PC memory cards. The 386SL kit, from Intel Corp., Santa Clara, Calif., lets engineers and system architects observe the processor's performance under conditions that simulate a notebook PC. The SuperSet Evaluation kit contains the necessary hardware, software, and documentation to experiment with all of the operating modes and functions of the 386SL family. The kit also includes a 20-MHz CPU. Call a local Intel sales office for more information.

Designers working with SCSI devices will find their tasks become less complex with the SCSI Device Management System (SDMS) from Award Software, Los Gatos, Calif., and NCR Corp., Colorado Springs, Colo. The SDMS is a complete software development package that supports the NCR family of SCSI processors and controllers. The kit consists of a resident SCSI BIOS that manages all hardware-specific functions and a series of SCSI device-management modules that supply operating systems, SCSI controllers, processors, and peripheral support. For more information, call Award Software at (408) 370-7979. Award is also distributing a PC memory card evaluation kit, designed by Databook Inc., Ithaca, N.Y. The kit lets OEMs evaluate the cards, the drives, and the application software on-site. *RN*

IMAGING BASED ON IONS TRACES IC WEAKNESSES

An imaging technique, called single-event upset imaging, is so precise that it allows researchers to isolate weaknesses or faults in ICs due to ionizing radiation down to individual transistors. Developed at Sandia National Laboratories, Albuquerque, N.M., the scheme takes advantage of the temporary but critical disruptions in IC memory cells that result from colliding semiconductor molecules and high-energy cosmic rays. The scheme employs ion microbeam probes to study the radiation-induced upset condition and plots the results on a micron-resolution "map" that shows where the upsets occur. The maps are then compared to the chip layout to determine the actual circuit element that was upset. Previously, entire chips were tested to identify malfunctioning circuits and eventually pinpoint the sensitive elements through measurements and complex calculations. However, the location of the upsets can't be precisely determined or imaged as with the single-event upset imaging scheme. In the imaging scheme, nuclear microprocesses direct narrow ion beams at a fixed point on a target and use various analysis methods to determine the target's composition by analyzing the scattered ions. Because the ion beam can selectively irradiate a single memory cell, transistor, or even a piece of a transistor (such as the drain or gate), it can detect upset-prone regions even within devices. Contact Barney Doyle, (505) 844-2609. *DB*

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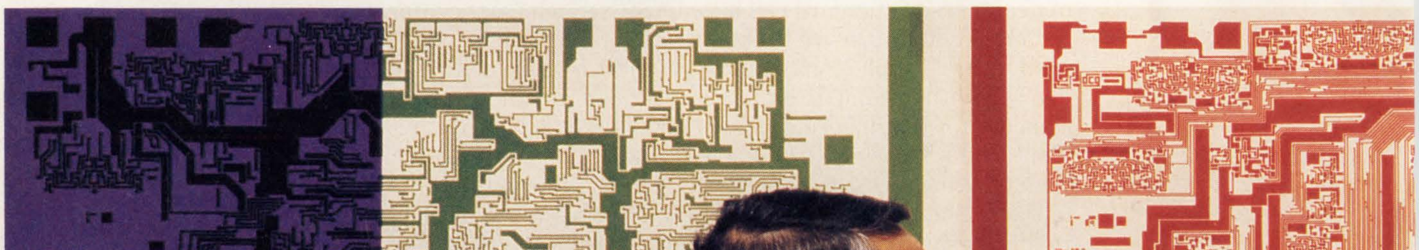

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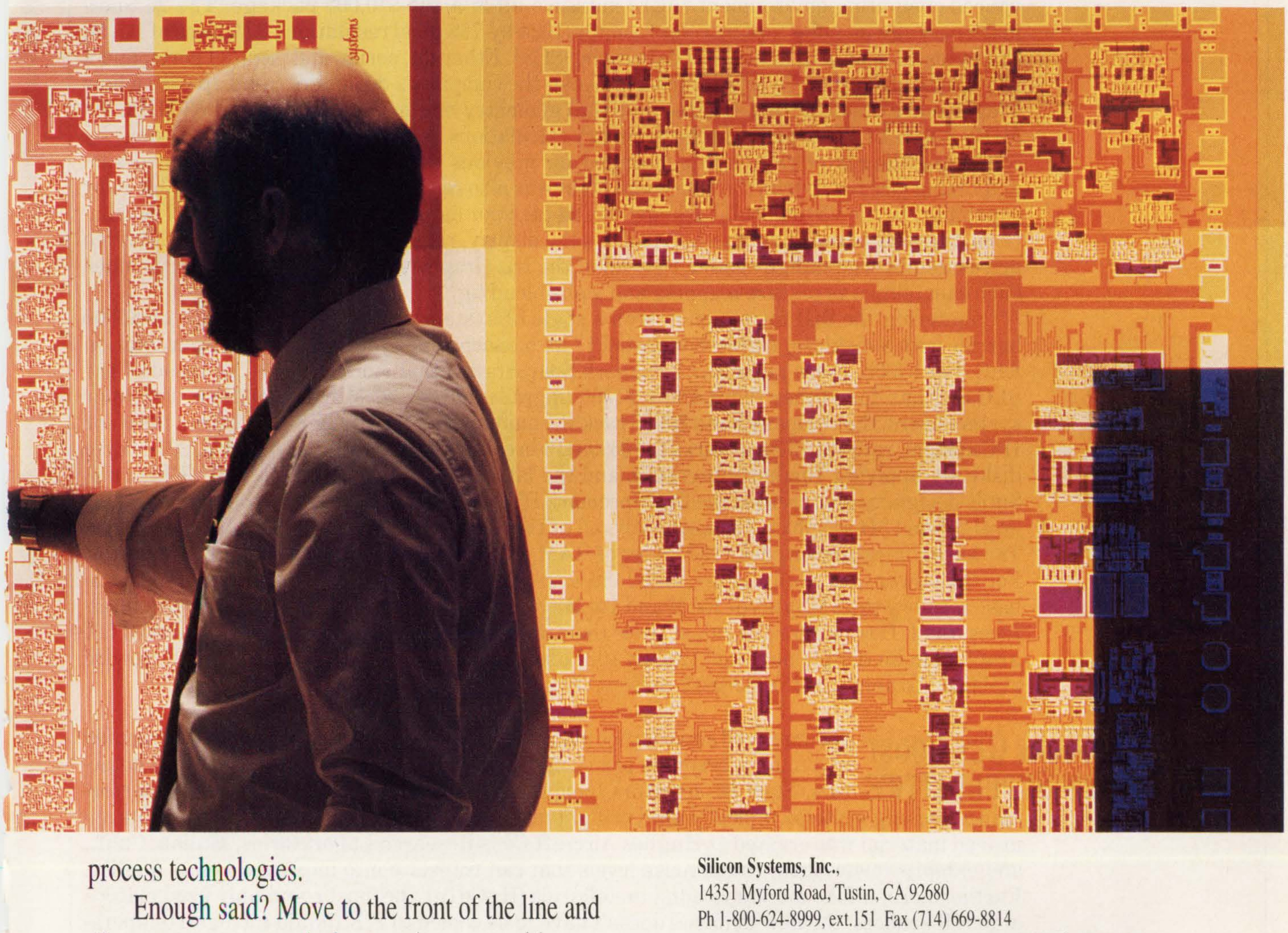

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UHF Class-AB Transistor Nets Performance Record

A linear UHF-TV transmitting transistor sports the broadest bandwidth yet achieved for class-AB operation, says its developer Philips Components in Eindhoven, the Netherlands. Working between 470 and 860 MHz, the BLV62 delivers at least 150 W in modular UHF TV transmitters. A rugged device that incorporates two npn silicon planar epitaxial transistor sections in a push-pull configuration, the BLV62 has a power gain of at least 8.5 dB combined with an output capacitance of less than 1 pF/W per side. The device features internal input matching for optimum wideband performance and high gain. The typical efficiency is 50% for a nominal 28-V supply. The maximum dc collector current is 12.5 A. *JG*

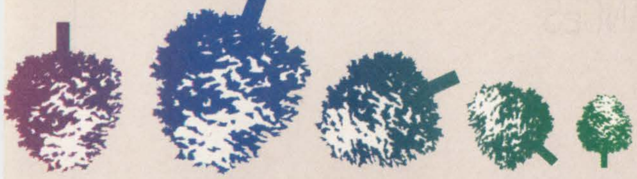
2D, 3D Workstations Set New Price Lows

In a flurry of integration and architectural improvements aimed at lowering cost and improving performance, Silicon Graphics Inc. and Sun Microsystems Inc., both of Mountain View, Calif., have unveiled new low-cost 2D and 3D workstations. The Iris Indigo workstation from Silicon Graphics puts 3D color graphics, CD-quality audio (thanks to a built-in Motorola 56001 DSP chip), and compatibility with the advanced-computing-environment (ACE) initiative all in a sub-$10,000 package. The 26 Specmark package includes a 16-in. color monitor (1024-by-768-pixel resolution); 8 Mbytes of RAM; 32 kbytes each of instruction and data cache; SCSI, Ethernet, serial, and parallel ports; and a 236-Mbyte disk drive. To attain such a low cost, the company's designers came up with a new graphics architecture that creates a virtual geometry engine by allowing the 33-MHz, 30-MIPS R3000A CPU to perform the geometry calculations. Additional integration was done by combining the raster engine chip designed for previous workstations with scan conversion and timing circuits to trim the chip count. Cost was also reduced by using a virtual 24-bit color capability. In the virtual 24-bit scheme, the 24-bit color data is employed for internal calculations, but is dithered down to 8 bits to drive the display, reducing the complexity of the video drive circuits. The Indigo system runs all of the Iris Graphics Library software and includes such capabilities as texture mapping and alpha blending.

Countering the SGI introduction with a spate of systems, Sun has cracked the sub-$5000 barrier with a diskless, highly-integrated 17-in. monochrome system called the SparcStation ELC. For $4995, users get a 20.1 Specmark SparcStation that runs at twice the speed of the SLC and has four times the RAM; a $1300 upgrade adds a 207-Mbyte hard disk. For color system users, the company has a $9995 package built around the ELC CPU, or offers the color IPC system, rated at 13 Specmarks for $6995 (16-in color display, 8 Mbytes of RAM, 207-Mbyte disk). By applying further integration and the latest 40-MHz combination CPU/FPU chip, Sun's designers also created the 24.2 Specmark IPX, an upgrade to the IPC that includes GX-level 2D and 3D graphics. Consequently, all of the SBus slots on the motherboard are freed. The base configuration packs 16 Mbytes of RAM, a 207-Mbyte drive, and a 16-in. color monitor. For the power user, Sun has upgraded the SparcStation II to 24.7 Specmarks and upped the base memory to 32 Mbytes of RAM and 424 Mbytes of disk storage. With improved disk interfaces, the I/O transfers can run at twice their previous speed. A system with accelerated GX graphics (8-bit double-buffered 1280 by 1024 pixels) goes for $22,495. Contact Chris Surowiec at Silicon Graphics, (415) 335-1832; or Steve Tirado at Sun, (415) 336-9011. *DB*

IR Sensors Get Boost From New Superlattice

An improved superlattice material that combines gallium-indium-antimonide and indium arsenide promises to improve the sensitivity of infrared detectors. Such IR detectors form the heart of focal-plane arrays—high-performance sensing systems typically used in night-vision systems and space applications. The improved material was created at Hughes Aircraft Co.'s Research Laboratories, Malibu, Calif., and exhibits lower background noise levels that can translate into improved image quality. Furthermore, unlike mercury-cadmium-telluride (HgCdTe), the most commonly used material for IR sensors, the new material doesn't have to be cooled to 77K (liquid-nitrogen temperature) to operate. The material can detect light at longer wavelengths than HgCdTe, opening applications for earth-monitoring applications by NASA. The molecular-beam epitaxy process used to fabricate the superlattice detectors provides a highly uniform and defect-free set of material layers. This also permits larger, higher-density imaging arrays (such as 512 by 512 points) to be fabricated. Those larger arrays, in turn, permit designers to shift from complex scanning arrays to simple staring arrays. Portions of the work was done under contracts with the Defense Advanced Research Projects Agency and the Office of Naval Research. *DB*



DIODE-SWITCH-BASED DESIGN LEADS TO 16-BIT 0.5-LSB DAC WITH 500-NS SETTLING TIME

Using diodes instead of conventional transistor switches has allowed the PMI Div. of Analog Devices to develop a 16-bit current-output digital-to-analog converter (DAC) that settles to within a 0.5 of a least-significant bit (LSB) of 16 bits in under 500 ns, over a full-scale input step voltage. Moreover, the DAC maintains monotonicity over the full military temperature range and is radiation-hardened. The circuit will be described in the upcoming sixth annual IEEE Bipolar Circuits and Technology Meeting (BCTM), Sept. 8-9, in Minneapolis, Minn.

Conventional bipolar DACs use an array of binary-weighted current sources. The sources are controlled by a voltage reference and steered to an output port by transistor switches. The output port is commonly connected to an op amp's summing point, which acts as a virtual ground.

Theoretically, the effects of finite transistor current gain (beta) and the beta's change with temperature cancel each other out if the transistors are perfectly matched. However, this type of architecture has flaws that start impacting the accuracy level of DACs at resolutions beyond 12 bits.

For example, preventing ringing and slow-settling thermal tails from occurring at all of the bias points can become a nightmare. Moreover, higher-resolution converters demand low power-supply currents to limit warm-up drift effects. In addition, beta mismatches require the use of trimming. This can be done, but it doesn't hold over temperature. Finally, beta changes significantly when exposed to ionizing radiation.

To beat these problems, PMI's Derek Bowers designed his DAC circuit with diodes. Conceptually, binary-weighted currents are generated by area-scaled diodes D_{1a}, D_{2a}......D_{na}; and resistors R_1, R_2.......R_n; under the control of a servo amplifier *(see the figure, part a)*.

When the bases of the switch transistors are biased negative, these currents flow freely to the output. If they're driving an op amp's summing point (the expected load), it represents a virtual ground. Biasing a switch-transistor's base positive shunts the transistor's respective current source to V_{bias}, the 5-V rail in the circuit.

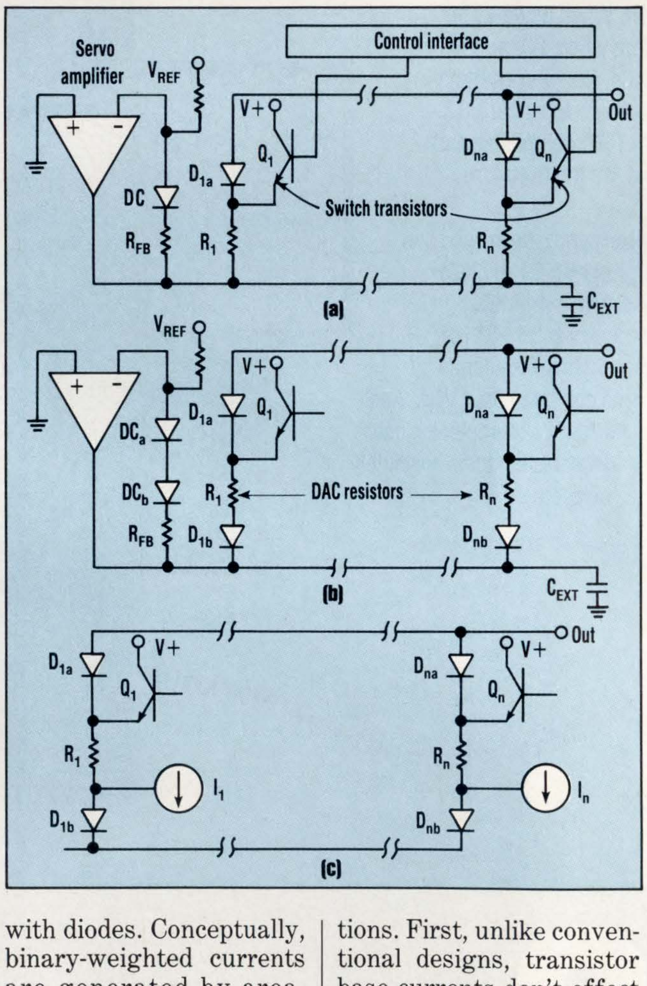
This technique of using diodes offers two attractions. First, unlike conventional designs, transistor base currents don't effect the output accuracy. Second, the op amp's output is the only significant internal circuit node that must settle. The output is prevented from moving by means of a large, external capacitor. As Bowers notes, the op amp must be stable driving a large capacitance.

However, the scaling scheme presents a problem. The most-significant-bit diode must be 65,536 times the size of the LSB diode. Even if this were practical, and it's not, the resulting output capacitance would destroy the speed of the circuit. However, the LSBs are less critical to both the speed and accuracy of a practical converter.

Therefore, a more-or-less conventional R-2R-network handles the 16-bit DAC's 7 LSBs. In addition, the DAC's 5 MSBs are segmented to ensure monotonicity over a wide temperature range. That is, they're split into 31 equal current sources. A scaling ratio of 16:1 is still required between the segment weight and bit 9. Consequently, Bowers located an additional set of diodes (D_{1b}, D_{2b}.....D_{nb}) below the DAC resistors (and in series with resistor R_{FB}), which permit area scaling by factors of four rather than two *(see the figure, part b)*. As a result, all of the switching transistors can be minimum-geometry devices.

The capacitance of the additional diodes is unimportant because very little voltage change occurs at this end of the resistors. While eliminating the speed penalty, the added diodes actually increase the die area. However, adding current sources I_1, I_2 .... I_n into the lower diodes—in opposition to their respective bit weights—eliminates that problem *(see the figure, part c)*.

In actuality, the switch-



ing diodes are npn transistors. Because they all have a common collector, they're located in the same pocket of epitaxial material, further reducing output capacitance. The collector-base connection is made at the output bonding pad using Kelvin techniques to ameliorate the effects of the inevitable voltage drops across metallization runs.

Bipolar Process

The 16-bit DAC chip is built on a conservative 20-V washed-emitter bipolar process with a minimum feature size of 5 μm. The cutoff frequency f_t of its vertical npn transistor is 1.2 GHz; that of its lateral pnp transistor 8 MHz. The process has access to laser-trimmed thin-film resistors and two levels of metal. The DAC has no thermal tails when settling due to a careful layout that takes thermal effects into consideration.

The BCTM conference has become a leading showcase for bipolar and biCMOS semiconductor technologies, including silicon, silicon-germanium alloys, and heterojunction III-V materials, for high-speed digital and analog ICs. Its 12 sessions cover a wide range of subjects, including transistors from the latest submicron bipolar processes with silicon cutoff frequencies f_ts to 37 GHz; complex high-speed ICs, such as a 23-GHz silicon multiplexer; and a 4-GHz transmitter with an output of 50 mW. The 4-GHz transmitter uses a gallium-arsenide/aluminum-gallium-arsenide heterojunction bipolar transistor.

Other sessions address self-aligned devices on a bonded silicon-on-insulator wafer, npn transistors with silicon-carbide emitters, and ion-implanted silicon-germanium pnp transistors. Various issues, including modeling, system design, packaging, device physics, and high-frequency characterization, are also explored.

For additional information about the BCTM, contact Janice Jopke, Conference Coordinaton Services, 6611 Countryside Dr., Eden Prairie, MN 55346. Phone: (612) 934-5082, fax: (612) 949-2518.

FRANK GOODENOUGH

Logic-Controlled Element Replaces Analog And Mechanical Switches

By driving an n-channel MOS transistor with a CMOS logic gate, a novel switching element with less than 250 ps of signal propagation delay can be implemented for systems that need signal switching and bus-swapping operations. Developed by Quality Semiconductor Inc., Santa Clara, Calif., the switches exhibit less than a 5-Ω on-resistance, present less than a 2-pF load, and have low-noise characteristics.

The switches can connect into a TTL system just like a wire, because when the switches are turned on, the signals think they're flowing through a wire rather than a pass transistor. When off, the switch appears to the system just like an open circuit, effectively blocking any signals into or out of the system. When on, the switches allow over 64 mA per switch of pass-through current.

In addition to serving as bus switches, the QuickSwitch elements with their short, 5-ns turn-on or turn-off times could serve as replacements for digital and mechanical switches in load-switching schemes within automatic test equipment and in RF/video signal-routing applications. The fast switching speed and direct-connection capability enable the switches to be used in low-level video switching, and the digital routing of various video signals, such as digital TV, multimedia systems, and high-frequency video crosspoint switching applications. The QuickSwitches are 10 to 100 times faster than traditional analog switches in these applications.

The switch elements, which can replace the buffers and transceivers in lightly-loaded applications that don't require bus repowering, are bidirectional and require no direction control, just like a mechanical switch. The basic switch element will be employed in two families of logic switches, one designed for bus switching that allows signals to flow through or be blocked, and the other aimed at bus-exchange applications in which signals must be transposed or rerouted.

Furthermore, as with a mechanical switch, the Quickswitch elements consume no power. Less than 10 mA is required to power an entire chip with 10 single-line switches (the QS54/74QST3384 family) or five sets of bus-exchange switches (the 3383 family). The low 5-Ω on-resistance of the switches allows inputs to be connected to outputs without adding noticeable propagation delay and without generating additional ground-bounce noise. However, a second series, the 3584 and 3583, includes 25-Ω resistors in their 24-pin packages to reduce reflection noise in high-speed applications. To protect device inputs, undershoot clamp diodes are embedded in the chips.

The 3384/3584 contains two banks of five switches, with each bank controlled by one logic input. Each bank has five inputs and five outputs, and when both banks are used together, the switches can be inserted into a 10-line bus. Or each bank can be controlled independently. The 3383/3583 is a little more complex, and contains two sets of 10 high-speed switches. By cross-connecting the switches and providing a bus-exchange control line, input signals from A and B input lines can feed directly to C and D output lines, respectively. They can also be transposed so that A inputs are fed to the D outputs, and B inputs are fed to the C outputs. With such a scheme, the chip can serve as a quad 2:1 multiplexer or form low-delay barrel shifters. For more information, call Bill Scharrenberg at (408) 450-8020.

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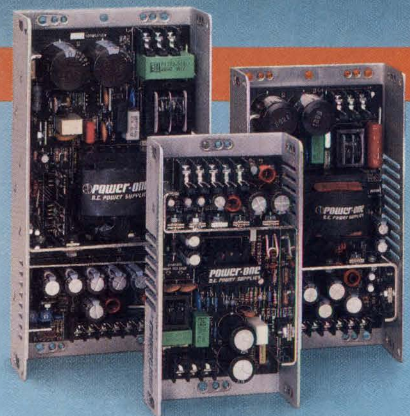

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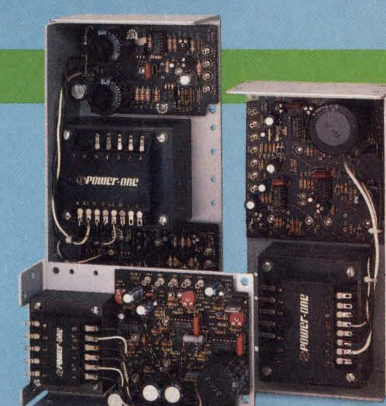

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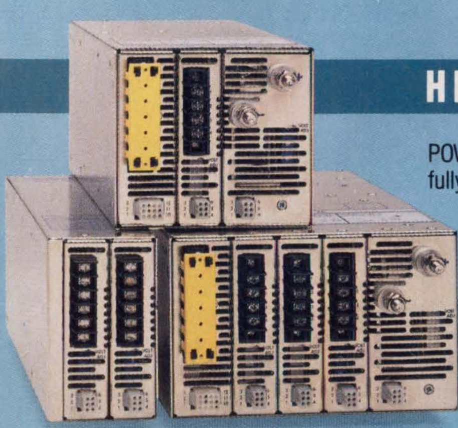

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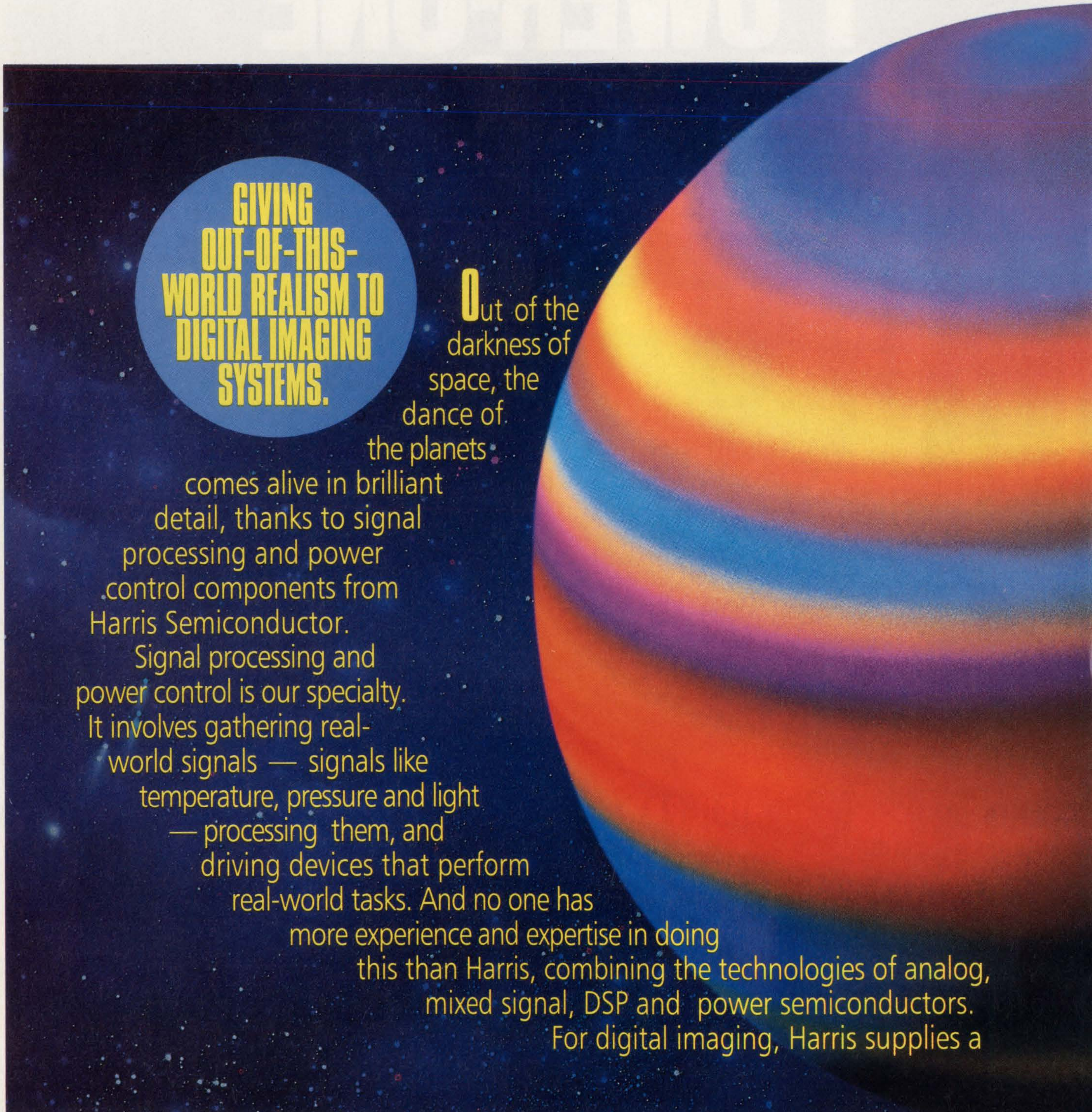

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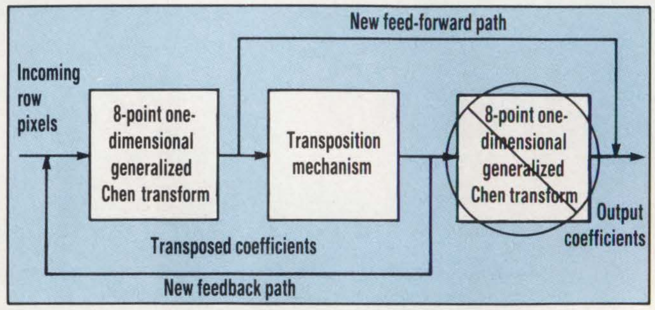
Improved Algorithm Scheme Trims Multiplications, Speeds Image Compression and Expansion

Lossy data compression for image storage and retrieval has centered around the Joint Photographic Experts Group (JPEG) standard for still images and the newer standard for motion video from the Motion Pictures Expert Group (MPEG). However, when implementing the algorithm with software or hardware, one of the most time- or silicon-area-consuming operations that must be performed repeatedly is the important step of multiplication.

An improved algorithm developed by Ricoh Corp. at their research center in Menlo Park, Calif., maintains JPEG/MPEG compatibility yet eliminates all multiplications in the compression portion of the computations.

The algorithm, dubbed the generalized Chen transform (GCT), is a variant of the discrete cosine transform that's employed by most companies that now are offering JPEG image-compression and -decompression hardware or software.



To execute the GCT compression algorithm with 8-by-8-pixel blocks, just 608 additions are needed for one frame. Although that's more additions than other "fast" algorithms proposed by Hein, Chen, and Lee, the GCT also requires fewer subsequent multiplication operations during the quantization stage—just 64.

That's only one-third the

number of multiplications that are required by the next most-efficient algorithm. The GCT algorithm can thus take in eight pixels, feed them through no more than six levels of an arithmetic network, subject them to no multiplies, table lookups, or control, and, finally, deliver eight coefficients. Compression ratios of 2:1 to 100:1 can be achieved with the algorithm.

In a conventional implementation, the pixel data is fed into a one-dimensional 8-point GCT block *(see the figure)*. The resulting data is passed on to a transposition block that rearranges the data for a second 8-point GCT to work on. However, by feeding back the transposed information into the first GCT block and then tapping the GCT block's output at the right point in time, the entire second GCT block can be eliminated (as indicated by the circle-slash sign in the diagram).

This simplifies the overall structure and reduces the complexity of the hardware implementation. The GCT performs all of the calculations through add and shift operations rather than multiplications, reducing the complexity of any hardware implementation and minimizing power consumption.

The GCT-8 implementation can compress both continuous color as well as gray-scale images, and can do the compression at reasonable rates with a software-only implementation of the algorithm. And when the algorithm is implemented in silicon, Steve Blonstein, the project leader, estimates that real-time video compression would be practical.

For instance, on a 68030-based Macintosh IIfx, the software compression of a 512-by-512-pixel, 24-bit full-color image (768 kbytes) requires just 3.5 seconds—including the color space conversion, GCT transformation, quantization, and Huffman encoding. That translates to a software compression speed of about 200 kbytes/s and a compression ratio of about 25:1. If the Macintosh is upgraded to the more powerful 68040 microprocessor, the compression time drops to just 1 second.

Excluded from the time are factors such as disk access time, compressed-file save time, or painting of a window.

The company is currently seeking to license the patented technology to both software and silicon developers. It also plans to integrate the technology into its own line of office and consumer products. Contact Ed Onstead at (408) 281-1436.

DAVE BURSKY

New Layer Structure Promises To Deliver Extreme-Speed Transistors

If manufacturers of integrated chips exploit the results of semiconductor work done at a German research institute, designers may soon have a new high-speed compound semiconductor device at their disposal. Consequently, new applications in optoelectronics and communications would be opened.

The device is based on an indium-phosphide/gallium-indium-arsenide material combination. For this InP/GaInAs semiconductor compound, the researchers at the Institute for Thin Film and Ion Technology in Jülich, Germany, have come up with a layer composition that make it possible for semiconductor devices to achieve extremely high electron velocities.

Specifically, the composition achieves electron mobilities up to 450,000 $cm^2/V\text{-}s$ at low temperatures. Given the results it has obtained thus far, the Jülich group foresees the development of extremely fast and low-noise field-effect transistors (FETs). Also possible is the development of high-electron-mobility transistors (HEMTs).

Conventional high-speed transistors used in supercomputers and communications systems generally employ a gallium-arsenide/aluminum-gallium-arsenide (GaAs/AlGaAs) layer combination. But in many applications, this material system is inferior to the InP/GaInAs that the Jülich institute is currently working with.

One advantage of this material system over GaAs/AlGaAs is that it lends itself well to fabricating semiconductor lasers suited to transmit data through glass fiber networks. This is because the wavelength of such lasers optimally matches the wavelength of the glass fiber. This is not the case for a GaAs/AlGaAs laser, according to the researchers at the institute.

Another advantage is that the InP/GaInAs material combination enables integrated circuits to be fabricated with optoelectronic devices and high-speed transistors on the same semiconductor chip. The high level of integration achieved in this manner helps to minimize the size of equipment and simplifies its design.

The high mobility of the

InP/GaInAs semiconductor compound is a function of exact control of the indium-to-gallium ratio in the GaInAs layer. It's also a function of an optimized structure of the device layers.

Free electrons form a quasi two-dimensional electron gas in the GaInAs layer, directly at the transition between the indium-phosphide and gallium-indium-arsenide layers. In this gas, the electrons fly nearly ballistically and are therefore extremely mobile.

The Jülich researchers obtained this layer structure by an epitaxial growth process. In other words, it's the crystalline deposition of the semiconductor materials.

The dopant atoms, which are the origin of the free current-carrying electrons, are spatially separated from the two-dimensional electron gas. Therefore, the electrons aren't scattered by the dopant atoms' electrical charge, eliminating a major cause for electrical resistance.

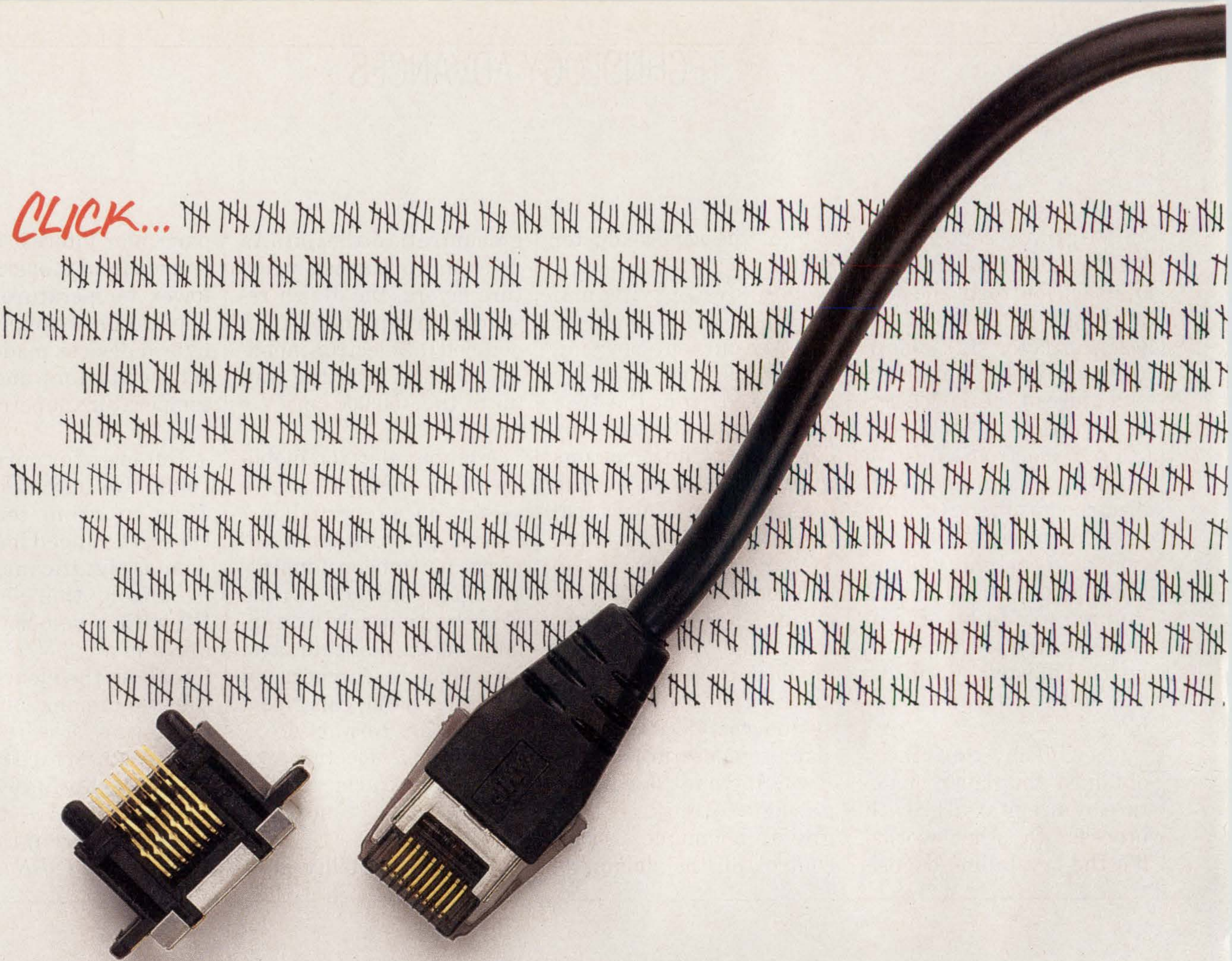
Until now, the highest reported mobility in a two-dimensional electron gas in an InP/GaInAs material system was 180,000 cm^2/V-s at a temperature of 50K. By using metal organic gas-phase epitaxy as a growth technique, precise control of the indium-to-gallium ratio in the GaInAs layer, and optimized-structure layers, the Jülich research group more than doubled the electron mobility, pushing it all the way up to the 450,000-cm^2/V-s level.

A higher electron mobility value—600,000 cm^2/V-s—was once reported by a French group. But that value has never been duplicated again, neither by the French group nor by anyone else, the institute says. The Jülich researchers, on the other hand, can give a recipe for how the extremely high electron mobility they've achieved can be reproduced time after time.

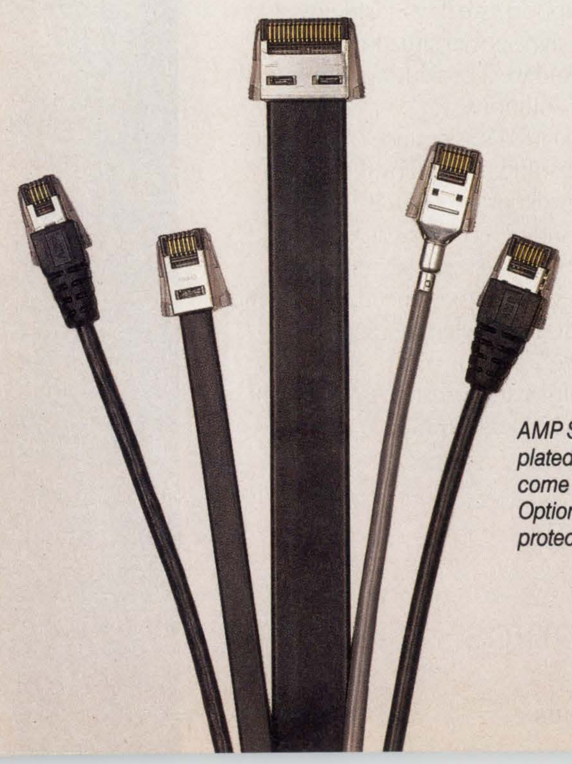
The high mobility is of particular interest in electronic circuits operated at lower temperatures. One application example is in hybrid devices made up of semiconductors and high-temperature superconductors.

But even for pure semiconductor circuits operating at room temperatures, the speed improvement is significant. While in silicon, the electrons fly with a velocity of 40 km/s in a 0.3-V/μm electric field, the electrons in the two-dimensional electron gas at the InP/GaInAs interface reach a 10-times higher velocity—400 km/s—at the same field strength.

JOHN GOSCH



Great ideas tend



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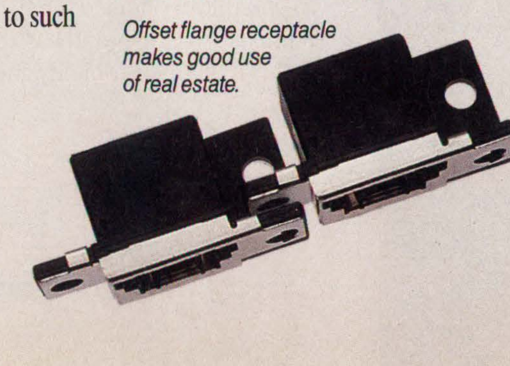

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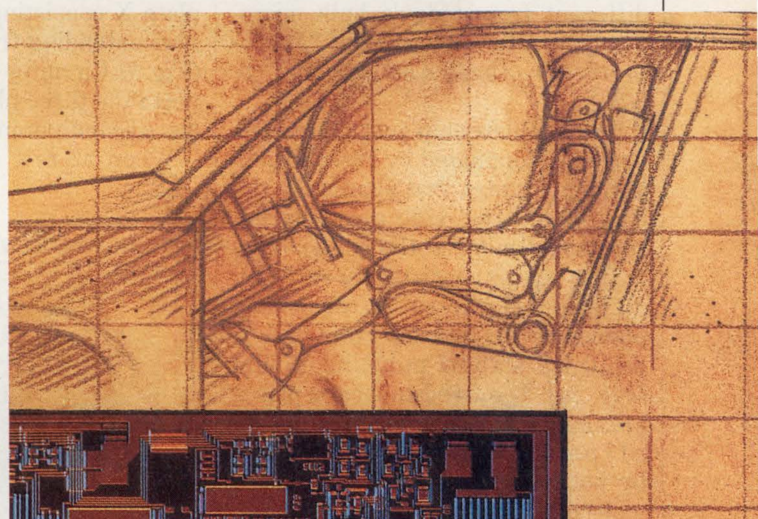
ACCELEROMETER'S MICROMACHINED MASS "MOVES" IN PLANE OF IC; ON-CHIP CIRCUIT CONTROLS IT AND SENSES G WITH FORCE-BALANCE TECHNIQUES.

AIRBAGS BOOM WHEN IC ACCELEROMETER SEES 50 G

FRANK GOODENOUGH

What's the hottest new item in today's cars? Nine times out of ten, the answer is the airbag. As a result, there's a burgeoning need for a reliable and low-cost IC accelerometer with a 0-to-±50-g linear analog voltage output. Present airbag accelerometers are electromechanical, involving multiple sensors, leading to high cost and questionable reliability. An IC sensor, on the other hand, is inherently more reliable and potentially lower in cost. But for an IC sensor to be useful in airbags, however, it would have to be priced at just a few dollars in large production volumes, a price that conventional bulk micromachining techniques have yet to meet.



Using surface micromachining instead, Analog Devices designed and built such a device for automotive airbag deployment. Its ADXL50, a ±50-g IC accelerometer, represents the company's most innovative chip for the automotive industry. Moreover, it meets that industry's specifications for an airbag-deployment sensor *(see "Automotive accelerometers," p. 49).*

The ADXL50 is also the first in a family of IC accelerometers from Analog Devices, and their initial micromachined part. Compared with other micromachined production parts, the device is said to claim several firsts, such as:

- The first "surface-micromachined" accelerometer device to be manufactured in production volumes.
- The first micromachined sensor with an extensive amount of active on-chip signal-conditioning circuitry.
- The first micromachined sensor IC whose moving part (the accelerometer's proof mass) moves in the plane of the chip.
- The first force-balance micromachined sensor.
- The smallest-size micromachined acceleration sensor.

Without surface-micromachining technology, none of these feats would have been possible.

Today, bulk-micromachined sensors are in high-volume production. They measure absolute manifold pressure in every car's engine-control system; throw-away devices measure continuous, intravenous blood pressure during surgery; and differential-pressure sensors in building environmental-control systems measure air flow. On the other hand, surface-micromachining technology, like that used by Analog Devices for their accelerometer, has until now only been at home in academia, corporate R&D labs, and a few low-volume applications. It is vastly different from today's bulk micromachining technology *(see "Micromachining, bulk and surface," p. 50)*.

The complete chip, just 120 mils on a side, is dominated by signal-conditioning circuitry that surrounds the tiny 40-mil-to-a-side acceleration sensing element in the center *(Fig. 1)*. The sensor consists of a variable, differential, air capacitor whose plates are cut (etched) from one, 2-μm-thick slab of polysilicon film *(Fig. 2a)*. The fixed capacitor plates are simple cantilever beams supported 1 μm above the chip, in free space, by polysilicon anchors that form a molecular bond with the chip *(Fig. 2b)*. To get some idea of how small these dimensions are, it should be noted that a human hair is typically 20-μm thick.

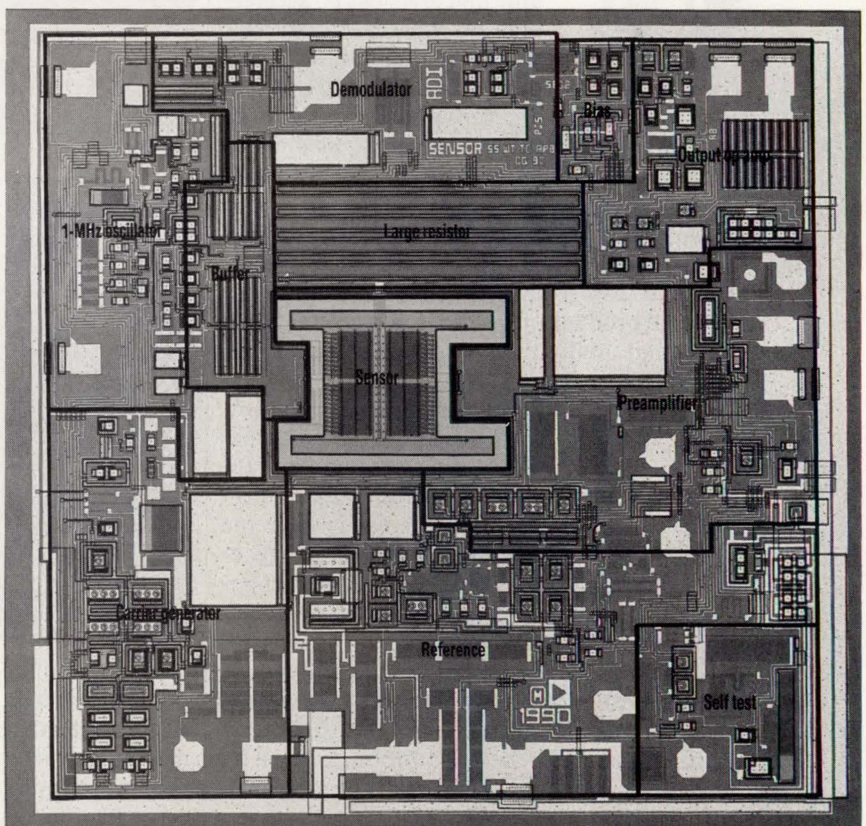
The accelerometer's proof mass (the effective mass whose inertia transforms an acceleration along an input axis into a force) moves relative to the rest of the chip when sensing acceleration. The proof mass' 50-odd fingers form the movable plate of the variable capacitor *(Fig. 2c)*. The fingers are supported at each end by a tether, which is a simple beam held off the chip by anchors at each end, similar to those supporting the fixed plates. In addition to supporting the mass, the tether provides the mechanical spring constant and force that restrains the proof mass and restores it to the zero position. To put it another way, the inertial force due to acceleration, $F = mA$, is balanced by the force of the spring, $F = kx$, where m is the proof mass, A is acceleration, k is the spring constant, and x is the displacement of the mass.

Consequently, $F = kx = mA$. Solving for A, we get $A = x\,(k/m)$, where k/m is a constant, a function of the device. By knowing k/m for a given accelerometer and measuring the displacement of the mass, acceleration can thus be measured.

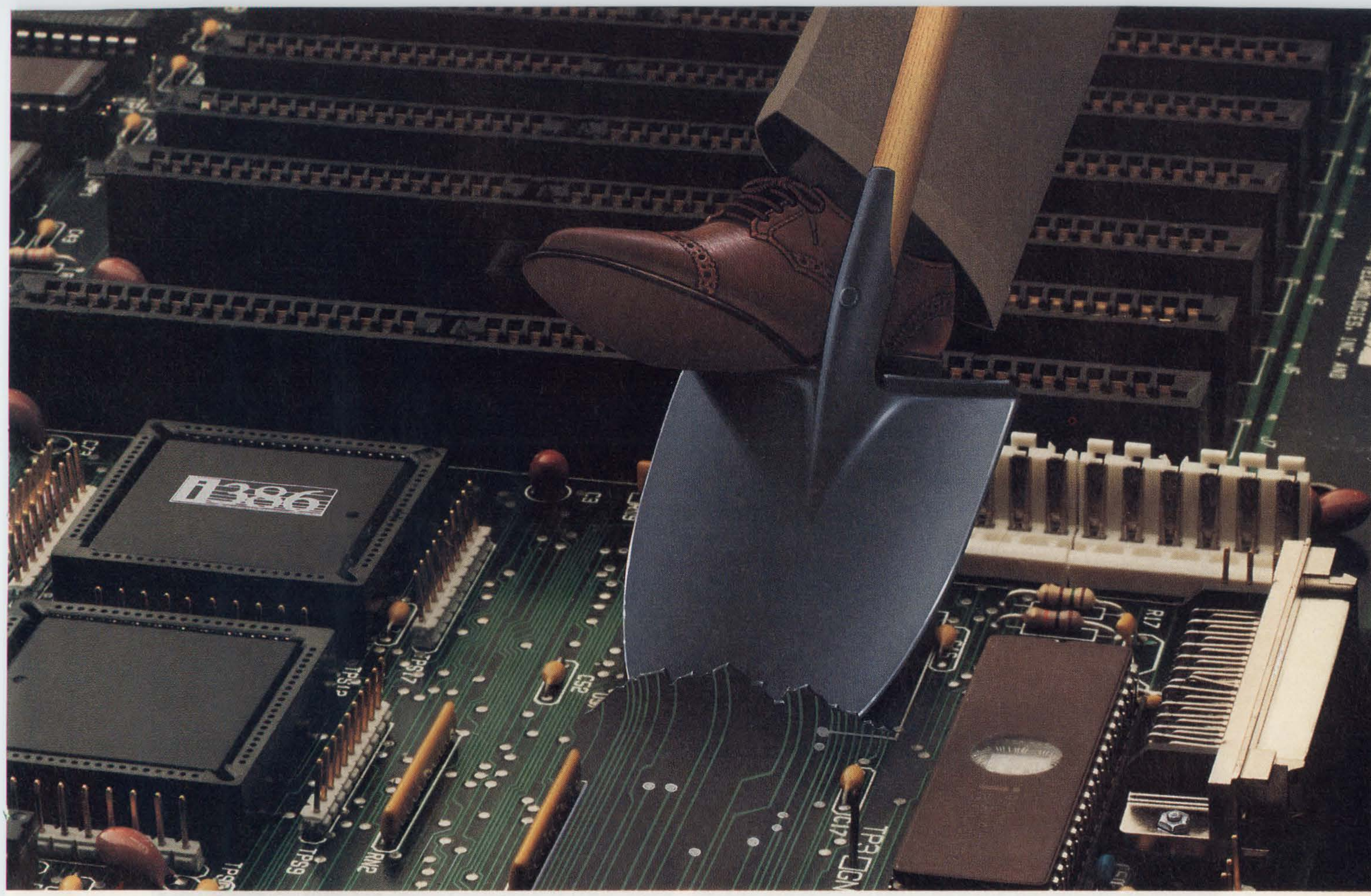
The two sets of fixed capacitor plates (Ys and Zs) are electrically connected in parallel within the chip (at the base of the anchors). This forms a pair of independent capacitors, X-Y and X-Z, with the moving plate X consisting of all of the fingers extending from the proof mass *(Fig. 3)*. Circuitry within the chip connects the three plates to the on-chip signal-conditioning circuits.

When at rest (experiencing constant velocity), each of the fingers forming the movable plate X is positioned by the tether an equal distance between a pair of fixed-plate fingers. That is, when at rest, each X finger is equidistant from a Y finger and a Z finger. When exposed to deceleration (a crash) or acceleration, the moving Y and Z fingers move toward one set of the fixed X fingers, and away from the other. The relative motion creates unequal distances, and therefore unequal capacitances, between the movable plate and each set of fixed plates. For example, if the mass moves to the right, the capacitance value between it and the Z plate increases while the capacitance value between mass and the Y plate decreases. In the equivalent circuit of the sensor, the moving X plate is shown closer to the Z plate *(Fig. 2c, again)*.

Although the ADXL50's sensor



1. LARGE ACCELERATIONS **of up to ±50 g can be measured by this tiny sensor that's surrounded by signal-conditioning circuits, all on one chip. Designed for automotive air-bag deployment, the ADXL50's proof mass is part of a differential and variable capacitor whose common plate moves in the plane of the chip.**



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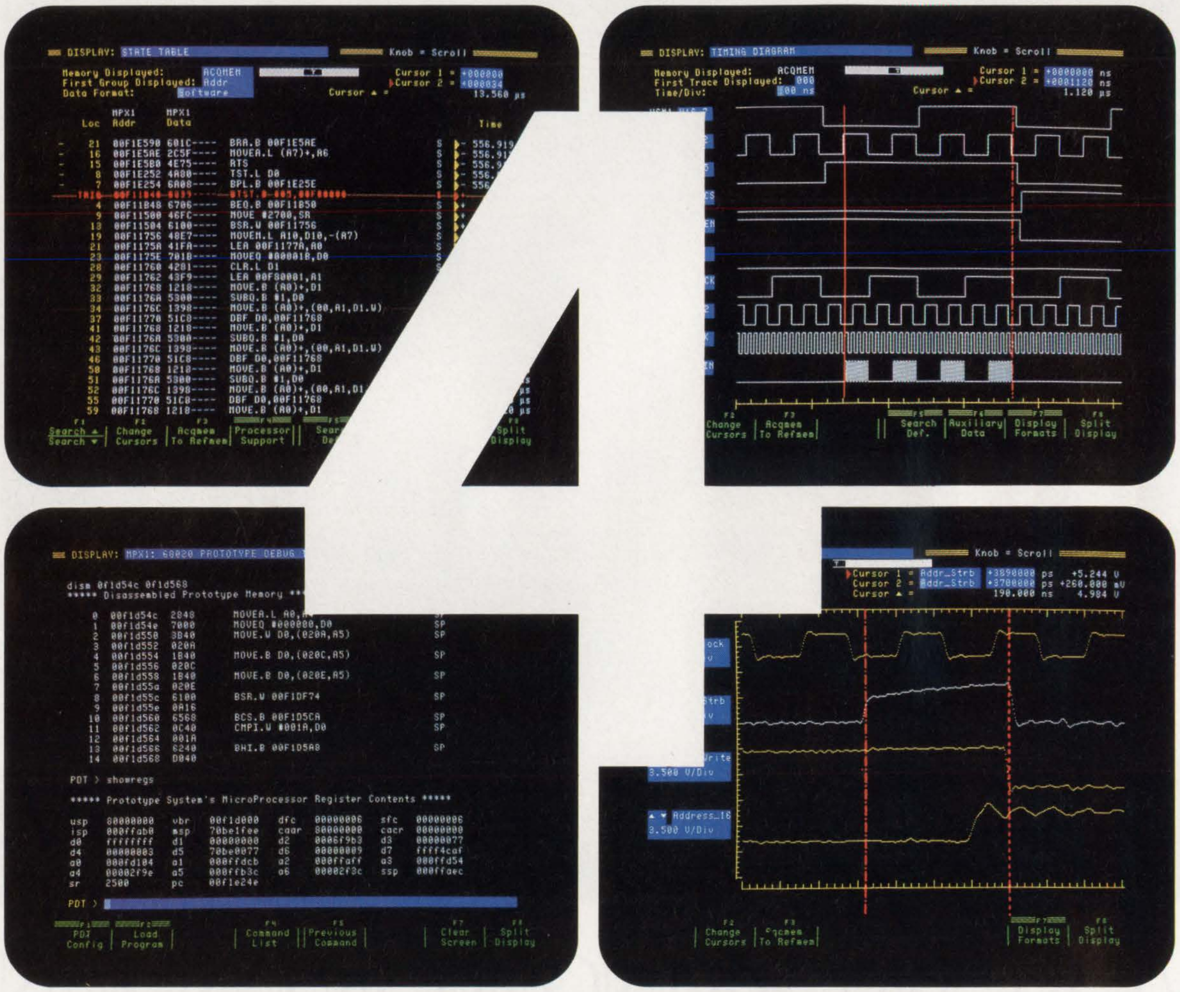


±50-g IC ACCELEROMETER WITH SIGNAL CONDITIONING

and circuit actually form a closed, force-balance feedback loop, operation is best explained first by describing open-loop operation *(Figs. 2a, 2b, and 2c, again).*

Complementary (equal in amplitude but 180° out of phase) 1-MHz square waves V_A and V_C are applied respectively to the Y and Z plates. At rest (equal capacitance between the moving Y and Z plates and both sets of fixed X plates), equal amplitudes of waveforms V_A and V_C are coupled to the movable plate where they subtract from each other, resulting in a waveform V_B of zero amplitude. However, when the sensor experiences acceleration—for example, if X moves closer to Z—the amplitude of V_C coupled to X is greater than that of V_A. When subtracted from each other, a square wave exists at point X, the output of the moving plate V_B. Its amplitude is the analog of both the magnitude and the direction of the acceleration.

A buffer amplifier converts the variable capacitor's high source impedance to a low impedance which drives a phase-sensitive demodulator (a full-wave rectifier running in synchronism with the 1-MHz excitation signal). The demodulator contains a low-pass filter (an off-chip capacitor) and provides a low-frequency (dc-to-1000-Hz bandwidth) analog voltage representing the signature of the acceleration. This voltage is applied to a preamplifier whose output goes off chip along with the minus input and the output of the output op amp.

Users can control signal bandwidth and amplitude with the off-chip capacitor C, and the off-chip resistors R_1, R_2, and R_3. The airbag system digitizes the signature, and applies it to a special-purpose digital-signal processor circuit, which makes the decision to deploy. Adding capacitors to the resistor network around the op amp can provide antialiasing filtering for the analog-to-digital converter circuit.

A typical automotive system runs off one positive supply rail, so the chip's output can't easily swing negative. Therefore, an offset voltage (1.8 V) from a reference is added to the preamplifier and to the op-amp input.

Nominal output (no acceleration) is 1.8 V. Now the output can swing more positive to indicate positive (increasing forward velocity) acceleration, and less positive to indicate negative (decreasing forward velocity) acceleration. Both are needed in the airbag application because a built-in test of the complete accelerometer is made every time the ignition switch is turned on. Positive acceleration is simulated during test to ensure that the airbag is *not* deployed. It's implemented by applying voltage pulses between the fixed and movable plates, creating an electric field between them that attracts the X plates toward one set of fixed plates (Y or Z).

The equation for acceleration, $A = x(k/m)$, indicates that the phenomenon is a function of the displacement x of the mass and the spring constant k. In an open-loop system, the measured displacement then becomes a function of the oscillator's amplitude and frequency; the parasitic capacitance within the chip; and the transfer functions of the buffer, demodulator, and filter. All of these are functions of time and the automotive temperature range (–55 to +125°C). In addition, the spring constant of the polysilicon tether can change with time and temperature. Put together, they can all add up to prevent meeting the 3%-to-5% accuracy specification needed.

To desensitize the accelerometer from time and temperature effects,

AUTOMOTIVE ACCELEROMETERS

Automobiles represent a large and growing application for accelerometers. Although the major emphasis for accelerometers is presently devoted to airbag deployment, they'll eventually be used in antilock braking systems (ABSs), where ±1 g of acceleration is needed; automatic door locks (±5 to 10 g); and active-suspension systems (±20 g).

Present airbag-deployment accelerometers are electromechanical. Multiple sensors are connected in series and parallel and are distributed throughout the vehicle, adding to wiring-harness weight, cost and complexity. Each sensor employs a proof mass working against a spring. When displacement occurs, the mass closes or opens a circuit. The sensor system required for each individual vehicle model (two- or four-door sedan, station-wagon, etc.) is unique. In addition, the present system can't accurately evaluate the signature of the event. On the other hand, deployment systems using the ADXL50 will employ just one sensor and its associated circuitry located in the passenger compartment—potentially even on the steering column with the airbag. The signal-conditioning circuitry and the digital-signal processor can be programmed to handle different vehicle types. The improvement in reliability is rather obvious. When the ADXL50's specifications are compared with those required by automotive makers for airbag deployment, it easily meets them *(see the table).*

ADXL50 VS. INDUSTRY REQUIREMENTS

Specification	Industry requirement	ADXL50
Unit cost	\$10	\$5
Measurement range	±50 to ±100 g	±50 g
Noise	Less than 1 g	0.12 g
Frequency range	dc to 1000 Hz	dc to 1000 Hz
Temperature range	–50°C to +125°C	–50°C to +125°C
Absolute accuracy over temperature and supply voltage	>5%	3%
Linearity	>1%	0.5%
Shock survival	2000 g	2000 g
Power supply	5 V	5 V
Output	High level, buffered	0.25 to 4.75 V

±50-g IC ACCELEROMETER WITH SIGNAL CONDITIONING

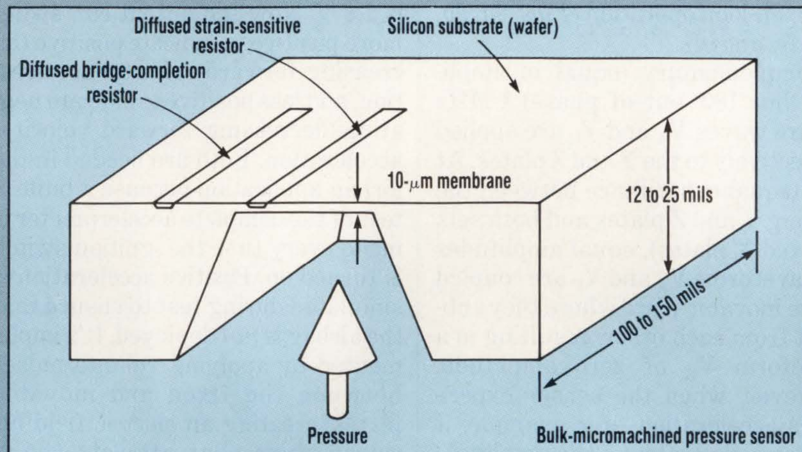
MICROMACHINING, BULK AND SURFACE

Most mass-produced automobiles built since the advent of EPA-mandated pollution-cutting engine-control systems contain bulk-micromachined silicon pressure sensors. Such a sensor, known as a manifold absolute-pressure or MAP sensor, measures the absolute air pressure at the intake manifold. It's built by etching a cavity virtually all the way through the bulk of a silicon wafer, leaving a thin (10-μm) silicon membrane as the pressure-sensing diaphragm *(Fig. A)*. One or more strain-sensitive piezoresistive resistors are diffused into the membrane, and additional resistors are diffused into the area outside the membrane. The resistors are connected electrically to form a Wheatstone (strain-gage) bridge.

A bulk-micromachined accelerometer is built in a similar manner *(Fig. B)*. The center section of the membrane is left thick to form the proof (inertial) mass. The displacement of the mass during acceleration, perpendicular to the rest of the die, is a direct function of acceleration. With the exception of four small bridges holding the mass, the membrane is etched through. The bridge's spring constant provides the restraining/restoring force that determines how far the mass will move (i.e. its sensitivity). Piezoresistive resistors are diffused into the mechanical bridges, and bridge-circuit completion resistors into the remaining silicon. Signal conditioning for both sensors is similar.

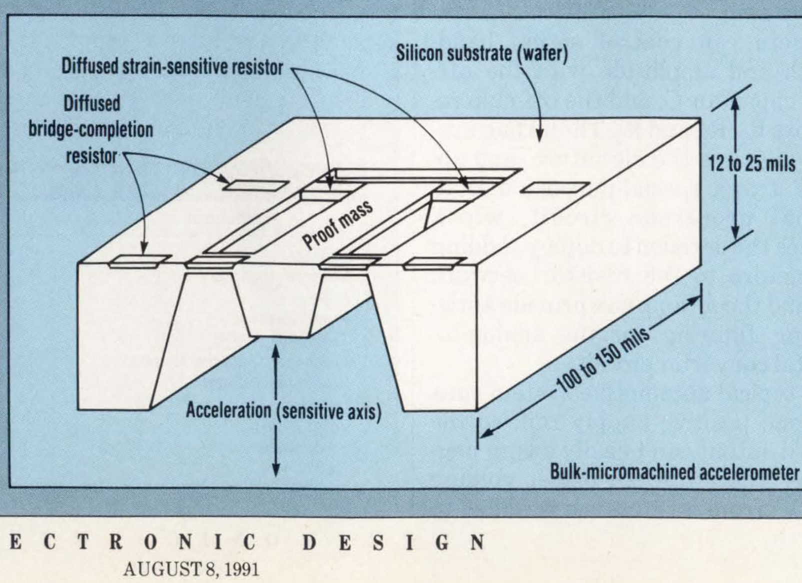
At first glance, this looks like a good approach. Typical full-scale voltage from the bridge is 250 mV (relatively easy to bring to a full scale of 2.5 V). Moreover, bulk micromachining of silicon is a mature technology.

There are problems, though. For one, trimming and temperature-compensating the piezoresistive bridge signal is a nightmare. The bulk process also isn't readily compatible with the process flow in a standard IC fabrication facility. For another, a minimum-sized sensor on a minimum-sized chip was desired. The smaller size means more ruggedness and lower cost. A bulk-micromachined sensor, on the other hand, requires between 10,000 and 25,000 mils^2 of silicon for the sensing element alone. Signal-conditioning circuitry could double the silicon area. Yet Analog Devices wanted the sensing element plus the signal-conditioning on one chip, to save space and for reliability (MAP sensors use off-chip signal conditioning). The reasoning for this should be obvious. If a MAP sensor dies, the car dies. If an air-bag-deployment sensor dies, the driver could be in serious jeopardy.



Bulk-micromachined pressure sensor

Surface-micromachining, on the other hand, allowed Analog Devices to build a rugged sensor and circuit, on one small chip, that was virtually insensitive to time and temperature effects, over the automotive-temperature range. The device is built on BiMOSII, a relatively mature 4-μm, 26-V, biCMOS process which has been intertwined with micromachining. In the sensor area, a 1-μm thick sacrificial oxide is deposited on the passivation dielectric. Openings are etched through both insulators to n$^+$ diffusions in the substrate made earlier. A 2-μm thick slab of polysilicon is then deposited on the oxide, and the n$^+$ diffu-



Bulk-micromachined accelerometer

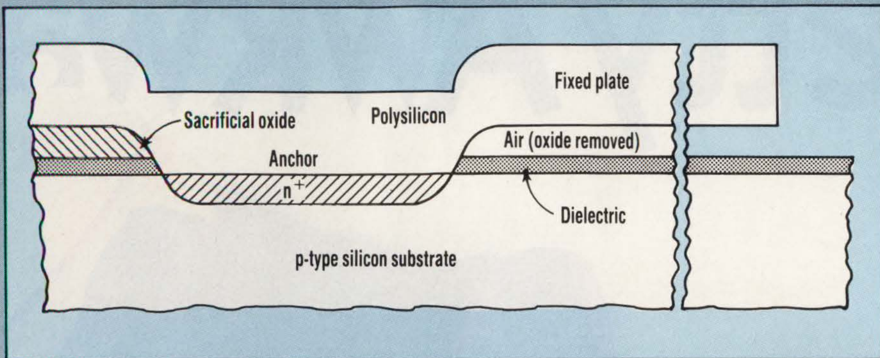
Analog Devices' design team went to a closed-loop force-balance architecture *(Fig. 4)*. To simplify the figure, the sensor has been replaced by its equivalent circuit.

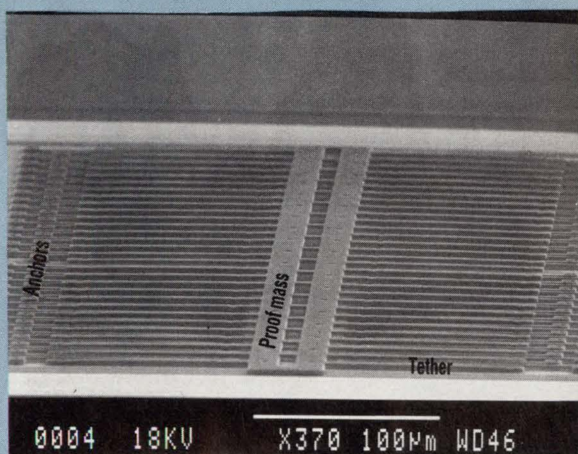
With the exception of the square waves driving the fixed plates of the sensor, the active and passive elements of the closed-loop design are identical to those of the open-loop approach. These carrier waveforms (V_A and V_C) are now riding on positive and negative dc-reference levels: $+V_R$ (3.4 V) and $-V_R$ (0.2 V). The negative-feedback loop will try to drive the 1-MHz signal, V_B, on the moving plate. This indicates proof-mass displacement, to zero, by modulating V_0 (preamplifier output). That is, the dc voltage at the output of the preamplifier is applied to the moving capacitor plates (via the feedback path). It creates an electrostatic force between the fixed and moving plates that opposes the inertial force of the mass and restores the mass to the neutral position, reducing V_B to zero. The preamplifier output signal is thus a direct function of the inertial force, and therefore of the acceleration. Because it's a high-gain servo loop, the proof mass actually will never leave its neutral position by more than 1/100 of a micrometer. The spring constant k, as well as the other open-loop error sources, are embedded in the loop gain. With no acceleration, $V_O = 1.8$ V. At full acceleration (±50 g), $V_O = \pm 1.0$ V.

An accelerometer isn't a typical IC that can be stuck anywhere on a pc board, pointing in any direction. Its sensitive axis must be lined up with the expected acceleration axis and that axis must be clear to the user. However, the ADXL50's axis is hidden in a hermetically sealed 10-pin TO-5 can. To meet that problem, Analog Devices mounted the chip in the package so that the sensitive axis lines up with the tab on the package's header *(Fig. 5)*.

What's Ahead?

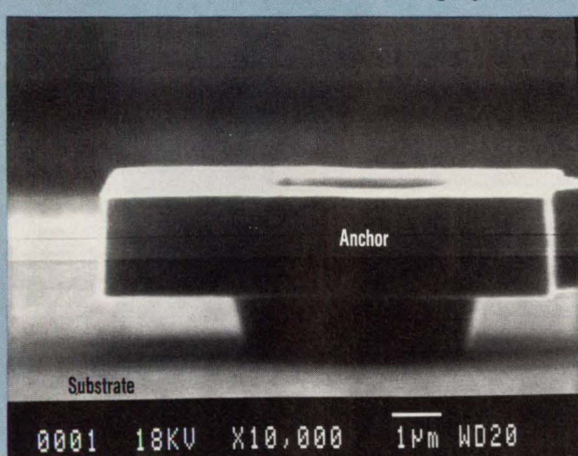
Presently, Analog Devices is concentrating on producing this chip in volume, following intense work on the design over the past 18 months.

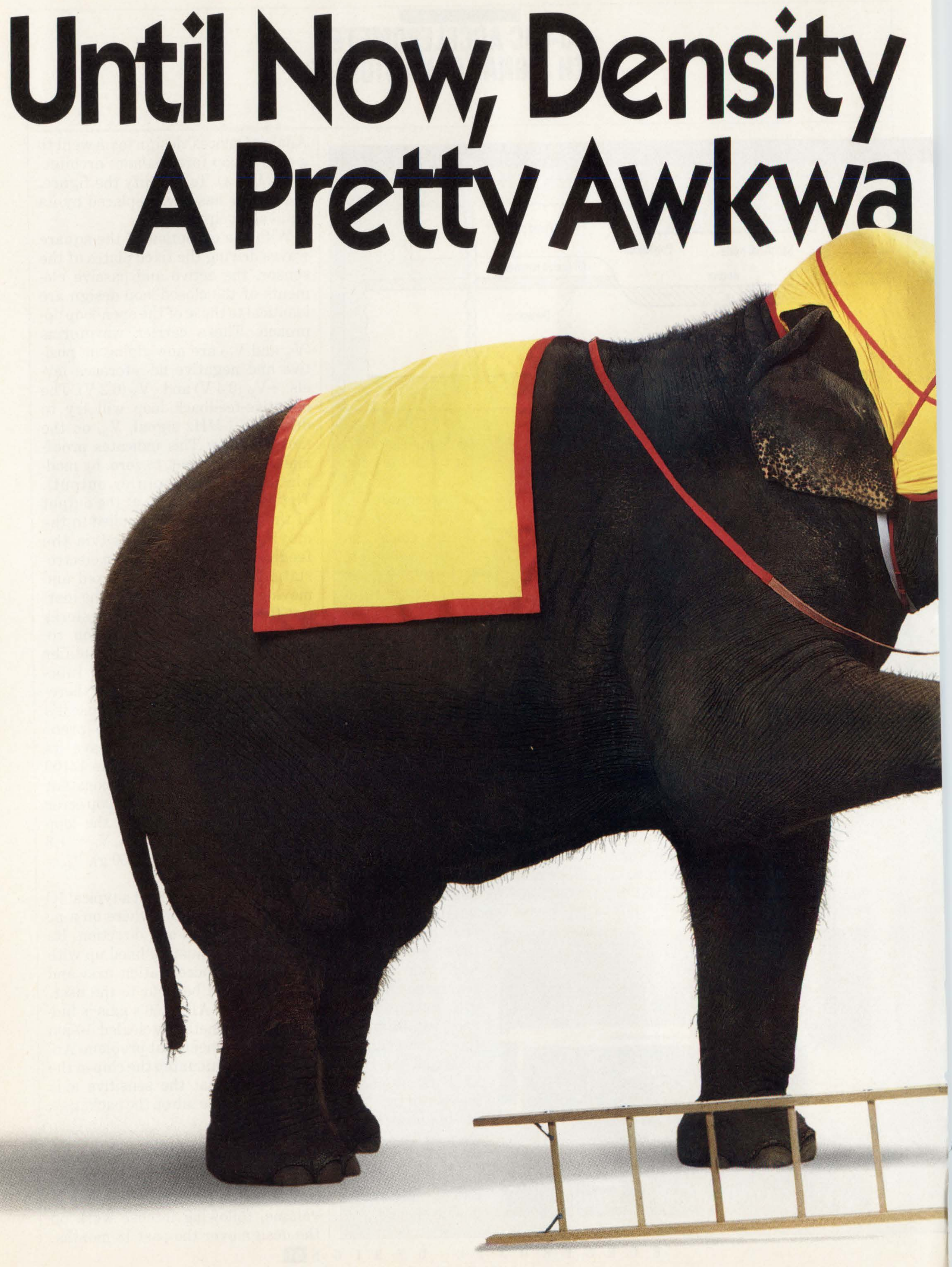




sions to which it makes a chemical (and electrical) bond *(Fig. C)*. The sacrificial oxide is then etched from under the polysilicon, leaving empty space.

The capacitor fingers are made by etching narrow slots in the now "floating" slab of polysilicon using an isotropic (unidirectional) reactive-ion etchent (RIE). The technique is similar to that used in making DRAM trench capacitors. Whereas 0.75-µm design rules and 1X (no reduction) lithography is used for the 4-µm circuitry, the trenches in the polysilicon are defined with a stepper using a 5X reduction lens to achieve the 1-µm spacing between the capacitor plates (the closer the spacing, the more sensitive the accelerometer). Accelerating 50 g results in a displacement of about 0.01 µm in a closed loop, and ten-times that for an open loop. Each of the 50 or so sets of capacitor plates are about 100-µm long *(Fig. D)*. The polysilicon deposited on the n^+ diffusion, through the opening in the oxide and dielectric, forms the single anchor for each cantilevered fixed capacitor plate and the two anchors supporting each of the simple-beam tethers *(Fig. E)*. The diffusion also interconnects the plates and signal-conditioning circuits.

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MACH 120*	1200	48	15ns	50 MHz	68	MASC 120
MACH 220*	2400	96	15ns	50 MHz	68	MASC 220
MACH 130	1800	64	15ns	50 MHz	84	MASC 130
MACH 230*	3600	128	15ns	50 MHz	84	MASC 230

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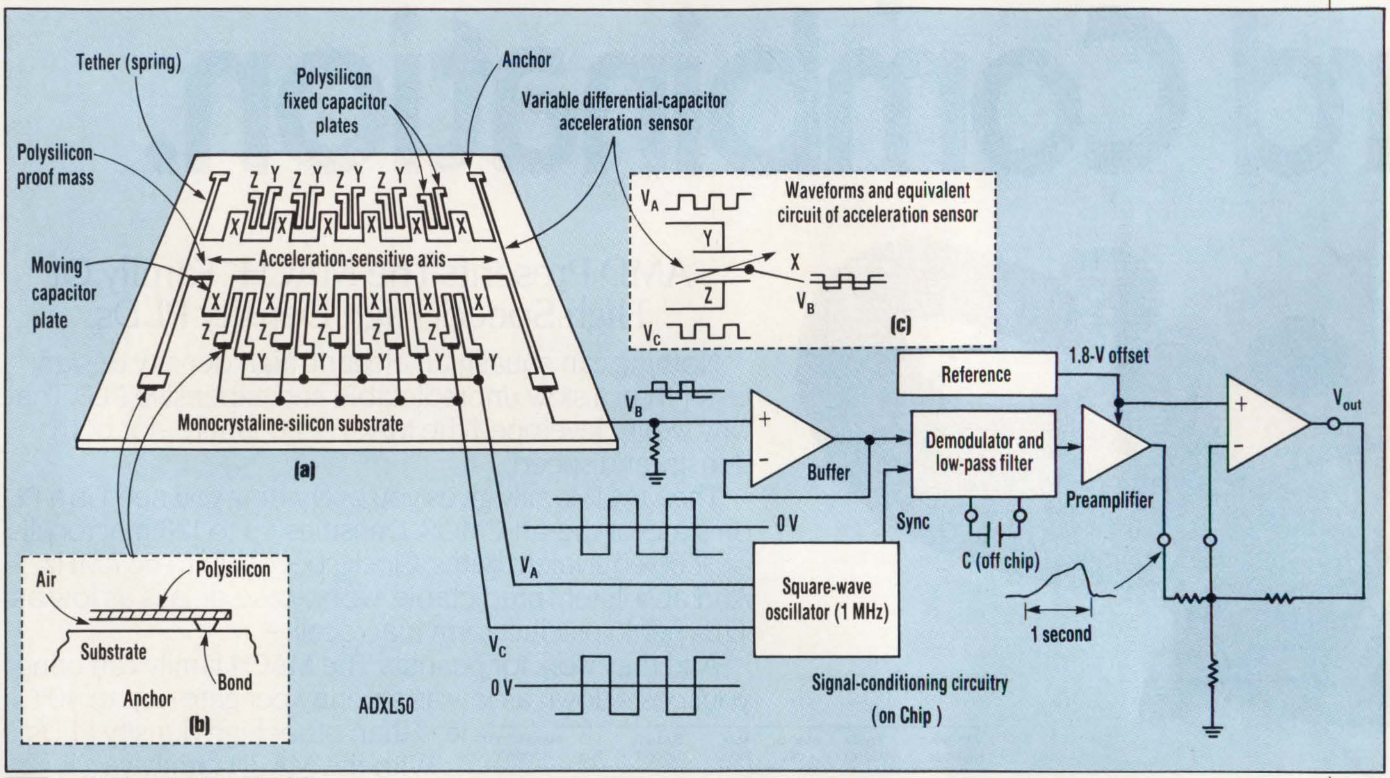
±50-g IC ACCELEROMETER WITH SIGNAL CONDITIONING



2. THE PROOF MASS of Analog Devices' IC accelerometer is surface-micromachined from polysilicon. Its fingers (X) form the moving plates of a variable differential capacitor (a). These moving X fingers as well as the stationary Y and Z fingers are simple cantilever beams held off the chip by silicon-bond anchors (b). Complementary 1-MHz square waves are applied to the micromachined fixed plates (Y and Z). The differences in the square waves' amplitudes are picked off the accelerometer's main part of the proof mass formed by the X fingers (c).

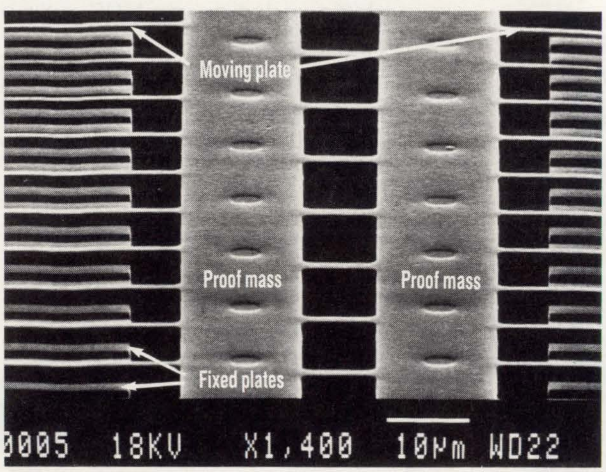
However, in about a year, you'll start seeing additional members to their accelerometer family rated for both higher and lower levels of g. The ultimate goal is to have devices rated from fractions of a g to several 1000 g.

Outside the automotive market, who needs \$5 to \$50 accelerometers with a linear output? At the low-g end, there are applications in levels, inclinometers, and tilt meters. If acoustic rangefinders can replace measuring tapes, how about an electronic framing square?

In the midrange of g levels, there are applications in shock recorders that accompany the shipment of expensive and fragile equipment. The recorders keep track of accelerations experienced along the way, in case damage is apparent on arrival.

High-g applications range from smart munitions to sports, like instrumenting a baseball. This isn't some wild concept, because there are now baseballs for the blind where the ball continuously produces an audible beep! A golf ball may be more difficult.

However, the major application for low-cost, accurate accelerometers is probably in vibration sensing for "machine health" and preventive maintenance. The goal is to determine the vibration signature of a normally operating machine and that of a machine needing maintenance (for example, due to bearing wear). Vibration sensors (accelerometers) mounted on or embedded within the machine constantly monitor its signature and feed it to a digital-signal processor that can



3. AN SEM microphotograph of the ADXL50 IC accelerometer shows the surface-micromachined fixed and moving plates of a differential and variable capacitance. These were created using 1-μm lithography, with steppers defining the areas of polysilicon to be reactive-ion etched.

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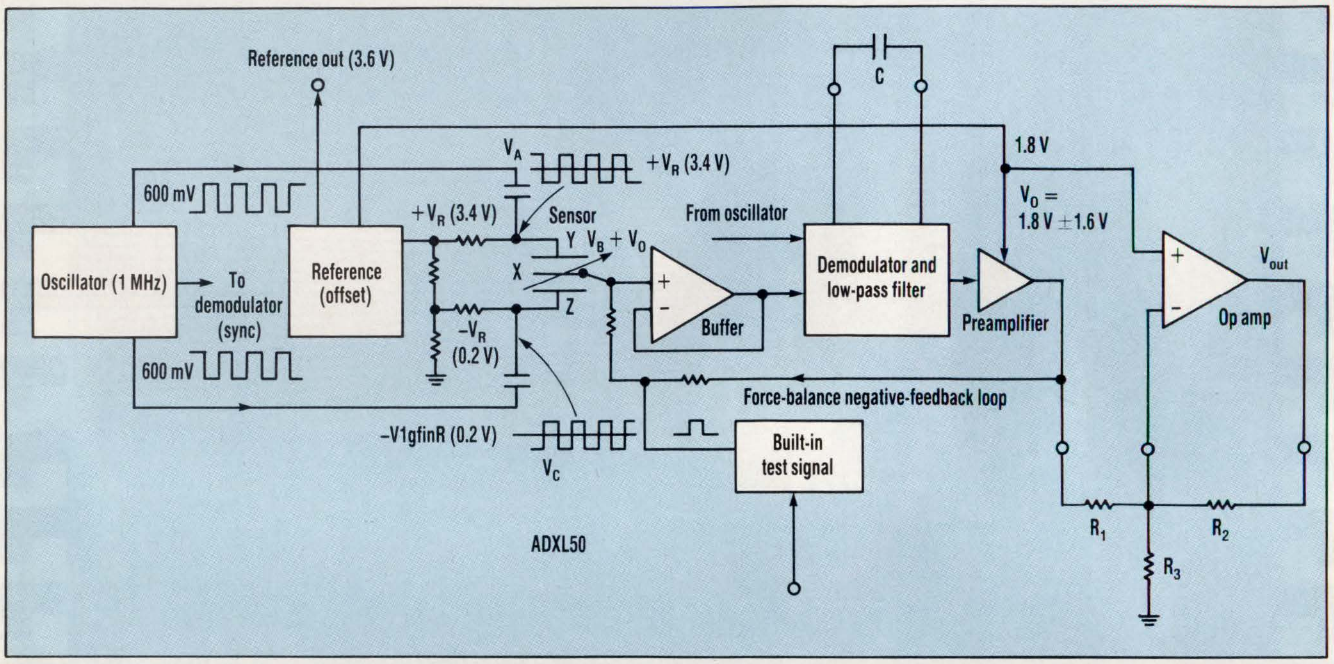
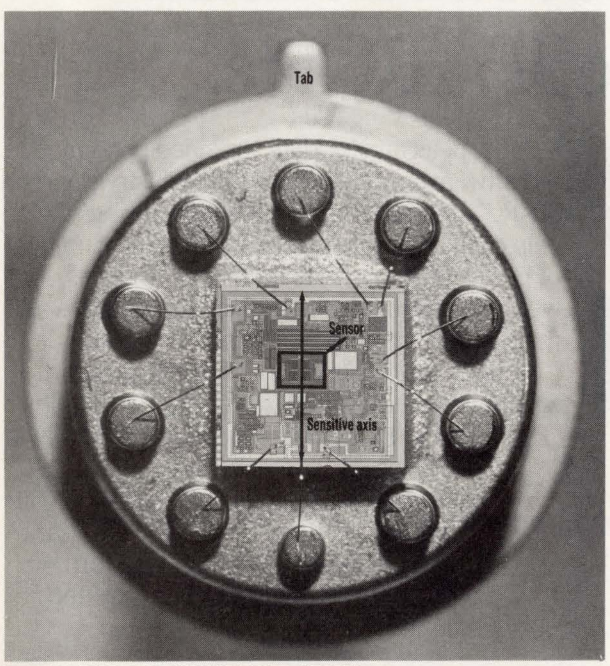
±50-g IC ACCELEROMETER WITH SIGNAL CONDITIONING



4. THE FORCE-BALANCE FEEDBACK LOOP of the ADXL50 IC accelerometer creates an electrostatic force between the fixed (Y) and (Z), and moving (X) plates of a differential and variable capacitor. The force restores the proof mass to its neutral position.

distinguish between good, bad, and different signatures, and alert the machine's operators and/or even shut it down if necessary.

Vibration-sensing and preventive-maintenance applications range from large rotating machinery, such as those found in power plants, to precision machine tools where tool wear can be sensed. The ADXL50 accelerometer is a natural for the transportation industry, where it can not only monitor power plants (from jet engines to truck and marine diesels), but also keep track of major shocks received by the structure (such as hard landings). Here the goal is to anticipate early machine fatigue that can cause major disasters.



5. THE SENSITIVE AXIS of the ADXL50 IC accelerometer in the center of the chip is lined up with the tab on the outside of the 8-pin TO-5 can. This allows the axis to be installed parallel to the expected acceleration phenomenon.

The technology of surface micromachining will permit the next generation of Analog Devices accelerometers to offer multiple sensors (complete with signal conditioning) per chip. These can be used in several ways. If mounted orthogonally they can sense acceleration vectors, which in the airbag application can help the digital-signal processor determine if a crash did occur. Two or more sensors with the same sensitive axis can provide redundancy and/or can lend themselves to "voting" type decision-making by the processor.□

PRICE AND AVAILABILTY

The ADXL50 comes in a 10-pin TO-5 can. In automotive volumes, the ±50-g accelerometer is expected to sell for about $5 each by 1994 ($5 in volume was the first specification set on day one when the development program started). The present price is $21.75 each in quantities of 1000.

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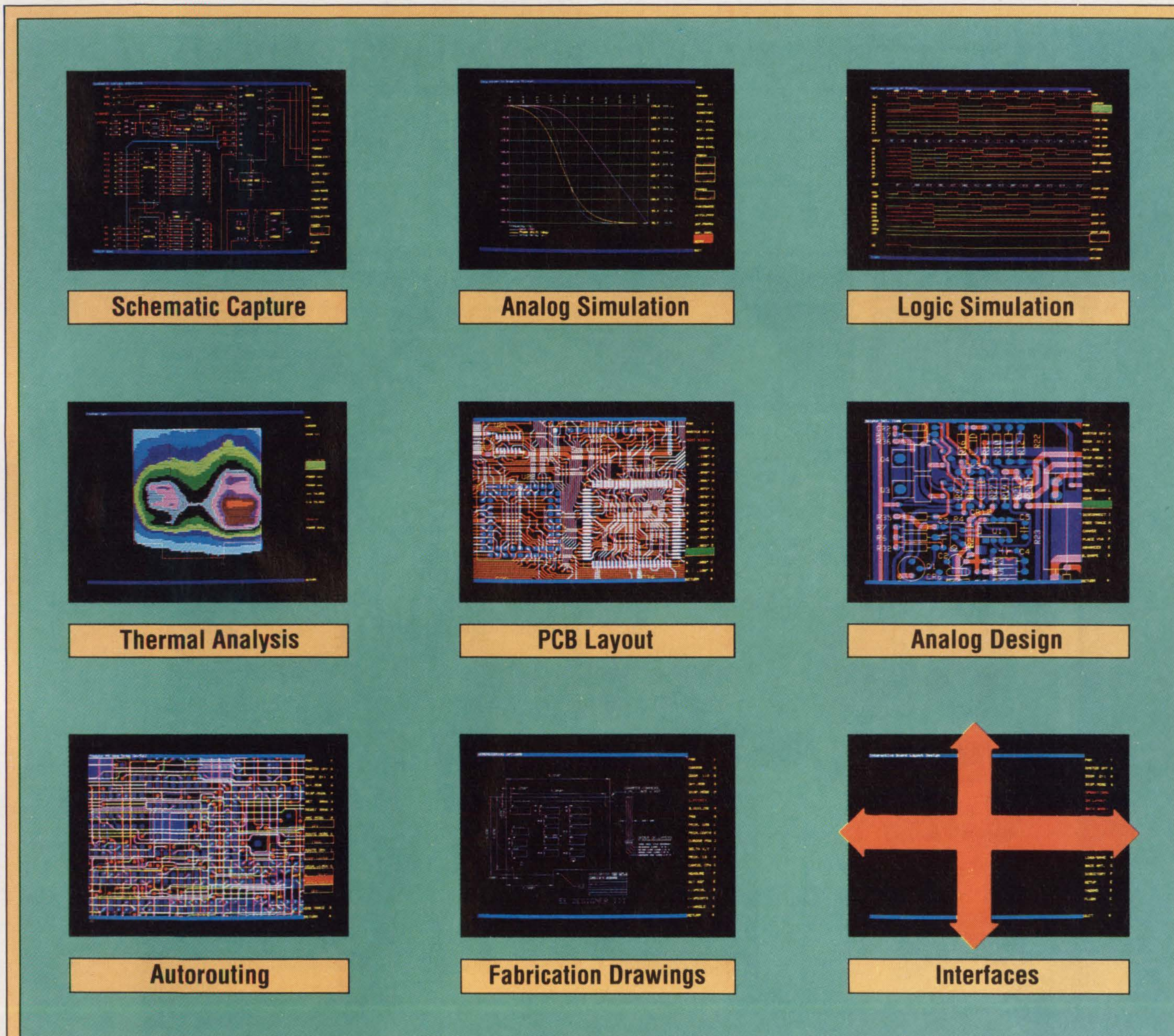

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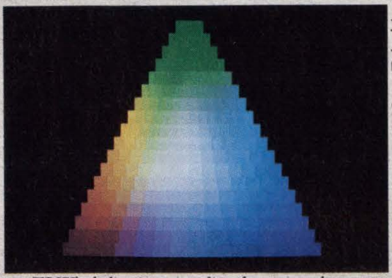

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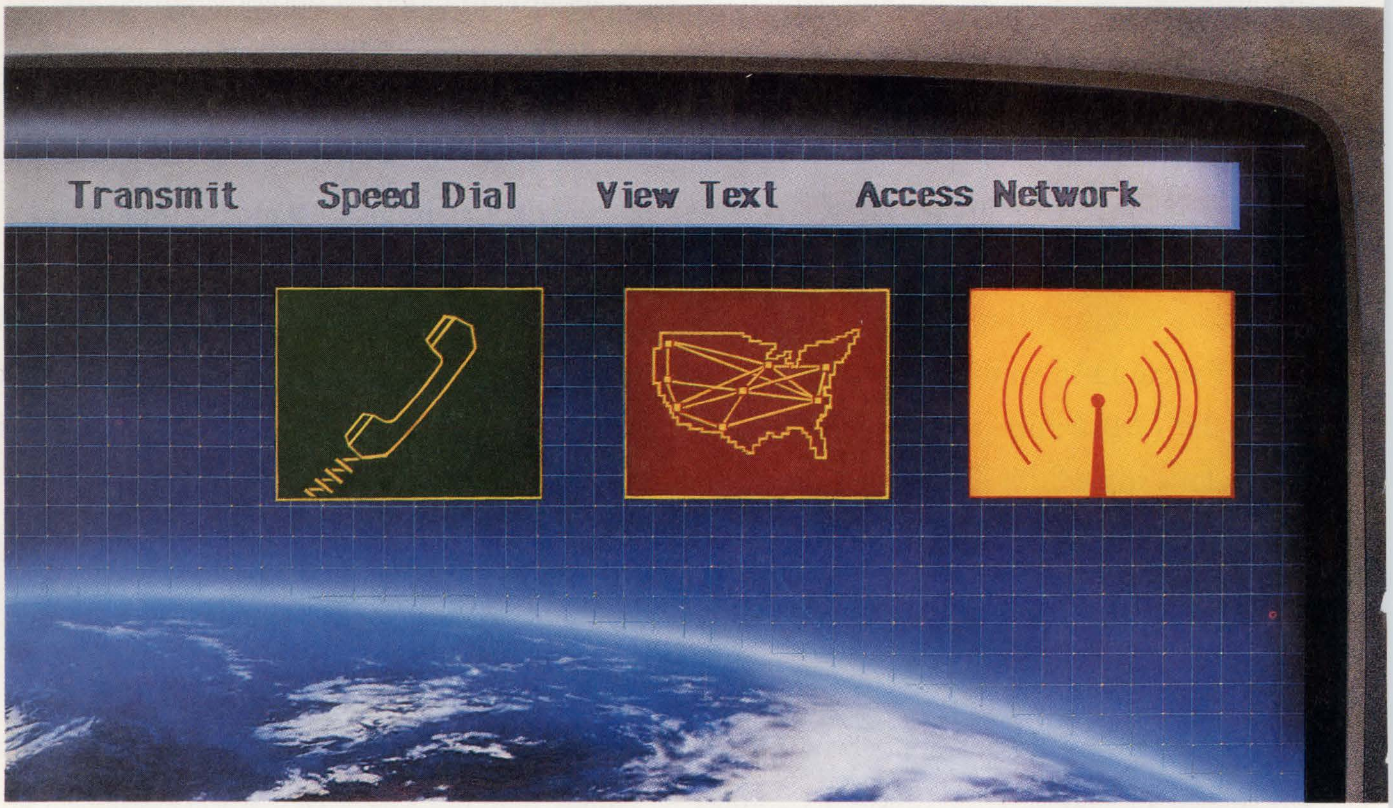

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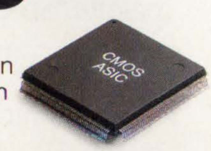

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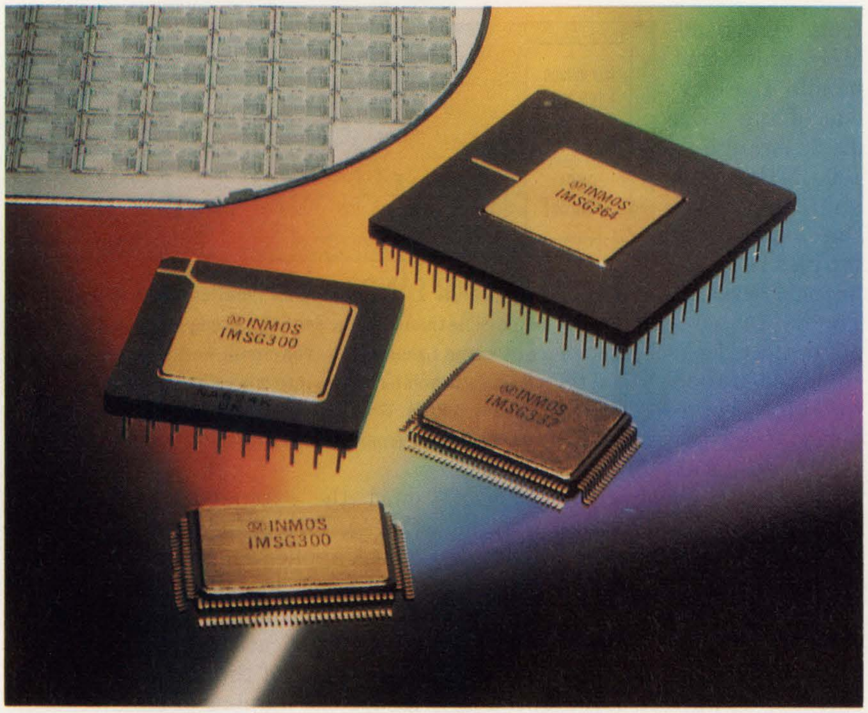


DAVE BURSKY

THE LATEST RAMDACs OFFER MORE SIMULTANEOUS COLORS AND HIGHER LEVELS OF INTEGRATION.

RAMDACs Enhance PC and Workstation Displays

Numerous advances in display control circuits and combination digital-to-analog-converter and memory chips have yielded the scintillating graphics of today's workstations and PCs. These combination DAC and memory chips, known as color palettes or RAMDACs, feed the red, green, and blue (RGB) signals to the displays. But as PC display resolutions push into the megapixel realm and workstations move to multi-megapixel levels and true-color 24-bit images, RAMDACs are being driven to their performance limits. Future-generation RAMDACs must handle higher pixel rates, provide larger color palettes, and integrate more of the base-system logic.

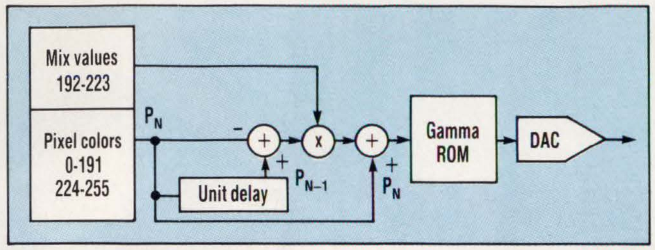
RAMDACs are gaining higher levels of integration with more functions being squeezed onto the same chip. Improved processing with faster and smaller transistors yields faster converters and logic, which translates into higher RAMDAC speeds and greater packing densities. The higher integration levels will bring about future RAMDACs containing a voltage reference, a sense comparator to detect the attached monitor type, and more memory or logic to implement or accelerate functions—a hardware cursor for example. A few companies have even incorporated the entire VGA controller on the chip with the RAMDACs, offering a true single-chip solution. *(see "Toward the single-chip video subsystem," p. 63).*

Although analog-video inputs have long been the standard for workstation monitors, the standard triple RAMDAC really didn't take hold in PCs until IBM introduced the video-graphics-array controller and changed the video interface from digital to analog. The original G171 triple 6-bit DAC and 256-word-by-18-

bit color palette memory from Inmos—adopted by IBM for VGA cards—spurred on a race between a dozen companies for compatibility and improved integration and performance. That race has put RAMDAC prices on a downward spiral. The basic VGA-compatible RAMDAC sells for well under $10 in large quantities. True-color devices, which are just entering the market, range from about $15 to over $100 (in lots of 10,000 or more), depending on features and clock frequency.

For high-end display systems, multiple single-channel RAMDACs would typically be employed by the workstation designers to get the highest-performance image generation. This includes such devices as Brooktree's 170-MHz Bt462, which packs a 1024-word-by-8-bit color palette, and the 360-MHz ECL-compatible Bt492 with its single 256-word-by-8-bit color palette. But this kind of performance comes at a price. Chips like the Bt492 cost several hundred dollars each. Triple units like the 200-MHz Brooktree Bt468 now provide the integration needed to make low-cost but high-performance workstations practical.

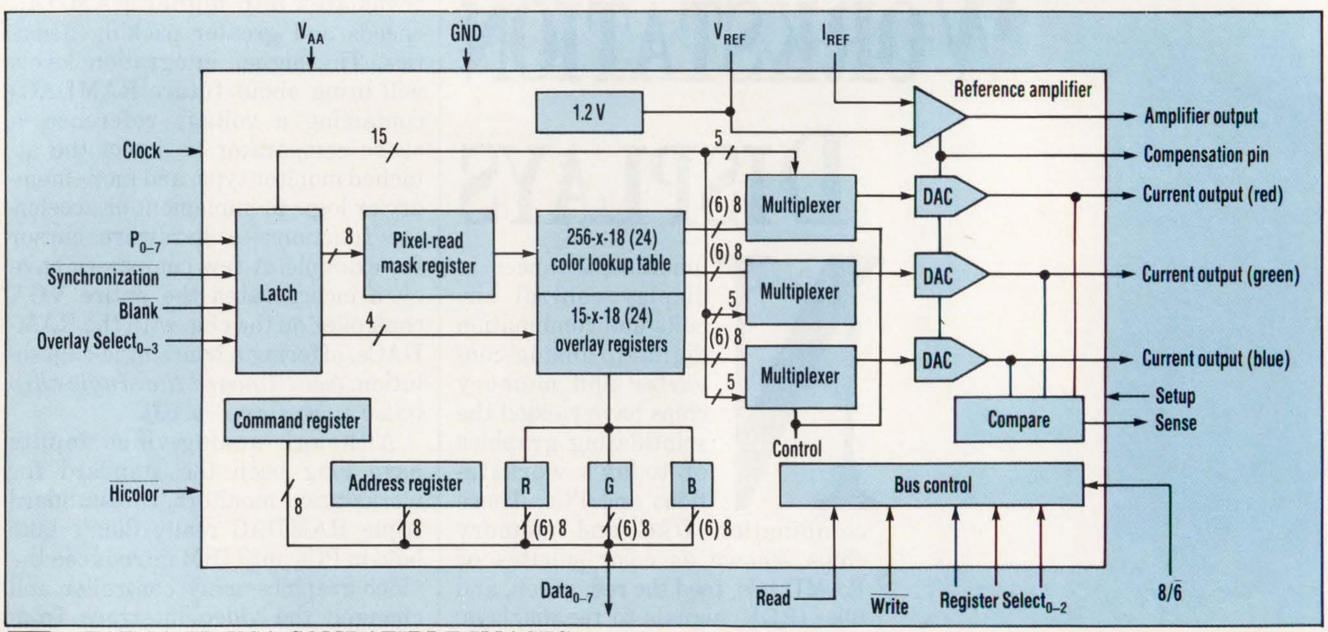
The integration race has spawned a wide choice of RAMDAC options and performance levels, ranging from simple 30-MHz units that handle the low-end of the VGA display range to 100 - MHz - plus units that drive the powerful workstation graphic screens. The 8514A standard that IBM released upped the pixel count but not the color palette, thus allowing speed-enhanced versions of existing RAMDACs to serve the higher-resolution market. Although the 8514A standard has been around almost as long as the VGA standard, its popularity is still restrained by the high cost of support silicon. Rather, designers have opted to push VGA performance up the curve so that the super-VGA chips deliver the same functionality minus the hardware assist from the 8514A logic. Consequently, today's high-end super-VGA cards deliver the 1024-by-768-pixel resolution with 256 simultaneously displayable colors.



1. SMOOTHER LINES or more simultaneously displayed colors are possible thanks to the continuous-edge graphics scheme developed by Edsun Laboratories. The circuit works by turning 32 of the color-palette pointer values into mix values and adding a gamma-correction ROM. Working RAMDACs that incorporate the algorithm are available from Analog Devices.

Most recently, IBM upped the PC graphics stakes one more time with the introduction of yet another standard, the extended graphics array (XGA). This standard plays off the 8514A application interface (the programmer's interface), and will run any 8514A software that was written to the application interface. Implementations of the XGA standard increase the number of simultaneously displayable colors, from the 256 available to VGA controllers to 65,536 when the XGA color screen employs the 640-by-480-pixel VGA resolution. At higher resolutions, the number of simultaneous colors drops back to 256.

Even though IBM seems to dictate new levels of baseline standards for PC graphics, many companies have created supersets, such as the 800-



2. TARGA OR VGA-COMPATIBLE IMAGES are supported by the Sierra HiColor RAMDACs. They read in 16 bits in two sequential bytes over the P input lines and interpret 15 of those bits as the 5:5:5-bit RGB signals for the Targa mode (the 16th bit is discarded).

by-600-pixel enhanced VGA mode, and, of course, the 1024-by-768-pixel super VGA mode. Those independently arrived at modes are now being standardized by the Video Electronics Standards Association, San Jose, Calif., so that one video driver routine can be used by all adapters and programs.

Some chip suppliers are experimenting with an "ultra-VGA" mode that provides 1280 by 1024 pixels. Those high pixel counts, coupled with the high screen refresh rates and noninterlaced displays needed to avoid flicker, pushes the clock rate of RAMDACs up to 85 MHz and beyond. It also forces the off-chip frame-buffer memories to transition from standard dynamic RAMs to the dual-ported VRAMs, because access rates hit 80 MHz.

The low-end of the VGA display market is extremely price sensitive, and any improvement in screen resolution has to come at minimal cost. That's just what Edsun Laboratories, Waltham, Mass., achieved when it developed an antialiasing scheme its calls continuous-edge graphics (CEG). RAMDACs incorporating CEG are fabricated for Edsun and sold commercially by Analog Devices as the ADV7141, 7146, and 7148. Those chips are designed to drop into sockets already established by the Brooktree Bt471, 476, and 478, as well as the SGS-Thomson (Inmos) G171 VGA RAMDACs.

With standard RAMDACs, the visual aliasing (jagged edges on what should be straight lines or curves) is the result of color truncation during image generation. The CEG algorithm compensates for the truncation by calculating the weighted average of two adjacent colors, and assigns shades of those colors to neighboring pixels to fool the eye into seeing a smooth edge (just as it would see if more pixels were used). To do the computations, the chip uses only 223 of the 256-palette pixel values to point to distinct colors; the remaining 32 values are interpreted as operation codes to compute specific mix ratios by on-chip CEG logic (the one remaining pixel code is reserved for internal use) *(Fig. 1)*.

Although such computations would be too burdensome for the host CPU that drives the VGA display, dedicated logic on the VGA RAMDAC keeps the computations to a minimum by reducing the color blending. Therefore, the current 8-bit VGA frame buffer and standard control, and BIOS software can be used. The chip also contains gamma correction to compensate for the nonlinear relationship of the screen phosphors to the displayed color. System upgrades then require that the non-CEG RAMDAC be replaced with the CEG unit, and the video-

TOWARD THE SINGLE-CHIP VIDEO SUBSYSTEM

To reduce the board space occupied by the color-display subsystem, chip designers have gradually integrated many system functions onto one chip. Already, multiple digital-to-analog converters have been integrated onto one chip along with the RAM that forms the color lookup table. More recently, designers have integrated some of the simple support functions. One such function is a comparator that helps to determine the monitor type attached to the display output. Other functions moving onto the RAMDAC include the voltage reference and video timing circuits that sometimes incorporate control for the high-speed video RAMs.

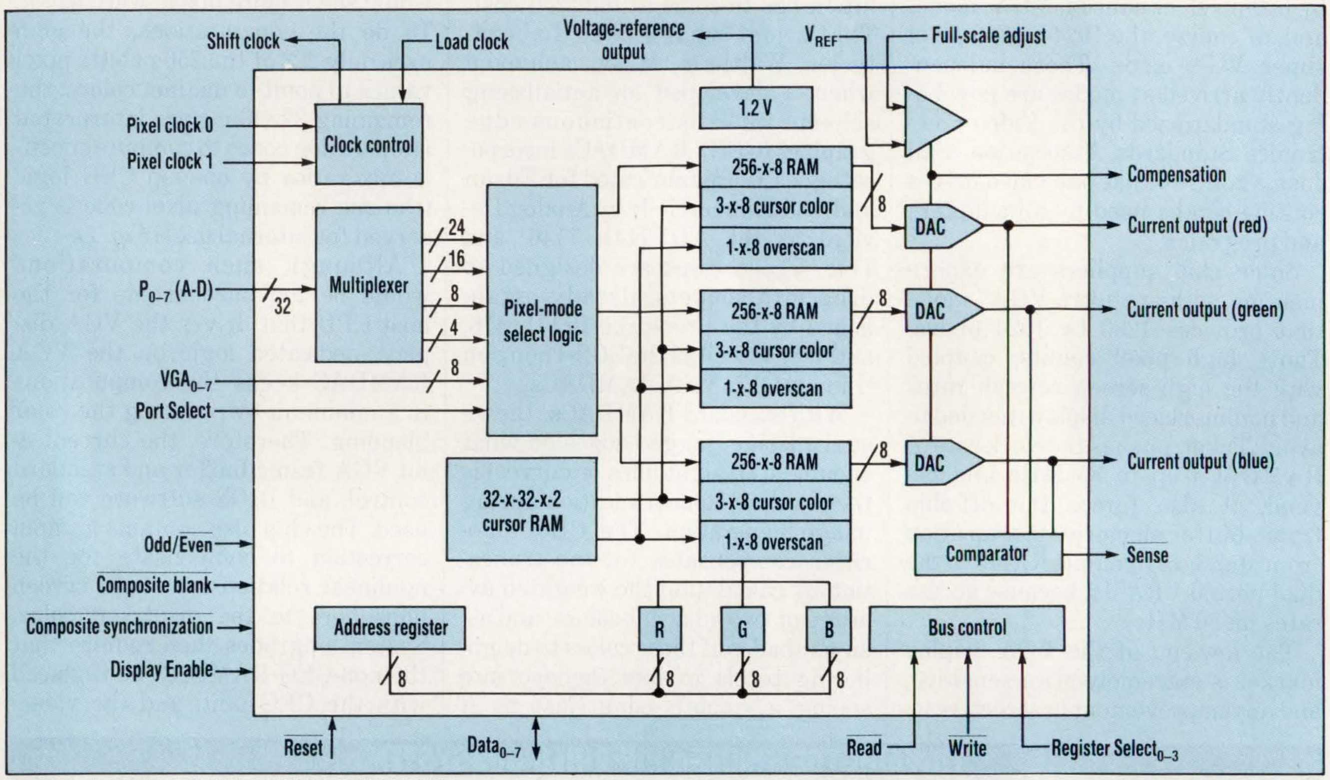
Several companies—Acumos, Chips and Technologies, Cirrus Logic, S-MOS Systems, Western Digital, and a few others—have taken the next step of integrating the digital VGA controller onto the RAMDAC chip. These companies have reduced the board area required for a color display controller to just two or three square inches and just six chips.

For example, Acumos' AVGA1 and the forthcoming AVGA2, which combine RAMDACs and full-VGA controllers, claim the highest level of integration. The chips also support the extended 800-by-600-pixel 16-color display mode. Programmable memory-timing clocks can be internally generated at frequencies up to 44.7 MHz.

The AVGA2 packs the same basic functions but is aimed at super-VGA displays. It can operate at internal clock rates up to 65 MHz, addresses up to 512 kbytes of external DRAM (the AVGA1 addresses only 256 kbytes), and delivers 256-color displays with resolutions of 800 by 600 pixels, or 16-color images with 1024-by-768-pixel resolution.

Taking aim at portable systems, S-MOS Systems has applied a low-power CMOS process to the design of the highly integrated SPC8100 chip. The process lets the chip dissipate just 1% of its 1-W active power level when in standby. With the high level of integration, the designer can implement a complete VGA display subsystem with just five components—the controller, two 64-kword-by-16-bit DRAMs, and two clock oscillators. Designers opted to keep the clock oscillators off the chip so that the on-chip power-management logic could be used more efficiently. Thus, four power-down modes were set up so that intelligent power-management features could be employed by the system.

The 82C455 from Chips and Technologies, the CG-GD6340 from Cirrus Logic, and the 90C12 and 90C20 from Western Digital also aim at portable system applications. The Cirrus chip actually supplements a flat-panel chip set or single-chip controller and can make a standard 8-color LCD panel appear as if it had 256 simultaneously displayable colors. Gaining some degree of distinction, the 90C20 from Western Digital was recently selected by IBM Corp. for use in its latest-generation laptops. It supports both LCD and CRT operating modes.



3. A SEPARATE CURSOR RAM and a three-word color memory let Brooktree's Bt484 RAMDAC accelerate cursor operations for such software as Microsoft Windows 3.0. Additional logic integrated on the chip supplies the voltage reference and the display comparator.

driver software be updated. With the algorithm activated, VGA monitors can appear as though they have 1280-by-1024-pixel resolution, even though only 640 by 480 pixels might be displayed.

The CEG algorithm can also be employed for applications other than boundary smoothing. The mixing (or subtle shading) could help generate solid models or display photographs. With 32 blends of 223 colors, up to 792,000 colors can be simultaneously displayed. Software drivers have been written for Lotus 1-2-3, AutoCAD, and Windows 3.0, and more are expected later this year. No modifications are needed to the application software. However, the modified drivers may increase the execution time by a small amount.

Some RAMDACs are being developed with more colors instead of higher resolution. The SC1148x family of HiColor RAMDACs from Sierra Semiconductor boosts 8-bit (256-color) pseudo-color images to 15-bit (32,768-color) images. The top-of-the-line chip in the series, the SC11484, includes triple 8-bit DACs with a 256-word-by-24-bit color lookup table (CLUT), and 15 24-bit overlay registers that help eliminate software typically associated with overlay cursors, grids, menus, and EGA emulation *(Fig. 2)*.

The HiColor chips use 15 of the 16 available bits, conforming to the Targa format defined by Truevision, Indianapolis, Ind. In this format, 5 bits are used for each of the RGB signals. The overlay registers help the chip maintain color integrity when multiple windows are displayed and the user switches back and forth between them. Clock rates of 50, 66, or 80 MHz can be selected, depending on the display resolution. Antialiasing is also supported to improve the displayed-line smoothness.

Sierra also released another family of RAMDACs—the SC11485, 7, and 9—which support the full 65,536-color choice of the XGA standard. The chips can also handle the 15-bit Targa format and the standard 256-color VGA modes. By operating at 80-MHz clock rates, the RAMDACs can drive 1024-by-768-pixel displays with flicker-free 70-Hz noninterlaced refresh rates. Although these chips provide the XGA color variety, when coupled with VGA and super-VGA controllers, they don't offer the same drawing speed. XGA implementations are many times faster, because many of the basic drawing operations are accelerated by dedicated circuits.

The recently released Bt484 RAMDAC from Brooktree Corp. is a good example of how high-performance RAMDACs can add "snap" to drawn images, and can expand to true-color images with more memory. The chip controls external video RAMs (VRAMs). It also enables designers to build systems with adjustable color depths of 4, 8, 15, 16, or 24 bits per pixel, and system clock frequencies of up to 85 MHz. Not only does the chip pack the triple palette memories, but it also supports two graphics modes: the XGA 5:6:5 RGB color mode for the full choice of 65,536 colors, and the Targa 5:5:5 mode for 32,768 color images.

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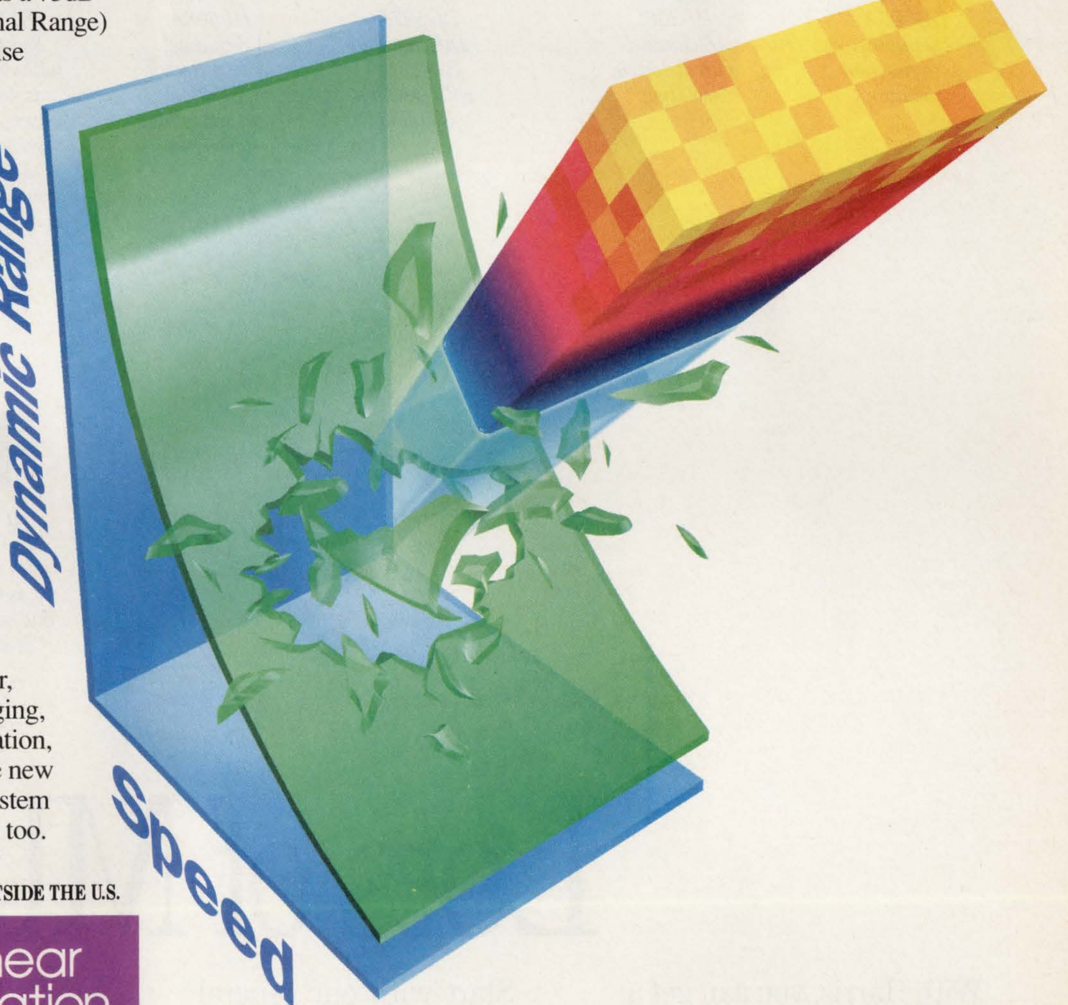

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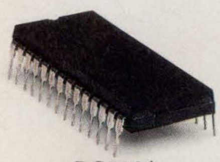

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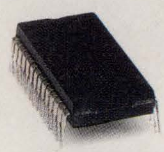
HI-506. 16-channel with dielectric isolation.



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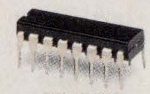
HI-508A. 8-channel with dielectric isolation and overvoltage protection.

HI-548. 8-channel with dielectric isolation, overvoltage protection, and Rds_{ON} matching.



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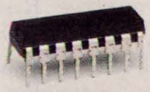
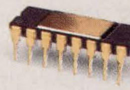


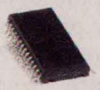
DG508A. 8-channel with junction isolation.

HI-508. 8-channel with dielectric isolation.

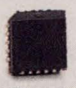


DG509A. Differential 4-channel with junction isolation.

HI-509. Differential 4-channel with dielectric isolation.

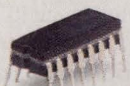


HI-507. Differential 8-channel with dielectric isolation.

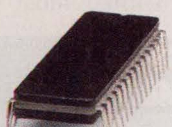


HI-509A. Differential 4-channel with dielectric isolation and overvoltage protection.

HI-549. Differential 4-channel with dielectric isolation, overvoltage protection, and Rds_{ON} matching.



IH-5208. Differential 4-channel with dielectric isolation, fault protection, and Rds_{ON} matching.



IH-5116. 16-channel with dielectric isolation, fault protection, and Rds_{ON} matching.

HI-507A. Differential 8-channel with dielectric isolation and overvoltage protection.

HI-547. Differential 8-channel with dielectric isolation, overvoltage protection, and Rds_{ON} matching.

IH-5216. Differential 8-channel with dielectric isolation, fault protection, and Rds_{ON} matching.

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The chip's 256-by-24-bit on-chip CLUT is typically used for VGA displays, and is bypassed when true-color information is sent to the display *(Fig. 3)*. Four byte-wide pixel-input ports handle the direct video color data. Internal gamma correction is included for true-color images. Anti-sparkle circuitry, to improve display stability, and a separate VGA port were also incorporated. When the VGA port is used with the pixel ports, true-color images and VGA frames can be selected on a frame-by-frame basis, opening the door to many multimedia applications.

In addition to offering XGA equivalent image coloring, the Bt484 can help systems come closer to XGA performance because it supports hardware cursors to accelerate Windows 3.0 applications. The 32-by-32-by-2-bit cursor patterns with its own three-color palette can be held on the chip to improve display response time and eliminate the need to redraw the cursor after every move. In line draws, for example, the processor must first locate the cursor's position, save the location information, draw the line, and then redraw the cursor—all of which could place a noticeable burden on the processor. By handling the cursor in hardware as an overlay, processor overheads are reduced and cursor flicker is almost entirely eliminated.

The logic also eliminates a graphics primitive and the previously required cursor collision detection. Both the cursor shape and color can be held in the Bt484's cursor memory. The host system need only supply the cursor coordinates.

Registers on the chip handle multiple true-color modes. Also, special VRAM interface and timing circuitry simplifies the control of the external VRAMs. The VRAM support provides the serial clock output to the memory chips and lets the clock adjust as the multiplexer setting on the pixel port changes from 8:1, 4:1, 2:1, or 1:1. Although it may be a while until the Bt484 finds its way into laptop systems, the chip does have a power-down mode that trims the current consumption to less than 50% of the active level.

Another true-color family of RAMDACs, the IMS G300 series from the Inmos Div. of SGS-Thomson also sports the four pixel ports and triple 8-bit video DACs and 256-by-24 CLUT employed in the Bt484. Like the Bt484, the IMSG332 packs an on-chip three-color cursor memory. However, the cursor memory on the G332 is organized as a 64-by-64-by-2-bit plane. An on-chip video timing generator sets the chip apart from the Brooktree device. The generator is fed by an external low-frequency clock (5 MHz) that's captured by an on-chip phase-locked loop and multiplied up to the appropriate video-signal frequencies.

The timing block is a finite-state machine that accepts a number of screen-control parameters and can be configured to free-run, providing composite or separate synchronization signals. Or it can lock onto an external synchronizing source. In either case, it supplies a composite-blank signal and can supply tesselated or plain composite sync.

Because the chip can handle a top clock frequency of 110 MHz, it was designed to directly tie into VRAMs, just as with the Brooktree RAMDAC. Later this year, the Inmos Div. hopes to release a 135-MHz version. The G364, which is an extension of the G332 with a 64-bit pixel port, makes it possible for data to be fed in even faster without a change in the external clock rate.

Hitachi, one of the few Japanese companies to offer a triple RAMDAC, has just released a pair of high-speed biCMOS units—the HDA153120 and 153130. They can display colors from a palette of over 16 million. The former produces displays with a resolution of 1280 by 1024 pixels and operates with 200-MHz dot rates; the latter is intended for slightly lower performance and has dot rates of up to 135 MHz. Although the 153130's speed is lower, it provides users with the choice of 6- and 8-bit modes. The software-switchable modes let users work from 260,000 or 16 million colors.

Just coming out of development is a combination true-color and pseudocolor RAMDAC—the Inmos IMS G180 and 181. Unlike most other

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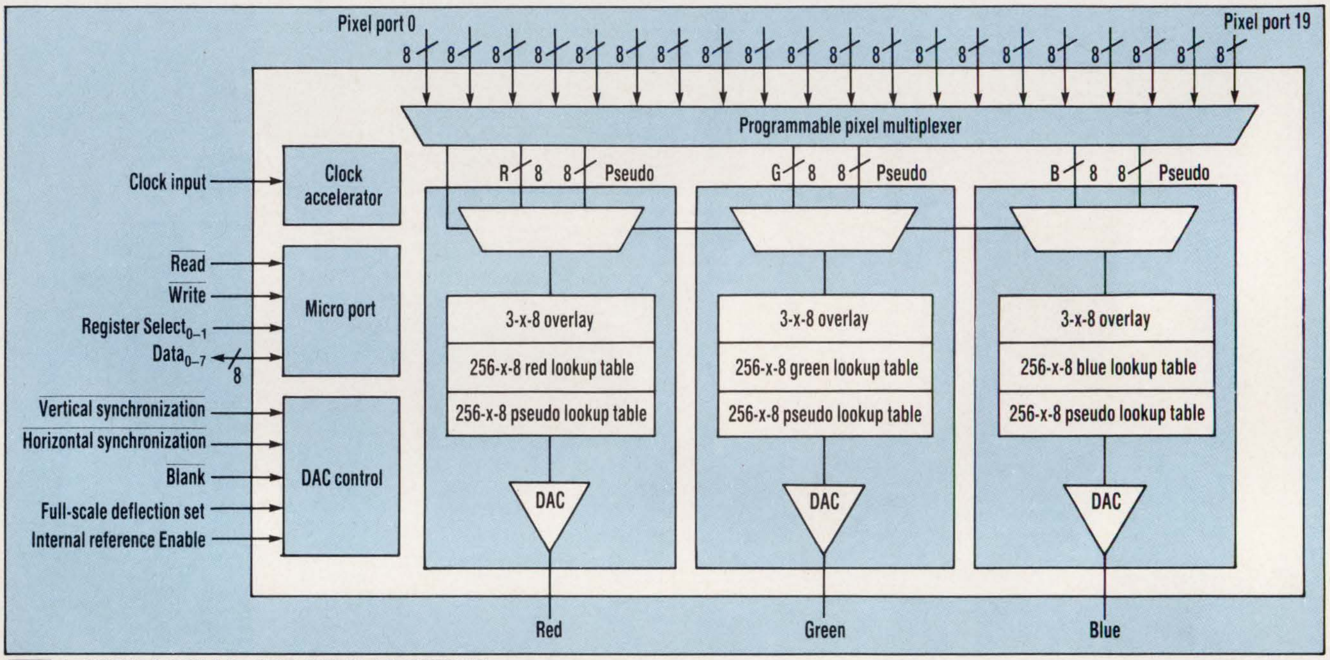
Consider this a guide rather than a definitive list.



4. WITH DUAL COLOR PALETTES, the IMS G180 and 181 triple RAMDACs from the Inmos Div. of SGS Thomson can provide gamma-corrected true-color and 8-bit pseudo-color images to a display simultaneously. As a result, picture-within-picture images can be created.

RAMDACs that contain triple DACs and one CLUT memory of 256 by 24, the G180 and 181 contain dual 256-word memories, one for true-color gamma correction and another for pseudo-color images *(Fig. 4)*. By programming the on-chip pixel-port multiplexer, the chips can be set to work with a range of pixel sizes—8-bit pseudo color, 16-bit RGB, or 32-bit (24-bit RGB plus 8-bit pseudo color) presentations. In the 32-bit mode, true-color and pseudo-color images can be displayed simultaneously on the same screen. That allows programmers to create applications around picture-within-picture capabilities. Furthermore, there are three 3-word-by-8-bit overlay tables available for cursor display.

The true-color images produced by high-end RAMDACs enable systems to generate screen images near photographic quality. The 24-bit resolution of the RAMDACs gives users 16.8 million available colors to work from. Extra bits can be added to the memory. But rather than use them for more colors, designers at Texas Instruments have added eight bits to form a color-overlay palette on its TLC34075. With the overlay palette, programmers can combine 24-bit true-color images and pull-down (or pop-up) menus. And, they can do that without having to remap the true-color image in the background. The result is faster image updates due to less software overhead.

In addition to efforts to build high-performance 6- and 8-bit/pixel RAMDACs, the low end of the display market with 4-bit/pixel triple RAMDACs has two players—Motorola and SGS-Thomson. The Motorola chips, which are implemented in ECL, aim at high-speed displays and can handle 125-MHz data rates. The SGS-Thomson chips, the EF9369 and TS9370, are NMOS devices that operate at 30 and 45 MHz, respectively.

Totally integrated RAMDACs offered by Cirrus Logic, S-MOS, and Western Digital provide a low-chip-count solution for laptop systems and small-footprint base-level computers. Low power is also a key aspect in the design of parts for the portable-systems market. The Inmos Div. of SGS-Thomson, Sierra Semiconductor, and S-MOS have devised low-power chips that can drop standby current to as little as 200 μA (the Inmos G177). The G177 actually offers three operating modes. The lowest power drawn is in the standby mode, in which the chip is completely powered down. The Review mode maintains the data in the CLUT while powering down the rest of the chip, trimming the power to 500 μA. During Normal operation, the chip appears identical to the IMS G176, a 66-MHz, triple RAMDAC with a 256-by-18 CLUT.

The SC11475 and 11477 from Sierra are also triple RAMDACs, offering higher active performance with a peak frequency of 80 MHz. The 11475 packs triple 6-bit converters and the 11477 has triple 8-bit units. Thus, they contain 256-by-18 and 256-by-24-bit CLUTs, respectively. They also include 15 overlay registers (18- and 24-bits wide, respectively). When switched into their Sleep modes, the chips cut their power consumption to about 5 mW, regardless of whether a current or voltage reference is used. The S-MOS SPC8100 combination controller and RAMDAC keeps the power drain to less than 1 mW in its lowest-power mode.□

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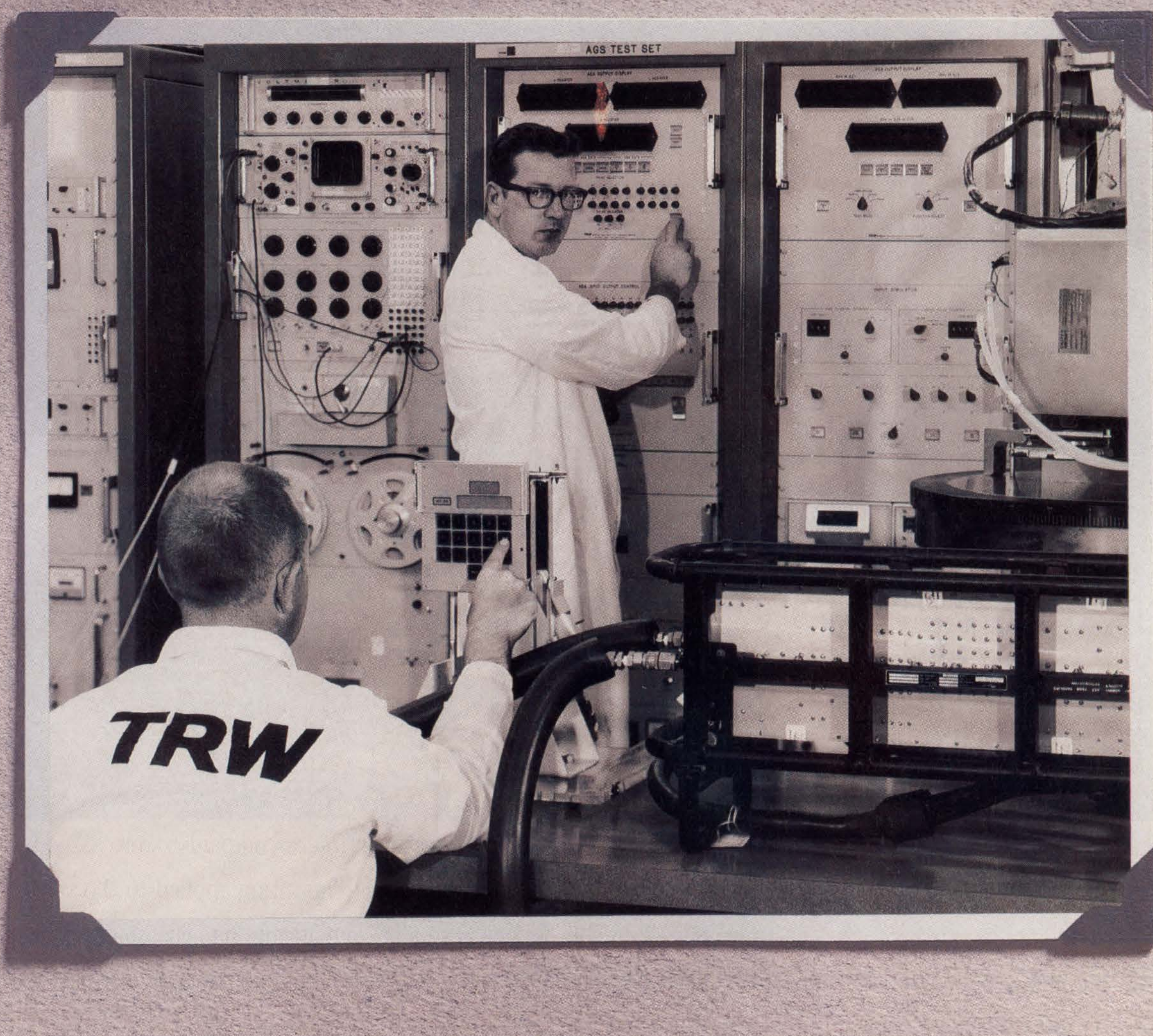

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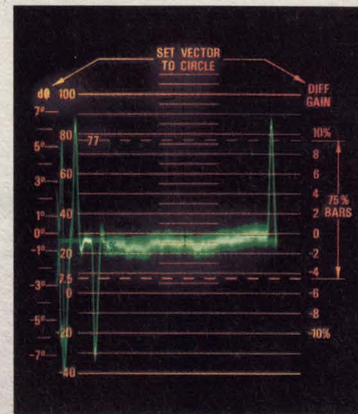

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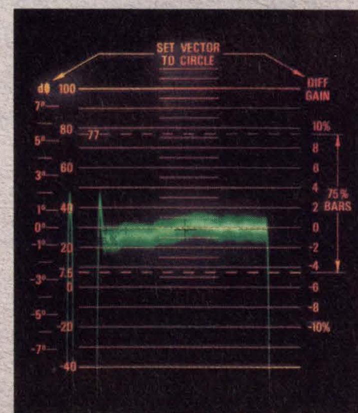

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DON'T TAKE YOUR ASIC PROTOTYPES FOR GRANTED

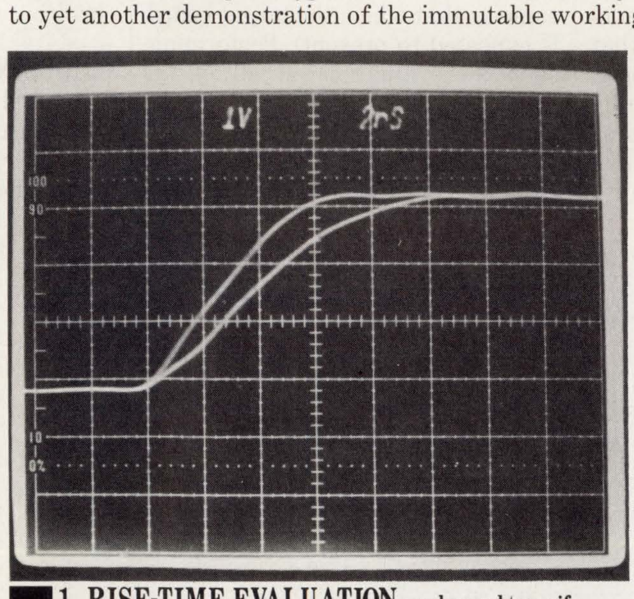
THOROUGHLY CHARACTERIZING ASICS BEFORE INTEGRATING THEM INTO A BOARD CAN SAVE LOTS OF TIME AND TROUBLE AFTERWARD.

You're an experienced engineer with a comprehensive array of powerful design and simulation tools at your disposal. For your latest project, you designed a nifty application-specific integrated circuit (ASIC) for production by a reliable vendor. You sent the semiconductor fabricator your complete design files—including functional, at-speed, and ac test vectors. So it's reasonable to expect that the first prototype ASICs will function flawlessly in their intended operating environment, and are ready for volume production. *RIGHT?*

WRONG.

When those first prototypes arrive from the vendor, you will more than likely be treated to yet another demonstration of the immutable workings of Murphy's Law. No one, not the greatest designer in the world, knows for sure what a new device will do until it's plugged into a board and fired up. That's why you ordered prototypes in the first place—to see what nasty tricks Mother Nature had up her sleeve for you this time. Her repertoire, as we all know from past experience, is immense.

For example, consider the fact that capacitive loading from board runs can seriously impair device rise and fall times. A "pumping" phenomenon in the device can make actual propagation delays much shorter than those predicted by worst-case

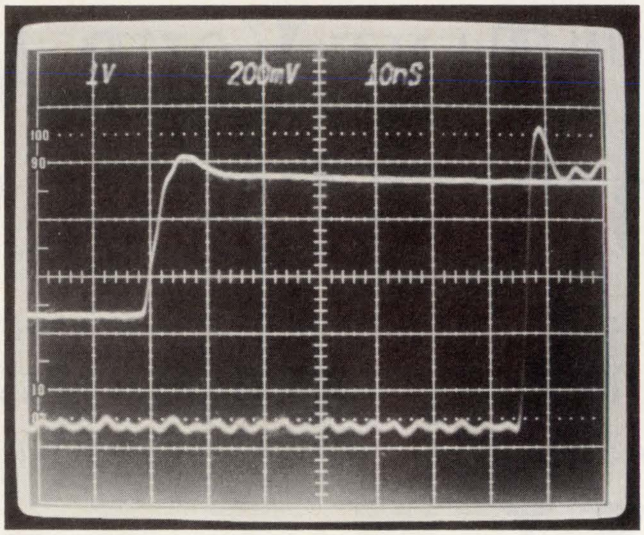


1. RISE-TIME EVALUATION can be used to verify prototype ASIC operation as well as to characterize loading effects for board design decisions. In this case, a TTL-output rise time is shown in an unloaded condition and with 22-pF loading.

JIM FENTON
Tektronix Inc., Walker Road Industrial Park, P.O. Box 4600, Beaverton, OR 97076; (503) 629-1394

simulation. Pin-to-pin crosstalk can cause clock jitter or even double clocking. Heat and voltage-swing problems may crop up, along with any of a wide range of other phenomena that we all must contend with in the real-world environment.

So it's probably most useful to regard the arrival of your prototypes as a time to do a reality check, to see what problems exist and to determine whether they're in the ASIC or the board.



2. THE MEASURED DELAY between a TTL input and an ECL output was 66 ns—quite a bit less than the 126 ns predicted by worst-case simulation. Left undiscovered, such disparities can lead to serious system design errors and timing problems.

Two Approaches

There are two main ways to determine how well an ASIC and a board work together. One is to design and build a prototype board, then plug in the ASIC to see how well it works. It sounds simple, but it requires substantial front-end design efforts in several areas.

Moreover, many of those efforts will have to be repeated to resolve design and compatibility problems that surface only after others have been dealt with. Furthermore, because device, board, and firmware problems are intermingled in a system environment, they can mask or modify each other, making it very difficult to determine where the problem lies. Building a prototype board for ASIC testing is therefore best described as a "combine - and - be - conquered" approach. In other words, it multiplies problems and the time required to find and fix them.

The second, preferable approach can be described by contrast as a "divide-and-conquer" technique. It involves characterizing prototypes before they're integrated into a system. It attacks problems at their source, where they can be more quickly and easily diagnosed and fixed.

A simple example of the type of characterization involved is a rise-time evaluation *(Fig. 1)*. In such a test, the ASIC's TTL-output rise time is observed both with and without capacitive loading (the amount of capacitive loading should be the same as that which the target board is expected to present). Performing such an evaluation on all of an ASIC's outputs provides a wealth of useful information.

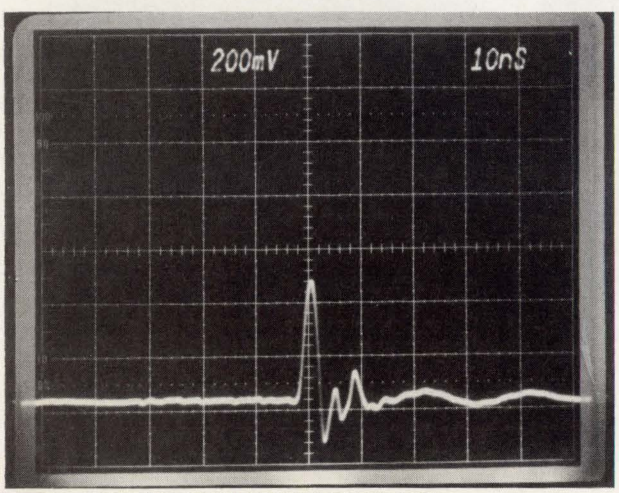
It not only immediately identifies violations of vendor specifications, it also isolates them to the ASIC. That can save untold aggravation later on, at the prototype board stage. In addition, such an evaluation provides a measure of the ASIC's ability to drive the anticipated capacitive load. If there's a problem, informed decisions can be made about addressing it in the ASIC or choosing the option of making it a board-design issue.

Other similar tests—setup and hold times, propagation delay, voltage-swing effects, simultaneous-switching effects, and so on—offer the designer equally valuable information about the ASIC's real-life operation. As with the rise-time evaluation, the results of those tests can be used to refine the specifications for the ASIC's operating environment (board layout, power budget, allowable supply variations, etc.), as well as simply to check out the prototype.

Choosing Equipment

An ASIC can be run through its paces on any production test system. However, production testers are usually kept busy on the production line, hence it's difficult to schedule time on them. Moreover, they typically require the specialized skills of a test engineer to set up and run tests. Obviously, that's not the best approach for evaluating prototypes.

For design applications, therefore, any of several available benchtop testers will provide a more economical and convenient means for ASIC prototype verification and characterization. To maximize efficiency, a benchtop system used for this purpose should allow direct downloading and conversion of simulation files. That ar-



3. SETTING UP SIMULTANEOUS switching of multiple TTL outputs can reveal a number of pinout and noise problems. In this case, simultaneous switching has induced a glitch on an ECL output.

rangement eliminates the need to re-create vectors in another language.

In addition, the system's editing facilities should be interactive and easy to use. One suitable tester is the Tektronix LV500 ASIC Verification System, which performed the tests discussed in this article. It enables vectors to be viewed and modified in several formats, including a familiar timing diagram.

Speed, number of channels, memory depth, and device interfacing are also important issues to consider when choosing a benchtop tester. The speed and number of channels, of course, must meet or exceed the speed and pin count of the devices to be tested.

Memory depth, while not so unambiguously prescribed, is still an extremely important consideration. Basically, the deeper the memory, the more powerful and flexible the stimulus/response handling.

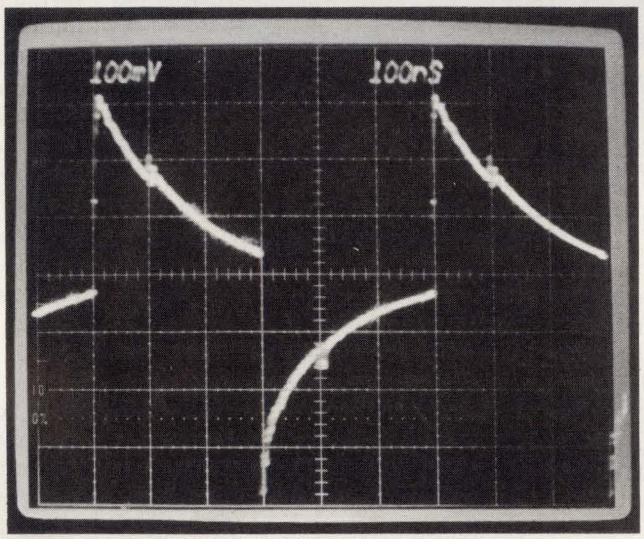
For example, it's quite likely thgat some tests can't be performed until the device under test (DUT) is in a particular state, and it may take a large number of vectors to get it into that state. The memory should be deep enough to hold the required vectors.

The mechanics of connecting the DUT to the benchtop tester is also important. The interface should be simple and direct, yet it must also keep the DUT pins accessible for oscilloscope waveshape and timing observations. At one extreme, direct-socketing, software-wired approaches are uncomplicated and inexpensive, but may restrict pin access for oscilloscope probing. On the other hand, a complex interface board is expensive and may introduce design problems of its own. A simple DUT board approach is usually the best choice for both efficiency and pin access.

As for the oscilloscope, it should be a high-quality instrument with sufficient bandwidth to handle the outputs of the benchtop tester. To get the most out of the LV500, a scope with a 350-MHz bandwidth is needed, and indeed the photographs in this article were taken from such an instrument.

If an analog scope is used (as was the case here), it should have a reasonably fast writing rate so that jitter extremes, metastable conditions, and other transient phenomena aren't overlooked.

Finally, the total input capacitance for the combination of the scope and probes must always be borne in mind because it can be an important consideration in some timing measurements. For example, part of the 22-pF loading in Figure 1 is contributed by the scope.



4. CAPACITIVE COUPLING FROM A TTL output to an attenuated input caused 300 mV of unwanted signal on the input pin.

Conducting The Tests

Conducting a test like the rise-time evaluation of Figure 1 starts with choosing a set of input vectors that will produce a transition on the output pin to be evaluated. The benchtop tester is then programmed to loop on that vector set so the output makes periodic transitions from one state to the other. The resulting repetitive stimulus signal makes for easy triggering and viewing with an oscilloscope.

The toggling output waveform should be examined closely for overshoot, ringing, or other aberrations that violate voltage margins. Each transition should also be examined by the designer for jitter that exceeds timing margins.

Then, the transition times should be measured. That should be done not only to ensure that they meet vendor specifications, but also to establish the actual edge speeds, which connecting runs on the board will have to handle.

Capacitive loading effects can be investigated by attaching small capacitors to the output pin. As mentioned earlier, the oscilloscope input capacitance will form part of the load on the pin and should not be neglected.

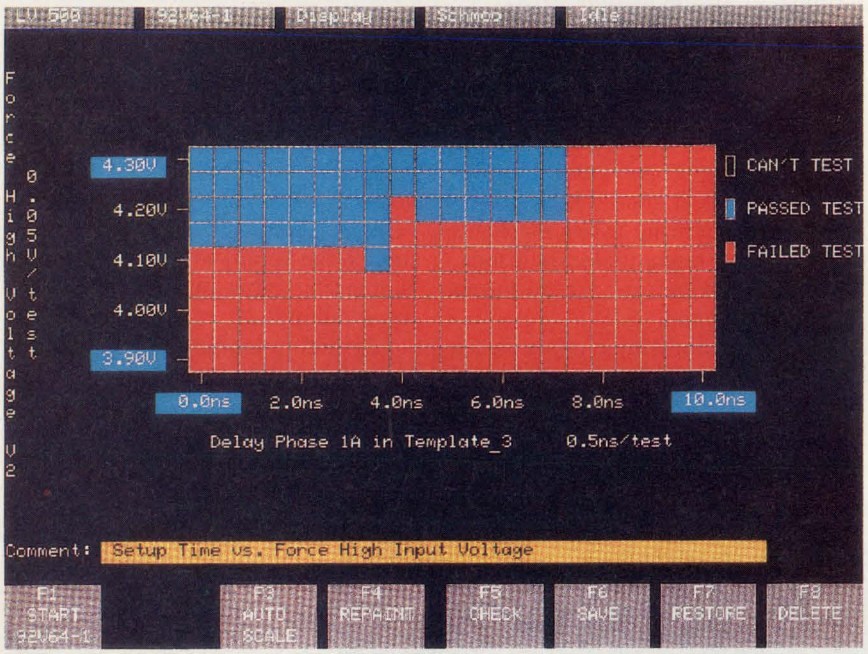
A similar approach can be applied to measure input-to-output propagation delays. That is, an appropriate set of vectors is selected in the benchtop tester's pattern display, and a looping function is set up on them. Then, using an oscilloscope in its dual-trace mode, the input and output waveforms are displayed and measured *(Fig. 2)*.

In the case of Figure 2, the test reveals a serious disparity between the actual device delay and the value predicted by worst-case simulation. The disparity helped identify a "pumping" phenomenon in the ASIC, in which a string of gates acted like a series of cascaded amplifiers. The result was a propagation delay time of about half that predicted by the simulation results.

Even if such disparities don't exist, it's still important to characterize the device's actual propagation delays. It identifies device paths that may need to have a delay element added or removed for proper internal timing.

Input/output bus skews can also be identified by such tests. The skew information can then be used in designing board run lengths to remove skew and improve overall system performance.

In addition to facilitating timing



5. VARYING ONE PARAMETER **while measuring another, known as Schmooing, allows characterization of various operating limits. This plot shows setup time versus input voltage swing.**

measurements, looping on selected vectors can help measure pin-to-pin crosstalk. Such measurements can identify problems in which state changes on one pin interfere with the signal on an adjacent one. These probllems are much harder to isolate when the ASIC is in it's board environment.

For example, the ASIC may have an ECL clock input surrounded by TTL outputs. That may or may not be a problem. To find out, the benchtop tester's pattern screen is edited to produce simultaneous transitions on all of the surrounding TTL outputs while the ECL clock input is monitored on the scope. The simultaneous switching can cause excessive clock jitter or possibly even double clocking. Similarly, simultaneous high-to-low switching of multiple TTL outputs in Figure 3 has induced noise on the ASIC die and caused a glitch on an ECL output.

CAPACITIVE COUPLING

Yet another type of pinout problem that proper testing can uncover may crop up when an attenuated input is located next to a TTL output *(Fig. 4)*. In that case, the result is capacitive coupling of the output signal to the input pin.

The test examples shown thus far use the benchtop tester essentially as a pattern generator to create repeated input and output conditions. If the tester has a dc parametric measuring unit (PMU) and x-y (Schmoo) capabilities, the tester can add another dimension to most tests, while at the same time increasing the number and types of tests that can be performed.

Schmoo capability, which displays changes in one parameter against variations in another, is valuable for establishing reliable operating ranges. It can be used to study how propagation delay varies with changes in input voltage swing. A very similar test could study the relationship between propagation delay and supply voltage.

Output rise and fall times could also be evaluated against voltage swing and supply changes. Such tests are especially important if the ASIC is intended foruse in a battery-operated device, such as a laptop computer.

Schmooing can also be used to run setup- and hold-time tests *(Fig. 5)*. For setup times, a data signal is walked into the clock signal in small (say, 500-ps) steps until a setup-time violation is forced. An appropriate tester can use the results of a such a test to create a one-dimensional Schmoo chart showing the point at which the data signal failed the setup time with respect to the clock. Similarly, a hold-time chart can be created by walking the clock signal away from the data signal to force a hold-time violation.

DC MEASUREMENTS

A dc PMU can also measure input/output leakage current on a pin, determine the input voltage trip point on an input comparator, or force a voltage or current on a pin to measure the resulting current flow or impressed voltage.

Device supply current and power consumption can also be accurately determined. Furthermore, these measurements can be combined with Schmoo plots to establish reliable operating regions for the device.

The key element in performing any of these or other characterization tests is having a benchtop tester with adequate capabilities. Equally important, the tester must be easy to use and should have a friendly user interface. That will minimize test setup time and encourage comprehensive testing. The end result will be better device and board designs and far fewer problems when the ASIC is actually plugged into the board.□

Jim Fenton, a senior electrical engineer in Tektronix's Hardware Evaluation Group, has a BSEE from the University of Michigan, Ann Arbor, and an MSEE from Oregon State University, Corvallis. Since joining the company in 1980, he has performed hardware evaluation engineering on the DAS9100, 1240, DAS9200, and Centurion logic analyzers.

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MODERATELY	542
SLIGHTLY	543

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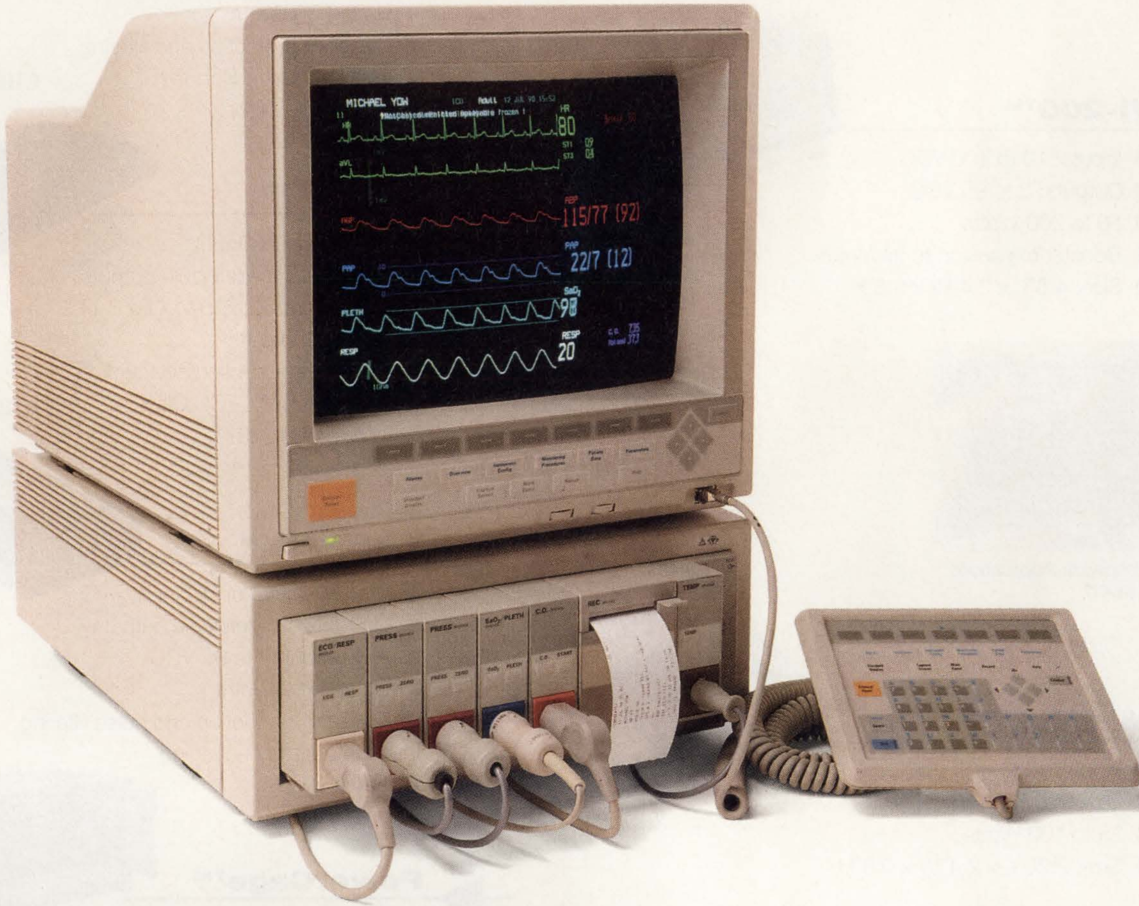

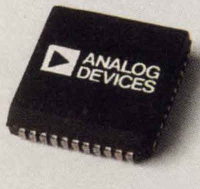

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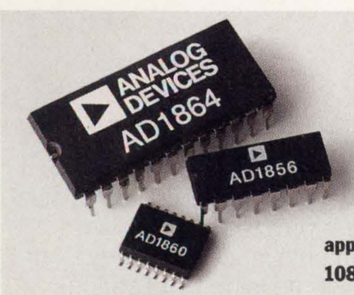

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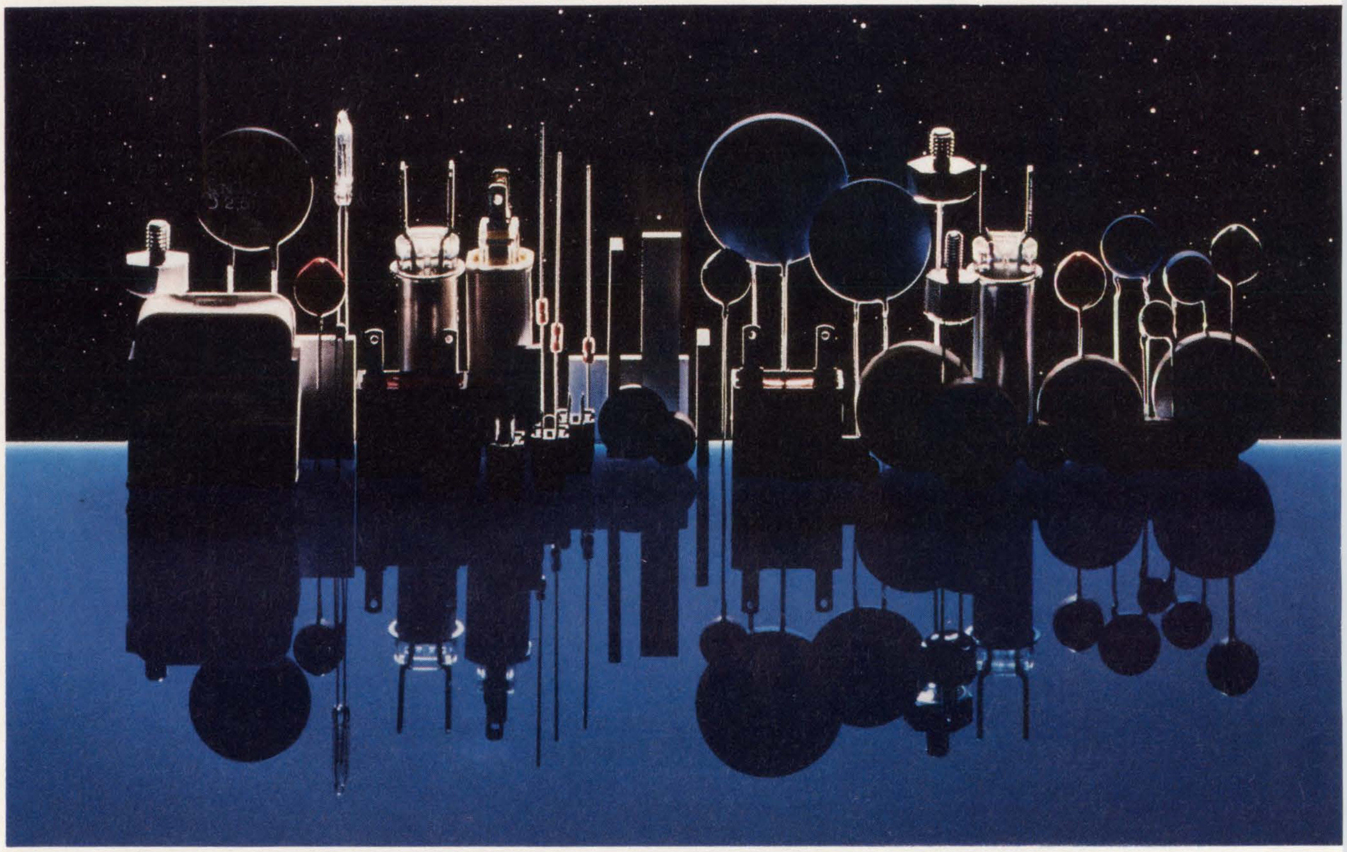

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Multiplexed Buses Unravel Auto Wiring

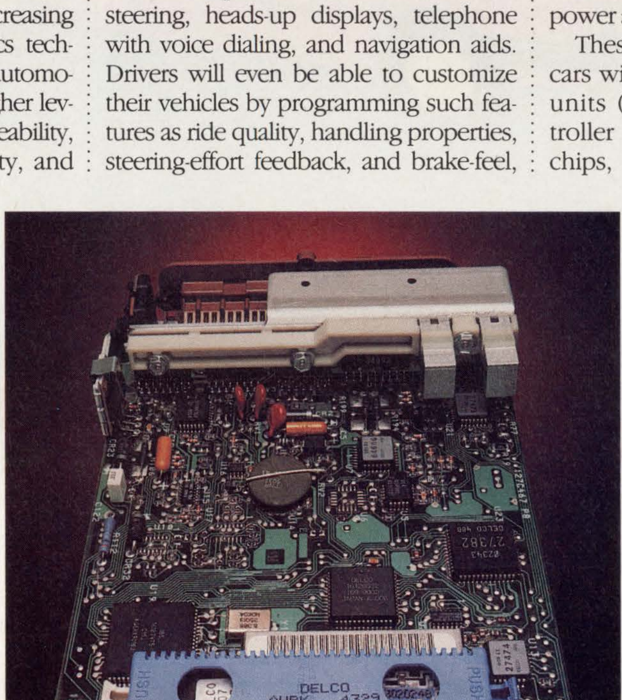
Automakers adopt networking techniques as proliferating electronic controls create wiring nightmares.

BY MILT LEONARD, *SENIOR EDITOR*

NEW CAR MODELS UNVEILED each year reflect the increasing contribution of electronics technology toward better automobiles. Electronics contribute to higher levels of vehicle performance, serviceability, product differentiation, reliability, and safety and convenience features. Sophisticated electronic systems are replacing functions traditionally performed by mechanical and electromechanical means for power-train control, vehicle control, as well as driver information systems.

As this trend continues, industry visionaries foresee totally integrated vehicle electrical and electronic systems with extensive software controls *(Fig. 1)*. The main intelligence of such systems will continue to be microprocessors and microcontrollers, working in concert with digital-signal-processing (DSP) chips, application-specific ICs (ASICs), intelligent power devices, and smart sensors and actuators *(see "The role of embedded controllers," p. 87)*.

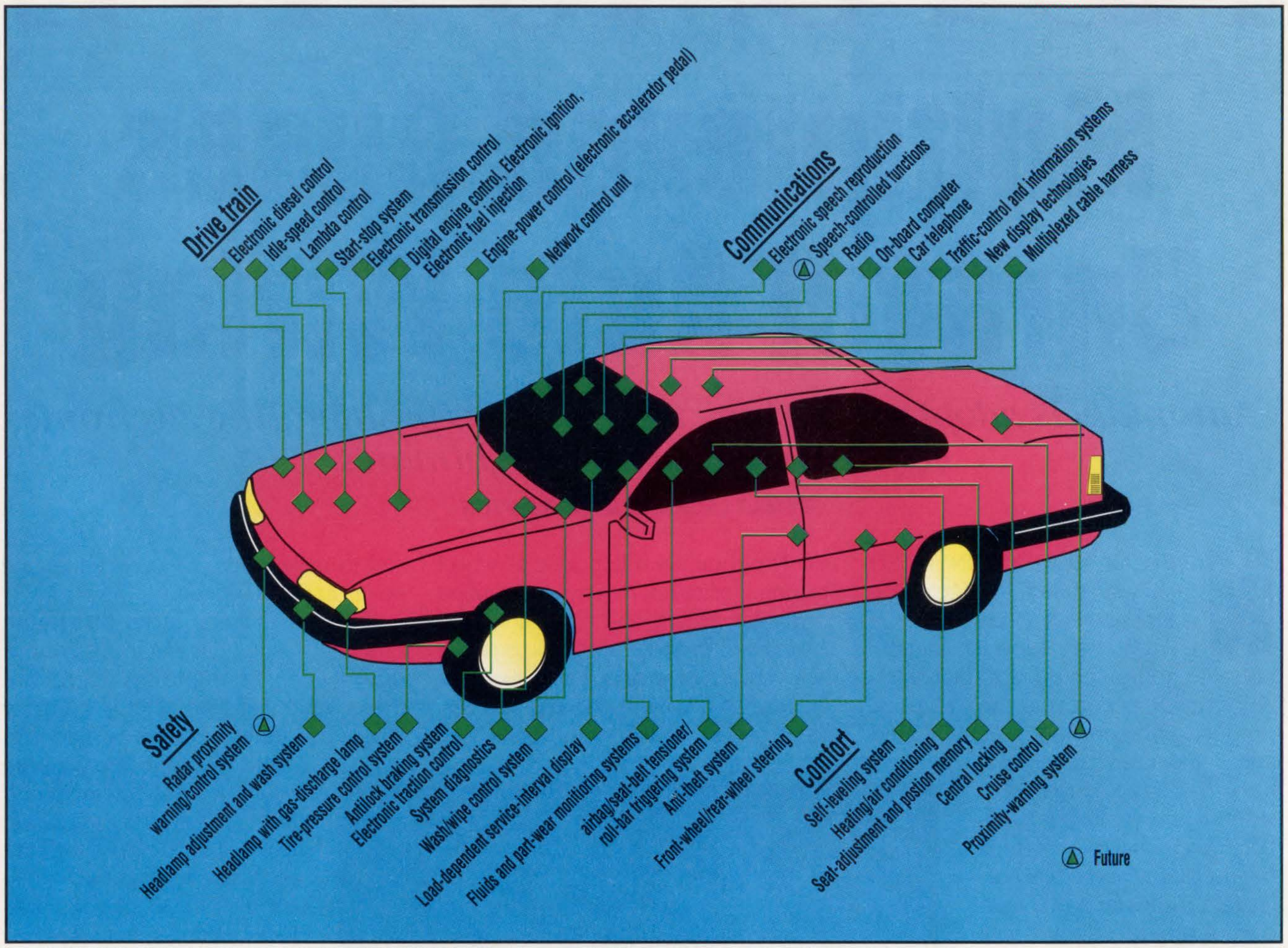
Such processing power will bring new standard features, including electrically assisted steering, reformattable driver-information centers with "soft" switches for user-defined functions, and zone-adjustable climate control. New options will include all-wheel steering, heads-up displays, telephone with voice dialing, and navigation aids. Drivers will even be able to customize their vehicles by programming such features as ride quality, handling properties, steering-effort feedback, and brake-feel, and to make trade-offs between engine power and fuel economy.



HIGH INTEGRATION LEVELS in MCUs, ASICs, and memory devices allow a single electronic-control unit to handle several interactive high-speed functions. Shown without its protective enclosure, this power-train controller from Delco Electronics Corp. continuously performs calculations for fuel and spark timing, using sensor data and calibration values for specific engine and drive-train combinations.

These predictions mean that future cars will bristle with electronic-control units (ECUs) containing microcontroller units (MCUs), ASICs, memory chips, bus-interface devices, and discrete components *(see opening illustration)*. Data-path widths will range from 4 bits for handling simple tasks, such as turn-signal control, to 32 bits for antilock-braking systems (ABSs) and traction control. In an investment research report last year, market analyst Morgan Stanley & Co. Inc., Bronx, N.Y., estimated that a luxury car will contain a dozen or more equivalent MCUs.

For the most part, these predictions can be turned into reality by existing enabling technologies. Silicon sensor technology is on pace to integrate complex logic and sensor structures on a single die. And the development of smart motors and actuators presents no serious technical challenge. The basic technologies for integrating logic with power-handling devices are already in place, as is the technology for intelligent power devices to control lighting, inductive solenoid and motor loads,



1. MULTIPLEXED AUTOMOTIVE NETWORKS can be applied to over 30 electronic-control modules associated with drive-train control, communications, safety, and comfort features. In a fully loaded vehicle, such a network would dramatically cut the wiring requirement from several miles for a conventional point-to-point wiring scheme to just one multiplexed cable containing a few conductors for power, control signals, and data.

and displays, and to perform dc-dc conversion for 12-to-5-V, 12-to-24-V, and 12-to-48-V automotive systems.

Perhaps the most critical challenge is finding an efficient way to implement data communication between automotive electronic subsystems. With the scope and complexity of a vehicle's electrical system virtually doubling every 10 years or so, the shortcomings of conventional point-to-point wiring schemes have become intolerable.

POINT-TO-POINT LIMITS

The increasing number of wiring cables and connector contacts is leading to long production times and higher labor costs, cramped body space, and decreasing reliability. Retrofitting and fault tracing are more time-consuming and expensive. According to Dr. Otto Holzinger, a director in the Motor Vehicle Equipment Div. of Robert Bosch GmbH, Stuttgart, Germany, over 100 cables and plug connections often must be installed in the dashboard area of an automobile alone for instruments and driver controls.

Similarly, luxury-class vehicles can have over 50 wires leading into the driver-side door to such control features as seat positioning, door locks, power windows, electrically operated exterior mirrors, keyless entry, and courtesy lamps. Another concern is the reliability of complex interacting functions, which for safety reasons, can't be exposed to the weaknesses of error-prone point-to-point wiring. For example, any hint of a driving wheel spinning on a slippery surface should result in a seamless shifting of gears in the automatic transmission. Simultaneously, the traction-control system should react instantly to reduce engine torque by intervening in the ignition and/or electronic throttle control. For this to happen, however, dozens of sensors, electronic controllers, and actuators must interact in a coordinated fashion.

Electronics has also invaded the realm of vehicle ride control. In response to sensor signals that measure wheel speed and road conditions, microcontrollers in adaptive-suspension systems automatically adjust the ride from hard to soft, using real-time high-speed processing.

Adaptive suspension systems use the same type of sensors required for ABSs, resulting in hardware redundancy, a greater degree of wiring-scheme complexity, and a higher level of cost.

The obvious solution, of course, is to multiplex data through one serial line or bus tied to the vehicle's ECUs, much like communications networks that interconnect computers and data terminals. Multiplexing allows data from different sources—sensors, switches, and ECUs—to be sent over a common bus, typically consisting of four wires. Two conductors are used for signal transmission, and the other two conductors are used for power and ground. Future systems with multiple supply voltages will require one or two additional power buses *(Fig. 2)*.

The benefits of networking multiplexed data are already being exploited by several car manufacturers. For example, the wiring harness of a 1989 Buick Riviera weighs about 86 pounds and contains 1.5 miles of wiring. Similarly, the Cadillac Allante in the same model year has about 180 major electrical interconnections.

The door assembly of a luxury car alone can require a fist-sized bundle of 54 wires running from the door to the car body through the hinge area. Multiplexing all the automotive data can reduce the wire count from 54 to 4.

Although impressive, these solutions are piecemeal and far from the ultimate goal of totally integrated, networked automotive subsystems in which sensors, actuators, ECUs, and display devices share data on a common bus. The issues regarding network topology—the wiring scheme for interconnecting electronic modules—are fairly straightforward and were resolved by auto makers early on. The major remaining obstacle is the lack of international networking-protocol standards for the automotive industry.

TABLE 1. IN-VEHICLE SERIAL COMMUNICATIONS REQUIREMENTS

Class	Speed (bits/s)	Latency (ms)	Error handling	Number of nodes
Class A	1000	20-50	Low	50-100
Class B	10-100,000	5-50	Medium	10-50
Class C	1,000,000	<5	High	5-10

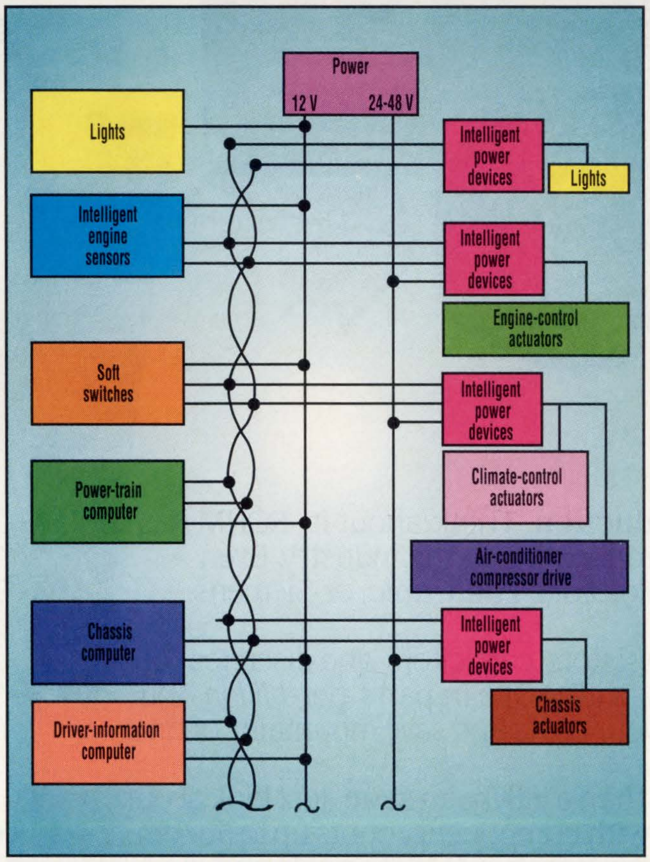
NETWORK TOPOLOGY

Automotive wiring designs have physical requirements that go beyond those for the communications and computer industries. The wiring scheme must allow ECUs to be interconnected in a vehicle without redesigning or requalifying the subsystem or the entire system. Adding new ECUs onto the network should also be possible without modifying the original network. And cables and connectors must be sturdy enough to withstand harsh commercial-service environments.

A related consideration is the type of topology or bus-wiring scheme used. A star-type design can be operated with a simple protocol *(Fig. 3a)*. However, the cost is high because a special star-point control unit is required. If the star point fails, the entire network shuts down. Moreover, the number of interface ports is limited to the original design.

A ring-type design is well-suited for unidirectional data flow, and allows high data rates with low overhead *(Fig. 3b)*. Another advantage is the limited cable length that each data transmitter has to serve. Like the star configuration, however, connecting new devices requires the ring to be opened, which upsets the original fixed-priority scheme. Although using a token-passing scheme solves the priority problem, the resultant delays in individual engine-management units can sometimes cause instability in overall control loops at the automotive vehicle-wide level.

The limitations of ring- and star-type topologies have led the auto industry to select a linear bus structure for high-speed networking *(Fig. 3c)*. This scheme gives every network node the same right to access the bus. Arbitration among nodes is done by prioritizing the addresses of the messages. Subsequent expansion and conversion to different configurations involves simple procedures. On the minus side, allowable cable length depends on the data-transfer rate if an inexpensive baseband-modulation technique is used.



***2. POWER REQUIREMENTS** in future auto designs will increase from today's 1 kW to about 3-6 kW, leading to a separate dual-voltage power-distribution system. Low voltage (12 V) will power most of a vehicle's electrical and electronic components. Between 12 and 48 V will power heavier loads, such as cooling fans, steering motors, chassis hydraulic actuators, and air-conditioning compressors.*

NETWORK SPEED

Laying the groundwork for networking standards development, the Multiplexing Standards Committee of the Society of Automotive Engineers (SAE) has partitioned the data-rate require-

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MOTOROLA	x		x	x	x				
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NEC	x	x		x	x			x	
OPTOREX			x						
PANASONIC	x		x	x		x		x	x
PHILLIPS	x			x	x				
SHARP	x	x	x		x				
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ments for automotive serial communications into three segments *(Table 1)*. These classifications pave the way toward developing network protocols for low-, moderate-, and high-speed application areas—just like the data-communications industry has developed standards and protocols for Ethernet, Sonet, FDDI, and other communicationsnetworks.

Class A defines parameters for body-control applications where high data speed and extreme accuracy levels aren't critical. These applications include headlights, tail lights, turn signals, driver-convenience features, and entertainment systems.

Most vehicle functions presently fall into the Class A category, which handles data rates up to 1 kbits/s and supports up to 100 nodes. Latency time, the interval between a transmission request and transmission initiation, is 50 ms. Class A functions typically are controlled by driver commands.

Class B refers to information-sharing systems with moderate speed (up to 100 kbits/s) and accuracy requirements that consist of up to 50 nodes. Application examples include communication between sensors and instrumentation clusters. Class B data doesn't control the automotive subsystems and isn't transmitted in real time.

Class B protocol development has received much attention in the U.S. due to the California Air Resources Board's (CARB) decision to mandate on-board diagnostics modules for emission-control testing. The state's On-Board Diagnostics (OBD) II mandate will allow emissions-testing centers to use computers to check the effectiveness of a vehicle's emissions-control equipment.

Emissions control is also a concern among European auto makers. In the past, each country set its own auto-emissions standards. Most companies could meet the standards for engines with displacements of 2 liters or less by adding electronic ignition to carbureted engines. Now, the standards-making responsibility belongs to the European Parliament, an advisory body representing the 12 states of the European Community. Effective next year, new standards issued by the Parliament are 50% more restrictive than existing standards, and roughly equivalent to those for U.S.-produced vehicles. The new limits will require using complete engine-management systems that include fuel injection.

Class C protocols are for real-time control applications with critical speed and accuracy requirements, such as communication between the engine and transmission, or between ABS sensors and brake actuators. The higher data rates of Class C (up to 1 Mbits/s) reduce the maximum number of nodes allowed to 10, and latency time decreases to under 5 ms.

This performance level is required for drive-train control functions that demand accurate high-speed communications between multiple electronic devices. In engine control, for example, sensors measure intake-air volume and temperature, engine speed, throttle-valve position, oxygen content in the exhaust gas, and engine temperature. From these values, the ECU calculates the best ignition points and fuel-injection rate. The control algorithm adjusts in an adaptive manner to suit altered engine and ambient conditions caused by factors like engine aging or changing atmospheric conditions. The ECU then is-

THE ROLE OF EMBEDDED CONTROLLERS

EMBEDDED CONTROL IN automotive electronic-control modules is served primarily by two kinds of devices: microprocessors and microcontrollers. The choice between the two depends on such things as performance targets, price sensitivity, and the volume of automotive data to be processed.

A microprocessor unit (MPU) provides the core functions for logical and arithmetic computation, but typically requires the support of external memory and other chips to form a complete processing unit. On the other hand, a microcontroller unit (MCU) integrates the MPU with memory, input/output (I/O) functions, and timing circuitry on the same chip. Some MCUs even include analog-to-digital converters and display drivers. One microcontroller can replace as many as a dozen or more support ICs.

MPUs are optimized for maximum computational speed and throughput for high-performance applications. They can be found in computers, workstations, and high-end embedded controllers for machine-vision and speech-processing applications. Conversely, MCUs are optimized for compactness, low-power dissipation, and low cost. They're generally found in applications that are impractical or impossible to implement with MPUs. For example, low-power consumption enables MCUs to operate in under-the-hood automotive controllers routinely exposed to temperatures exceeding 250°F.

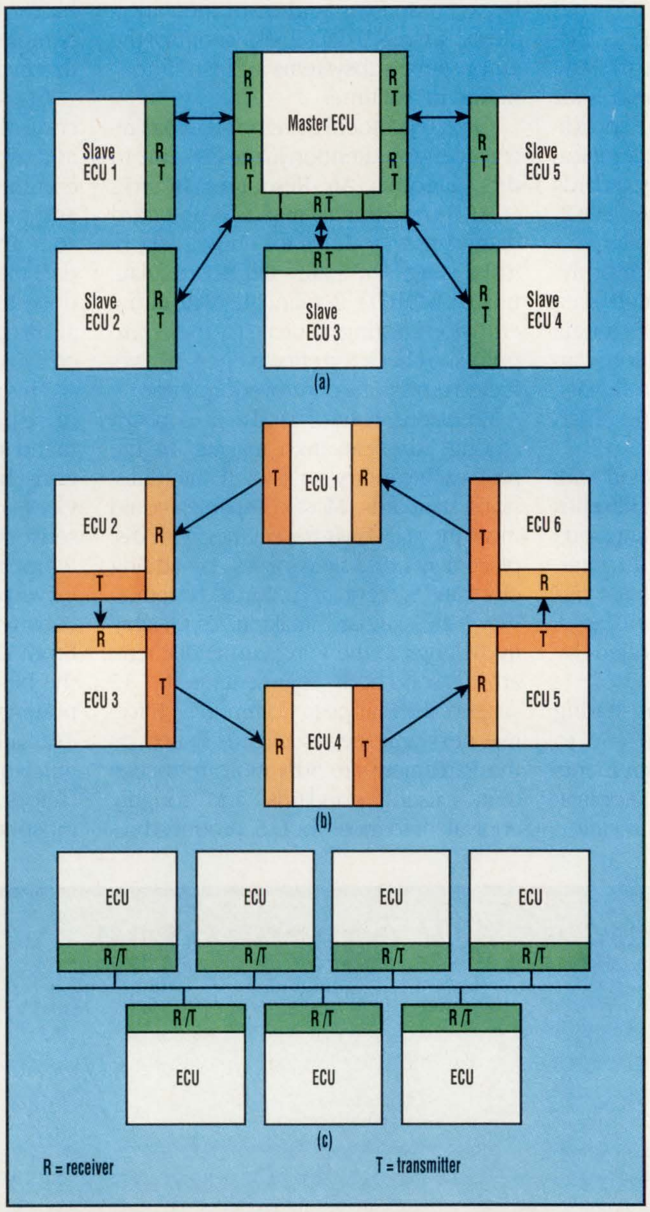
The automotive industry has been a traditional catalyst for advances in embedded control. This trend continues as control-intensive applications in modern road vehicles become more complex. Many conventional MCUs now spend most of their time handling interrupt requests from various system components, leaving very little time to compute critical engine parameters, such as spark timing and optimum fuel-flow rate. Instead, they must resort to using lookup tables for a list of "canned" solutions to engine-control problems. Based on rough approximations and average engine characteristics, these responses are far from accurate.

A better approach would be to measure all involved variables precisely, and compute a course of action based on the specific conditions at hand. As a result, semiconductor IC suppliers are responding to this need by offering a new crop of MCUs with on-chip timing and communication functions. Consequently, the MCU's CPU has time to perform real-time, algorithm-based control. The result is more efficient, cleaner, and more responsive automobile engine operation.

sues output commands to the various electronic subsystems that control engine operating parameters, such as throttle-valve position and ignition timing.

The enormity of the task becomes clear when you consider that the ignition pulses in a six-cylinder engine running at high speed are separated from each other by just a few milliseconds. To calculate the optimum ignition point in real time, huge amounts of data must be transferred between networked engine-control and transmission-control subsystems within a fraction of these few milliseconds. This means the network must support data-transfer rates between 100 kbits/s and 1 Mbits/s.

Another guideline for developing networking standards is provided by the Open Systems Interconnection (OSI) reference model, originally established for the data-communications industry by the International Standards Organization (ISO) for the data-communications industry. The model partitions the functions involved in data communications into seven layers *(Fig. 4)*. Each layer in a node believes it is communicating with its corresponding layer in another node. The layer does this by accepting messages from its neighboring vertical layer, adding control information to it, and passing this data to its neighboring layer below. The procedure is reversed at the receiving node.



3. COMMONLY USED BUS TOPOLOGIES for the data-communications industry include a star (a), a ring (b), and a linear configuration (c). An open linear-bus structure best meets the automotive requirements of configuration flexibility, expandability, and sturdiness.

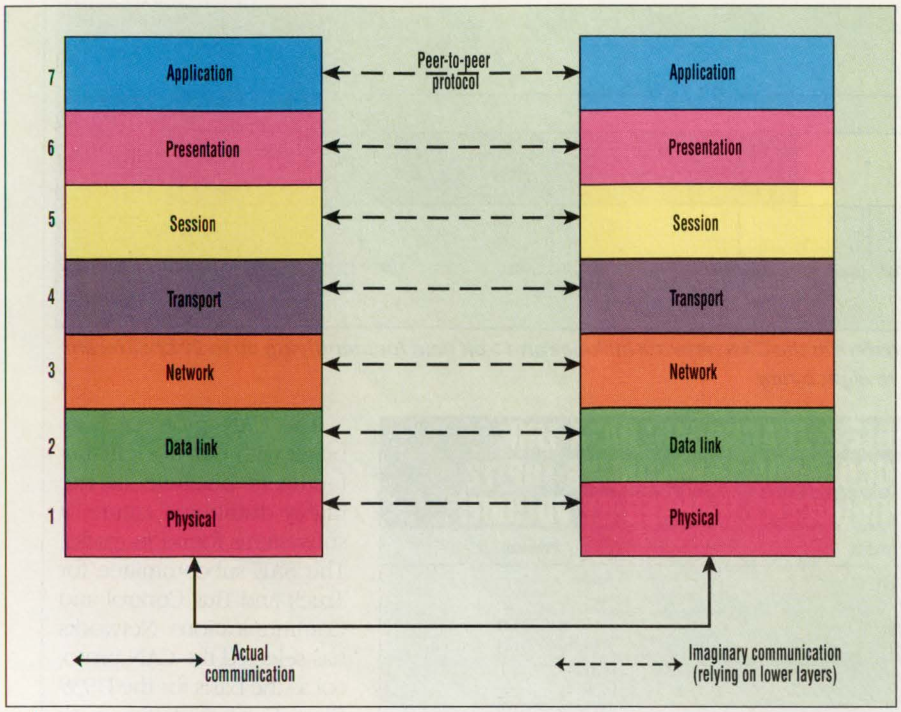
The physical layer is concerned with transmitting the data-bit stream. The data-link layer performs error detection and correction, and handles host-to-host control messages. Routing traffic and controlling congestion in a point-to-point network are the network layer's primary tasks. The transport layer provides reliable node-to-node communication while masking the details of the network operation from the session layer. The session layer sets up, manages, and tears down connections between programs being executed. The presentation layer performs any transformations needed for dialogues between incompatible nodes. The content and function of the top layer, the application layer, is user-definable.

Communication signals are transmitted and received by the various network nodes according to a set of conventions called a protocol. The protocol sets the rules for coding, address structure, transmission sequence, and error detection and handling. A protocol also defines the transmission medium (copper wire or optical fiber), transmission speed, and electrical-signal requirements. Protocols for automotive networking cover most of the functions assigned to the various layers of the OSI model.

A standard protocol would join reduced wiring costs and reduced component redundancy in offsetting the increased cost of electronics. It would also lead to standard ICs for implementing the protocols and enable electronic control modules from different manufacturers to communicate with one another. Spokesmen at International Rectifier Corp., El Segundo, Calif., said the lack of protocol standards has forced the company to design, manufacture, and stock a different intelligent power IC for each auto maker's proprietary protocol.

Unfortunately, no global standards presently exist for Class A, B, and C applications. As a result, car makers in the U.S., Europe, and Japan have forged ahead with their own proprietary multiplexing solutions, creating a highly fragmented standards environment *(Table 2)*. Compounding the problem is the difficulty of selling the increasingly more-expensive multiplexing technology to the marketplace. "The customer who must bear the cost of multiplexing perceives no user benefit," explains Mike Thompson, a strategic marketing manager at Signetics Co., Sunnyvale, Calif.

So far, automotive multiplexing techniques have been limited to partial networks. At the low-speed end, proprietary Class-A buses for passenger-com-



4. PROTOCOLS FOR AUTOMOTIVE networks are partitioned according to the guidelines set forth by the 7-layer OSI reference model of the ISO. As is evident in existing proprietary protocols, all layers aren't needed for automotive applications.

partment operations have been installed in vehicles from Japanese car makers Mazda Motor Corp. and Nissan Motor Co. In Europe, Class-A multiplexing is appearing in vehicles from the Fiat Group, PSA, and Volkswagen. Robert Bosch GmbH is demonstrating a Class-A solution for vehicle door applications.

Medium-speed applications are being implemented in Europe by the French-developed vehicle-area network (VAN), which is emerging in vehicles from The Fiat Group, PSA, and Renault SA. Because of the state of California's mandate on emission testing, much interest in the U.S. now centers on the SAE's proposed standard protocol for medium-speed Class-B applications. Designated J1850, the protocol uses a multiple-access bus-arbitration technique with nondestructive collisions.

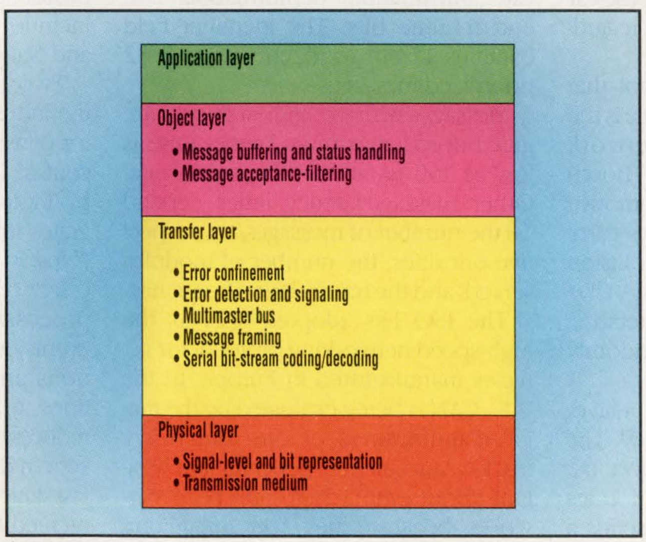
With this method, any network module can transmit if the bus is idle. While transmitting, a module must monitor the bus to ensure that no other device is transmitting. If the module detects transmission from another source, it stops transmitting and listens to the other message. This way, the dominant message isn't corrupted. The protocol also allows a cyclic redundancy check (CRC) to be generated on the message data. Based on the user application, other forms of hardware or firmware error checking can also be performed.

J1850 defines two data rates and two data-encoding techniques. A 41.6-kbit/s rate uses pulse-width modulation (PWM), and a 10.4-kbit/s rate uses variable pulse-width modulation (VPWM). Using VPWM data encoding can reduce required transmission speed so that the conventional logic section of an interface IC can be replaced with an 8-bit MPU equipped with appropriate software and hardware timers.

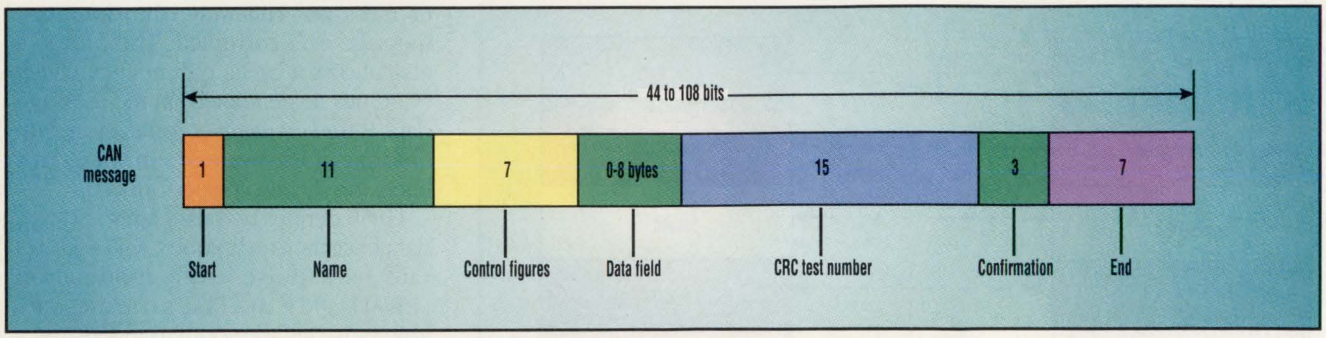
The J1850 protocol has been accepted in the U.S. by Chrysler Corp., Ford Motor Co., and General Motors. In Europe, the standard for Class-B diagnostic communications is designated ISO 9141. Unlike J1850, ISO 9141 reportedly doesn't require dedicated silicon to link data to external systems, since the serial data link of an on-board microprocessor already performs this function.

Because the European auto industry is using ISO 9141 as a diagnostic standard, ISO created a special subset of the standard, called ISO 9141 CARB, to avoid trade barriers. Although ISO 9141 CARB and J1980 are incompatible, they're close enough to be accepted by the state of California and the U.S. Environmental Protection Agency (EPA), provided a diagnostic tool for emission-related problems can distinguish between the two.

J1850 intends to make it easier to manufacture, drive, and service a car. But critics say the proposed protocol standard leaves too much room for different silicon implementations by different car companies. For example, in addition to allowing different transmission speeds and encoding methods, the specification in its present form also defines a number of options for implementing analog I/O functions, and filtering and synchronizing techniques. As a re-



5. THE CAN PROTOCOL developed by Robert Bosch GmbH for high-speed networking is based on a 4-layer version of the OSI reference model for networking. This implementation combines or omits three layers of the OSI model. A similar approach is taken by the proprietary SCP protocol developed by Ford and SGS-Thomson Microelectronics for intermediate-speed applications.



6. THE DATA FRAME for high-speed data transfers in the CAN network includes an 11-bit field for identifying up to 2032 different messages. Each message can consist of up to eight bytes.

sult, the J1850 hardware of Chrysler, Ford, and GM are presently incompatible.

Ford's version, the 40-kbit/s Standard Corporate Protocol (SCP), is based on a modified OSI model for networking. Developed by Ford and SGS-Thomson Microelectronics, Agrate, Italy, the system combines the transport and session layers of the model into one transport layer. GM's protocol operates at 10 and 10.4 kbits/s, and the Chrysler version runs at just under 8 kbits/s. In the face of the yet-unsolved standards puzzle, Chrysler elected to work with Silicon Systems Inc., San Jose, Calif., in developing a 3-chip semicustom solution. As for the Japanese car manufacturers, the jury is still out regarding the J1850 proposed standard.

The only networking protocol that has a chance for global acceptance is the 1-Mbit/s Controller Area Network (CAN), developed by Robert Bosch GmbH for Class A, B, and C automotive networks. The protocol employs carrier-sense, multiple-access with collision detection using arbitration (CSMA CD/A). Through a multimaster architecture, prioritized messages are sent randomly on a serial bus.

CAN is structured around a 4-layer version of the OSI model *(Fig. 5)*. The protocol handles bus contention between messages of different priorities by arbitration. This procedure sends a message identifier along the bus, bit-by-bit, until the highest-priority message gains control of the bus to send data. The advantage of this protocol is that multiple automotive subsystems can report data at one time, and data can be acted upon continuously.

TABLE 2. DIAGNOSTIC DATA-LINK PROTOCOLS FOR THE WORLD'S TOP 12 CAR PRODUCERS (RANKED BY VOLUME)

Car maker	Protocol
General Motors Corp.	J1850
Ford Motor Co.	J1850
Toyota Motor Corp.	J1850 or ISO9141
Nissan Motor Co.	J1850 or ISO9141
Volkswagen	ISO9141
Fiat Group	ISO9141
Chrysler Corp.	J1850 or ISO9141
PSA	ISO9141
Renault SA	ISO9141
Honda Motor Co.	J1850 or ISO9141
Mazda Motor Corp.	J1850 or ISO9141
Mitsubishi Motors Corp.	J1850 or ISO9141

A CAN dataframe contains from 44 to 108 bits *(Fig. 6)*. Bit fields within the CAN dataframe identify the start of the frame and the type of message being sent, and contain control figures, data, CRC information, conformation, and end-of-frame bits. The identifier field contains 11 bits to identify up to 2032 prioritized messages.

Messages with the highest priority are guaranteed a maximum latency time as low as 150 µs at a 1-Mbit/s data rate. Other message-latency times depend on the number of messages, the respective priorities, the number of modules served, and the transmission frequency.

The ISO has adopted CAN as the high-speed networking protocol for vehicles manufactured in Europe. In the U.S., CAN is being evaluated by the major manufacturers of cars and heavy trucks. Auto makers generally are hesitant about embracing high-speed networks because they feel integrating more functions into control modules is a more cost-effective approach. Where European cars have separate modules to control fuel injection, ignition timing, and transmission functions, U.S. designs integrate engine control and transmission control into one module.

The CAN protocol fares better with U.S. truck manufacturers because of the highly distributed nature of subsystems found in trucks. The SAE subcommittee for Truck and Bus Control and Communications Networks has selected the CAN protocol as the basis for the J1939 Class C network for truck and bus vehicles.

During the CAN protocol's development, Bosch worked with the Automotive Div. of Intel Corp., Chandler, Ariz., in the design of an application-specific 16-bit microcontroller. Working with a host microcontroller, the AN 82526 implements all of the functions of the CAN protocol. Other licensees for the chip include Motorola Inc., Signetics Co., and National Semiconductor Corp.

Two years ago, Motorola introduced the industry's first 32-bit microcontroller for consumer and industrial embedded-control applications. Developed jointly by Motorola and GM, the device integrates the equivalent of nine peripheral chips. In addition to the 68020 microprocessor core, the 68332 includes a second processing unit that services timing events, a module that supplies synchronous and asynchronous communications, a system-integration module that reduces external chip count and provides system debug capability, and 2 kbytes of fast static RAM. These functions are implemented by a total of 420,000 transistors on the chip.☐

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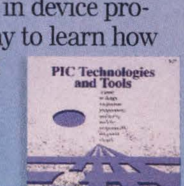

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QUAD HIGH-SIDE SWITCH HAS THERMAL WARNING

RATED FOR 6-TO30-V OPERation, the IR8400P/LMD18400 quad high-side switch controls four automotive loads, such as lamps and actuators in engine-control and antilock-braking systems. Each switch connects a 1-A load to the battery instead of ground to avoid accidental short-circuiting of the battery. Peak current rating for each of the four high-side switches is 3.75A.

On-chip logic circtuitry protects a load from burnout by limiting the device if power drawn by the load exceeds 15W. An early warning feature notifies a host microcontroller to take appropriate action when the chip's operating temperature approaches dangerous limits. Packaged in a 20-pin DIP, the chip combines bipolar, CMOS, and DMOS technologies. ***National Semiconductor Corp.**, 2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052-8090; Al Kelsch, (408) 721-6937. International Rectifier, 233 Kansas St., El Segundo, CA 90245; Arnold Alderman, (213) 607-8899.*

CIRCLE 551

INTELLIGENT POWER CHIPS DRIVE AUTOMOTIVE LOADS

TO REPLACE DISCRETE COMPOnents and electromechanical relays in road vehicles, the HA13702A bulb driver and HA13703A solenoid driver each combine digital logic circuits with power transistors on one IC. The HA13702A can control headlights, tail lights, turn signals, and instrument-panel illumination. The HA13703 can be used in automatic transmissions, or to control fuel injectors, antilock braking systems, and active suspension systems.

Both high-side switches can shut down in response to excessive load current, voltage, or temperature, and then signal the cause of failure to a local microprocessor. The drivers are also protected from reverse battery voltage and overvoltage from a malfunctioning alternator or voltage regulator. Housed in a 5-lead TO-220 package, the HA13702A is priced at \$3.15 each, and the HA13703A costs \$3.65 each, both in quantities of 1000. ***Hitachi America, Ltd.**, Hitachi Plaza, Brisbane, CA 94005-1819; Joe Kontur, (415) 244-7194.*

CIRCLE 552

SIMULATOR VERIFIES SUBSYSTEM DESIGNS

THE AUTOMOTIVE PACKAGE USED with the Saber simulator includes a library of models to simulate automotive electrical, mechanical, and optical subsystems. Predefined models for lamps, fuses, complex switches, and control blocks allow designers to observe automotive circuits operating together prior to the manufacturing stage of a vehicle. The Saber simulates any technology that can be described mathematically. Running with Saber on standard platforms, such as Sun, HP/Apollo, and DEC workstations, the Automotive package costs \$5000 for a single-user license fee. ***Analogy Inc.**, 9205 S.W. Gemini Dr., Beaverton, OR 97005; (503) 626-9700.*

CIRCLE 553

SWITCH-MODE CONTROLLERS OPERATE TO 1 MHz

THE TSC38HC42-45 LINE OF biCMOS switch-mode controller ICs delivers more than five times the output drive of bipolar equivalents. Intended for use in automotive ignition and antilock braking systems, the controller IC can drive current directly to individual engine spark plugs. As an option to a centralized ignition coil, each controller IC can convert low-voltage dc from a battery to high-voltage dc for a more precisely controlled spark. Available in 8- and 16-pin ceramic DIPs, the TSC38HC42-45 controller ICs are priced at \$0.89 each in quantities of 100,000. ***Teledyne Semiconductor**, 1300 Terra Bella Ave., Mountain View, CA 94039-7267; (415) 968-9241.*

CIRCLE 554

PRESSURE SENSORS MAKE PRECISION MEASUREMENTS

PRESSURE SENSORS IN THE NPH (TO-5 and TO-8 headers) and NPI (all-media compatible) families from NovaSensor with improved output-signal stability cover a pressure range from 2-in. H_2O to 10,000 psi. The pressure-sensing die has a 5-kΩ nominal bridge resistance and a 16-mV/V full-scale output for middle-range pressures.

The bridge resistance has a typical temperature coefficient of 0.25%/°C, and pressure sensitivity is –0.2%/°C. Stability over the first 100 hours after power is applied is about 10 mV/V, or 0.04% FSO for higher pressure ranges, and 0.15%, or 0.003-in. H_2O for the lowest pressure range of H_2O. For 100-piece quantities, the NPH devices are \$24 each, and the NPI sells for \$37 each. ***NovaSensor**, 1055 Mission Ct., Fremont, CA 94539; (415) 490-9100.*

CIRCLE 555

SERIAL EEPROMS BOAST FAST LOADING SPEED

FOR REAL-TIME AUTOMOTIVE applications, four families of serial EEPROMs can be loaded with data at rates of 1 byte/ms, which is at least five times quicker than prior devices. The 24CXXA family comes in bit organizations of 128 by 8 bits, 256 by 8 bits, and 512 by 8 bits. The 85CXX family is functionally equivalent to the 24CXXA family, but has a different pin configuration. Both families are loaded with data through the 2-wire (serial clock and address/data lines) I^2C bus data-transmission protocol.

The 93CXX family has 16-by-16-bit and 64-by-16-bit organizations and is loaded through a 3-wire interface (a serial clock line, a chip-select line, and a data I/O line). Offering selectable bit organization, the 1-kbit 59CXX family is an enhancement of the 93CXX family that provides status information during data transfers. Most of the devices support 100,000 erase/write cycles for systems requiring frequent data updates. Byte-read times are 200 ms for the 24CXXA and 85CXX families, 25 ms for the 93CXX family, and 20 ms for 59C11 family. The EEPROMs are available in 8-pin plastic DIPS and are priced from $0.55 to $1.57 each in quantities of 10,000. ***Microchip Technology Inc.**, 2355 West Chandler Blvd., Chandler, AZ 85224-6199; (602) 963-7373.*

CIRCLE 556

SPEECH SYNTHESIZER ICs TALK TO DRIVERS

A FAMILY OF FIVE ROM-based speech-synthesizer chips are targeted for automotive convenience and safety applications. The devices use a 12-bit digital-to-analog converter coupled with a 4-bit straight adaptive differential pulse-code modulation (ADPCM) algorithm to produce a synthesized voice, said to be close to human voice quality.

Three synthesizer family members are available. They include the MSM6373, the 6374, and the 6375. The members have 256 kbits, 512 kbits, and 1 Mbit of on-chip memory, respectively. The 6376 can operate with up to 16 Mbits of external memory, and the 6378 uses 256 kbits of OTP EPROM.

The 6373, 6374, 6375, and 6376 ROM-based speech-synthesizer chips are available in 18-pin plastic DIPs with prices ranging from $5.23 to $11.16 each in quantities of 25,000. The 6378 is available in a 16-pin DIP and sells for $15.21 each in quantities of 100. ***Oki Semiconductor**, 785 North Mary Ave., Sunnyvale, CA 94086; (408) 720-1900.*

CIRCLE 557

SYSTEM REPLACES ECUs IN PERFORMANCE CARS

THE HALTECH F4 SYSTEM, which consists of a replacement engine controller with two Motorola 68HC11 microcontrollers, a range of temperature and position sensors, and programming software and cables, peaks the fuel-injection and ignition functions in high-performance auto applications. The system replaces the entire existing electronic control unit (ECU) of a performance road vehicle. System requirements for programming the replacement ECU's fuel injection and ignition timing include an IBM PC/XT, /AT, or compatible PC with 512 kbytes of memory and a standard RS232C port.

System options include fuel injectors, throttle bodies, injector mounts, pressure regulators, a supplementary injector driver pack for staged injection, and ignition amplifiers and coils. The unit can program ignition systems with or without distributors. The Haltech F4 is priced at $1590 each. ***ITAC Automotive Technology**, 3121 Benton St., Garland, TX 75042; (214) 494-3073.*

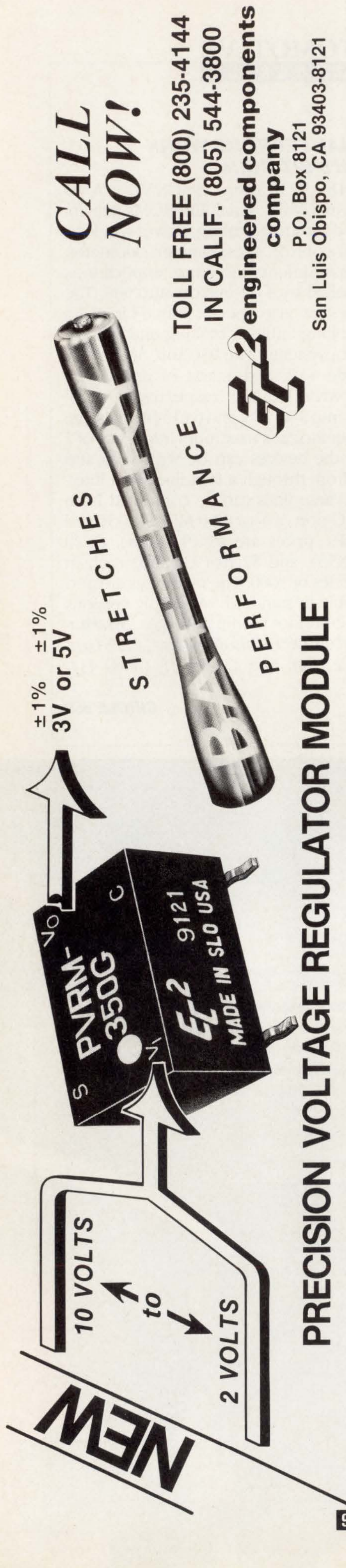
CIRCLE 558

SERIAL EEPROMS WORK WITH 8-BIT MCUs

THE 93CX66, 93CX56, AND 93CX46 CMOS serial EEPROMs are intended for smart- seating, power-window, mirror-control, speedometer/odometer, and instrumentation-panel applications controlled by 4-bit microcontrollers. The devices can also operate with 8-bit MCUs controlling antilock braking and engine-control systems. The 93CX66, 56, and 46 provide 4, 2, and 1 kbit of nonvolatile read/write storage, respectively, organized into 256, 128, and 64 16-bit registers.

Operating at a maximum frequency of 2 MHz, the devices can be written to and read from through a four-line serial interface. These lines can be controlled from the I/O port of 4- or 8-bit MCUs. Packaged in DIPs, prices are $5 (93CX66), $3.20 (93CX56), and $2.10 (93CX46) each in quantities of 1000. The memories are also available in standard 5-V supply versions and SO surface-mount packages. ***International CMOS Technology, Inc.**, 2125 Lundy Ave., San Jose, CA 95131; (408) 434-0678.*

CIRCLE 559



PRESSURE SENSOR IS SIGNAL-CONDITIONED

THE MPX5100A IS A 0-15 PSI, pressure sensor that integrates the sensing element, offset calibration, temperature-compensation circuitry, signal amplification, and an absolute pressure reference on the same chip. The sensor can be linked directly to MPU-based systems, and has analog-to-digital inputs to calibrate its output from 0.5 V to 4.5 V.

Temperature is compensated over the range of 0°C to +85°C. The sensor uses a silicon shear-stress strain gage, which has a ±0.2% FSS typical over the range of 0 to 15 psi absolute pressure. Available in the basic element or top- or side-ported packages, the sensor is priced at $45 each in quantities over 100. An automotive version is available with a manifold-pressure transfer function and expanded temperature range. ***Motorola Inc.,*** *MD Z201, 5005 E. McDowell Rd., Phoenix, AZ 85008; (602) 244-4556 or 1-800-752-3621.*

CIRCLE 560

PIEZO FILM SENSOR EYES AIRBAG SYSTEMS

AS AN ALTERNATIVE TO PIEZOresistive types, the ACH-01 accelerometer uses a multilayered piezoelectric polymer film as the sensing element for deploying airbags. The film laminate is bonded to an alumina substrate and a powdered-metal inertial mass. The substrate also includes a low-bias current FET that provides a low output impedance, and a high-impedance resistor that allows low-frequency operation. The device operates continuously in temperatures up to 150°C and is priced at $5 each in quantities of 300,000. ***Atochem Sensors Inc.,*** *P.O. Box 799, Valley Forge, PA 19482; (215) 666-3500.*

CIRCLE 561

ADCs TARGET AUTO APPLICATIONS

TWO INDUSTRIAL-GRADE (–40 TO +85°C) analog-to-digital converters meant for sensing systems that monitor manifold absolute pressure, mass air flow, and engine temperature offer a conversion time of 8 ms. Each of the converters has eight analog input channels, an on-chip voltage reference, and multiplexer and track-and-hold functions. Package options are plastic or ceramic DIP, and 14- and 20-pin SO packages. In 100-piece quantities, the ADC08038 with a q1-LSB linearity error is priced at $3.95 each. The more-accurate version (q0.5-LSB linearity error) goes for $5.95 each.

An industrial-grade 18-bit converter, the ADC1061 with q1-LSB linearity error, offers a 1.8-ms conversion time for mobile communications applications. Maximum power consumption is 235 mW. The 5-V TTL- and CMOS-compatible device accepts input analog voltages from 0 to 5 V and works with an external 5-V reference. For 100-unit quantities, the 20-pin plastic DIP version sells for $11.90 each, the 20-pin cerDIP version for $14.90 each, the 20-pin SOIC version for $12.90, and the 20-pin cerDIP version for $44.70. ***National Semiconductor Corp.,*** *2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052-8090; (408) 721-5000.*

CIRCLE 562

RISC MCUs SPEED ALGORITHM EXECUTION

TWO NEW 8-BIT MICROCONtrollers have a throughput of 5 MIPS to control motors and servos requiring high-speed execution of algorithms. Both devices are available in EEPROM and OTP (one-time programmable) versions for in-circuit programming. Programs and codes can be loaded at the end of the production line through a special connector. Both parts are available in plastic DIP, ceramic DIP, and SOIC packages. The PIC16C55 comes in a 28-pin version, and the PIC16C54 is available in an 18-pin package. The PIC16C54 and PIC16C55's 4-MHz plastic DIP versions sell for $2.40 and $2.95 each, respectively, in quantities of 2500. ***Microchip Technology Inc.,*** *2355 West Chandler Blvd., Chandler, AZ 85224-6199; (602) 963-7373.*

CIRCLE 563

MINIATURIZATION COMES TO LED DISPLAYS

THE SL(X)2016 SLIMLINE DOMINO display module from Siemens Components is the industry's first 4-character, stackable LED display with built-in logic functions. The 0.4-in.-high by 0.784-in.-wide plastic package can be stacked horizontally and vertically. Pin spacing for the 14-pin device is 0.100 in. Built-in CMOS drive circuitry reads 128 special ASCII characters, including English, German, Italian, and Scandinavian languages.

The integrated circuit includes memory, a ROM decoder, multiplexing circuitry, and LED drivers. The 5-by-7 dot-matrix LED characters are 0.186 in. high with their centers spaced 0.197 in. apart. In quantities of 100, red displays cost $20.35 each, and high-efficiency red, green, and yellow displays cost $20.90 each. ***Siemens Components, Inc.,*** *19000 Homestead Rd., Cupertino, CA. 95014; Rick Waltonsmith, (408) 725-3423.*

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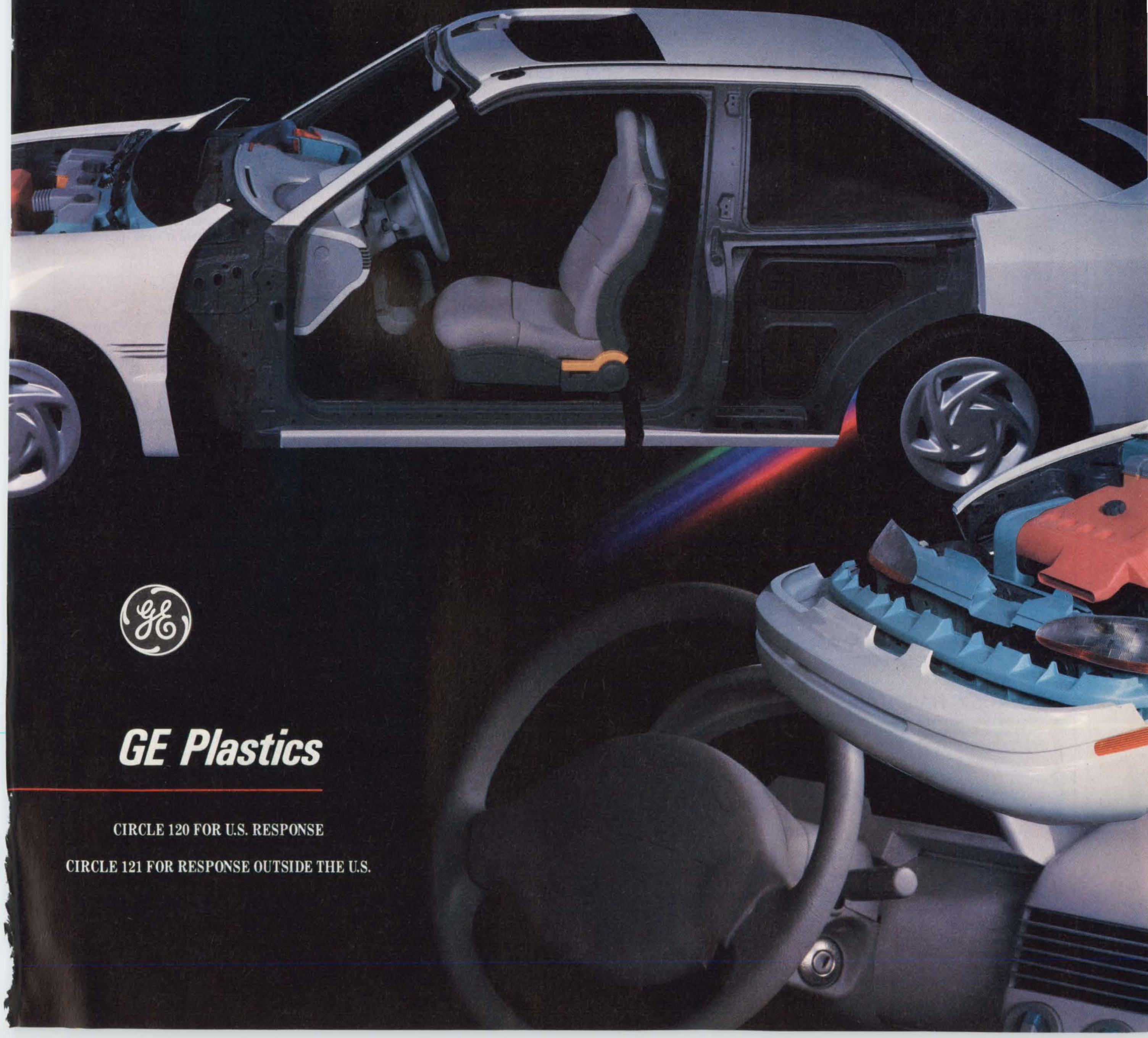

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AUTOMOTIVE ELECTRONICS RESOURCE FILE

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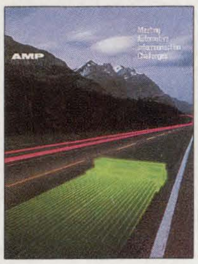
AUTOMOTIVE INTERCONNECTIONS



Information on the AMP approach to the automotive industry, describing the company's specialized group that has the sole focus of helping the automotive industry solve its interconnection problems.

AMP Incorporated, Harrisburg, PA
CIRCLE 600

MULTIFUNCTION SYNTHESIZERS

Complete overview including all specs on Keithley's new line of multifunction synthesizers. Based on Direct Digital Synthesis, DDS allows accuracy down to 0.0005% and provides greater precision at lower frequencies. Up to 12 digit resolution. Burst Trigger Gate functions.

Keithley Instruments Inc., Cleveland, Ohio
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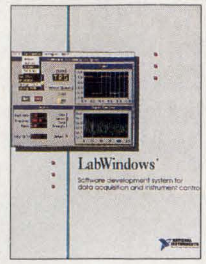
LabWindows®



Free eight-page brochure describes LabWindows® 2.0 instrumentation software. LabWindows is attractive to programmers using QuickBASIC and C for test, data acquisition, and instrument control applications. The new User Interface Library makes it easy to create graphical user interfaces for application programs. Package also includes extensive data analysis libraries. (800) 433-3488

National Instruments
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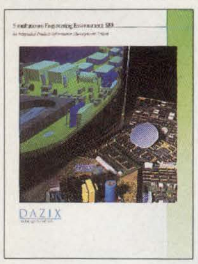
SIMULTANEOUS ENGINEERING ENVIRONMENT:SEE



This brochure offers an overview of the DAZIX Simultaneous Engineering Environment (SEE). SEE is an integrated product management information system. SEE integrates data, tools, and users—and automates the product development cycle.

DAZIX, An Intergraph Company, Huntsville, AL
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DC-DC POWER SUPPLIES

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Melcher Inc., 200 Butterfield Dr., Ashland, MA
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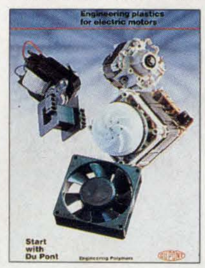
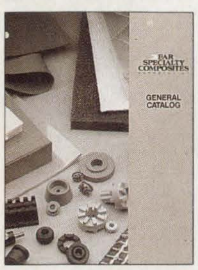
ENGINEERING PLASTICS



Catalog covers engineering polymers used in electric motors. Applications include plastic bearings, extensions of thermoplastic motor frames, rotor insulation, and protective devices.

Du Pont
CIRCLE 605

NEW NOISE CONTROL CATALOG



E-A-R's 28-page, new, full-line catalog contains valuable performance characteristics for the control of noise, vibration, shock, motion and mechanical energy.

E-A-R Specialty Composites Corp., Indianapolis, IN
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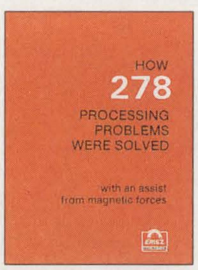
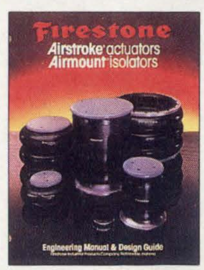
278 PROCESSING PROBLEMS SOLVED



58-page booklet from Eriez Magnetics describes how company solved 278 processing problems...with an assist from magnetic forces. Booklet charts actual problems encountered by processing companies, & the corresponding Eriez solution.

Eriez Magnetics, Erie, PA
CIRCLE 607

FIRESTONE ENGINEERING MANUAL & DESIGN GUIDE



Firestone's flexible air springs (*Airstroke®* actuators; *Airmount®*-isolators) offer significant advantages over conventional actuators & isolators. 100-pg. manual provides operating characteristics for many of company's standard air springs.

Firestone Industrial Products Co., Noblesville, IN
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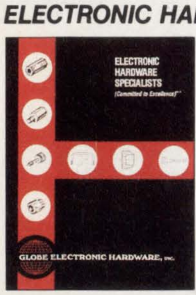
ELECTRONIC HARDWARE



FREE 204-pg. cat. details its comprehensive line of electronic hardware. Design drawings, specs, material & finish choices are incl. Avail. hardware incl. jack screws, handles & ferrules, thumb screws, shoulder washers, standoffs & spacers, shoulder screws and more.

Globe Electronic Hardware, Woodside, NY
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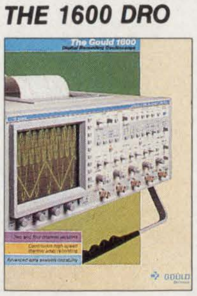
THE 1600 DRO



Users of scopes & hard copy recorders will both welcome the arrival of the DRO. If you want fast screen dumps of your data, hard-copy records of high-speed spurious events, or ability to print & archive test results for presentations or for legal purposes, the 1600 DRO is ideal for your appl.

Gould Inc., Cleveland, OH
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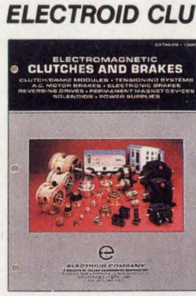
ELECTROID CLUTCHES & BRAKES



Complete 160-pg product line cat. Broad range of electromagnetic devices for rotary motion control. Incl. clutches, brakes, clutch/brake modules, tensioning systems, power supplies, permanent magnet devices and solenoids.

Electroid Co., Springfield, NJ
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Discrete Products Division

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Philips Components

PHILIPS

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A Look Back At A Company Built On Looking Ahead.

CENTENNIAL 100 1891-1991

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Gerard Philips insisted on strong research as the basis of innovation and quality.

In 1891 Gerard Philips was a young engineer dedicated to research as the single most important doorway to future product quality and technical innovation. Today the Philips organization worldwide is distinguished by that dedication to quality in the design, materials, and manufacturing processes which go into its products.

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Problem-solving, in a variety of ways, is a driving force of product quality improvement. Thus, departmental quality circles are an integral part of QIS—identifying and analyzing problems, then devising and implementing solutions.

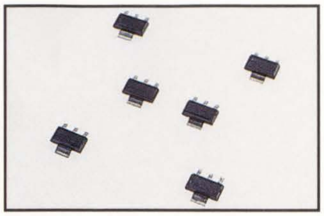
In addition, Philips has adopted the international ISO 9000 standard as its global quality system, to ensure consistent product quality from all Philips manufacturing facilities. Currently, an aggressive plan for certification is underway throughout Philips' discrete semiconductor operations.

The philosophy of making the product right the first time by using such tools as SPC and FMEA with verification by means of PPM measurement ensuring high reliability and long-life expectancy gives a sound basis for choosing Philips Components.

Our century-long spirit of innovation continues. Use the attached reply card to learn more about our products.

On front: Early production combined the art of glass-blowing with the sciences of physics and chemistry.

Low On-Resistance D-MOS FET Now In 1 Watt SMD® Package.



Now you can specify an N-channel enhancement mode vertical D-MOS FET in Philips' versatile SOT-223 surface mount package.

With a typical $R_{DS(on)}$ of 1.8 ohms, the device is specifically designed to provide very fast and controlled switching at low voltages where power consumption becomes critical.

The BSP108 type is intended for use in relay functions, high-speed switching functions and motor control.

Typical applications include disc drive controller boards, telecommunications switching, and precise motor control.

BSP108 samples are available now.

Longer-Life Capacitors For AC Motor Start: Series 3500 Aluminum Electrolytics.

These electrochemical devices carry operational ratings from 50 Hz to 65 Hz at −40 °C to +65 °C, and are designed to maintain stable electrical characteristics after 75,000 starts. 110VAC and 125VAC.

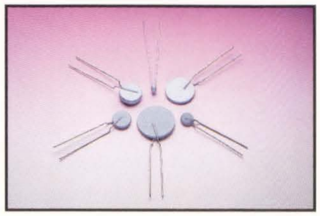
One case style, with choice of four terminal types. All have a special metal-to-metal under-cover connection for positive terminal contact with the capacitor roll tabs.

Construction includes aluminum foil which is etched to increase its effective surface area — increasing the capacitance per unit volume of the finished capacitor. The molded plastic housing requires no insulation.

Available to meet both EIA Type I and Type II specifications.

On special order, units can be supplied with bleeder resistors soldered across the terminals.

Small, Fast, And Sensitive PTC Overload Thermistors.



New thermistors respond in as little as 0.1 seconds, to protect circuits from current overload. They react to 1.5 times the normal load (at 25 °C).

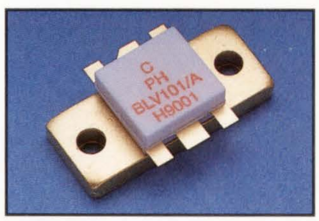
Based on the latest developments in PTC ceramics, these small devices (footprint: 0.2" lead spacing) can withstand high maximum currents for their body size.

Voltage ratings 30 Vdc to 60 Vdc, 145 Vrms and 265 Vrms.

Applications include loudspeakers, ballasts, small motors (VCR, automotive, CD, etc.), rechargeable batteries, and transformers.

Available in bulk or tape and reel.

Enhanced Reliability And Performance In New 50 W UHF Power Transistors.



New NPN silicon planar epitaxial transistors from Philips Components are primarily for common-emitter, class AB operation in base-station transmitters.

Both use a 26 V supply voltage and deliver 50 W output power.

BLV101A, in the 850 to 900 MHz range, delivers power gain greater than 8.5 dB.

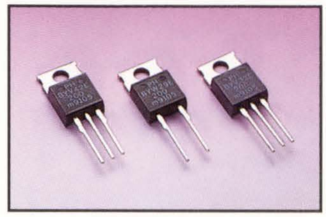
BLV101B, in the 900 to 960 MHz range, delivers power gain greater than 7.5 dB.

Both are in a ceramic-capped, 6-lead flange package, with all leads isolated from the flange.

Both feature implanted ballasting resistors for optimum temperature profile...high input and output impedances for easy matching...gold metallization for excellent reliability.

Delivery: 10 to 12 weeks ARO.

NEW: Ruggedized Rectifiers With Ultra-Fast Recovery.



New BYW29E, BYV32E, and BYV42E Series devices are high-efficiency, glass passivated, ruggedized rectifier diodes, primarily for use in switchmode power supplies.

Reverse voltage ratings (VR) are 100, 150, and 200 V. When subjected to excessive reverse voltages, these rectifiers can clamp electrostatic discharges and voltage spikes with energies as high as 30 milli-joules, to avoid equipment damage.

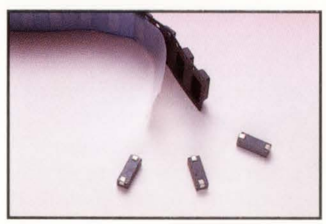
Reverse recovery time is less than 25 nsec, and the soft-recovery characteristic minimizes RF emissions. So these ruggedized rectifiers require smaller snubber circuits than conventional diodes — allowing manufacturers to reduce their equipment's overall size, weight, and cost.

Forward voltage drop is less than 0.85 V at maximum rated current.

BYV32E and BYV42E Series rectifiers contain two common-cathode diodes and have excellent diode matching due to their monolithic construction.

Delivery is 8 weeks ARO.

NEW: Ferrite Beads For Surface Mount Production.



New beads are in .335" (8.9mm) and .160" (4.6mm) size categories, and are manufactured of 4S2 ferrite material.

Impedances match those of the most frequently used tape and reeled beads-on-wire.

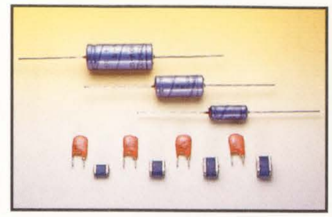
Construction: a piece of flat tinned cooper wire passed through and crimped on the rectangular ferrite bead.

Packaging: on tape with 8mm between centers, wrapped on 13-inch reels (2,800 pieces per reel) in accordance with EIA Standard 481A.

Applications: EMI/RFI suppression.

Samples now available.

For Harsh Environments: Solid Aluminum Capacitors.



Sudden shock...long-term vibration. Sub-zero cold...searing heat. Oil and water, dust and grime.

For applications (like automotive) involving conditions like these, specify SAL solid aluminum capacitors by Philips Components.

They are particularly rugged, and perform reliably despite substantial physical and chemical abuse. SAL units tolerate wide variations in electrical loads, and withstand reverse voltages and ripple currents.

They have low-drift characteristics and no inherent failure mechanisms.

These SAL capacitors operate from −40 °C to +175 °C, and are available in axial, resin-dipped, and surface mount configurations.

XX1610 Image Intensifiers Perform Like GEN III But Offer GEN II Economy.

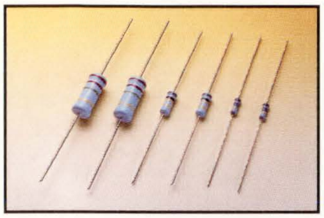
Philips Components XX1610 Image Intensifiers have minimum guaranteed sensitivity of 500 μA/lm and typically provide 650 μA/lm. Guaranteed minimum signal-to-noise ratio is 15.5; warranted life is 7,500 hours.

Developed to surpass S25 and GaAs photocathodes, XX1610 tubes were evaluated by the U.S. Army for possible night-vision use.

The evaluation report said sensitivity was "the highest ever seen" for an S25 cathode, and tube life was "at least equal to that of third-generation tubes."

The Army's conclusion: "Philips second-generation tubes...considered to be...competitors for use...with third-generation requirements."

Extra-Stable High Value Resistors For 68 Megohm, 10 KV Service.



New VR Series resistors are for use in circuitry where high resistance, stability, and reliability are required in the presence of high voltages.

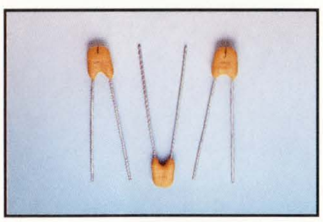
The VR Series includes resistance values to 68 megohm and voltage ratings to 10 kilovolt. Power ratings are 1/4, 1/2, and 1 W at 70 °C; 5% tolerance level is available.

The VR Series is constructed of cermet film, deposited on a high-grade ceramic body. The resistance layer is helically grooved, then plated copper leads are welded to the end caps.

Light blue epoxy coating protects against destructive environmental conditions. The resistors are color-banded for easy identification.

Availability: stock to 10 weeks ARO.

Gap-Kap® Capacitor Includes Spark Gap For Cost-Saving Over-Voltage Protection.



This special ceramic capacitor provides a safe, reliable discharge path for stray transient overvoltages and static voltage buildup. So circuit designers can specify lower-voltage components (at lower cost) with assurance that over-voltage conditions will be prevented.

Gap-Kap capacitance range, .75 pF to .02 mF; tolerances ±10%, ±20%, or maximum value.

Working voltages 1000 to 3000 VDC; arc voltage 1000-2000, 2000-3000, or 4000-6000 VDC.

For applications in a wide range of industrial and commercial equipment.

SMD® Tantalum Chips Offer Extended Capacitance.

Philips is introducing a new line of conformally coated tantalum chip capacitors for use in high-reliability and medical applications.

The 49EC Series capacitors offer high capacitance density with low ESR values at 100 kHz and low DC leakage current. They're designed for operation from −55 °C to +85 °C with rated DC voltage applied. At 67% of rated voltage, the temperature range can be extended to +125 °C.

The new capacitors, though non-military, are pad-compatible and interchangeable with established MIL-C-55365/4 CWR06 conformally coated and CWR09 molded tantalum chips.

Depending on the voltage rating, 49EC chips offer two to three times the capacitance values of CWR06 and CWR09 products in the same case size. Rated DC voltages of 4, 6, 10, 15, 20, 25 and 35 volts are available in each of eight case sizes. These sizes are identical to those of CWR06 devices. Gold-plated or hot solder-dipped terminals are available. Standard capacitance tolerances include ±20%, ±10% and ±5%.

Delivery is 12 to 14 weeks ARO.

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CIRCLE 521

MAKE ALTERNATE-ACTION SWITCH

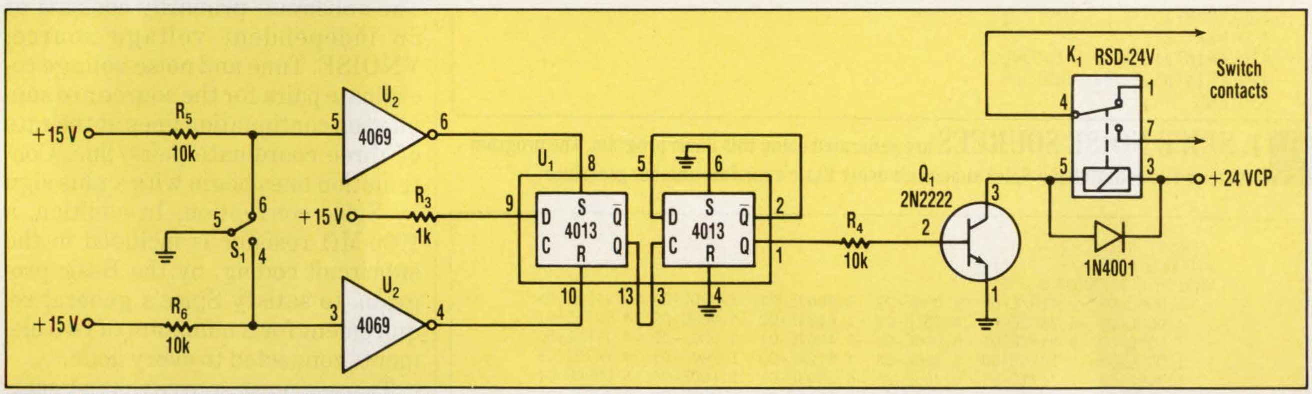
STEPHEN TOMPOROWSKI
Philips Medical Systems, 710 Bridgeport Ave., Shelton, CT 06484; (203) 926-7367.

Frequently, when upgrading old equipment, it's difficult to find pushbutton switches that are the same as those used. And to find a pushbutton switch with equivalent momentary and alternate-action capabilities is next to impossible. Obviously, for cosmetic reasons, a row of pushbutton switches would look and mount better if they're all alike.

One solution is to electrically transform the momentary switch into alternate action. This circuit debounces the switch and introduces alternate action simultaneously. It doesn't matter how many poles the switch has, because the relay supplies as many poles as needed.

One half of U_1, a 4013 CMOS D flip-flop, and 1/3 of U_2, a 4069 CMOS hex inverter, form a switch debouncer *(see the figure)*. When a pushbutton switch, S_1, is pushed, the flip-flop's state is changed from set to reset, changing Q from high to low. Because the flip-flop is set or reset on the first high, subsequent highs or lows on the same line, as in a bouncing switch contact, have no effect on Q's state. With both set and reset low, the flip-flop retains the previous state. If the inverters weren't there, the bounce state could cause both set and reset to be high—an unstable state in the 4013. This may provoke Q to toggle.

When S_1 is released, Q is returned to the high state because the flip-flop is again set. It's this edge that causes the 4013's second half to toggle. This half is set up as a one-bit counter with the $\overline{Q}$ output tied to the D input. Because only one rising edge occurs per switch push, this second section acts like an alternate-action, push-on, push-off switch. The Q output can then be used to drive a high-gain transistor to pull in a relay. The RS relay is used here as an example.□



THIS CIRCUIT TRANSFORMS **a momentary switch into an alternate action switch. It also debounces the switch.**

CIRCLE 522

CREATE SPICE NOISE SOURCES

DONALD B. HERBERT
26824 Via Desmonde, Lomita, CA 90717; (213) 325-7249.

To determine a circuit's time response to an input stimulus characterized as Gaussian noise, Spice is usually the best option. However, Spice doesn't contain a built-in noise source. Nevertheless, noise sources can be routinely modeled in Spice using the supplied capability. A simple PC Basic program uses the random number generator supplied in Basic to create Gaussian noise data with specified rms values *(Fig. 1)*. The program outputs the noise data to a file called NOISE.MOD in the form of a Spice subcircuit model. The model primarily consists of a piece-wise linear (PWL) independent voltage source that's described by randomly selected voltage coordinate values generated in the program.

The program uses the formula:

RANDG = RMS * (SUM – 6)

to generate each Gaussian noise value at prescribed time intervals. RANDG represents the noise value, RMS is the desired rms value, and SUM is the sum of twelve uniform random numbers, each selected over the interval of 0 to 1. The Basic RND function obtains the random numbers *(see statements 260 through 280, Fig. 1)*. The RMS value, which is specified as 1 in statement 170, can be changed to any RMS value. The program uses the Randomize statement and Timer function to get a new random number seed each time the program is executed *(see statement 180, Fig. 1)*.

By repeatedly using the same noise data, the effect of circuit-parameter variations can be easily assessed. However, because a different set of random numbers generates the voltages in the PWL source

```
100 ' *****************************************************************
110 ' *              THIS PROGRAM GENERATES A PWL NOISE SOURCE              *
120 ' *                IN THE FORM OF A SPICE SUBCIRCUIT MODEL                *
130 ' *                   WRITTEN BY: D. B. HERBERT  3/20/91                  *
140 ' *****************************************************************
150 '
160 DEFSNG A-H,O-Z
170 NPOINTS=250 : RMS=1! : SFACT=1E-09
180 RANDOMIZE TIMER
190 OPEN "NOISE.MOD" FOR OUTPUT AS #1
200 PRINT#1,".SUBCKT NOISE  2  1"
210 PRINT#1,"*SOURCE NODES: +  -"
220 PRINT#1,"VNOISE 2 1 PWL(0.0 0.0
230 N=1
240 FOR I = 1 TO NPOINTS
250  SUM = 0!
260  FOR J = 1 TO 12
270   SUM = SUM + RND
280  NEXT J
290  RANDG(N)=RMS*(SUM-6)
300  IF N < 3 AND I < NPOINTS THEN 390
310  FOR J =1 TO N
320   IF J = 1 THEN PRINT#1,"+";
330   PRINT#1,USING" ##.###^^^^";(I-N+J)*SFACT;
340   PRINT#1,USING" ##.####^^^^";RANDG(J);
350  NEXT J
360  IF I >= NPOINTS THEN PRINT#1,")";
370  PRINT#1," "
380  N=0
390  N=N+1
400 NEXT I
410 PRINT#1,"R 2 1 1000MEG"
420 PRINT#1,".ENDS NOISE"
430 END
```

1. SPICE NOISE SOURCES are generated using this Basic program. The program creates a file containing a Spice subcircuit using Basic's random-number generator.

```
.SUBCKT NOISE  2  1
*SOURCE NODES: +  -
VNOISE 2 1 PWL(0.0 0.0
+  1.000E-09 -1.4197E+00  2.000E-09  3.8369E-01  3.000E-09 -2.9951E-01
+  4.000E-09 -5.7405E-01  5.000E-09 -1.6189E+00  6.000E-09 -4.9975E-01
+  7.000E-09 -9.8147E-01  8.000E-09 -3.4067E-01  9.000E-09 -2.1782E+00
+  1.000E-08 -1.2316E+00  1.100E-08  1.8124E+00  1.200E-08 -4.9475E-01
+  1.300E-08 -1.7571E-01  1.400E-08 -6.3993E-01  1.500E-08  5.0396E-01
+  1.600E-08  6.3560E-01  1.700E-08  3.1041E-01  1.800E-08  4.4709E-01
+  1.900E-08 -1.4849E+00  2.000E-08 -2.7774E-01  2.100E-08  2.0206E-01
+  2.200E-08  2.0134E-01  2.300E-08  1.2677E+00  2.400E-08  4.3708E-01
+  2.500E-08  4.2109E-01  2.600E-08 -2.0529E-01  2.700E-08  1.1837E+00
+  2.800E-08  4.5195E-01  2.900E-08  8.8940E-01  3.000E-08 -1.6009E+00
+  3.100E-08  6.8480E-01  3.200E-08 -5.6125E-01  3.300E-08 -4.7116E-01
+  3.400E-08  1.8627E-01  3.500E-08  1.1930E+00  3.600E-08  1.0693E+00
+  3.700E-08  2.6131E-01  3.800E-08 -6.7178E-01  3.900E-08  1.3019E-01
+  4.000E-08 -1.9844E+00  4.100E-08  2.0087E+00  4.200E-08 -3.2210E-03
+  4.300E-08 -1.0818E+00  4.400E-08 -2.0506E+00  4.500E-08  6.9279E-01
+  4.600E-08  1.3638E+00  4.700E-08  9.7891E-01  4.800E-08 -1.4573E+00
+  4.900E-08 -7.6445E-01  5.000E-08  1.6012E+00  5.100E-08 -2.6580E-01
+  5.200E-08  4.6722E-01  5.300E-08  2.5588E+00  5.400E-08  8.8088E-01
+  5.500E-08  1.6059E+00  5.600E-08  3.9494E-01  5.700E-08  1.5845E+00
+  5.800E-08 -6.2537E-01  5.900E-08  2.0160E+00  6.000E-08 -2.3003E-03
+  6.100E-08 -7.6554E-01  6.200E-08  2.5437E-01  6.300E-08  3.8630E-01
+  6.400E-08 -2.0526E+00  6.500E-08  4.3055E-01  6.600E-08  6.9198E-01
+  6.700E-08  1.1387E+00  6.800E-08  9.1587E-01  6.900E-08  9.4650E-02
+  7.000E-08  8.5932E-01  7.100E-08 -3.0502E-01  7.200E-08  5.7504E-01
+  7.300E-08  1.4865E-01  7.400E-08 -1.0717E+00  7.500E-08  1.4771E+00
+  7.600E-08  5.9674E-01  7.700E-08 -1.4856E+00  7.800E-08  1.0707E+00
+  7.900E-08 -9.3020E-02  8.000E-08  1.6529E+00  8.100E-08  1.1382E-01
+  8.200E-08  4.5850E-01  8.300E-08  4.0641E-01  8.400E-08  4.1531E-01
+  8.500E-08 -1.3126E-01  8.600E-08 -7.3646E-01  8.700E-08 -6.0270E-01
+  8.800E-08  5.5592E-01  8.900E-08 -2.9894E-01  9.000E-08 -3.4232E-01
+  9.100E-08  3.0152E-01  9.200E-08  7.4657E-01  9.300E-08  5.3265E-01
+  9.400E-08  8.1282E-01  9.500E-08 -1.4591E+00  9.600E-08 -1.3409E+00
+  9.700E-08 -1.7146E+00  9.800E-08 -1.0992E+00  9.900E-08 -4.6256E-01
+  1.000E-07  9.6553E-01)
R 2 1 1000MEG
.ENDS NOISE
```

2. THIS LISTING TYPIFIES the Spice subcircuit models produced by the Basic program. The listing was obtained with NPOINTS set to 100.

each time the program is executed, repetitive runs can also be made with different noise data.

The program is set up to generate 250 time points at time intervals of 1 ns. To get a different number of time points and/or time intervals, the values given for Npoints and Sfact, respectively, should be changed. Also, the PWL function defined by statement 220 has an initial value of zero at time zero. The program can easily be modified to randomly choose the initial value as well. Likewise, the mean value of the generated noise defaults to zero. However, a nonzero mean can be implemented in a simulation by placing a dc source in series with the noise source.

A listing of a noise subcircuit generated by the program was obtained with NPOINTS set to 100 *(Fig. 2)*. The subcircuit primarily consists of an independent voltage source, VNOISE. Time and noise voltage coordinate pairs for the source are supplied on continuation lines at the rate of three coordinate pairs/line. Continuation lines begin with a plus sign by Spice convention. In addition, a 1000-MΩ resistor is included in the subcircuit coding, by the Basic program, to satisfy Spice's general requirement for a minimum of two elements connected to every node.

To use a noise source that's generated by the Basic program, the content of NOISE.MOD would typically be included in the Spice input data file. It would also supply a reference to the subcircuit with a pseudo-element definition. For example, the line

XNOISE 1 0 NOISE

in the Spice input data would connect the noise source in the subcircuit from node 1 to node 0 (ground).☐

References:

Miller, Alan R. *Pascal Programs for Scientists and Engineers*, Sybex Inc.; 1981.

Vlaidmirescu, A. et al. *Spice Version 2G.6 User's Guide*, Dept. of Electrical and Computer Engineering, University of California, Berkeley, CA; 1983.

CIRCLE 523

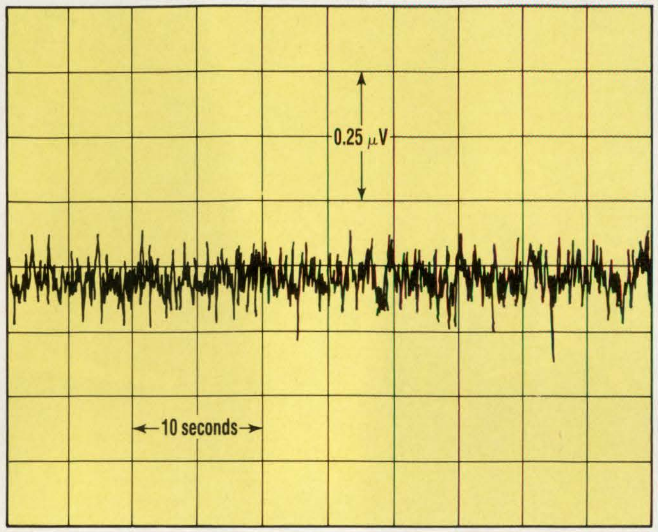
CHOPPER FETS IMPROVE AMP

JIM WILLIAMS
Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035; (408) 954-8400.

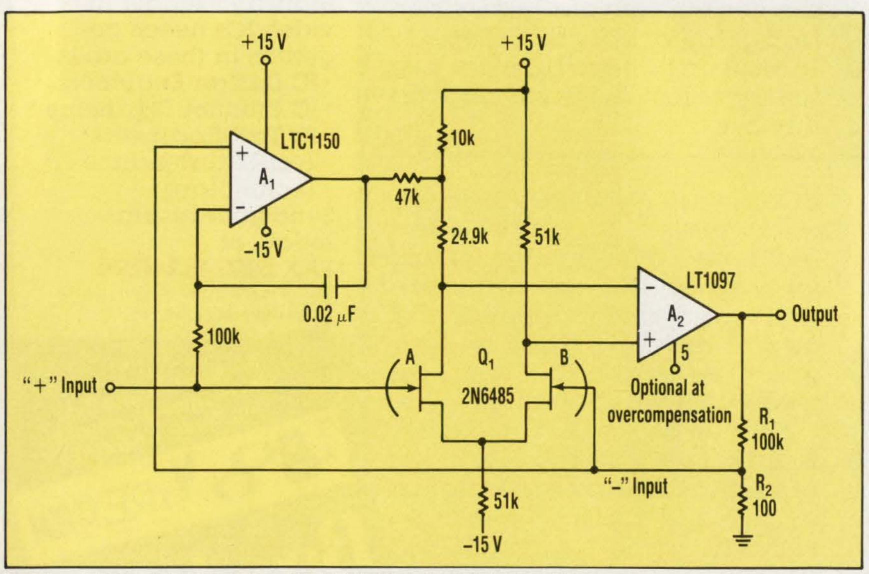
Combining the low drift of a chopper-stabilized amplifier with a pair of low-noise FETs results in an amplifier with 0.05-μV/°C drift, offset within 5 μV, 50-pA bias current, and 200-nV noise in a 0.1- to 10-Hz bandwidth. The noise performance is especially noteworthy because it's almost eight times better than monolithic chopper-stabilized amplifiers.

The FET pair (Q_1) differentially feeds A_2 to form a simple low-noise op amp *(Fig. 1)*. Feedback, supplied by R_1 and R_2, sets the closed-loop gain (1000 in this case). Although Q_1 has very low noise characteristics, its 15-mV offset and 25-μV/°C drift are poor. A_1, a chopper-stabilized amplifier, corrects these deficiencies by measuring the difference between the amplifier's inputs and adjusting Q_{1A}'s channel current to minimize the difference. Q_1's skewed drain values ensure that A_1 will be able to capture the offset. A_1 supplies whatever current is required into Q_{1A}'s channel to force the offset within 5 μV. Also, A_1's low bias current doesn't appreciably add to the overall 50-pA amplifier bias current. As shown, the amplifier is set up for a noninverting gain of 1000, although inverting operation and other gains are possible.

The circuit's noise performance—measured in a 0.1-to-10-Hz bandwidth—is almost an order of magnitude better than any monolithic chopper-stabilized amplifier *(Fig. 2)*. Yet it still retains low offset and drift. A_2's optional overcompensation can be used to optimize damping when low closed-loop gains are used.□



2. PLOTTED IN A 0.1-to-10 Hz bandwidth, the circuit's noise is eight times better than monolithic chopper-stabilized amplifiers.



1. THE CHOPPER-STABILIZED FET PAIR combines the best of both worlds. Q_1 exhibits extremely low noise, and its offset and drift are reduced with A_1, a chopper-stabilized amplifier.

IFD WINNER

IFD Winner for February 28, 1991

M.S. Nagaraj, ISRO Satellite Centre, Digital Systems Div., Airport Rd., Vimanapura P.O., Bangalore 560 017 India. His idea: *"Measure Duty Cycle To 0.5% Accuracy."*

IFD Winner for March 14, 1991

Steven R. Blackwell, UDS/Motorola, 5000 Bradford Dr., Huntsville, AL 35805; (205) 430-8112. His idea: *"Frequency Divider is Programmable."*

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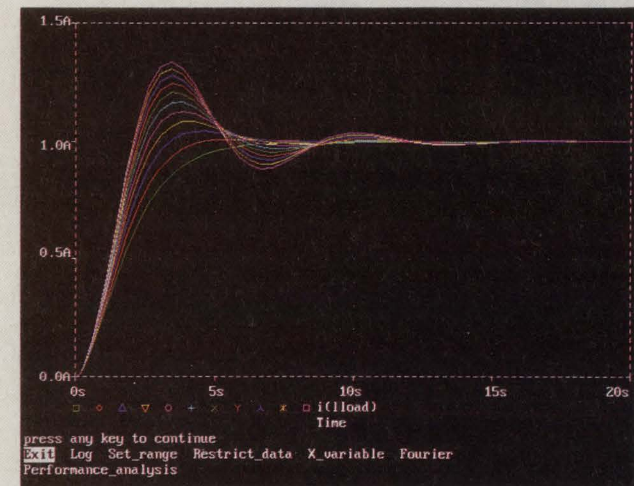
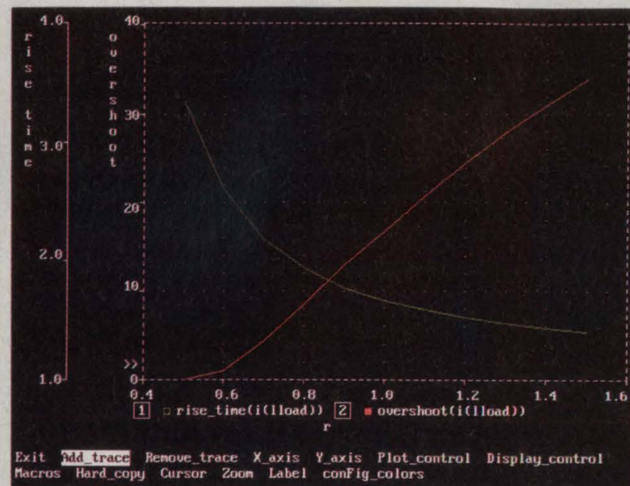
BE14

CIRCLE 227 FOR U.S. RESPONSE   CIRCLE 228 FOR RESPONSE OUTSIDE THE U.S.

We Deliver Answers



Current through an inductor with stepped resistance



Rise time and overshoot as a function of resistance

Explore the Intricacies of Your Circuit Design...

Using PSpice's Probe 5.0 with Performance Analysis

With Probe's new **Performance Analysis** feature, in-depth examination and processing of PSpice simulations is at your fingertips. By applying any number of user-defined goal functions (such as pulse-width or overshoot) to multiple PSpice waveforms, a circuit's behavior can be tracked as a function of changing conditions (such as temperature, source voltage, or model parameter values). It becomes easy to plot quantities like propagation delay versus temperature, bandwidth versus Q, or pulse-width versus component value. **Performance Analysis**, along with Probe's well-known high-resolution graphical display of simulation and post-processed results, makes it easier than ever to visualize trends in the circuit's behavior.

Other features lending to Probe's popularity include multiple Y axes on a single plot (new for 5.0), fast Fourier transforms, and simultaneous display of analog and digital waveforms. Probe's interactive plotting capabilities offer the user complete control; axes can be freely defined and traces can be added to the display as functions of other waveforms or arithmetic expressions of voltages and currents.

Probe 5.0 is sold as an option to MicroSim Corporation's popular PSpice 5.0 circuit simulator— part of our Circuit Analysis package. Every copy sold comes with our extensive customer/product support. Our expert engineering team is always on hand to answer your technical product questions.

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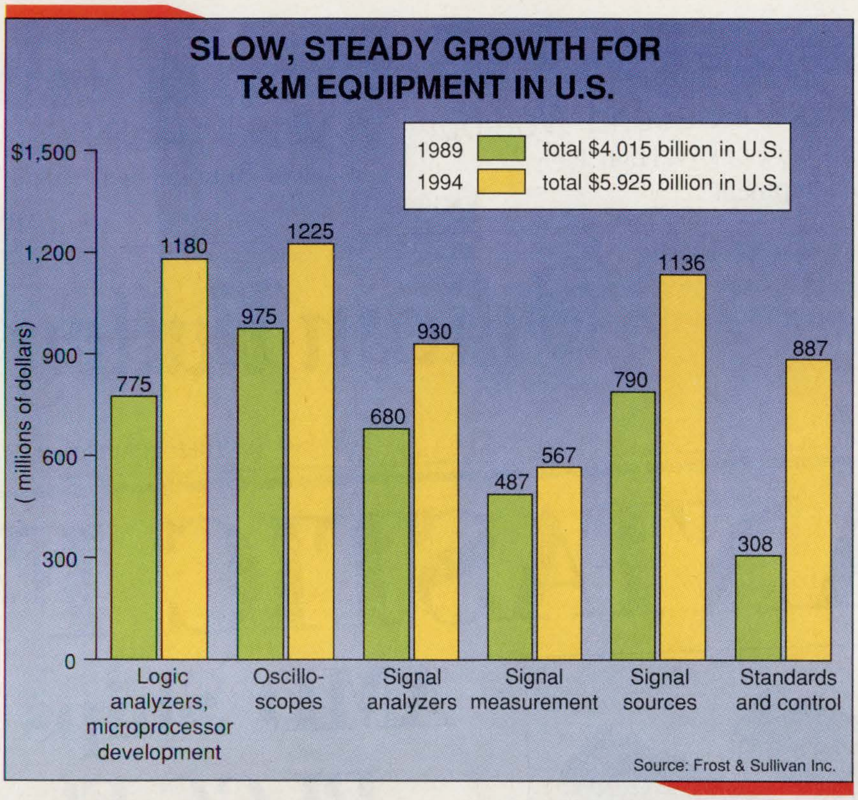
CIRCLE 124 FOR U.S. RESPONSE **CIRCLE 125 FOR RESPONSE OUTSIDE THE U.S.**

ELECTRONIC DESIGN

QUICK LOOK

EDITED BY SHERRIE VAN TYLE



MARKET FACTS

As a mature industry, test and measurement equipment is showing slow but steady growth in sales. The market for T&M equipment, which stood at $5.680 billion in 1989, was worth $5.977 last year, according to Frost & Sullivan Inc. In 1991, the New York market researcher pegs the market at $6.399 billion. And by 1994, worldwide sales of T&M equipment should hit $8.989 billion.

Growth won't be even in all sectors, however. U. S. consumption of T&M equipment is lagging because of leaner military budgets, cutbacks in corporate research and development money, and an economic recession. But other areas are doing well, such as test equipment that supports the latest crop of semiconductor devices, computer-based products, and communications equipment.

The push for quality should help fuel demand for improved T&M equipment. Also in demand: integrated test systems to pare production costs, digital oscilloscopes, microprocessor development systems, and VXIbus-based modular instruments.

HOT PC PRODUCTS

An 80286-based PC can run at least three times faster with a 386SX cache-based upgrade module from Aox Inc. The 1.5-by-1.5-by 0.6-in. Stax SX doesn't take up an expansion slot or need cables and is easy to install, the company says. The module comes in 16- and 20-MHz clock speeds and PGA or PLCC packaging. The module works with an 80287 math coprocessor, avoiding an upgrade to a 387 coprocessor. The 16-MHz module sells for $279, a 20-MHz version for $329. For more information, contact Aox, 486 Totten Pond Rd., Waltham, MA 02154; (800) 726-0269. CIRCLE 451

For engineers and managers who communicate with their counterparts in Japan, EZ Japanese Writer software translates English sentences into Japanese characters. From EJ Bilingual Inc., the program has a 50,000-word vocabulary, to which a user can add 20,000 words.

With the program, a user actively composes a translation. That's important, the company says, because English and Japanese have different grammatical structures and an English word like president has three different translations in Japanese, depending on the context. The software, which lists for $1200, runs on an IBM PC, XT, AT or compatible with 640k RAM. For more information, contact the company at 2463 Torrance Blvd., Suite 1, Torrance, CA 90501; (213) 320-8139; fax (213) 320-3228. CIRCLE 452

Concern among PC users about carpal tunnel syndrome, backstrain, and eyestrain is giving rise to low-cost products that help alleviate these problems. For users who rest the keyboard in their lap while working, the Lap Cat from PC Compatibles uses a lightweight foam base to position any PC compatible keyboard at the correct height and angle to minimize strain on muscles and nerves. The Lap Cat also helps maintain distance from the monitor for radiation protection. The lap rest sells for $39.95. For desktop keyboarding, the Wrist Perch supports the wrists and palms with a lightweight foam shelf that extends under the keyboard. It lists for $19.95. An adjustable Foot Turtle footrest, which puts the proper curve into the lower back, goes for $29.95. Contact PC Compatibles, 55 Valley View, P.O. Box 46, Chappaqua, NY 10514; (914) 238-7818; fax (914) 769-0788. CIRCLE 453

News Flash

SPORTS

The 90 Nanosecond Workout
An Exhaustive Look At High Tech Training Equipment
PAGE 2B

SCIENCE AND TECHNOLOGY

Virtual Reality
Close But No Cigar
PAGE 8I

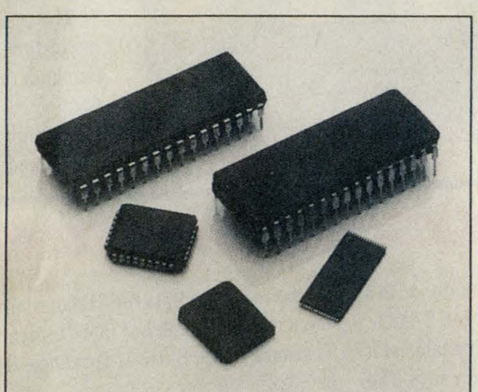
Silicon Valley G

25 CENTS

SERVING NORTHERN CALIFORNIA SINCE 1

FANTASTIC FL

AMD Ships 2 PLCC Flash



How Fast Is A Flash? A Direct Comparison

Density	AMD	Fastest Competitor
256K	90ns	120ns
512K	90ns	120ns
1 Mbit	90ns	120ns
2 Mbit	90ns	150ns

SUNNYVALE — The computer industry takes a giant leap forward in performance with the help of the new Flash memory family from Advanced Micro Devices, Inc.

Flash memory is a high-density, reprogrammable, non-volatile technology that has a bright future in computation, laser printers, network and telecommunications hardware. Many military systems use Flash technology in radar and navigational applications.

Flash memory also has the potential to eliminate mechanical hard disks and the need for cumbersome batteries. These are two of the biggest and heaviest obstacles in laptop and notebook computer applications.

Today, Flash memory is the most cost effective replacement technology for UV EPROMs and EEPROMs in applications that require in-system programming. Flash memories can literally be reprogrammed in a flash — hence the name.

Standard, But With A Little More Flash

AMD's Flash memory family effectively etches in silicon the de-facto standard for this burgeoning technology that is compatible with Intel's initial Flash architecture.

Because AMD Flash memories are pin-for-pin compatible with the now standard architecture, AMD is positioned as an alternate source for design engineers and purchasing agents alike.

"Alternate source may be an inadequate term," said Jerry Sanders, chairman and CEO of Advanced Micro Devices. "Given our speed and feature set, our customers think of us as a superior resource."

Indeed, AMD's Flash memory family offers designers significant performance advantages (see chart), with speeds almost twice as fast as the nearest competitor.

Engineer Spontaneously Combusts At Meeting

Vice Pr
At Lo

From AMD.


FOOD

Chips And Salsa

A Business Person's Guide To Silicon Valley Restaurants PAGE 7F

zette

MORNING EDITION

ASHES!

Megabit, 90ns,

Memories

The AMD Flash family offers designers and purchasers many packaging options. Particularly popular is AMD's advanced 2 Megabit, PLCC part. Other packaging options include PDIP, CDIP and LCC in 256K, 512K, 1 Mbit and 2 Mbit capacities. TSOP packages will be available in the second half of this year. (LCC not currently available in 2 Mbit.)

AMD's 2 Mbit Flash memories come complete with embedded program and erase algorithms on board. These automatic algorithms speed up the design process and considerably shorten time to market. Previously, engineers were required to develop tedious and time-consuming algorithms to implement in-system reprogrammability. AMD's automatic algorithms also allow several Flash memories to be written or erased at once, without tying-up the CPU. The system is now free to perform other tasks while these operations are in progress. AMD plans to include embedded algorithms in a future release of its 1 Mbit part.

The Ultra-Violet Blues

Flash technology is particularly suited to applications requiring reprogramming in place, because these devices can be reprogrammed in seconds, and within the system.

To update the code on a UV EPROM, the part must first be removed from the system. Once removed, erasure can take up to a full 20 minutes. After reprogramming, the part is then plugged back into the system. The process can result in damage to other components, costly service calls, and headaches.

Flash memories, on the other hand, can be bulk erased in about one to two seconds, without system disassembly. Reprogramming can then be accomplished via floppy disk, over phone lines, or even ISDN

(continued)

ident To Speak

Stop the presses!

Advanced Micro Devices makes big news again—this time with an enhanced family of Flash memory devices.

That's good news for veteran and new Flash users alike.

Because our Flash devices are pin-for-pin compatible with Intel's existing Flash memory architecture, they establish the *de facto* industry standard.

Our standards, however, are a bit higher. And so are yours.

That's why our Flash Memory family offers densities, speeds and packaging options that improve performance and save board space. For instance, our advanced 2 Mbit PLCC part with a scant 90 nanosecond delay.

You can also choose from Flash devices in 256K, 512K and 1 Mbit densities. As well as packaging options that fit your design best, including CDIP, PDIP, LCC, TSOP, and PLCC.

And you'll find implementation faster and easier than ever, because we've included automatic programming algorithms on all our 2 Mbit devices, and soon on our 1 Mbit parts, too. So you'll spend less time writing code, and take less time getting products to market.

To keep up to date with all the latest and greatest in Flash memory, call AMD today at **1-800-222-9323.** And start making some headlines of your own.

Advanced Micro Devices

901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088. © 1991 Advanced Micro Devices, Inc.

CIRCLE 229 FOR U.S. RESPONSE CIRCLE 230 FOR RESPONSE OUTSIDE THE U.S.

QUICKLOOK

BEST SELLERS

Which technical books are the most popular in Silicon Valley?

ELECTRONICS:

1. *C Language Algorithms for Digital Signal Processing* by Paul Embree. Prentice-Hall, 1990. ***$50.***

2. *Intuitive Operational Amplifiers* by Thomas Frederikson. McGraw-Hill, 1988. ***$26.95.***

3. *Noise Reduction Techniques in Electronic Systems* by Henry Ott. John Wiley & Sons, 1988. ***$47.95.***

4. *Design Guidelines for Surface Mount Technology* by John Traister. Academic Press, 1990. ***$49.95.***

5. *Spice for Electronics Using Pspice* by Mohammed H. Rashid. Prentice-Hall, 1990. ***$23.***

COMPUTER SCIENCE:

1. *C Programming Language*, second edition, by Brian Kernighan and Dennis Richie. Prentice-Hall, 1989. ***$32.***

2. *Programming Windows* by Charles Petzold. Microsoft Press, 1990, ***$28.95.***

3. *Inside Macintosh*, vol. 6. Apple Computer. Addison-Wesley, 1991. ***$39.95.***

4. *Object-oriented Design & Applications* by Grady Booch. Addison-Wesley, 1991, ***$38.50***

5. *C++ Primer* by Stanley Lippman. Addison-Wesley, 1989. ***$30.50.***

This list is compiled for *Electronic Design* and assembled for the magazine's Quick Look section by Stacey's Bookstore, 219 University Ave., Palo Alto, CA 94301; telephone (415) 326-0681; fax number (415) 326-0693.

DID YOU KNOW?

... that cellular phone sales are up 24% over 1990. Overall, U. S. electronic exports reached $72.8 billion last year, a record high and an 11.6% increase over 1989.

... that a survey of purchasers of home office equipment found that 59% either bring overflow work home; are self-employed and work at home; work part time or freelance at home; or work full time at home.

As for products, 33% of those surveyed own an electronic typewriter; 28% own a PC; 23% own a printer.

Electronic Industries Association Consumer Electronics Group

KMET'S KORNER

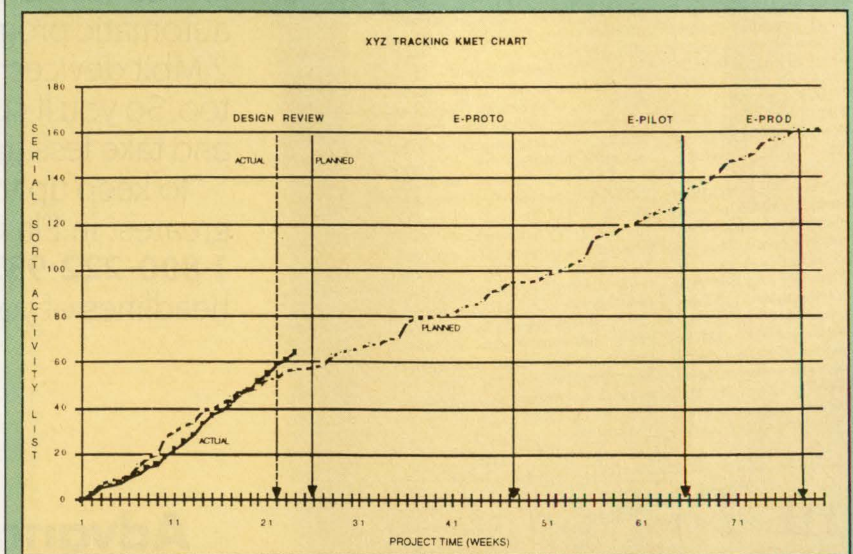
BY RON KMETOVICZ
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458; fax (408) 253-6085

As the new product-development team begins to gain some understanding of reality, a steady-state condition begins to emerge. Managers go to their once-a-week meetings. Participants work on their tasks as they report on progress and problems. Data is collected, analyzed, and reported; problems are identified and resolved. The process begins to work in a uniform, steady, and, most of the time, predictable, fashion. To show the new product development system in motion, the KMET chart becomes active once again.

A milestone slip is easily read from the KMET Chart below. The baseline plot shows the predicted milestone completion dates with a dashed arrow. In the case of Project XYZ, the Design Review milestone was reached four weeks ahead of the planned date. Milestone slip is the primary parameter under the control of the project/program manager during the execution phase. The manager and his/her team do everything possible to prevent milestones from moving in the wrong time direction. Often, the network must be adjusted to achieve this objective.

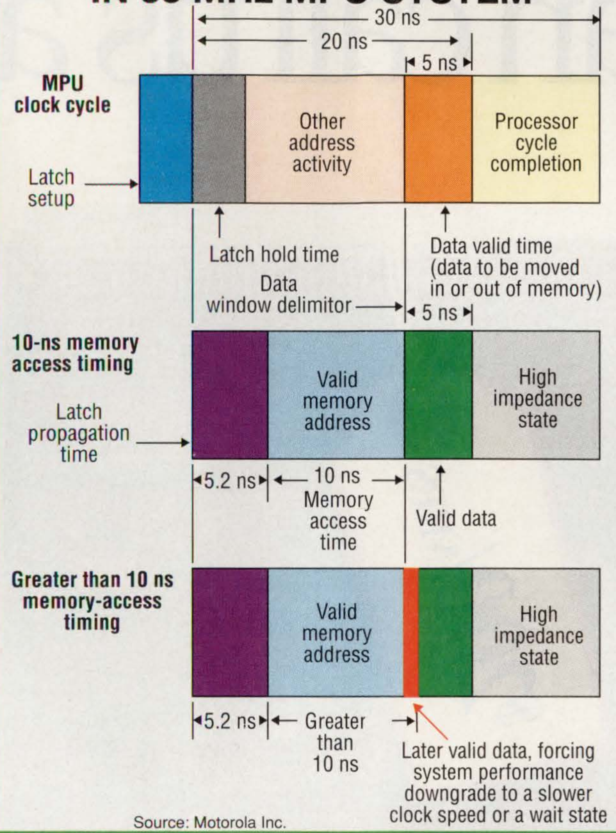
Many textbooks on planning refer call the execution phase the tracking phase. If tracking were the only responsibility of the project/program manager, then this would be time for rest and relaxation. In reality, tracking means real-time synthesis of solutions to problems as they are revealed over time. Actions taken to solve problems show up as modifications to the network from which the KMET chart is produced. The dynamics of network modification and adjustment to the realities of actual task completion dates is shown by the actual line in the illustration.

The appearance of a change in plans over time is a likely phenomenon. The KMET chart provides the window into the project/program network to keep it measurable and visible. At any point during the execution phase, it is simple to glance at the chart to obtain an indication of how much the plan has changed since the reference plan was produced. The chart prevents projects from being terminally in the planning phase and not the execution phase by giving the project/program manager the freedom to modify plans to keep milestone slips under control. *This is real-time, seat-of-the-pants, concurrent, new product development project/program management in action.*



HOW IT WORKS

AVOIDING WAIT STATE IN 33 MHz MPU SYSTEM



Source: Motorola Inc.

Motorola shows that a wait state can be avoided in a 33-MHz microprocessor system by using a static RAM cache memory with 10-ns access time. A slower memory degrades performance or forces a wait state.

OFFERS YOU CAN'T REFUSE

A free disk demonstrates DDA, a digital design analysis program that performs 65 tests on each net of a design. All the active devices are tested to be operated within their guaranteed specifications. This analysis achieves at least 98% fault isolation. DDA analyzes a 100-chip design in about 10 seconds when running on a 33-MHz PC and isolates circuits that cause problems, including erratic operation and poor reliability. Contact Digital Design Analysis, 150 El Camino Real, Suite 200, Tustin, CA 92680; (714) 573-8730; fax (714) 573-8736. CIRCLE 454

An audiotape course on understanding dB and dBm is free from Scott Training Associates. The 60-minute cassette covers the origins of dB notation, conversion by calculator and by hand, power specification in dBm, and use of dB to specify return loss, insertion loss, and gain. The tape comes with a 25 pages of charts and exercises.

For more information, contact Scott Training Associates, 101 First St., Suite 392, Los Altos, CA 94022; (415) 965-1624.

CIRCLE 455

ENVIRONMENTAL WATCH

As concern grows over the earth's depleted ozone layer, electronics companies are working to eliminate chlorofluorocarbons (CFCs) from pc-board processing (*Electronic Design*, June 27, p. 18). Toshiba Corp. recently eliminated CFC 112 and 113 from its semiconductor cleaning process.

To do that, workers at Toshiba examined and measured each cleaning process against three means of eliminating CFCs: abolishing the CFC washing process; using a different cleaning method; and using a substitute cleaner, such as Techno Care, a CFC substitute Toshiba came up with for cleaning pc boards. As a result, CFCs are no longer used in producing the company's 1- and 4-Mbit DRAMs, ASICs, bipolar ICs, optical semiconductors, and discrete devices.

Toshiba subsidiary, Toshiba America Electronic Components Inc. has its headquarters in Irvine, Calif.

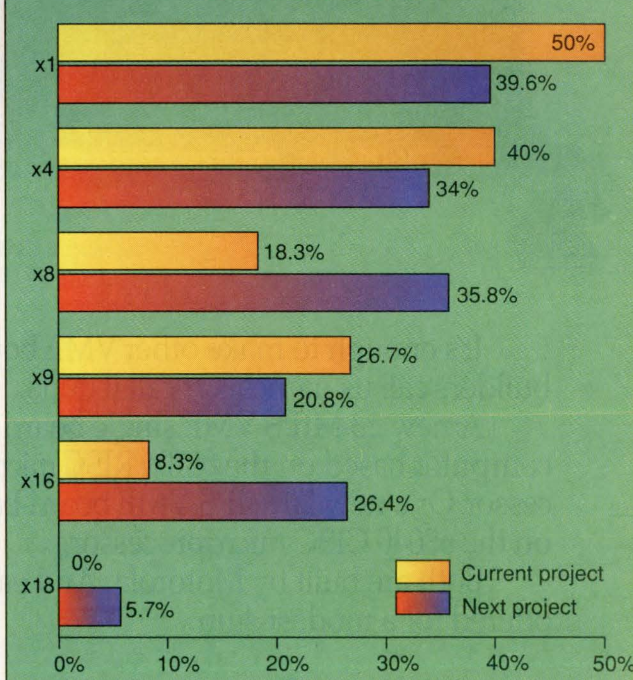
QUICK REVIEWS

A popular book on software engineering is now being offered in a hypertext version, which affords non-linear browsing of text, online searches, and reusable graphics. *Wicked Problems, Righteous Solutions: A Catalogue of Modern Software Engineering Paradigms* by DeGrace & Stahl, looks at how software is written. The hypertext version is available for the Macintosh (HyperCard versions 1.2.x or 2.0) and Toolbox for the PC (requires Windows 3.0). Either version is $29.

Contact DeGrace & Stahl, 1420 NW Gilman Blvd., Department 2583, Issaquah, WA 98027-5399; (800) 752-4889. CIRCLE 474

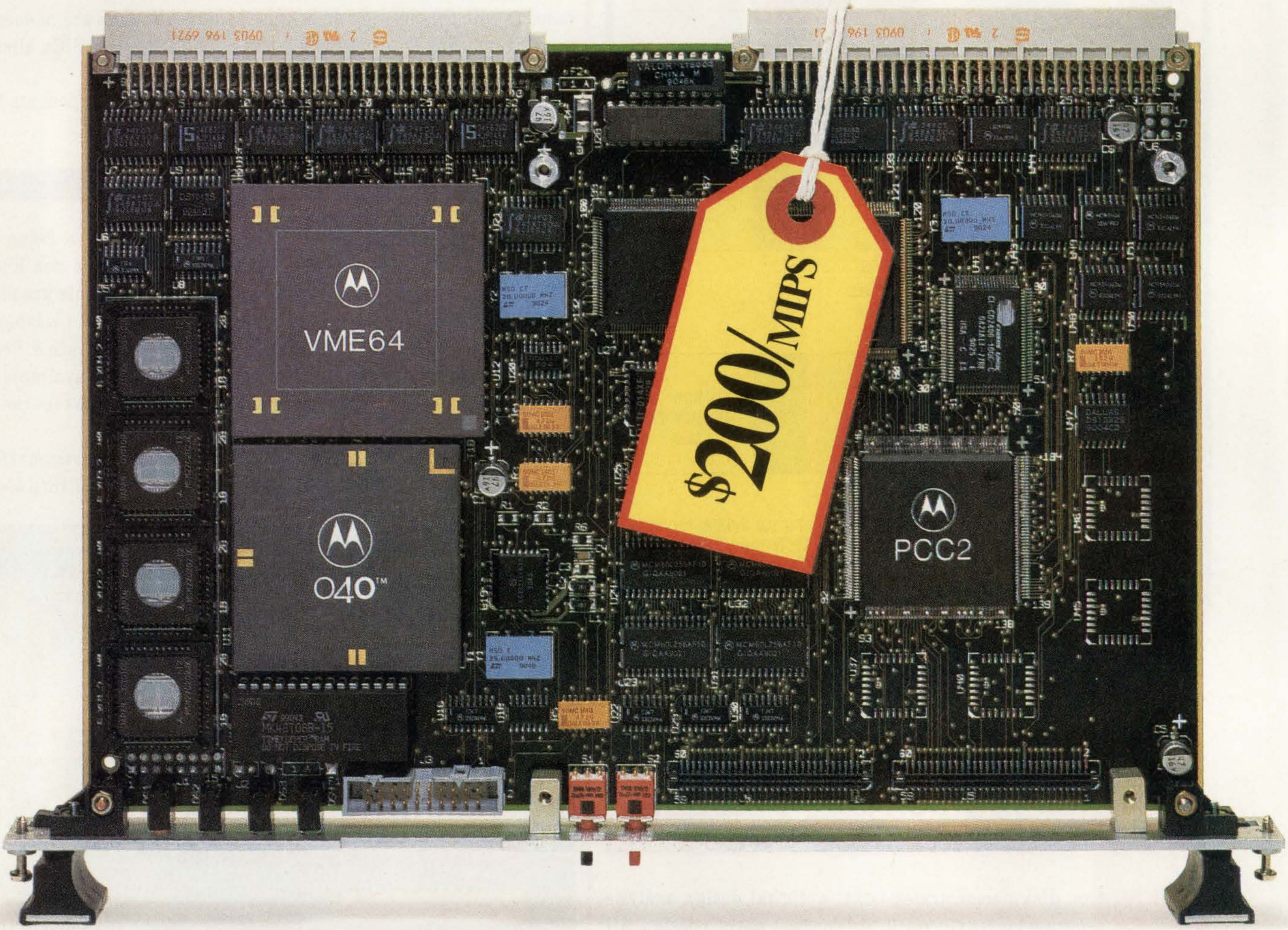
DRAM SURVEY

WHAT DRAM ORGANIZATION DO YOU NEED?



Source: a survey of Electronic Design readers by Penton Publishing Inc.

The competition You can call us at



It's enough to make other VME board builders call us names. Or call it quits.

A new 23 MIPS VME single board computer based on the 88100 RISC microprocessor. Or a new 20 MIPS VME board based on the 68040 CISC microprocessor.

Both are built by Motorola. And each is offered for a modest sum.

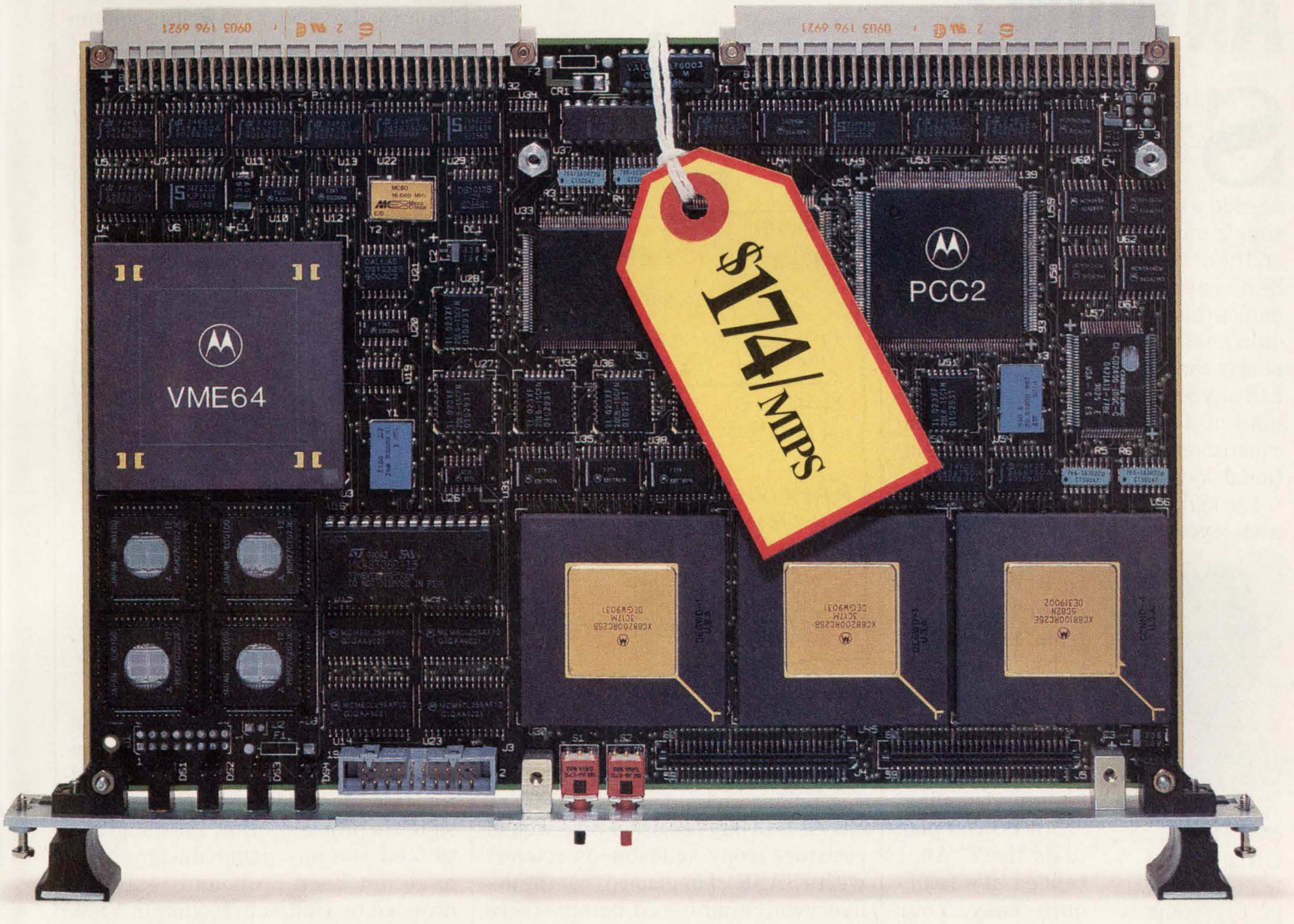
A mere $3,995 per board.

For all you multiplication buffs out there, that comes out to just $174/MIPS for the RISC board.

A far cry from the $1,000/MIPS you've been asked to pay for somebody else's board.

And it's just $200/MIPS for the

will call us ruthless. 1-800-234-4VME.



CISC board. A whole lot less than you'll pay elsewhere.

The MVME187 (RISC) and MVME167 (CISC) boards employ VME D64 architecture. Boosting the VMEbus bandwidth to a full 40MB/s.

And both boards come with four 32-bit timers. SCSI and Ethernet connections. Plus the Motorola name and all it implies.

For a free color brochure, call the 800 number above. And see why the competition undoubtedly wishes we'd call the whole thing off.

Malcolm Baldrige National Quality Award

MOTOROLA
Computer Group

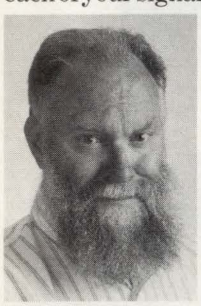
CIRCLE 204 FOR U.S. RESPONSE

CIRCLE 205 FOR RESPONSE OUTSIDE THE U.S.

WHAT'S ALL THIS MULTIPLICATION STUFF, ANYHOW?

Several months ago, I got a strange call from a "customer" (I get a lot of strange phone calls). He said he needed a multiplier circuit to do some simple multiplying, such as 5 V X 8 V, and he needed 0.02% precision. He said he had already talked to several companies that make multipliers, and they didn't have any circuits with precision nearly that good. Then he asked if we had any ideas. I gathered that he was kind of desperate, and that he had called us *even though* he knew that National doesn't make any multipliers.

I asked, "Oh, what is the range of each of your signals?" He said, "Oh, one input goes from 5 V to 9 V, and the other input goes from 4 volts to 8 volts." I replied, well, if you want 0.02% accuracy, that's a piece of cake. I could hear his jaw dropping. "How do you plan to do that?" Ah, I replied, it's really quite easy. Your dynamic range is narrow enough, so we can do an expanded-scale amplification of your signals and feed them into a decent multiplier. Then take the output voltage from the multiplier and combine it with some constant offsets and some linear-gain signals, and add them all up with some precision resistors, and there's your output.

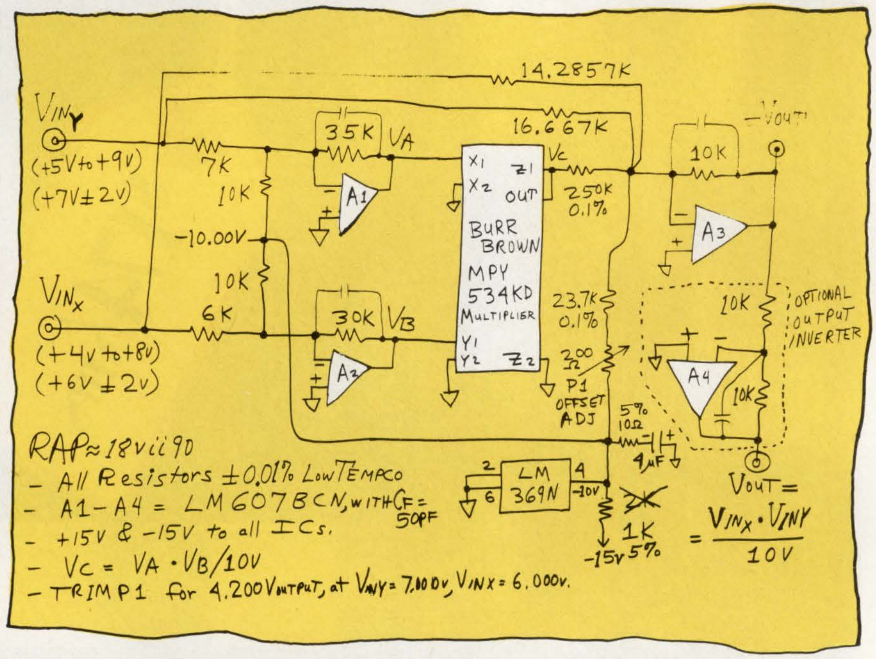


BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

He said, "Precision resistors–aren't they the ones that cost \$10 each?" I said, "Heavens no, a couple bucks gets you some good ones." So the first thing I sent him was a description of how easy it is to buy precision wire-wound resistors (copy available on request with a SASE). I explained that the delivery can be quite good, because there are several competing companies (some of them are right down the road from each other, in southern New Hampshire) that can sell you resistors with excellent accuracy, 0.01% or better, and at reasonable prices. Delivery is also excellent, if you want to pay a little surcharge for that. When I need good resistors, I usually look in the EEM or the Gold Book, and shop around at two or three of the vendors to do a sanity check and make sure I have not over-specified or under-specified the resistors I need. I sent him a copy of that page in the EEM, "Precision Wire-wound resistors," so he had his choice of a dozen good suppliers.

Then I sent him a schematic similar to the one adjacent. I told him I've done something like this before, and you can't go wrong.

I never heard from him again. So I like to think that it worked okay for him. Then, as I began thinking of good topics and good ideas to write a column about, I remembered this problem. I fished a couple inches down in the file of papers on my desk and dug up the problem and the solution. Now, I had told this guy, "This is a guaranteed design. No problem." But, I'm not going to feed *you* any paper designs that have not been built and tested. I dropped by Haltek in Mountain View and bought a few of the resistors that I needed. Then I gave the whole batch to my technician and told him that it had to work. I said to come back when the output error is less than 2 mV.



Note, I don't usually tell my technicians that, because I'm perfectly capable of making mistakes, *every* kind of mistake. I usually tell the tech, "Leave extra room in case we have to change some things in the input area..." or whatever. But in this case, I just told him to leave the leads of the resistors at full length, as a sort of a strain-relief loop, so when they're soldered, it doesn't

heat up the body of the resistor.

How does this circuit work? It works beautifully (no, that's not what I meant). It works by taking advantage of the full dynamic range of the multiplier. If you merely feed in a signal in the range of (+5 V to +9 V) to the terminals of the multiplier, you're using only 1/5 of the usable range or span of the multiplier. So, let's take the signal input, subtract 7 V, and amplify it by a gain of -5. *That* signal, which we feed to the input of the multiplier, now has a range of ± 10 volts. Therefore, we're exercising the multiplier over its entire rated operating range. We do likewise for the other input. Now to get the signal at the output of the multiplier combined into the output, a gain of 1/25 is needed. The *errors* of the multiplier are also attenuated by this factor of 25–that's the key to getting the accuracy you want. Most of the signal goes through the linear gain stages, and only a little of the output comes through the multiplier.

A reasonably-priced ($40) multiplier, such as Burr Brown's 534KD (see, I told you National doesn't make any multipliers) with an accuracy spec of 0.5%, can provide a performance of 0.02% in this circuit. Now, the amplifiers are pretty inexpensive (National's LM607BN with $V_{OS} \leq 60\ \mu V$ is barely $1.20) and the 13 precision resistors are going to cost you about $30. But, they get you to a place you could not get to otherwise.

– What do we want from our MULTIPLIER?

– We want $V_{OUT} = \frac{V_{INX} \cdot V_{INY}}{10V} \pm 0.02\%$

but only in a limited range, $4V \leq V_{INX} \leq 8V$ and $5V \leq V_{INY} \leq 9V$.

– Let's define new VARIABLES:

– Let $(-VA) = (V_{INY} - 7V) \cdot 5$
Let $(-VB) = (V_{INX} - 6V) \cdot 5$ } and then multiply $VA \cdot VB$.

Then $V_C = \frac{(-VA)(-VB)}{10V} = \frac{VA \cdot VB}{10V} = \frac{25(V_{INX} - 6V)(V_{INY} - 7V)}{10V}$

So $\left[\frac{VA \cdot VB}{10V \cdot 25}\right] = \left(\frac{V_{INX} \cdot V_{INY}}{10V}\right) - \frac{6V}{10V} V_{INY} - \frac{7V \cdot V_{INX}}{10V} + \frac{42V^2}{10V}$

REARRANGING –

$\left(\frac{V_{INX} \cdot V_{INY}}{10V}\right) = \left(\frac{VA \cdot VB}{10V \cdot 25}\right) + 0.6 V_{INY} + 0.7 V_{INX} - 4.2V$

– So all we have to do is generate VA & VB, feed them to a multiplier, and take a summation:

$V_{OUT} = \left(\frac{V_{INX} \cdot V_{INY}}{10V}\right) = \frac{V_C}{25} + 0.6 V_{INY} + 0.7 V_{INX} - 4.2V$.

That is easy to do –

A3 sums all those voltages with the required gains – the gain from V_C to V_{out} is $\frac{1}{25}$;

– the gain from V_{INY} to V_{OUT} is $\frac{6}{10}$;

– the gain from V_{INX} to V_{OUT} is $\frac{7}{10}$;

– and the 23.7K adds in a 4.2 VOLT offset, which is trimmed for best accuracy:

When $V_{INY} = 7.000V$,
$V_{INX} = 6.000V$,
$VA \cong VB \cong V_C \cong 0$,
so just trim V_{OUT} to 4.200V using offset ADJUST P1.

A4 lets you have an inverted POLARITY.

RAP 2iii91

Paul built up the circuit, and tested it at several values of V_{IN}. I must admit, he had to change one resistor value–I provided a 2k resistor to feed the LM369, and Paul figured out quickly that it should be 1k to provide 5 mA. The -10-V bus refused to regulate because the loads on that node drew more than the 2.5 mA I was providing through the 2k.

Referring to the box of data, you can see that the worst output error was about 0.7 mV or 0.007%, about 9 times better than the accuracy of the multiplier used by itself. It's always nice to know that when you tell a guy, "This circuit can't go wrong," it really does work the way you said it would.

All for now. / Comments invited! /
RAP / Robert A. Pease / Engineer

Address:
Mail Stop C2500A
National Semiconductor
P.O. Box 58090
Santa Clara, CA 95052-8090

P.S. I was talking about this circuit with some friends, and they agreed you could do this with digital multipliers, but that would not be cheap nor easy, either. But then I countered, how about one ADC and an MDAC? (multiplying DAC)–those things can be inexpensive and quite accurate. I'll build one of those and see if it's worth writing about.

Thu, Oct 11, 1990 3:24 PM

Vin Y	Vin X	Vout	Column 5	Verror
5.0000	4.0000	-1.999399	-2.000000	0.000601
6.0000	4.0000	-2.399693	-2.400000	0.000307
7.0000	4.0000	-2.799666	-2.800000	0.000334
8.0000	4.0000	-3.199520	-3.200000	0.000480
9.0000	4.0000	-3.599620	-3.600000	0.000380
5.0000	5.0000	-2.499626	-2.500000	0.000374
6.0000	5.0000	-2.999929	-3.000000	0.000071
7.0000	5.0000	-3.499720	-3.500000	0.000280
8.0000	5.0000	-3.999440	-4.000000	0.000560
9.0000	5.0000	-4.499300	-4.500000	0.000700
5.0000	6.0000	-2.999830	-3.000000	0.000170
6.0000	6.0000	-3.600000	-3.600000	0.000000
7.0000	6.0000	-4.199930	-4.200000	0.000070
8.0000	6.0000	-4.799750	-4.800000	0.000250
9.0000	6.0000	-5.399350	-5.400000	0.000650
5.0000	7.0000	-3.500170	-3.500000	-0.000170
6.0000	7.0000	-4.200100	-4.200000	-0.000100
7.0000	7.0000	-4.900130	-4.900000	-0.000130
8.0000	7.0000	-5.600000	-5.600000	0.000000
9.0000	7.0000	-6.299500	-6.300000	0.000500
5.0000	8.0000	-4.000470	-4.000000	-0.000470
6.0000	8.0000	-4.800290	-4.800000	-0.000290
7.0000	8.0000	-5.600360	-5.600000	-0.000360
8.0000	8.0000	-6.400360	-6.400000	-0.000360
9.0000	8.0000	-7.200230	-7.200000	-0.000230

Ideal Output V

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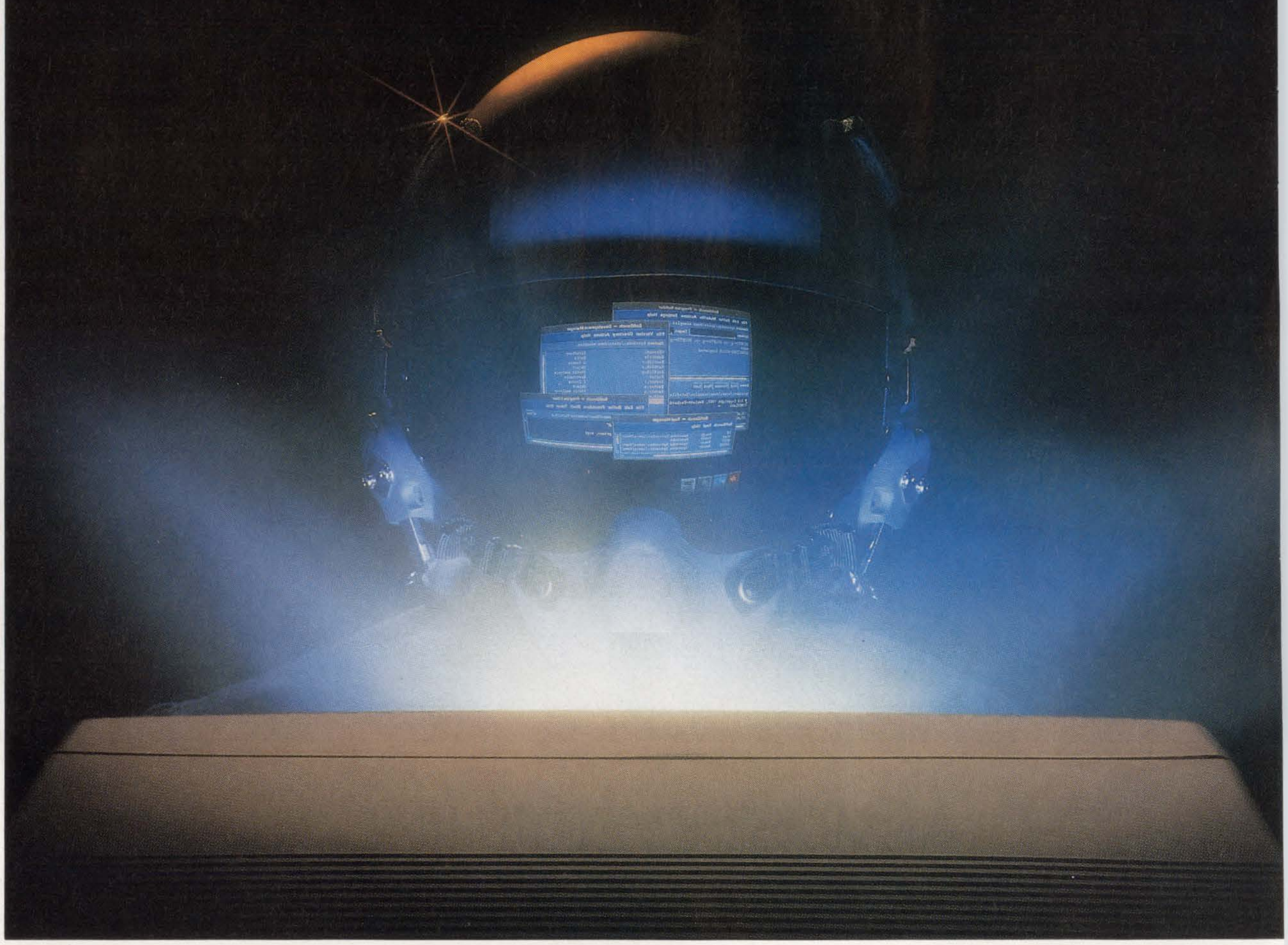

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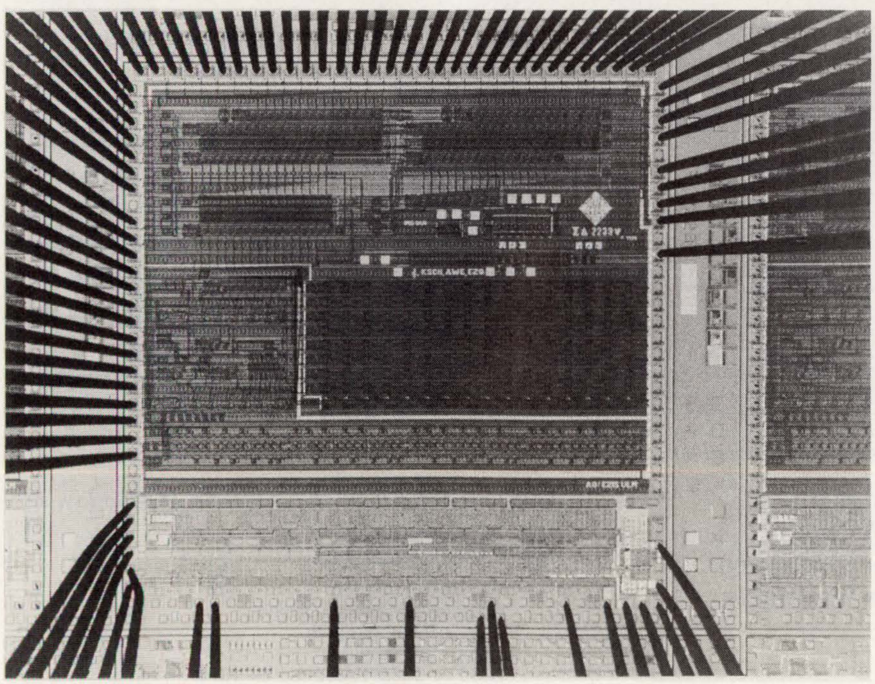
MIXED-SIGNAL ARRAY JOINS HIGH-FREQUENCY ANALOG SECTION FOR GIGAHERTZ FREQUENCIES WITH DIGITAL SECTION FOR 50-MHZ OPERATION.

BICMOS ARRAY SPEEDS COMMUNICATIONS DESIGN

JOHN GOSCH

Designers of circuits for advanced communications equipment now have added firepower in their corner. It comes in the form of a bipolar-CMOS analog/digital array, a development aid from Telefunken Electronic GmbH. The mixed-signal array lets communications-systems designers check out and optimize circuit functions before the chips are committed to production.



1. OVER 132,000 DEVICES are crammed into this tiny biCMOS analog/digital chip, which is about 50-mm² in area. The Telefunken array contains high-frequency analog circuits interfaced on the chip with a sea-of-gates array for digital-signal-processing tasks.

For a systems maker, the new combination array from the Heilbronn, Germany, company meets an important criterion: To react fast to changing customer demands for equipment performance at a reasonable cost, and to alter the circuits accordingly. The device, the U3351BM, can serve as the basis for developing innovative communication systems, even when operating with small production runs *(Fig. 1)*.

In communication circuitry, interfaces between the high-frequency analog signals and the digital-signal-processing stage are becoming ever more important. The U3351BM prototypes that interface (thus simplifying its design) because it has both the analog bipolar high-frequency (HF) array and the digital bipolar-CMOS sea-of-gates (SOG) array on the same chip *(Fig. 2)*.

In the two arrays, the cells are arranged in a matrix, with each cell containing a multitude of mutually isolated circuit elements. The HF array, which occupies about 10 mm^2 in area, has 638 npn and 80 pnp transistors, as well as 1928 resistors and 62 capacitors. The 35-mm^2 SOG array has 126,375 MOS components and 3625 npn transistors. Thus, the entire chip, which measures about 50 mm^2 in total, contains more than 132,000 circuit elements.

The U3351BM's configuration and characteristics suit it for prototyping intelligent interfaces between the analog and digital worlds. The analog side handles frequencies up into the gigahertz range, and the sensitivity of the low-noise input transistors enables the device to be directly coupled to sensors, such as photodiodes. Well-dimensioned output transistors offer sufficient drive power for controllers and signal sources, like laser diodes, without the need for additional external power stages.

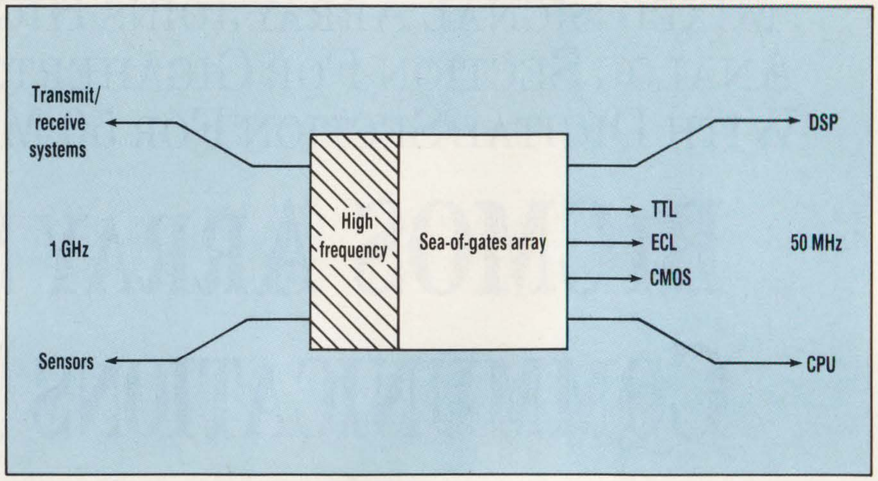
On-Chip Computing Power

As for the digital SOG array, its complexity makes it possible to put computing power on the chip so that signals can be processed already at the interface stage. The array supports all common signal levels—for example, CMOS, TTL, and ECL. This allows communications with such external components as memories and microprocessors.

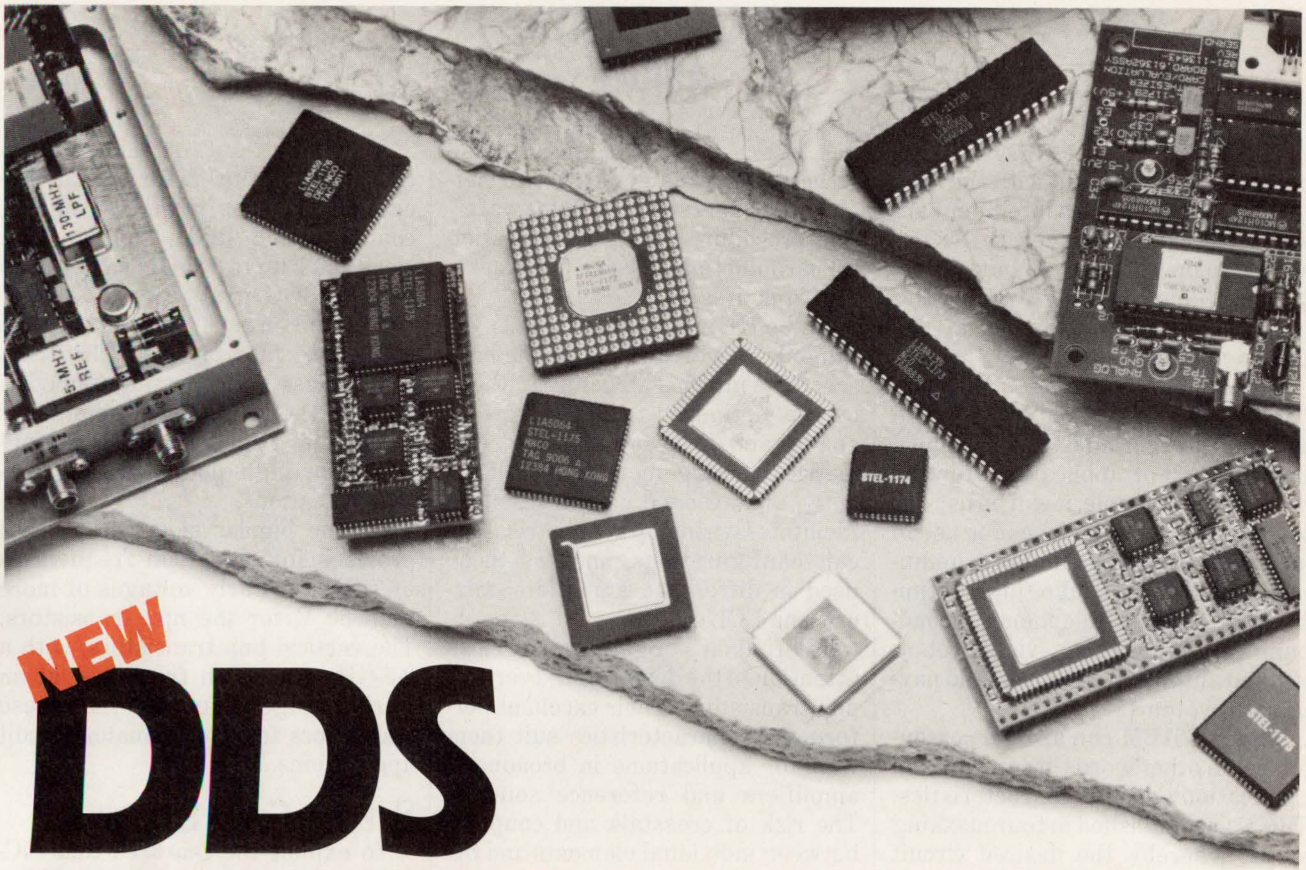
The Telefunken combination array has two important advantages over competing devices, advantages that suit it to many high-speed analog/digital applications.

First, biCMOS driver circuits are part of the basic cell. These circuits can be used on each loaded internal cell output without affecting the surrounding CMOS logic.

Second, the combination of the bi-



2. INTERFACING BETWEEN ANALOG and digital circuits is simplified on the Telefunken U3351BM biCMOS chip. The device aims at making communications-systems development easier.



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STEL-1377	miniature assembly based on 1177 MIL Spec version now available NEW
STEL-1378	miniature assembly based on 1178 NEW
STEL-1277	based on 1177, 0-25 MHz
STEL-2272	based on 2172, 0-130 MHz
STEL-2273	based on 2173, 0-400 MHz
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polar analog HF array with the digital SOG array enables intelligent analog/digital interfaces to be designed to operate at high output frequencies and with high computing power, while also operating at low power consumption.

The combination array's ability to handle different signal levels, such as CMOS, TTL, and ECL, opens up a broad range of applications for the device. For example, it can be used to build prototype interfaces for use in such applications as mobile communications, digital audio, high-definition TV, cordless telephones, broadband communications, video, robotics, and automotive security and navigation systems.

The U3351BM can also be personalized. In other words, it can be given application-specific characteristics. This is accomplished in four masking steps, whereby the desired circuit structure is transferred via two metallization layers to the master wafer. The procedure cuts the fabrication turnaround time to just a few weeks, Telefunken says.

In the HF array, 34 basic cells, arranged in two rows, form the core area. The internal structure of these cells is optimized to configure fast analog and ECL circuits. The symmetrical arrangement of the differently dimensioned npn transistors facilitates wiring up symmetrical circuit configurations, such as those used in difference amplifiers, mixers, and ECL gates.

Telefunken's engineers paid close attention to the design of the vertical pnp transistors. Their excellent performance characteristics suit them well for applications in broadband amplifiers and reference sources. The risk of crosstalk and coupling between individual elements and between the cells is avoided by low-resistance channels used as contacts to the substrate.

A powerful cell library is available to the HF array. It encompasses preamplifiers and mixers for operation at frequencies up to 950 MHz, controllable amplifiers for applications up to 100 MHz, as well as comparators and ECL gates with delays of around 500 ps.

The basic cells of the SOG array provide a flexible base structure for implementing macrocell-oriented systems. All known CMOS circuit technologies—including static and dynamic logic—can be used with this structure. The SOG array is also suitable for integrating regularly structured circuits, such as RAM and ROM blocks.

One problem with complex digital arrays is getting sufficient drive power from them. The biCMOS technology used by Telefunken solves this problem with bipolar transistors. A cell is incorporated with biCMOS drivers so that the surrounding CMOS logic remains unaffected by these drivers.

Over 3500 interconnection possibilities area available to tie the biCMOS drivers to highly loaded cell outputs after the cells are in place. Measurements at different basic cells typically used for signal processing, such as registers, adders, counters, and ROM, confirm that clock rates up to 50 MHz can be used with the SOG array.

Telefunken uses a 1.2-μm biCMOS process to fabricate the U3351BM. The process, which was developed as part of the European Community-sponsored Esprit project, is optimized for high-quality analog/digital applications.

On the bipolar side, the process provides for transition frequencies of 7 GHz at Early voltages of more than 50 V for the npn transistors. The vertical pnp transistors, with a 2.5-GHz transition frequency at an Early voltage around 50 V, suit these transistors for use in analog-circuit applications.

SPECIAL CAD STATION

To exploit the features that biCMOS technology and the analog/digital combination array offer, Telefunken engineers developed an array-specific computer-aided design station. The design platform for the SOG array is based on GDT (Geometric Data Tape) software developed by Mentor Graphics Corp., Beaverton, Ore.

In addition to the GDT packages for layout generation and multilevel simulation, special generators and routines are implemented so that the technology data, array structure, and the cell library are known to the system. The CAD platform thus supports all the necessary design and verification steps, beginning with the technology level on up to the final step, the complete personalization of the array.□

PRICE AND AVAILABILTY

The U3351BM comes as a 144-pin-grid-array package. It will be priced at about $300 each in quantities of 1000 units, and will be available during the fourth quarter of this year.

Telefunken Electronic GmbH, P.O. Box 3535, D-7100, Heilbronn, Germany; phone: (0049) 7131-672519; fax: (0049) 7131-672340. **CIRCLE 512**

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CIRCLE 134 FOR U.S. RESPONSE CIRCLE 135 FOR RESPONSE OUTSIDE THE U.S.

NEC

SPARC UP SYSTEMS WITH CPU/FPU AND CHIP SET

The merger of the Sparc integer CPU and the floating-point coprocessor onto one chip makes the MB86903 one of the highest-performance Sparc family processors now available. Housed in a 207-lead pin-grid-array package, the Fujitsu combination CPU and FPU is the key component that complements a workstation motherboard chip set released earlier this year by the company.

Both a 33- and a 40-MHz version of the CPU/FPU chip are available. At 33 MHz, the MB86903 delivers a throughput of 24 MIPS of integer processing and 4 MFLOPS of floating-point horsepower. The 40-MHz version ups those numbers to 29 MIPS and 5 MFLOPS. Prices for CPUs are $239.60 and $304.50, respectively, in 5000-unit lots. Supporting the MB86903 is a set of five chips with which designers can build a compact Sparc-based motherboard.

Included in the chip set are the 86921 cache manager, tag store, and Mbus manager; the 86980 Mbus DRAM and 8-bit peripheral bus controller; the 86981 DMA, VRAM, and CRT controller; the 86985 Mbus-to-Sbus interface controller; and the 86986 Mbus-to-VMEbus controller. The 86921 is pinout-compatible with the Cypress Semiconductor 604 memory management unit, but expands the cache addressing to 256 kbytes. The 86980, which can address up to 512 Mbytes of main memory, also controls up to eight 8-bit peripherals over a local bus. Four channels of DMA control as well as interfaces to an 8-bit SCSI controller and an Ethernet controller are built in. A video controller that can handle an 1152-by-900-pixel, 8-color or monochrome display is also built in.

Fujitsu Microelectronics, Advanced Products Div., *77 Rio Robles Ave., San Jose, CA 95134-1807; John Meyer, (408) 456-1000.* **CIRCLE 571**

■ *DAVE BURSKY*

SPEEDY CACHE RAMS OPTIMIZED FOR SPARC

A family of 16-kword-by-16-bit cache RAMs, which delivers data in as little as 20 ns, lets system designers push Sparc-based systems to their maximum speed. The L7C157 from Logic Devices is pin-compatible but faster than the CY7C157 from Cypress Semiconductor. Housed in a 52-lead plastic or ceramic leaded-chip carrier, the RAM includes self-timed write lines, data input and output latches, and common I/O lines. Initially, three speed grades will be available—33-, 24-, or 20-ns access times—which match up with CPUs that operate at 25, 33, or 40 MHz. A 16-ns version of the RAM that will mate with the forthcoming 50-MHz CPU is in development. RAMs screened to MIL-STD-883C class B are also available. In lots of 100, the 33-ns grade of L7C157 sells for $57.16 apiece (plastic LCC).

Logic Devices Inc., 628 East Evelyn Ave., Sunnyvale, CA 94086; Tim Flaherty, (408) 720-8630. **CIRCLE 572**

DCT PROCESSOR HANDLES 15 MPIXELS/S

A bidirectional discrete-cosine transform processor, the ZR36020, can operate on 8-by-8-pixel blocks of image data and perform 2D forward and inverse DCTs. Incoming data can feed the ZR36020 processor at rates of up to 15 Mpixels/s.

The chip serves as a dedicated processor in a system—the host system controls the transformation direction and data format via the chip's control lines. Once initialized, the CMOS chip operates continuously at data rates up to 15 Msamples/s and delivers an 8-by-8-pixel DCT every 4.2 μs.

The DCT chip employs 16-bit two's-complement coefficients and has four user-selectable image data formats—8-bit unsigned with an internal level shift of 128, 8-bit unsigned with no internal level shift, 9-bit two's-complement, and 8-bit two's-complement. A very efficient design lets the DCT chip squeeze into a 44-pin plastic quad-sided flat package. Cascading the DCT chip with the soon-to-be-released image coder results in a DCT-based image-compression system that conforms to the emerging JPEG standard. The DCT processor consumes less than 625 mW when in the active mode and less than 10 mW when in the standby mode.

In quantities of 100, samples of the ZR36020 processor go for $79 each. In large quantities, the price can drop to less $20 each.

Zoran Corp., 1705 Wyatt Dr., Santa Clara, CA 95054; Isaac Shenberg, (408) 986-1314. **CIRCLE 573**

SOPHISTICATED SCSI CHIP MOVES 10 MBYTES/S

In addition to transferring data at rates of 5 or 10 Mbytes/s for normal or fast SCSI synchronous data rates, the TEC200 and 220 SCSI chips simplify many system operations thanks to on-chip intelligence. As a result of that intelligence, each of the two chips can perform additional information processing through the Queue tag and ID message checks, extended-message byte handling, and group-2 command handling. Asynchronous data transfers of up to 7 Mbytes/s are also supported. The chips consist of a SCSI-2 controller, a buffer manager, and a disk controller-formatter, all integrated into one package.

The buffer manager supports the use of static or dynamic RAMs and can transfer data to the memories at maximum rates of 13.5 Mbytes/s. As part of the buffer logic, proprietary data-flow circuitry monitors the state of the buffers and eliminates processor overheads during simultaneous high-speed data transfers to SCSI controllers and disk drives. Such a feature, combined with multisector handling of disk information (including automatic bad-sector skipping), gives the chip the ability to streamline data handling and to meet the increased speed demands of SCSI-2 systems.

As part of the disk controller, an error-checking and correction circuit implements a 64-bit ECC to ensure correct data is read from the drive. The chip also contains 30 programmable registers that allow users to adjust disk timing and operation to match the system requirements. Disk sector sizes, for example, can be set as large as 8 kbytes.

The TEC200 is available in a 100- or 120-lead plastic quad-sided flat package (single-ended SCSI or single-ended plus direct-connect to differential transceivers). The 100-pin version is the TEC200, and the 120-pin version the TEC220.

In quantities of 5000, the TEC200 is priced at $34 each while the 220 is priced at $45 each. Production quantities of the two SCSI chips are available immediately.

Emulex Corp., *3545 Harbor Blvd., P.O. Box 6725, Costa Mesa, CA 92626; Gary Des Rochers, (714) 662-5600.* **CIRCLE 574**

■ *DAVE BURSKY*

SPECTRUM ANALYZER WORKS TO 1 GHZ

A portable RF spectrum analyzer, the Model 2610, features a 1-GHz range in a package that measures only 4.5 by 11.8 by 13.4 in. and weighs only 20 lbs. Users can select a 1-MHz fixed-bandwidth setting that locks the 3-dB bandwidth at 1 kHz, regardless of the scan-width setting. This feature is ideal for observing video, TV, and CATV signals without complex setups. The instrument has a 70-dB dynamic range, and can be calibrated anywhere, using its internal 100-MHz, 80-dBμ signal. A front-panel switch selects either a 50-Ω (common in two-way communications applications) or 75-Ω input (used in TV applications). The unit comes with an ac line cord, dc source connector, and internal battery and recharger. The Model 2610 is available for immediate delivery at a price of $2995.

B+K Precision, 6470 W. Cortland Ave., Chicago, IL 60635; (312) 889-1448. **CIRCLE 575**

FLEXIBILITY HIGHLIGHTS FUNCTIONAL TESTER

By simply changing the test software, designers can functionally test boards running most 8- and 16-bit microprocessors with the DT-816 Functional Test System. The DT-816 employs an advanced ROM emulation technique that provides complete communication between the unit under test (UUT) and the ATE system in ASCII code. Software packages for individual microprocessors include kernal (CPU and ROM), memory, and I/O read/write tests. User test routines can be written in C or assembly code. The tester comes with a tutorial and examples of test source code to help in the development of specialized test routines for serial, parallel, and other support devices specific to the UUT. The unit has eight external triggers controlled by the test software running on the UUT. These triggers can control external instruments such as logic analyzers and oscilloscopes.

The DT-816 will be available in September. The $2495 price includes one software package; Additional packages cost $295.

Development Technology, 101 S. Court St., Lewisburg, WV 24901; (304) 647-9923. **CIRCLE 576**

UNIT EMULATES 486SX AND 487SX COPROCESSOR

The MICE-V-486 in-circuit emulator now supports the Intel 486SX microprocessor and 487SX coprocessor. A jumper on the 486 probe allows the user to select support for either the 486DX, 486SX, or 497SX. The emulator is rated to 33 MHz, well above the 486SX's current speed of 20 MHz. Features include a a fully qualified 8-kframe trace buffer, complex triggering, and extensive hardware debug features implemented in custom silicon on the emulator's probe. An optional source-level debug interface, called hyperSource, operates from a PC host and works with popular compilers, such as Microsoft C and Metaware High C. Users can begin debugging early in the hardware prototype phase, with a target whose only functional signal is a clock source. This feature, called Isolation Mode, lets users remove the 486 chip from the probe socket and connect logic analyzer clips to the pod to acquire timing information. Prices start at $29,500, with delivery in 4 weeks.

Microtek International Inc., Development Systems Div., 3300 N.W. 211th Ter., Hillsboro, OR 97124-7136; (503) 645-7333. **CIRCLE 577**

ARBITRARY GENERATOR FITS PC/AT SLOT

The AWG502 2-channel arbitrary waveform generator offers stand-alone-type performance in a PC/AT plug-in board. The unit supplies 12-bit resolution and up to 50-Mpoints/s on each channel. It features 64 kwords of RAM and 10 output filters for each channel. Multiple-segment looping ensures efficient memory usage. Each channel has its own 8-bit attenuator and 12-bit offset control. The generator comes with waveform-creation and management and operational software, as well as a function library, so users can create custom application programs. The library is compiled in Turbo C, and the source code is included so users can compile the library to other C dialects or translate it to different languages. The AWG502 costs $3500.

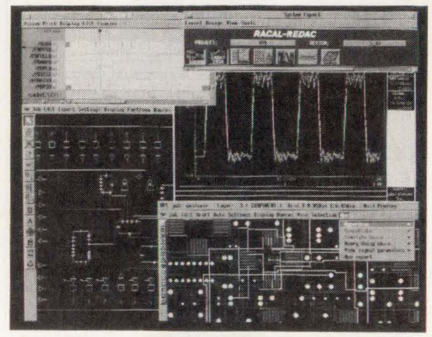
Signatec Inc., 357 N. Sheridan St., Suite 199, Corona, CA 91720; (714) 734-3001. **CIRCLE 578**

Tool Suite Analyzes The Impact Of Layout On Board Design

The Visula High-Performance Engineering (HPE) suite of tools focuses on the need to analyze the impact of physical layout on high-speed board designs. HPE can directly control the physical-layout process from design rules that govern critical factors, such as path delays, reflection, and crosstalk limits. All of the software is tied together under the company's Vision framework.

Several key elements let users control and analyze the impact of physical layout at all stages of the design flow. For instance, technology-independent rules are held in a library database. The database controls physical routing according to generic constraints relevant to particular design technologies and parts. These include pin ordering, impedance characteristics, and route spacings.

Also, entry of critical design parameters in the schematic environment controls routing of the physical board according to key constraints like minimum and maximum delay per net and crosstalk between nets. Components grouping and associated floor planning of layouts enables users to control physical design according to electronic functionality.



The Visula HPE toolset runs on DEC, HP/Apollo, and Sun workstations, and costs about $75,000. It will ship by the end of the summer.

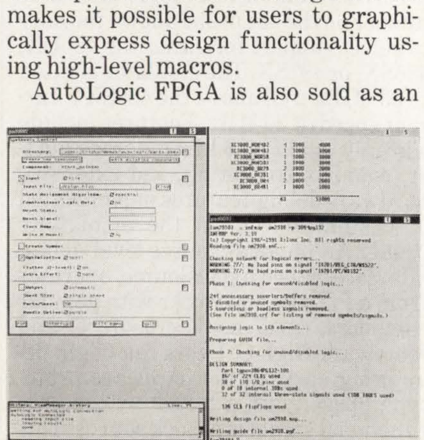
Racal-Redac Inc., *1000 Wyckoff Ave., Mahwah, NJ 07430; (201) 848-8000.* **CIRCLE 579**

■ *LISA MALINIAK*

Synthesis Technology Supports Three Top FPGA Vendors

Circuits created with Mentor Graphics' synthesis technology can be optimized for Actel, Altera, or Xilinx field-programmable gate-array (FPGA) architectures with AutoLogic FPGA. The product is built on the AutoLogic synthesis software for ASIC and IC design. Also, an optional product called AutoLogic Blocks makes it possible for users to graphically express design functionality using high-level macros.

AutoLogic FPGA is also sold as an option to AutoLogic product. It features pushbutton optimization for area and speed using a mix of Boolean minimization and factorization, state assignment, and technology-mapping algorithms. AutoLogic FPGA performs architecture-specific optimization. For instance, Mentor worked closely with Xilinx to ensure that the tool properly uses the Xilinx lookup table, the core element of its FPGA technology.



FPGA families supported in the AutoLogic FPGA product are: the Actel Act 1 and Act 2 families; the Altera Max 5000 family; and the XC2000, XC3000, and XC4000 families from Xilinx. AutoLogic FPGA will ship by the end of the summer in Mentor's Release 7.0 environment. It costs $5000 per supported vendor. AutoLogic for ASIC and IC synthesis goes for $25,000. The AutoLogic line of software will be available in the Release 8.0 environment by the end of the year.

Mentor Graphics Corp., *8005 S.W. Boeckman Rd., Wilsonville, OR 97070; (503) 685-7000.* **CIRCLE 580**

■ *LISA MALINIAK*

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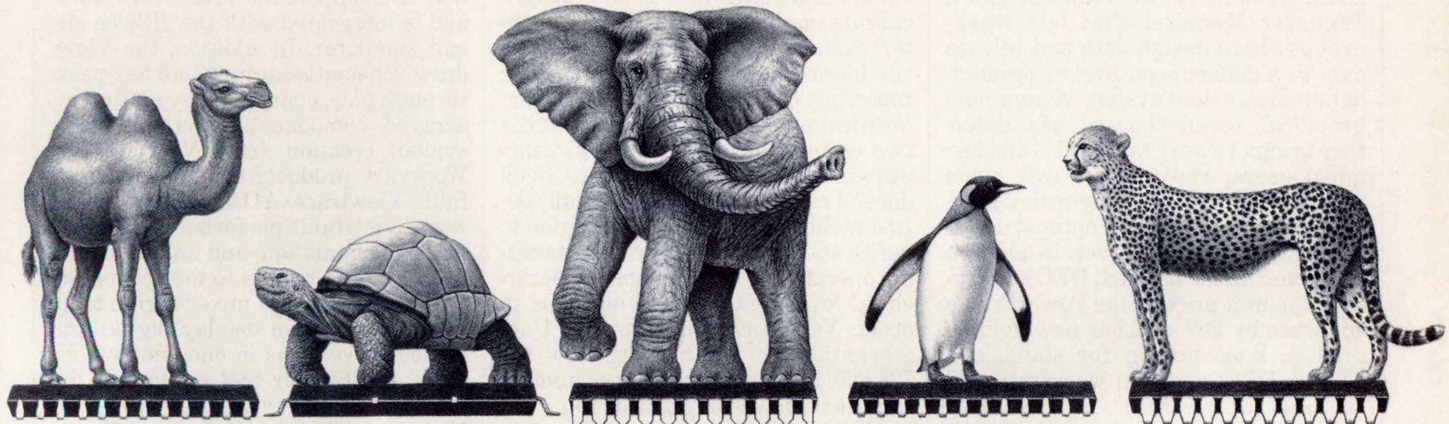

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	Model	Speed (ns)	Packaging	Data Retention Current	Special Features	Availability
128Kx8	CXK581000P	100/120	DIP 600mil	L/LL	B/X	Now
	CXK581000M	100/120	SOP 525mil	L/LL	B/X	Now
	CXK581100TM	100/120	TSOP (normal)	L/LL	B/X	Now
	CXK581100YM	100/120	TSOP (reverse)	L/LL	B/X	Now
	CXK581001P	70/85	DIP 600mil	L/LL		Now
	CXK581001M	70/85	SOP 525mil	L/LL		Now
	CXK581020SP	35/45/55	SDIP 400mil			Now
	CXK581020J	35/45/55	SOJ 400mil			Now
128Kx9	CXK77910J	17/20	SOJ 400mil		Sync ASM	3/Q '91
256Kx4	CXK541000J	25/30/35	SOJ 400mil			3/Q '91

L = Low LL = Low,Low B = 3 Volt X = Extended Temperature

SONY

Sony Corporation of America, Component Products Company, 10833 Valley View St., Cypress, CA 90630

Sony Canada, 411 Gordon Baker Rd., Willowdale, Ontario M2H 256

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CIRCLE 165 FOR RESPONSE OUTSIDE THE U.S.

PRICE CUT ON IMPROVED FRAMEWORK SOFTWARE

Engineers can enjoy all of the benefits of DEC's PowerFrame design-data-management software at a fraction of its original cost. Enhancements to the latest version of PowerFrame include a Transfer Manager that lets work-groups share design data and release data to a department level or product-data-management system. Also, a non-graphical, terminal-based user interface brings PowerFrame to PC and terminal users. PowerFrame was made faster with improved algorithms, reduced program size, and optimal use of the design-manager server. In addition to enhancing the product, DEC has lowered the unit price of the PowerFrame software by 20% and has new volume pricing. Base pricing for standalone Apollo, DEC, and Sun workstation licenses is set at $4000.

Digital Equipment Corp., 4 Results Way, Marlboro, MA 01752; (508) 467-5111. **CIRCLE 581**

IC VERIFICATION TOOL MAINTAINS HIERARCHY

Millions of transistors are no problem for the VeriCheck IC-verification software. VeriCheck performs hierarchical design-rule checking (DRC), layout-versus-schematic verification, electrical-rule checking, and layout-parameter extraction. Advanced algorithms run hierarchical verification and error reporting with distributed processing. Verification tasks are processed across two or more nodes on a workstation network. In addition, VeriCheck doesn't require that users manually define a chip's layout hierarchy prior to verification. It also performs undersizing operations on any number of hierarchical levels without causing gaps to occur. VeriCheck, which runs on Unix workstations, is shipping now for $80,000. However, potential customers can use it for a 30-day trial period.

Integrated Silicon Systems Inc., P.O. Box 13665, Research Triangle Park, NC 27709; (919) 361-5814. **CIRCLE 582**

UPGRADED CAE SOFTWARE EXPLOITS PC FEATURES

Enhancements and new products embellish the Workview 4.1 CAE software for ASIC, IC, and system design. For instance, the Viewsim/SD simulator now has support for VHDL structure, and is integrated with the HSpice circuit simulator. In addition, the Viewdraw schematic-capture tool has pass-through pins, connection by abutment, arrayed components, and automatic symbol creation from VHDL. New Workview products include the Viewfault, Viewtrace/AD, and Builder software. Viewfault performs deterministic fault simulation, and annotates the fault-grading results to the schematic. The Viewtrace/AD mixed-signal analysis software can display digital and analog waveforms in one window. Finally, the Builder tool automates the generation of synthesis libraries. Moreover, all of the Workview 4.1 tools have better support for the personal computer. For example, Workview runs in 800-by-600 VESA-compatible VGA graphics, and supports the Logitech C series mouse. Workview 4.1 is available now on both DOS and Unix platforms. Contact the company for pricing information.

Viewlogic Systems Inc., 293 Boston Post Rd. West, Marlboro, MA 01752-4615; (508) 480-0881. **CIRCLE 583**

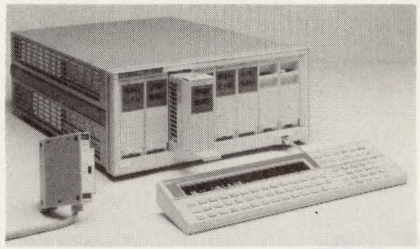
TIMING TOOL PREDICTS SYSTEM GROUND BOUNCE

The Crosstalk Tool Kit (XTK) 4.2 signal-integrity software features three major enhancements. First, the tool can now model simultaneous switching interactions with power and ground inductances for each chip on a pc board. These inductance effects are key to detecting ground-bounce problems. Second, it can perform system-level signal-quality analysis for multiboard and backplane designs. XTK 4.2 uses database information extracted from other EDA programs to calculate signal-line characteristics for every trace in a circuit configuration, as well as the crosstalk and other distortions. Finally, XTK 4.2 can use Spice data to automatically generate behavioral-simulation models for nonlinear circuit drivers and receivers. The XTK software, which runs on Unix workstations, will ship in the third quarter. Prices range from $27,000 to $69,000, depending on platform and network options.

Quad Design Technology Inc., 1385 Del Norte Rd., Camarillo, CA 93010; (805) 988-8250. **CIRCLE 584**

Mainframe-Based Power-System's High Density Saves Rack Space

Up to eight 150-W dc power-supply modules fit in just seven inches of rack space with the HP 66000A modular power system. The system's density and ease of configuration addresses the growing pressure to reduce the rack space required for programmable power in automatic-test-equipment (ATE) systems.



Compared to HP's existing single-output system power supplies of similar power, the HP 66000A supply requires only a quarter of the rack space for an eight-output system. The system's modular approach makes it easy to add or replace power modules that install from the front even when the system is powered up. The mainframe's special connectors can be ordered with built-in relays for programmable disconnect or polarity reversal.

A low-noise switching design results in a noise specification of 5 to 10 mV pk-pk. The output voltage and current can be read back over the HP-IB bus with 14-bit resolution.

Sequences of voltages, currents, and dwell times can be downloaded to the modules, which increases test throughput. Each module can store a sequence of up to 20 output settings. This feature is augmented by a flexible triggering bus for self-paced sequencing.

The HP 66000A mainframe costs $1900. An optional keyboard goes for $750. There are three modules currently available with ratings of 8 V and 128 W (66101A), 20 V and 150 W (66102A), and 35 V and 150 W (66103A). All are priced at $1750 each. The relay option for the connectors costs $180. Delivery is in eight weeks from receipt of order.

***Hewlett-Packard Co.**, 19310 Pruneridge Ave., Cupertino, CA 95014; (800) 752-0900.* CIRCLE 585

■ *DAVID MALINIAK*

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Four totally isolated dc-dc converters, each with positive and negative voltage outputs, come in one SIP package in the Power Convertibles HPR2XX Series of converters. Each of the four outputs delivers up to 750 mW of unregulated power to dual loads for a total output of 3 W. Input voltages include 5, 12, 15, and 24 V, while outputs are ±5.2, ±12, and ±15 V. Pricing is $16.89 in lots of 1000. Delivery is stock to four weeks.

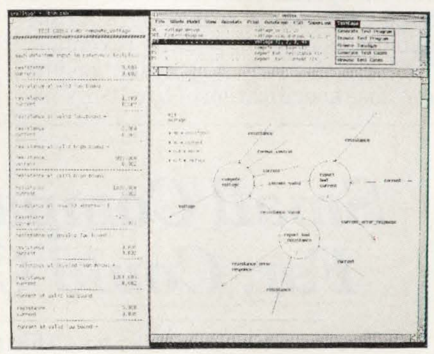
Burr-Brown Corp., Power Convertibles, P.O. Box 11400, Tucson, AZ 85734; John Conlon, (800) 548-6132. CIRCLE 586

SYNCHRONIZE C DESIGNS, SOURCE CODE

A C-language development environment that previously contained Software Through Pictures, Saber-C, and Framemaker or Interleaf TPS has grown considerably. The environment now includes reverse-engineering and code-generation modules, as well as the facilities to synchronize code and designs, query the shared repository, and navigate among the components. Using the environment, developers can modify either the design, the code, or both, with the assurance that they can be easily synchronized. The navigation facility enables users to move easily among the code, design, and documentation. The query function can be used to understand how objects in the system affect each other and to locate unused or redundant code. A small workgroup configuration costs about $10,000 per user. The environment is available now on Sun Sparcstations and on Digital Ultrix, HP 9000, and IBM RS/6000 workstations by November.

Interactive Development Environments Inc., 595 Market St., 10th Floor, San Francisco, CA 94105; (415) 543-0900. **CIRCLE 587**

CASE TOOL AUTOMATES TEST-CASE GENERATION



Programmers can now automate software-test-case generation with the Teamwork/TestCase tool from Cadre Technologies. TestCase is tightly integrated with the company's Teamwork family of CASE products. The TestCase tool uses standard testing methodologies, enabling designers and test engineers to leverage previous investments in their CASE models. It automatically defines the set of non-redundant test cases that will detect the most common defects. Also, it uses the software requirements to generate unique, traceable test cases for each requirement, employing techniques of boundary-value analysis, equivalence-class partitioning, cause-effect graphing, and error guessing. In addition, as requirements change and software is added or deleted, TestCase automatically regenerates the appropriate tests. Teamwork/TestCase is shipping now on Sun workstations and will ship by the end of the year on IBM workstations. Pricing starts at $9995.

Cadre Technologies Inc., 222 Richmond St., Providence, RI 02903; (401) 351-2273. **CIRCLE 588**

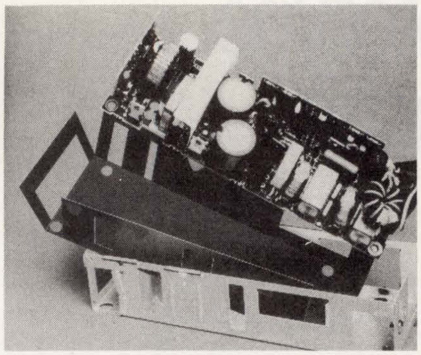
THICK-FILM MATERIALS FORM RESISTORS

Ultra-high stability is featured in the Series R8900 resistor system, a paste with a temperature coefficient of resistance of 100 ppm over a range of 10 Ω to 1 MΩ. In addition, the paste exhibits excellent electrostatic-discharge characteristics. The paste is calibrated on the company's C1214B 3:1 silver/palladium thick-film conductor material. Special calibrations are also available for gold and dielectric materials. Call for pricing and delivery.

Heraeus Inc., Cermalloy Div., 24 Union Hill Rd., West Conshohocken, PA 19428; (215) 825-6050. **CIRCLE 589**

POLYCARBONATE FILM RESISTS HEAT AND FLAME

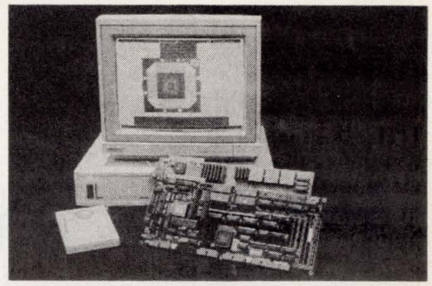
Superior electrical and flammability capabilities for electrical-barrier insulation is offered by Lexan FR700 polycarbonate film. The film boasts higher dielectric strength and flame retardance than competing materials, the company claims. It's easily fabricated with sharp folds or intricate die cuts. Call for pricing and delivery.



GE Plastics, PR No. 43-91, One Plastics Ave., Pittsfield, MA 01201; (800) 451-3147. **CIRCLE 590**

MACHINE-VISION SYSTEM GIVES COMPUTERS SIGHT

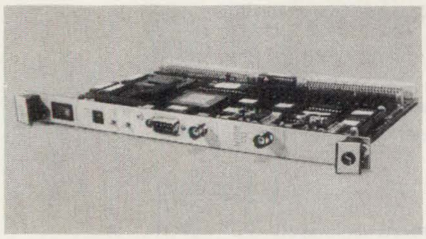
A PC-compatible machine-vision system is aimed at OEMs requiring high-speed positioning and automated-inspection capabilities. The RTI-680 vision system offers four camera inputs, standard PC-development tools, open-architecture software libraries, and custom-software support. Unlike traditional frame grabbers that transfer images to the PC for processing, the RTI-680 system transfers only computational results to the PC, freeing the host for other tasks. The system, including software, costs $6000 in single quantities.



CR Technology, 23062 La Cadena Dr., Laguna Hills, CA 92653; (714) 859-4011. **CIRCLE 591**

32-BIT BOARD CONNECTS VME SYSTEMS TO NTDS

VMEbus systems can be connected to MIL-STD-1397 Navy Tactical Data Systems using the 32-bit serial Hawke board from Sabtech Industries Inc. By going to 32 bits, the board eliminates historical 16-bit bottlenecks. The on-board software



suite makes VME-based NTDS systems easy to develop, debug, integrate, test, and maintain.

The board features a 32-bit Motorola 68020 processor and a VIC 068 VMEbus interface controller chip. It can accommodate up to 1 Mbyte each of system and user ROM, as well as a unique dual-ported 512-kbyte memory that can be dynamically repartitioned and reallocated for various uses. There's also on-board development software, including a built-in assembler, disassembler, and on-line debugger.

The Hawke is available in three different versions. There's a type D board for serial data on a coaxial cable, a type E board for low-level serial data on a triaxial cable, and a type J board for fiber-optic data. Aside from some individually required control signals, the user software is mutually compatible among the three boards. The type D and E boards sell for $4495 each, and the J board costs $4695 each. Large-quantity discounts are available.

Sabtech Industries Inc., 5411 East La Palma Ave., Anaheim, CA 92807; (714) 970-5311. **CIRCLE 592**

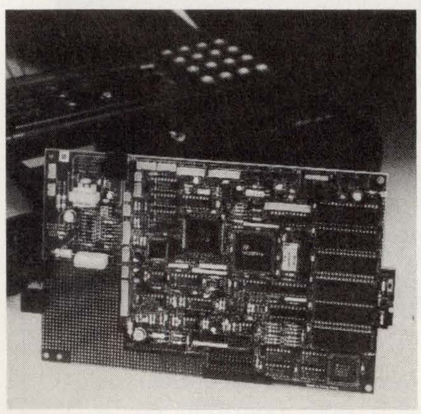
■ *RICHARD NASS*

BUILD ENHANCED FAX SYSTEM IN LESS TIME

Using the Dragon board from National Semiconductor Corp., users can develop a plain-paper or thermal-paper facsimile machine in six months or less. According to the company, the design previously took 18 months or longer. Dragon combines advanced software modules and specialized VLSI devices on one board. The board lets designers add new features to their fax-based products, such as adding fax capability to a laser, inkjet, or bubblejet printer, for around $30 per system.

The Dragon can be used as a design, development, and prototyping platform for a new standalone fax machine or in a multifunction peripheral. Such a system could combine the capabilities of a fax machine, a printer, a scanner, a copier, a modem, and an answering machine.

National says that this board is the first to use modifiable-software modules to execute the functions of a fax machine. This NSFAX software approach adds flexibility and accelerates time to market. For example, an OEM can add a special feature, such as special-tone or error detection, in less than a week. If done in hardware, this type



of task would take substantially longer. In addition, NSFAX can be modified to meet any geographic specification and conforms to all European, North American, Japanese, and South East Asian public telecommunication requirements. The board, part number NSV-FX16FAX-EDB, is available now for $1495. The NSFAX software is available for licensing in binary and source versions.

National Semiconductor Corp., 2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052; (408) 721-5000. **CIRCLE 593**

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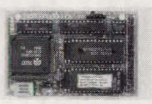

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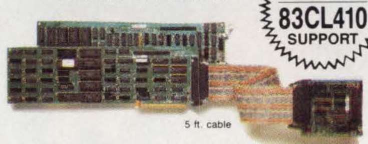

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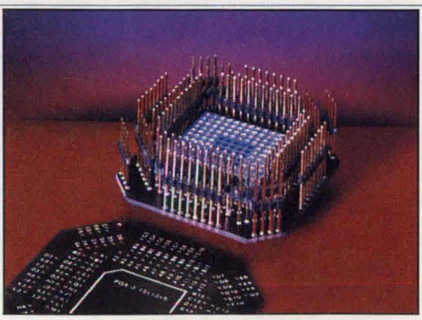

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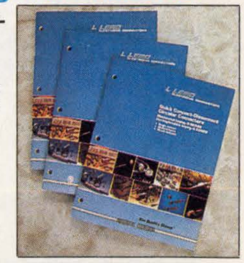

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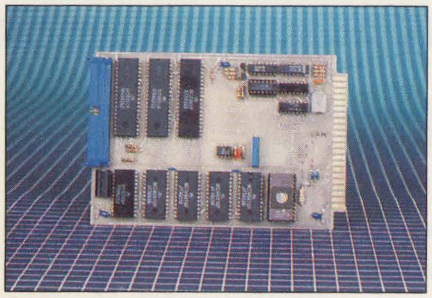

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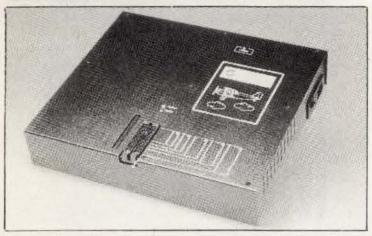

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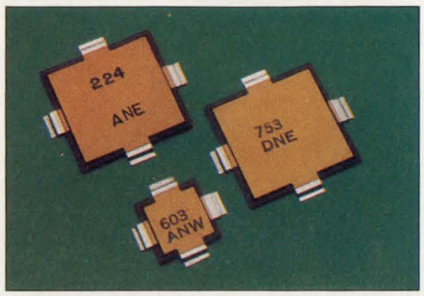

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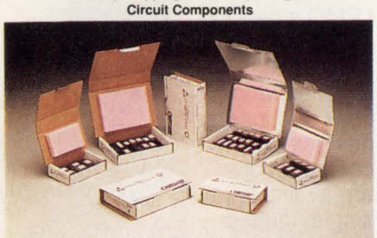

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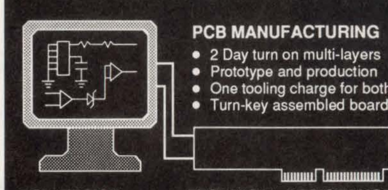

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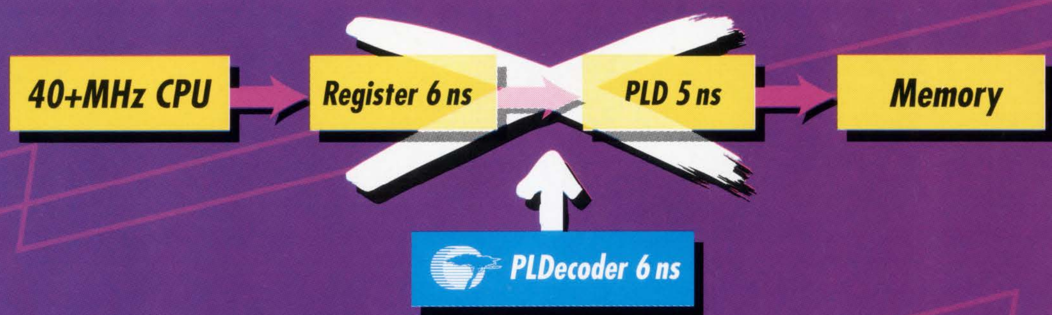

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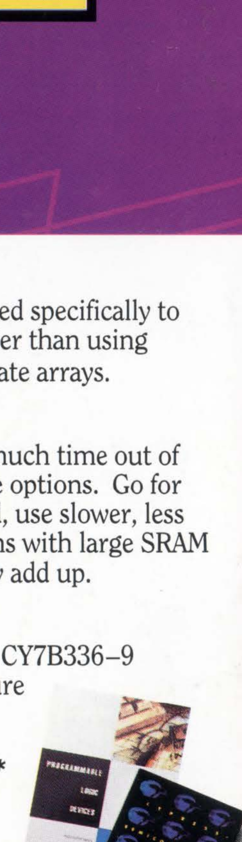

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