Electronics®

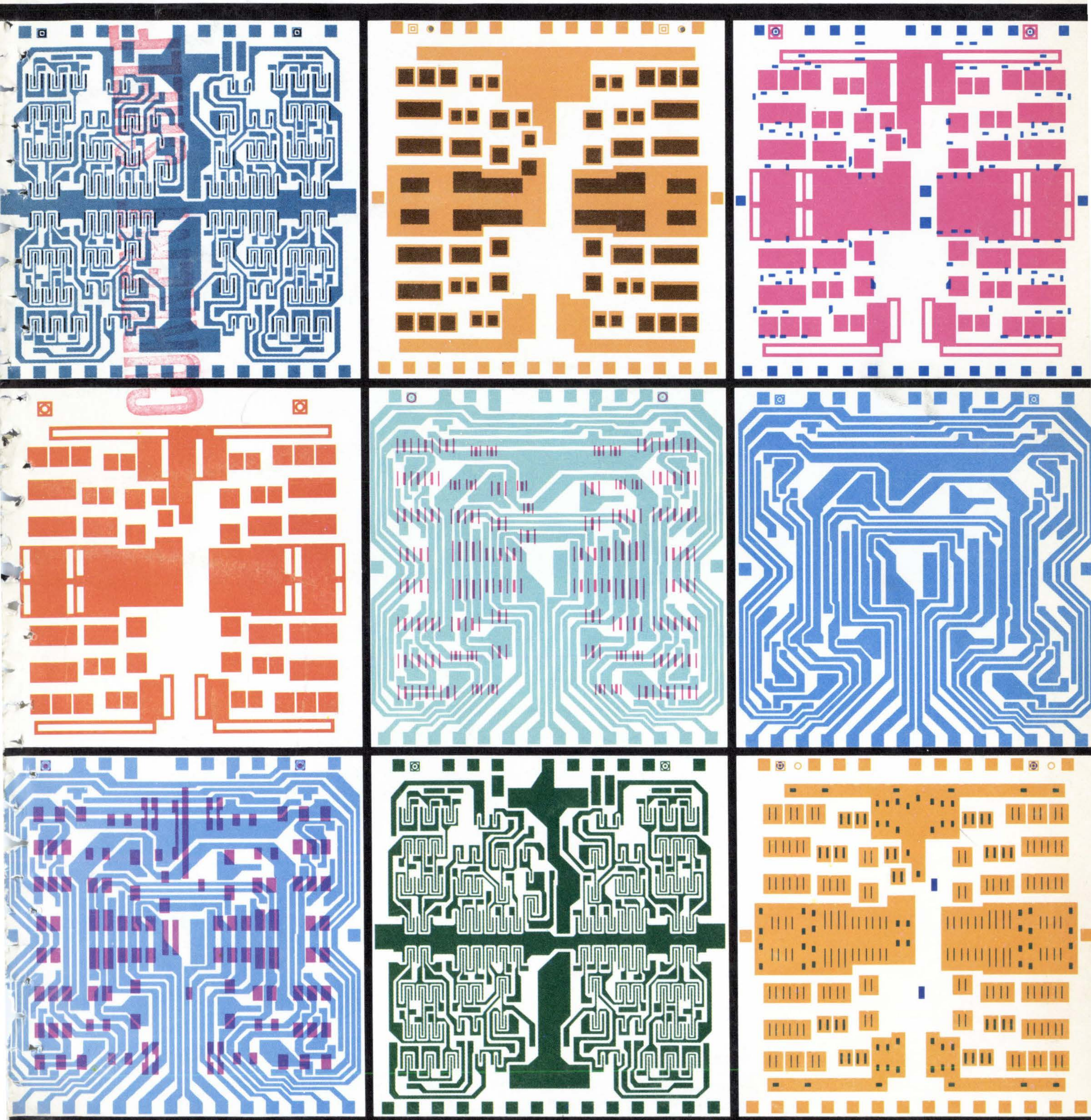
Shifting phases digitally: page 104

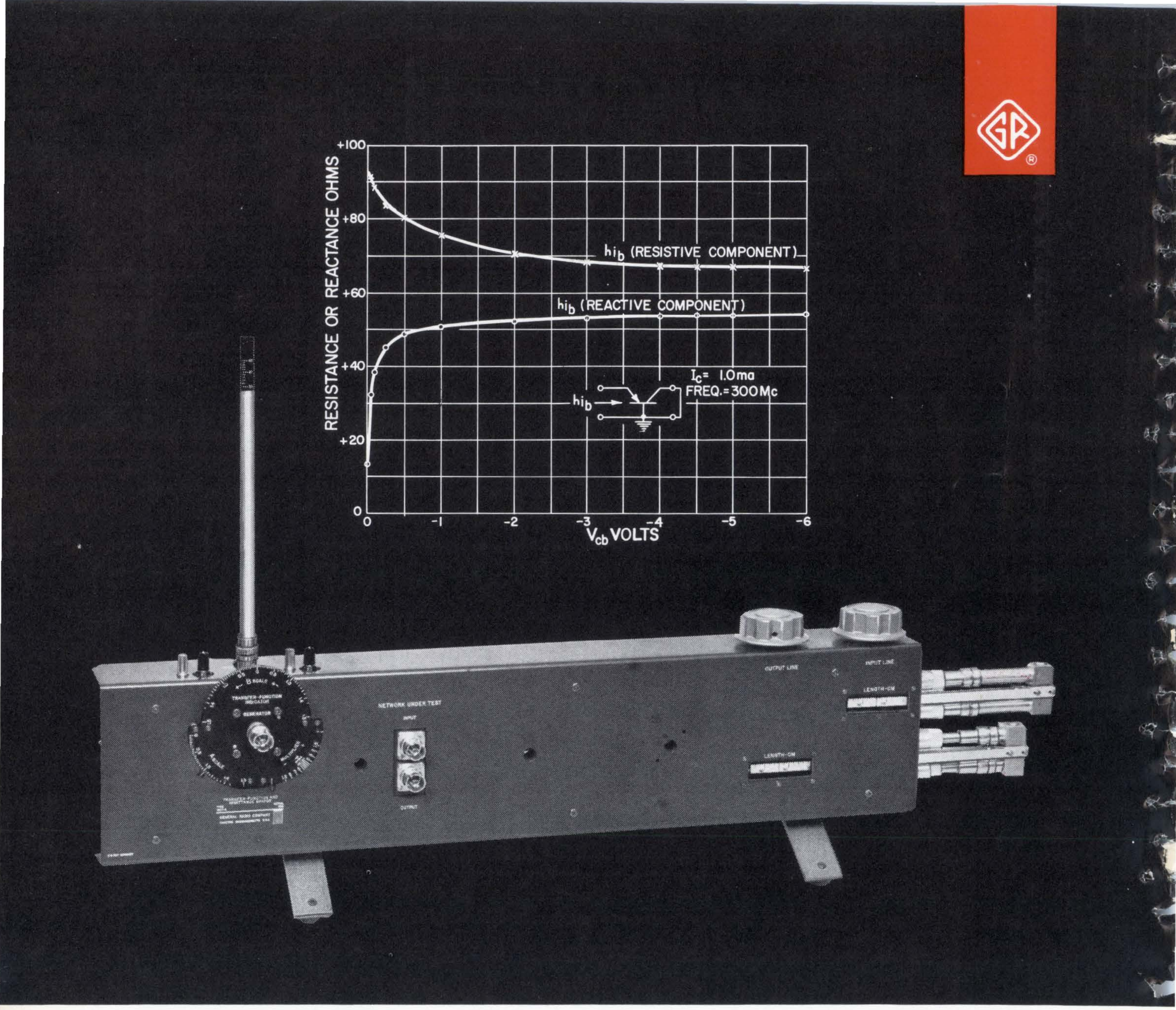
Norad's fabulous computer system: page 113

Special report on large-scale integration: page 123

February 20, 1967
$1.00
A McGraw-Hill Publication

Below: Many masks make up large-scale integration, p. 123





Measure transistor *h* and *y* parameters directly without resorting to the "New Math."

If you use *h* and *y* parameters in your design work, you can measure them directly with the 1607-A Transfer-Function and Immittance Bridge. You can measure h_{ob}, h_{oe}, h_{fb}, h_{fe}, h_{ib}, h_{ie}, h_{rb}, h_{re}, y_{ob}, y_{oe}, y_{fb}, y_{fe}, y_{ib}, y_{ie}, y_{rb}, y_{re}, as well as all open-circuit impedance parameters directly, without using mathematical transformations that could degrade data accuracy. These measurements can be made over a broad 25-MHz to 1.5-GHz range.

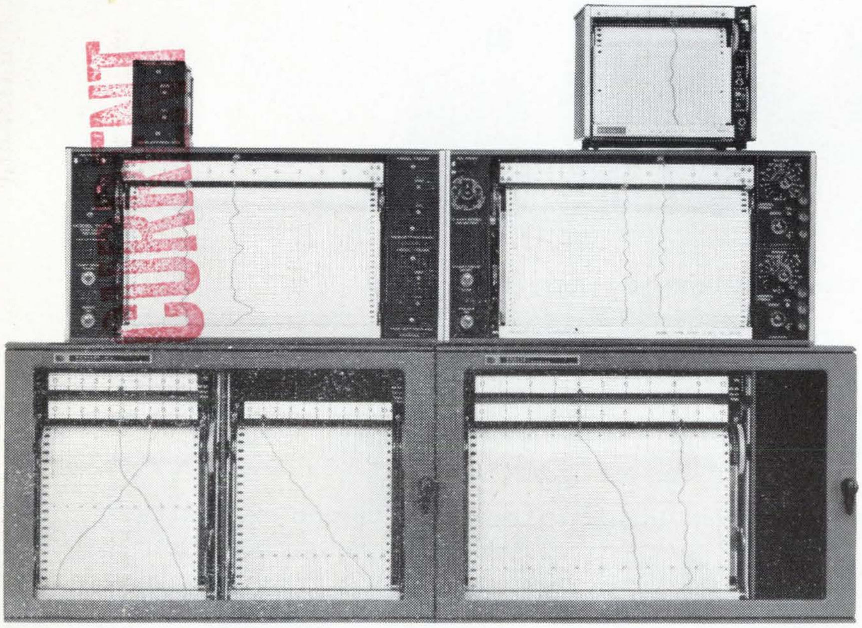
Since the 1607-A uses adjustable lines settable to half and quarter wavelengths, both open- and short-circuit conditions can be easily established. Eight specially designed, electrically invisible mounts for almost all popular transistor configurations provide a readily defined reference plane for measurements. No measurement corrections need be made for the mounts. Even transistors with 2-inch leads can be measured without correction (the mount "swallows" the leads). The transistor can even be mounted with some of its lead length exposed to simulate its eventual connection in the circuit. In this way, the parasitic effects of the leads can also be considered.

Price of the 1607-A is $1995; transistor-mount prices range from $65 to $115. For a complete description of the 1607-A, request our Engineering Reprints E107 and E109. Write General Radio Company, 22 Baker Avenue, W. Concord, Massachusetts 01781; telephone (617) 369-4400; TWX 710 347-1051.

GENERAL RADIO

Circle 900 on reader service card

multiple choice



which of these strip-chart recorders is best for your needs?

With three highly flexible groups of recorders, Hewlett-Packard offers you a range of reliable models for the widest laboratory and industrial application. They feature modular solid-state construction, improved ink or inkless electric writing systems, and a choice of mechanical or optical slidewires.

The 680 is a general-purpose laboratory-type model that provides high accuracy and swift response in a 5" writing width. Important features are a 3-position tilting chart magazine, plus multi-range inputs and chart speeds. The Model 680 is priced at $750.

In the 7100 Series, four recorders with plug-in modules provide customer-selected input level spans for versatile, general-purpose 10" recording capability. Lower-cost models (7127 and 7128) are designed primarily for use with gas chromatographs. Recorders are priced from $850 to $1300, and plug-in modules are priced from $200 to $350.

The new 5700 Industrial Series of strip-chart recorders offers modular design for rapid interchange of modules on line and minimum down-time. Choose sensitivity and speed from a wide selection of low-cost recorders and match the recorder to your particular need; convert later if requirements change. One- and two-pen models, 6" and 11" recording. A choice of four models priced from $825.

HEWLETT PACKARD hp MOSELEY DIVISION

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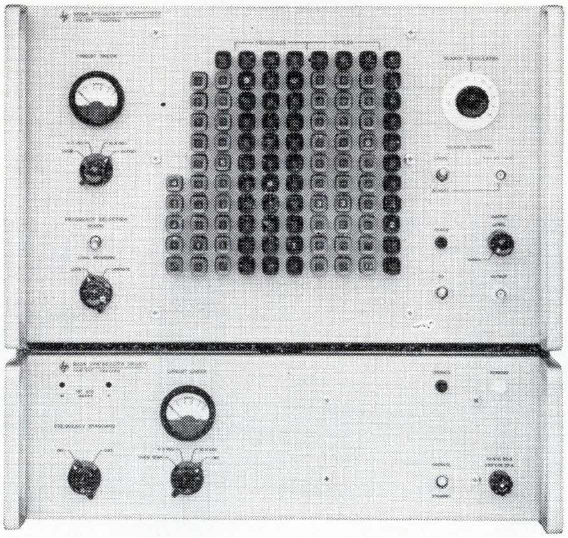
(Yes, 500)



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Model 5105A—$9150.

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HEWLETT hp PACKARD

2490

Electronics

February 20, 1967
Volume 40, Number 4

News Features

Probing the News

Electronics Review

Electronics Abroad

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Technical Articles

I. Design

II. Application

III. Large-scale integration

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Readers Comment

Misplaced division

To the Editor:

In the article "Jungle fighters on Chesapeake Bay" [Jan. 23, p. 153] the developer of the AN/GRC-64 radio is listed erroneously as the Delco Products Division of the Ford Motor Co. Delco Radio, of course, is a division of the General Motors Corp.

Hamlin Welling
Delco Radio Division
Kokomo, Ind.

Ode to a node

To the Editor:

The article, "Topology cuts design drudgery," [Nov. 14, 1966, p. 112] contains a most useful survey of network analysis by topological methods. I believe that these methods would find more application if the rules could be more easily remembered.

What is needed is an aid, maybe doggerel, which will stick in the memory.

Something like this:

Node to a network

Listen all if ye would fain,
Solve a network without slaving the brain,
Get input admittance from a sub-graph,
And dismiss determinants with a laugh.

Take the trees of network N,
Form the admittance products then,
Add admittance product set,
Delta is the sum you get.

Now short vertex one to one prime,
Make the two-trees, two edges each time,
Form the admittance products then,
Get delta one-one by summing again.

Delta over delta one-one is sought,
To find admittance at the input port.
Try it once and you'll soon see
Much more can be done with topology.

Peter Robinson
Needham Heights, Mass.

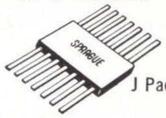
Aircraft separation

To the Editor:

In the article "Put to the test" [Jan. 23, p. 44], you identify the International Civil Aviation Organization as "the airlines industry group." ICAO is a specialized agency in relationship with the United Nations, with a membership of 111

You Can Get All These Microcircuits from Sprague Electric:

*SERIES SE100, NE100, US700 DTL LOGIC
(Signetics CS700)



J Package

Eighteen functions in two operating temperature ranges: —55 C to +125 C and 0 C to +70 C. Circuits include NAND/NOR gates, clock and line drivers, gate expanders, RST and JK binary elements, one-shot multivibrator.

Circle 481 on readers service card

*SERIES SU300, LU300 UTILOGIC★

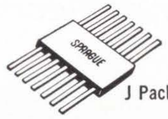
K Package

For use in commercial, industrial, ground support applications. Available in two operating temperature ranges, —20 C to +85 C, and +10 C to +55 C. Propagation delay of 15 to 40 nanoseconds.

★Trademark of Signetics Corp.

Circle 482 on readers service card

*SERIES SE400, NE400 LOW POWER LOGIC



J Package

Operating temperature ranges: —55 C to +125 C, and 0 C to +70 C. For use in Aerospace and other applications where low power drain is required. Optimized speed, noise margin.

Circle 483 on readers service card

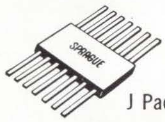
*SERIES SE500 LINEAR AMPLIFIERS

K Package

Operating temperature range: —55 C to +125 C. Two linear circuits available in 10-lead low silhouette TO-5 case. SE501K is a video amplifer, SE505K is a general purpose differential amplifier.

Circle 484 on readers service card

*SERIES SE800, NE800 TTL LOGIC



J Package

Designed for high-speed avionics systems. Eight high level circuits including four NAND Gates, Power Gate, Exclusive-OR Gate Input Expander, J-K Flip-Flop.

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UNICIRCUIT® RCTL LOGIC

(8x actual size)

Sprague Series US-0100 . . . a complete line of silicon monolithic digital building blocks featuring low power consumption (2 mW typ.)

Circle 486 on readers service card

UNICIRCUIT® mW RTL LOGIC

TO-5 Case

Types US-0908 through US-0921 . . . Fully interchangeable mW digital building blocks featuring power consumption of 2 mW/node and propagation delay of 40 nsec.

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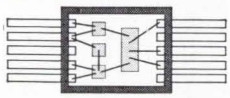
UNICIRCUIT® CUSTOM HYBRID CIRCUITS



Combine monolithic silicon circuits with tantalum or Ni-Cr alloy resistors. Close resistance tolerances, low temperature coefficient. Resistor matching, ±½%.

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UT-1000—Four-bit ladder network
UD-4001—Ladder switch for driving resistor ladder networks
UD-4024—Buffer amplifier

Circle 489 on readers service card

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We have a total capability to produce practically anything you want. Deposits from 5 to 200 millionths of an inch in thickness can be plated on almost any temper or diameter specialty wire or ribbon to your specification.

If you'd like to see what we can do with wire or ribbon, send for a sample today. Write: Sylvania Electric Products Inc., Parts Division, Warren, Pennsylvania 16365.

SYLVANIA

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sovereign governments; the airlines industry group is IATA, the International Air Transport Association.

The decision to reduce separations from 120 to 90 nautical miles was taken in December 1963 by ICAO on proposals from its member governments, not from the airlines. The 90 nautical-mile separation is still on ICAO's books as the minimum, although the implementing states are using a separation higher than that minimum.

The article also states that the navigational problems come from the accuracy—or the lack of accuracy — of existing navigational equipment. Actually, this is not so; existing equipment is quite accurate enough to keep aircraft with a 90-nautical-mile-wide path. The problem actually is dependability: how often do gross navigational errors occur because of equipment or human failure, errors large enough to put aircraft outside the path.

The tests are being run by ICAO member states, rather than by ICAO itself, and the ground radar equipment is being installed by governments.

Joachim Schypek
International Civil Aviation
Organization, Montreal

Filter debate

To the Editor:

I would like to comment on the article "FET's call the tune in active filter design" [Oct. 3, 1966, p. 98] which I read with considerable interest.

On page 99 the statement $R = R_1 + R_2$ should have been written as $R = R_1 = R_2$, a restricted case. Then equation,

$$\omega_n = \frac{1}{RMC_2} = \text{resonant frequency}$$

is correct.

But equation 3 is incorrect and should be

$$\rho = \frac{1}{M} + \frac{M}{2}(1 - K_2),$$

On page 100 the statement

$C_1 = C_2$

is a mistake. Equation 6 is the generalized case of the high-pass filter.

For the low-pass filter, the generalized equations should be as follows:

$$\omega_n^2 = \frac{1}{R_1R_2C_1C_2};$$

$$\rho = \frac{1 + \lambda 2}{2M\lambda} + \frac{M}{2\lambda}(1 - K_2);$$

where:

$$M^2 = \frac{C_1}{C_2} \quad \text{and} \quad \lambda^2 = \frac{R_2}{R_1}.$$

Edward Poncracz-Bartha
Member, Technical Staff
ITT Federal Laboratories
San Fernando, Calif.

The author replies:

The statement $R = R_1 + R_2$ should read $R = R_1 = R_2$, a necessarily restrictive case.

The generalized equations have no usefulness in the voltage tunable filters described in the article because R_1 must be equal to R_2 to be at all practical.

Pongracz-Bartha's remaining statements are true and they are well known to filter designers. It was not my intent that the article be tutorial. It was intended to outline a new active filter technique in sufficient detail to be useful to design engineers.

James M. Loe
Project engineer
Philco-Ford Corp.
Blue Bell, Pa.

People

The increasing demand for electronic equipment for the Vietnam conflict and the high risk involved in bidding on government contracts are two of the problems facing **David Shore,** new chief defense engineer for the Radio Corp. of America's defense electronics products group.


David Shore

Shore, formerly chief engineer in the Communications Systems division, says the Southeast Asian war "has created a demand for short-term-payoff equipment. Fewer Government dollars are available for longer-range research and development programs."

Risky business. The Pentagon's cost-effectiveness program has also put pressure on electronics companies. Shore says that with the number of fixed-price contracts growing, a company's proposal must be carefully prepared. "We practically have to have a 'talking dog' when we make a proposal—that is, we must be able to demonstrate how the equipment works and how much it will cost."


C. K. Law

The 47-year-old Shore will be responsible for the technical and engineering performance of the five divisions in his group—Communications Systems, Missile and Surface Radar, Astro-Electronics, Aerospace Systems and West Coast. He will also be in charge of RCA's systems engineering, evaluation and research, defense microelectronics, applied research and central engineering.

Program development. Succeeding Shore as chief engineer for the Communications Systems division will be **C. K. Law,** 43. As manager of the division's engineering operations, Law was called upon last year to reorient operations as the early Minuteman ICBM contracts neared completion. His job was to

replace the larger program with several smaller ones and coordinate efforts in engineering, marketing and management.

To assure that RCA takes full advantage of new technology, Law has set up a program development group to handle applications engineering, plan projects and consider proposals for new programs.

When **S.F. (Fred) Eyestone** took over as president of North American Aviation Inc.'s Autonetics division [Electronics, Feb. 6, p. 8] he reinstituted the "troika" administrative system, dropped last year, by appointing two executive aides.

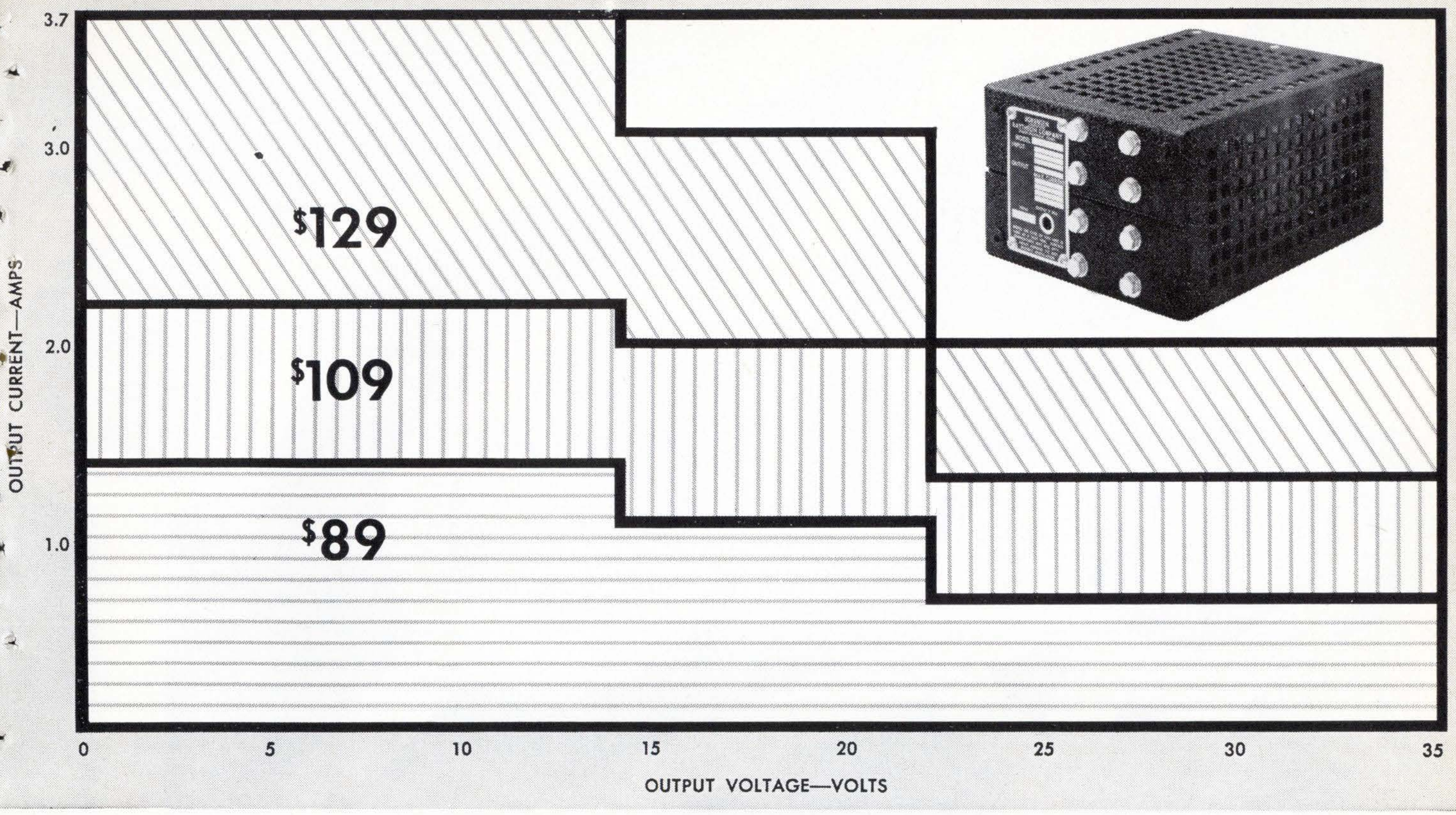
S. F. Eyestone

The three-man executive office is to provide greater depth in managing Autonetics, the most diversified of North American's operations. Eyestone points out that while work on the Minuteman ICBM guidance system and the Mark II avionics system will continue to dominate Autonetics' operations, "we would like very much to increase the portion of our business in smaller programs."

Moving up. To further this aim, George W. Leisz and William F. Sauers were named division executive vice presidents. Leisz, who now has executive responsibility for products, was formerly vice president of Autonetics' navigation systems operation. Sauers, who is in charge of programs, was vice president of Autonetics' electro sensor systems unit.

The smaller programs to which Eyestone refers include Autonetics' work in astrionics, information systems, and ocean systems.

Autonetics also plans to put increasing emphasis on its microelectronics capability and will be producing more specialized integrated-circuit devices for its own products. Eyestone said the division is "studying the kind of production line we would like to set up" for production of MOS arrays.



All-silicon QSA Series: 12 models; regulation ± .005%; response time 20 μs.

New Sorensen Modular Power Supplies

The new Sorensen QSA Series offers the only modular power supply line in the 0 to 35 volt range that combines ± .005% regulation line and load, 20 μs. response time, 71°C operating temperatures, 300 μV ripple—all at prices below other lines having lesser performance specifications. Sorensen's QSA Series modules are ideal for OEM, lab or system applications. They can be used as bench models (mounted in any position) or mounted in combinations of 3 or 4 in an optional 19" (3½" high) rack adapter. Other design features include: Load current vs. temperature, 110% @ 40°C—100% @ 50°C—85% @ 60°C—66% @ 71°C • Temperature coefficient 0.01%/°C • Stability 0.025%/8 hrs. • Models QSA10-1.4, QSA10-2.2 and QSA10-3.7 permit operation of up to 20 units in series; other units permit operation of 2 units in series; All models permit operation of 4 units in parallel • No turn-on/turn-off overshoots • Remote sensing • Remote programming • Ripple voltage peak to peak 3mV. All Sorensen power sources conform to proposed NEMA standards. For additional QSA Series details or for data on other standard/custom DC power supplies, AC line regulators or frequency changers, call your local Sorensen representative, or write: Raytheon Company, Sorensen Operation, Richards Avenue, Norwalk, Conn. Tel: 203-838-6571, TWX: 710-468-2940.

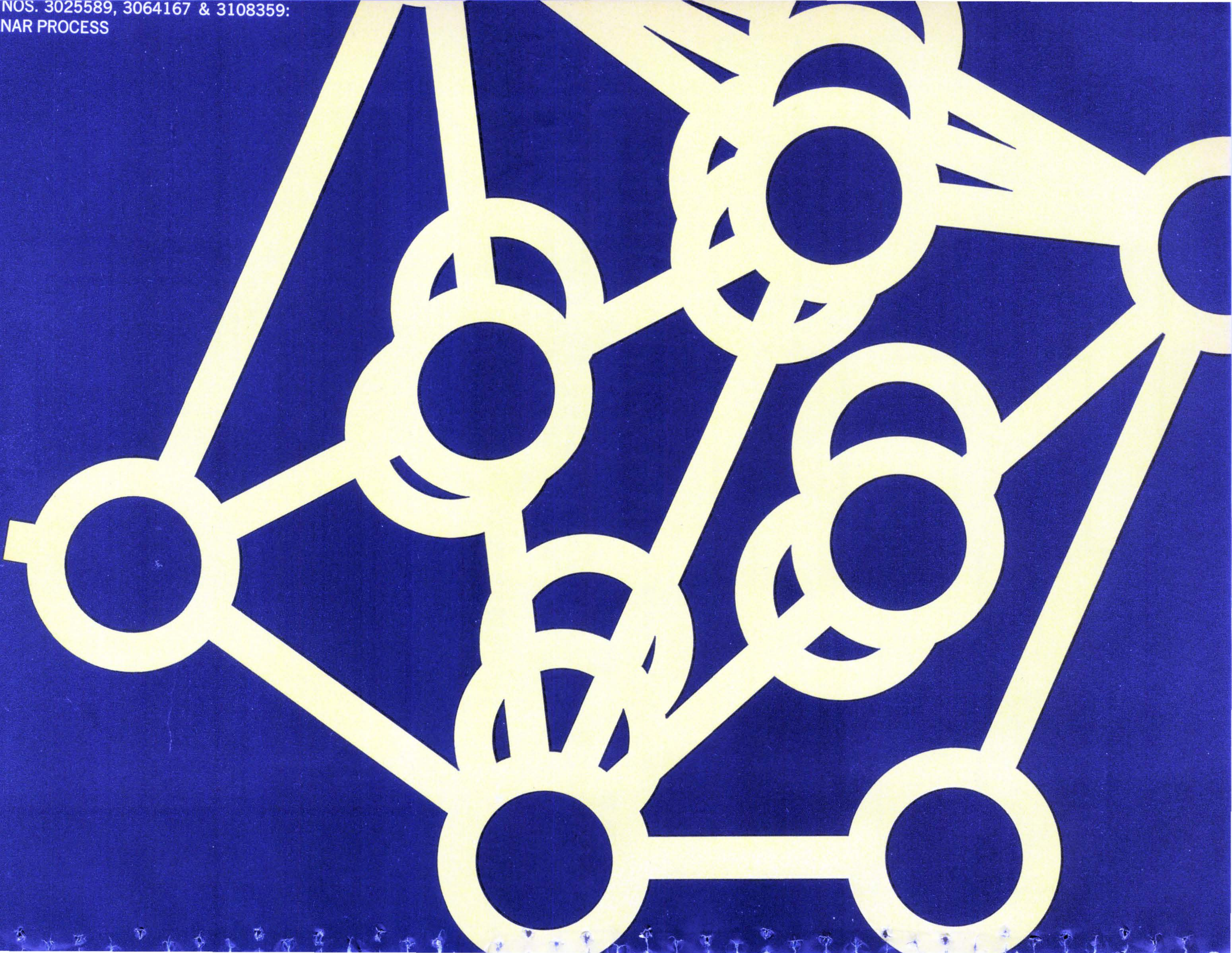
SPECIFICATIONS

MODELS (RANGES)	QSA10-1.4 (0-10V, 1.4A) QSA12-1.4 (8-14V, 1.4A) QSA18-1.1 (14-22V, 1.1A) QSA28- .7 (22-35V, .7A)	QSA10-2.2 (0-10V, 2.2A) QSA12-2.2 (8-14V, 2.2A) QSA18-2.0 (14-22V, 2.0A) QSA28-1.3 (22-35V, 1.3A)	QSA10-3.7 (0-10V, 3.7A) QSA12-3.7 (8-14V, 3.7A) QSA18-3.0 (14-22V, 3.0A) QSA28-2.0 (22-35V, 2.0A)
SIZES (IN.)	7 x 3-5/16 x 3-7/8	7 x 3-5/16 x 5-1/8	10 x 3-5/16 x 5-1/8
PRICES (U.S. List)	**$89**	**$109**	**$129**

RAYTHEON

Circle 11 on reader service card

PATENT NOS. 3025589, 3064167 & 3108359:
THE PLANAR PROCESS



Meetings

National Air Meeting on Collision Avoidance, Institute of Navigation; Dayton, Ohio, **Feb. 23-24.**

National Electric Automobile Symposium, Santa Clara Valley Engineers' Council; San Jose State College, San Jose, Calif., **Feb. 24-25.**

Electronic Industries Association Systems Effectiveness Conference, Electronic Industries Association; Statler-Hilton, Los Angeles, **Feb. 28-March 1.**

Numerical Control Society Conference, Statler Hilton Hotel, Detroit, **March 1-3.**

Particle Accelerator Conference—Accelerator Engineering and Technology, IEEE; Shoreham Hotel, Washington, **March 1-3.**

U.S. National Particle Conference, IEEE; Shoreham Hotel, Washington, **March 1-3.**

Symposium on the Effects of Radiation in Semiconductor Components, Faculte de Sciences of the University of Toulouse; Toulouse, France, **March 7-10.**

International Symposium on Residual Gases in Electron Tubes and Sorption-Desorption Phenomena in High Vacuum, Italian Society of Physics; Rome, **March 14-17.**

National Convention, Air Force Association; Hilton and St. Francis Hotels, San Francisco, **March 14-17.**

Temperature Measurements Society Conference and Exhibit, Temperature Measurements Society; Hawthorne Memorial Center, Los Angeles, **March 14-15.**

International Convention, IEEE; New York Hilton Hotel and Coliseum, **March 20-24.**

Symposium on Modern Optics, Polytechnic Institute of Brooklyn; Waldorf-Astoria Hotel, New York, **March 22-24.**

Lectures on Glass in Electronics, New York State Science of Technology Foundation; Polytechnic Institute, Troy, New York, **March 28-29.**

Photovoltaic Specialists Conference, IEEE; Sheraton Cape Colony Inn, Cocoa Beach, Fla., **March 28-30.**

Advancing Technology & Purchasing Management Workshop, Institute of Science & Technology; University of Michigan, Ann Arbor, Mich. **March 29-30.**

Structures, Structural Dynamics & Materials Meetings, American Institute of Aeronautics and Astronautics; Palm Springs, Calif., **March 29-31.**

Symposium on Microwave Power, International Microwave Power Institute; Stanford University, Stanford, Calif., **March 29-31.**

Conference on the Transport Properties of Semiconductors, Solid State Physics Committee of Institute of Physics; Canterbury, Kent, England, **March 30-31.**

International Electronic Components Show, FNIE; Porte de Versailles, Paris, **April 5-10.***

Call for papers

Instrument Society of America Conference & Exhibit, Instrument Society of America; McCormick Place, Chicago, Sept. 11-14. **March 1** is deadline for submission of abstracts to 1967 Conference Program Coordinator, Instrument Society of America, 530 William Penn Place, Pittsburgh, Pa. 15219

International Electronic Circuit Packaging Symposium, Wescon; San Francisco, Aug. 21-22. **March 15** is deadline for submission of abstracts to Papers Selection Committee, c/o Wescon, 701 Welch Rd., Palo Alto, Calif. 94304

Temperature Measurements Society Conference and Exhibit, Temperature Measurements Society; Hawthorne Memorial Center, Los Angeles, March 14-15. For further information write R.A. Finch, conference and exhibit chairman, Atomics International, P.O. Box 309, Canoga Park Calif.

Southeastern Instrument Conference, Instrument Society of America; Cocoa Beach, Fla., April 18-20. For further information write Arlie Keith, 1127 South Patrick Drive, Satellite Beach, Fla.

* Meeting preview on page 16

Is there really a choice in differential voltmeters? You bet! You can buy Fluke solid state dc, ac/dc, or true rms differential voltmeters or you can buy our vacuum tube versions. After you take a look at the brief specs of each model, it's a sure thing you won't care about anyone else's differential voltmeter (if there are any).

MODEL	INPUT VOLTAGE	ACCURACY % OF INPUT	INPUT IMPEDANCE	MAX. METER RESOLUTION	PRICE	NOTES
DC DIFFERENTIAL VOLTMETERS						
801B	0-500 VDC	±0.05%		50 uV	$ 485.00	
825A	0-500 VDC	±0.02%	Infinite at null	5 uV	$ 590.00	+$20 for rack models
821A	0-500 VDC-	±0.01%		5 uV	$ 795.00	
871A*	0-1100 VDC	±0.02%	Infinite at null	10 uV	$ 565.00	+$130.00 for
881A*	0-1100 VDC	±0.005%	to ±11V 10 Meg	1 uV	$ 825.00	rechargeable
885A*	0-1100 VDC	±0.0025%	above ± 14V	1 uV	$ 965.00	battery pack
895A*	0-1100 VDC	±0.0025%	Infinite at null to ±1100V	1 uV	$1,195.00	
AC/DC DIFFERENTIAL VOLTMETERS						
803B	0-500V AC or DC	±0.05% DC, ±0.2% AC	Infinite at null DC	50 uV	$ 875.00	
803D	0-500V AC or DC	±0.02% DC, ±0.1% AC	1 Meg, 35-50 pf AC	5 uV	$1,055.00	+$20 for rack models
823A	0-500V AC or DC	±0.01% DC, ±0.1% AC		5 uV	$1,215.00	
873A*	0-1100V AC or DC	±0.02% DC, ±0.2% AC	Infinite at null to 10	10 uV	$ 875.00	+$160.00 for
883A*	0-1100V AC or DC	±0.005% DC, ±0.1% AC	Meg above 11 VDC	1 uV	$1,215.00	rechargeable
887A*	0-1100V AC or DC	±0.0025% DC, ±0.05% AC	1 Meg, 40 pf AC	1 uV	$1,375.00	battery pack
TRUE RMS DIFFERENTIAL VOLTMETER						
931A*	0-1100V AC	±0.05% AC	1 Meg, 8 pf with BNC Input 1 Meg, 5 pf with probe	20 ppm of dial setting	$ 895.00	+$ 50.00 for permanent probe +$100.00 for rechargeable battery pack

*Solid State

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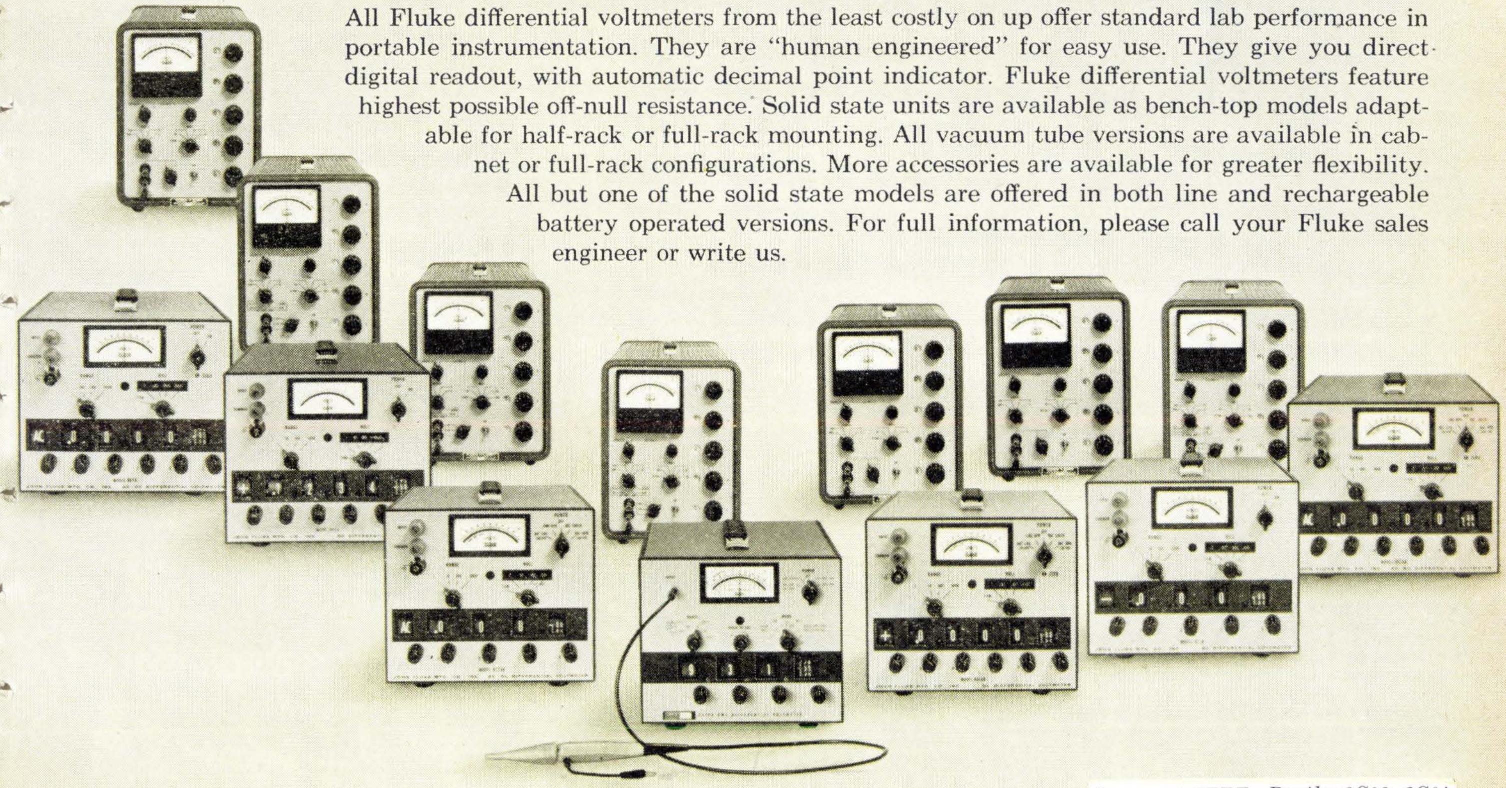
All Fluke differential voltmeters from the least costly on up offer standard lab performance in portable instrumentation. They are "human engineered" for easy use. They give you direct digital readout, with automatic decimal point indicator. Fluke differential voltmeters feature highest possible off-null resistance. Solid state units are available as bench-top models adaptable for half-rack or full-rack mounting. All vacuum tube versions are available in cabinet or full-rack configurations. More accessories are available for greater flexibility. All but one of the solid state models are offered in both line and rechargeable battery operated versions. For full information, please call your Fluke sales engineer or write us.



See us at IEEE, Booths 2C02, 2C04

Meeting preview

Semiconductors in Paris

The International Components Show in Paris, April 5-10, the continent's traditional meeting place for component companies and their customers, will demonstrate the strides European electronics companies have taken in the production of semiconductor devices.

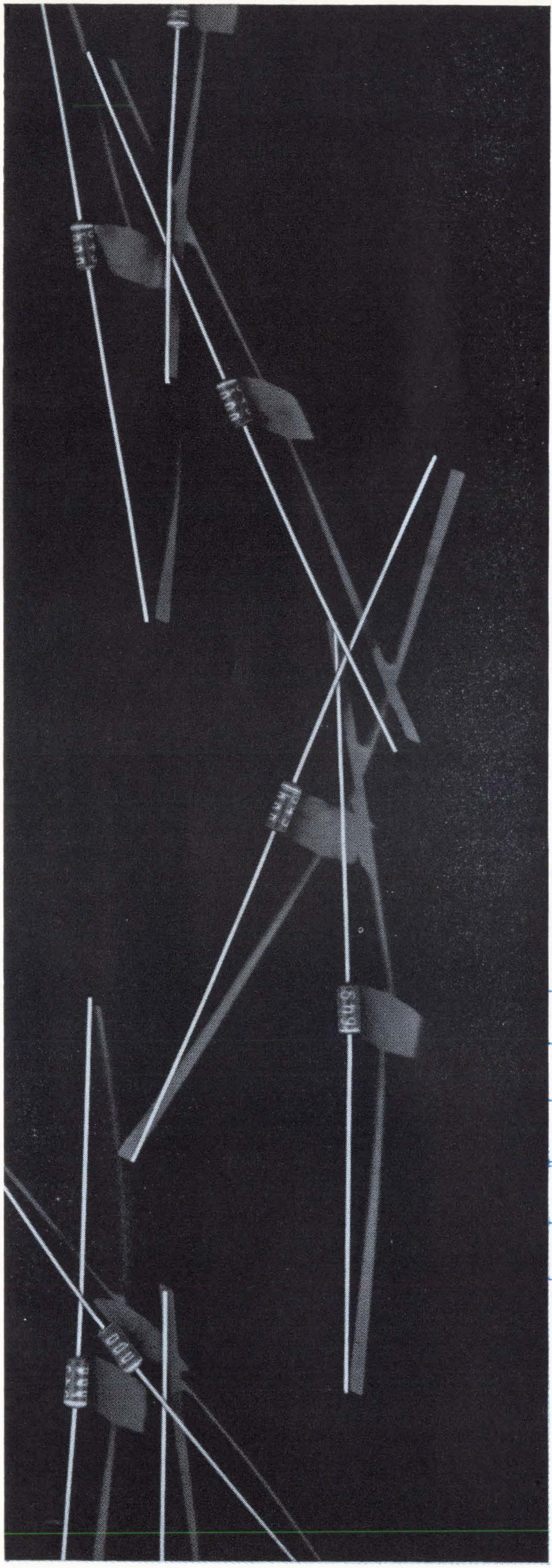
Among the market developments spurring this advance are the scheduled start of color television broadcasts in several countries next fall, the race to develop third-generation computers, and governmental demands for more sophisticated devices for space, aviation and defense.

Competition. Société Européenne des Semiconducteurs (Sesco), a joint venture of Thomson-Houston and the General Electric Co., says it will introduce a new line of power transistors for tv sets. La Radiotechnique, a Philips Gloeilampenfabrieken NV subsidiary and Thomson's top competitor in the French tv market, is also expected to unveil television components along with its rapidly evolving line of semiconductor radiation detectors.

Both Sesco and the semiconductor-producing subsidiary of CSF-Compagnie Générale de Télégraphie Sans Fil may take the wraps off the integrated circuits they are developing for an all-French third-generation computer that will be ready for delivery late next year or in early 1969.

Lineup. From elsewhere in Europe, only Elliott-Automation Ltd. of Britain has disclosed some of the items in its exhibit. Among the Elliott devices will be a range of diode-transistor-logic IC's in two-package form for commercial and military use. The company will also show a line of transistor-transistor-logic devices with propagation delays of 10 to 12 nanoseconds.

Show officials predict a strong showing by European firms struggling to close the production lead held by U.S. companies. Of the 709 exhibitors, 359 will be French electronics concerns. The U.S. will be represented by 121 companies. East Germany will be the only Eastern European exhibitor.



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Typical specifications

Forward Current I_F	Breakdown Voltage V_{BR}
20 mA min. @ V_F=1.0 V 1.0 mA min. @ V_F=0.4 V	10 V @ I_R=10 μA

Leakage Current I_R	Lifetime τ	Price
100 nA @ V_R=−5.0 V	120 ps	1 to 99, $3.00 100 to 999, $2.25

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2585

We wanted programmable logic cards for our circuit packaging system. We had to design our own.

Here's what they give you.

Modular circuit packaging

Our family of digital logic circuit cards gives you new solutions to your circuit packaging problems. With a selection of relays—wire contact, permissive-make and reed relays—and our modular circuit packaging system, you have the tools to easily breadboard new circuit designs. IBM's logic circuit packaging system handles a variety of packaging options and gives you the solution to numerous applications including data processing, digital logic testing, timing control, telemetering, and process and numerical control. We designed our packaging system to provide the kind of flexibility we needed in IBM data processing systems and to create total system economy.

Then we decided to make our flexible, low-cost packaging system even more versatile.

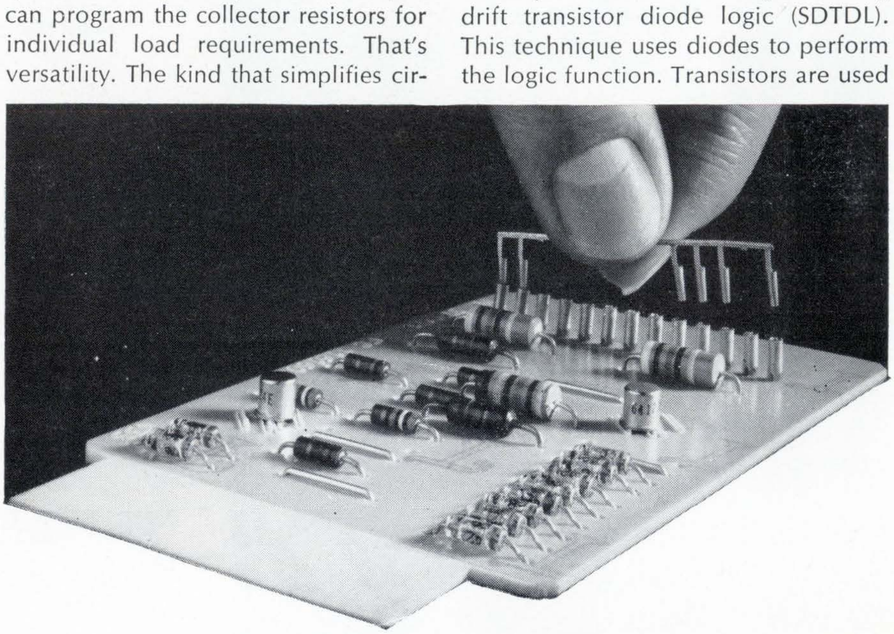
This programmable card performs the functions of many different circuit configurations. A program cap is shown being inserted to convert the card to one of those configurations.

Programmable circuit cards

To be truly versatile, a digital logic circuit card has to perform more than one function. So, when we developed our family of printed circuit cards we made five of them programmable. You can program each of these five cards to perform the functions of many different circuit configurations. You can program each of the five cards for high-speed or low-speed operation. And you can program the collector resistors for individual load requirements. That's versatility. The kind that simplifies circuit modification. Versatility that saves you the costs of in-process inventories. The kind that lets you design flexibility into your prototype designs.

SDTDL circuits

The remaining cards of the family are discrete cards acting as flip-flops, complementary emitter followers, NAND gates, AND gates, oscillators, power drivers, and single shot inverters. We developed these cards using saturating drift transistor diode logic (SDTDL). This technique uses diodes to perform the logic function. Transistors are used



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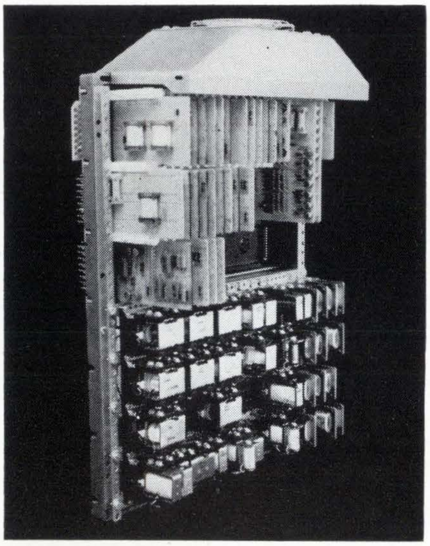
only to invert and amplify the logic output.

Performance data

Full and complete circuit data, in the most realistic terms, are supplied for each circuit and logic card. IBM Engineering Specification Sheets for all circuit configurations are available, as well as Data Sheets for each card. The engineering specifications list important data such as worst case parameters under various loading conditions, equivalent circuits, noise sensitivity, available output currents, loading equations, transient response, rise and fall curves, turn-on and turn-off delays, voltage levels and application notes.

Total packaging capability

The development of this group of digital logic circuit cards extends your overall packaging capability. With a selection of relays, programmable circuit cards, and low-cost flexibility in



packaging systems, IBM gives you the tools to simplify the problems of breadboarding your circuit designs. For the full story of simplified circuit packaging write IBM Industrial Products, 1000 Westchester Avenue, White Plains, New York 10604.

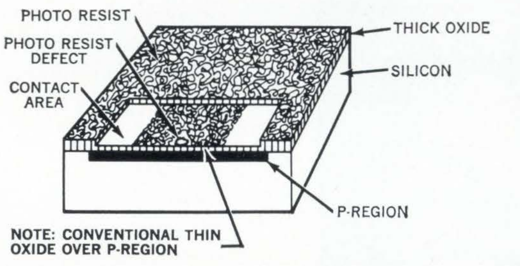
Circle 19 on reader service card

announcing...

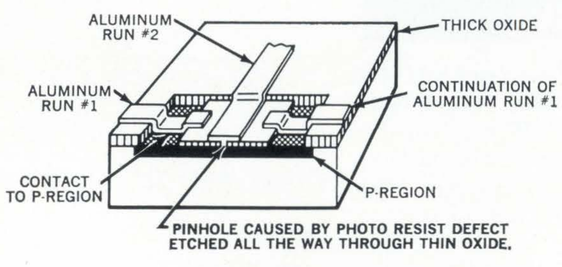
An exclusive thick-oxide process that now makes possible major progress in Large Scale Integration.

With the introduction of MTOS, Metal-Oxide-Silicon technology has now moved into the second generation of its development. This breakthrough is significant because it makes realizable major progress in Large Scale Integration through reliability and cost parameters that can now be achieved for the first time. The exclusive General Instrument MTOS (Metal-Thick-Oxide-Silicon) manufacturing process produces circuits of a substantially higher order of reliability, performance, circuit complexity and yields.

MOS PROCESS

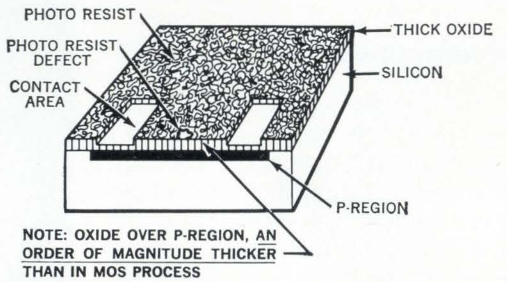


1-A. Conventional MOS crossover point prior to etching of thin oxide from contact areas. Note photo resist defect which will allow etchant to attack the oxide.

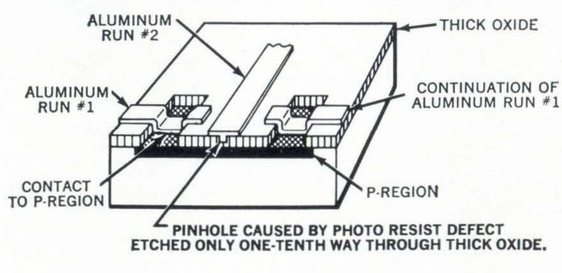


2-A. Completed conventional MOS crossover point. The pinhole in the thin oxide has caused a short-circuit between aluminum run #1 and run #2.

MTOS PROCESS



1-B. MTOS crossover point prior to etching of thin oxide from contact areas. Note photo resist defect which will allow etchant to attack the oxide.



2-B. Completed MTOS crossover point. Aluminum run #1 makes electrical contact to the conducting P-region which crosses underneath aluminum run #2. Contact is then made to the continuation of run #1. The two runs are separated by the thick oxide insulation layer.

MTOS

Second Generation MOS Technology

MTOS is a process for the manufacture of integrated circuits in which thick oxide is grown over the entire chip, except for the gate regions. The MTOS process produces an oxide layer ten times as thick over the P-regions as any other known process employed in the manufacture of MOS devices. This strengthened thick-oxide layer over the P-regions, and the sequence of steps used in the MTOS process, eliminate pinholes that could occur at crossover points, a major cause of failure in integrated circuits. Further, the thick oxide over the P-regions also minimizes the possibility of electrical short-circuits caused by the breakdown of the oxide resulting from a flaw in the oxide layer.

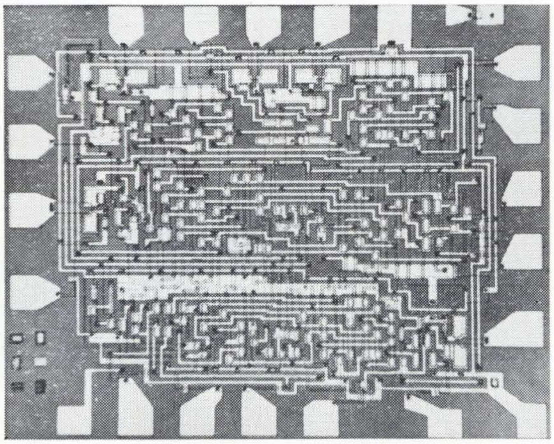


Photo above is of the MTOS Digital Differential Analyzer (MEM 5021), one example of General Instrument's LSI accomplishments (a single chip 86x70 mils contains 244 MOSFETS), and one of a complete line of MTOS ICs and single devices available from General Instrument in production quantities. Below is a listing of some of the more popular MTOS devices also available.

MEM 3050	Dual 25-Bit Shift Register	MEM 2008	Series Shunt Chopper
MEM 3021/3021B	21-Bit Shift Register	MEM 1008	Dual Exclusive OR/NOT Gate
MEM 3020	20-Bit Shift Register	MEM 1005	R̄-S̄-T Flip-Flop
MEM 3016-2	Dual 16-Bit Shift Register	MEM 1002	Dual 3-Input NOR-Gate
MEM 3012 SP.	12-Bit Serial In/Parallel Out Shift Register	MEM 1000	Dual Full Adders
MEM 3008 PS.	8-Bit Parallel In/Serial Out Shift Register	MEM 551, MEM 550	Dual P-Channel MOSFETS
MEM 2009	6-Channel Multiplexer	MEM 520, MEM 517/517A, MEM 511, 2N4353	P-Channel MOSFETS

Parametric enhancement is an additional benefit accruing to the user due to the MTOS process. Crossovers occuring over the thick oxide reduce stray capacitance, thereby offering higher frequency performance and faster switching speeds.

The inherently higher yields resulting from the thick-oxide process will reduce the cost per function to the user as well as offer greater complexity per chip area.

This advance in the art of MOS processing creates not only new standards of reliability, performance, circuit complexity and product availability, but is also of prime importance to the position of leadership held by General Instrument in the technology of Large Scale Integration.

MTOS devices are in stock and immediately available from your authorized General Instrument Distributor.

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The PDP-8/S offers security. Security in change. It is priced lower than many special purpose machines. More than 300 have been sold in the past three months. And chances are still good that your competition hasn't even looked into it. Why don't you.

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Editorial

A 'No' vote on Nike X

One of the controversial issues Congress will be tackling soon is whether the U.S. should start production of Nike X, the antimissile defense system. Although the weight of emotional arguments and public opinion tends to sway one toward believing this defense system should be built—after all, the Russians are building one —the cold, hard facts say no. Electronics magazine has rarely agreed with Defense Secretary Robert S. McNamara and seldom approved of his conduct, but it does support his stand on Nike X wholeheartedly. He, of course, has ruled "No production."

It is tempting to sit back and realize that even a sparsely deployed Nike X system would pump anywhere from $3 billion to $8 billion into the economy, while full deployment might inject as much as $40-billion. And the electronics industry would be one of the chief beneficiaries. But if the electronics industry cannot prosper without that kind of Government handout, it would be better off out of business. In fact, such expenditures could seriously cripple the economy by overheating it, thus hurting electronics companies as much as helping them.

There are good diplomatic reasons for not building Nike X installations now. The current attempt to persuade the Russians to hold off building such a system is only one. Then too, it seems clear that a Nike X system will not halt the spread of nuclear weapons or lessen the chances of nuclear war.

There is a good and fundamental tactical reason for not building Nike X, too: it won't be effective against the newest warheads and missiles. In atomic war, unhappily, half-measures in defense are as good as none.

But probably the most rational reason for delaying production of Nike X is technical. The system currently proposed is obsolete, having been designed five years ago. Technological advances made since could vastly improve it. Great strides have been made in understanding and designing phased-array radars since the pioneering work was done on the one for Nike X. Integrated electronics for microwaves will be in production within 18 months. And large-scale integration could lead to smaller, faster and cheaper computers for the system within the same time. With these improvements, the antimissile system could be more effective, faster reacting and cheaper. With them, it might even be possible to install a saturation system, if diplomacy breaks down, without bankrupting the economy.

Managers will tell you that engineers are never satisfied with a design and are never ready to release it to production. The complaint frequently has merit, but it shouldn't be applied to the improvement of Nike X. Today's antimissile system is comparable to the Army's old Jupiter, the first long-range (1,200 miles) missile. The Jupiter's liquid fuel made it unwieldy to fire and inaccurate compared to the solid-fueled Minuteman missile that followed it. With IC computers and hard launching sites, Minuteman has revolutioned the strategy of atomic warfare. A truly modern antimissile system would represent an even greater improvement over Nike X.

Nike X is the kind of system that can't be improved by adding bits of new hardware piecemeal. Rationality pleads that its deployment be held off until an up-to-date system is designed. Thus, rather than starting production of Nike X now, the Defense Department should accelerate development in those technical areas that will lead to a more efficient, more effective and cheaper system.

Typical day at an airline

Airlines continue to ignore modern electronics technology, Electronics has said pointedly before on this page [Sept. 19, 1966 and Nov. 14, 1966]. Airline executives, happily oblivious to what's happening in this field, are content to buy electronic systems so they can advertise them rather than use them seriously.

American Airlines, which has had more than its share of disappointments with its computer reservation system, exhibited this type of myopia when it ran a seven-column—nearly a full page —advertisement in New York newspapers on Wednesday and Thursday, Feb. 8 and 9.

"Yesterday was a typical day," the ad proclaimed, "and we filled 35,000 seats with 35,000 people. To do that without making one little mistake, we'd have had to use a computer. We did. Its name is Sabre . . ."

Typical day? An air passenger would hope not. This "yesterday" was the day a blizzard paralyzed the northeastern portion of the United States, canceling a large portion of American's and other lines' flights and all of American's service into Boston, New York and Washington. New York's three airports, for example, were closed for over 25 hours. The result: most flights cancelled; others rerouted to unwanted destinations; still others days late; reservations chaotic; check-in-lines winding serpentinely back and forth in front of counters. Maybe that *is* a typical day at American Airlines.

←Circle 22 on reader service card

Bourns Introduces INFINITRON™-Element 10-Turn Precision Potentiometers*

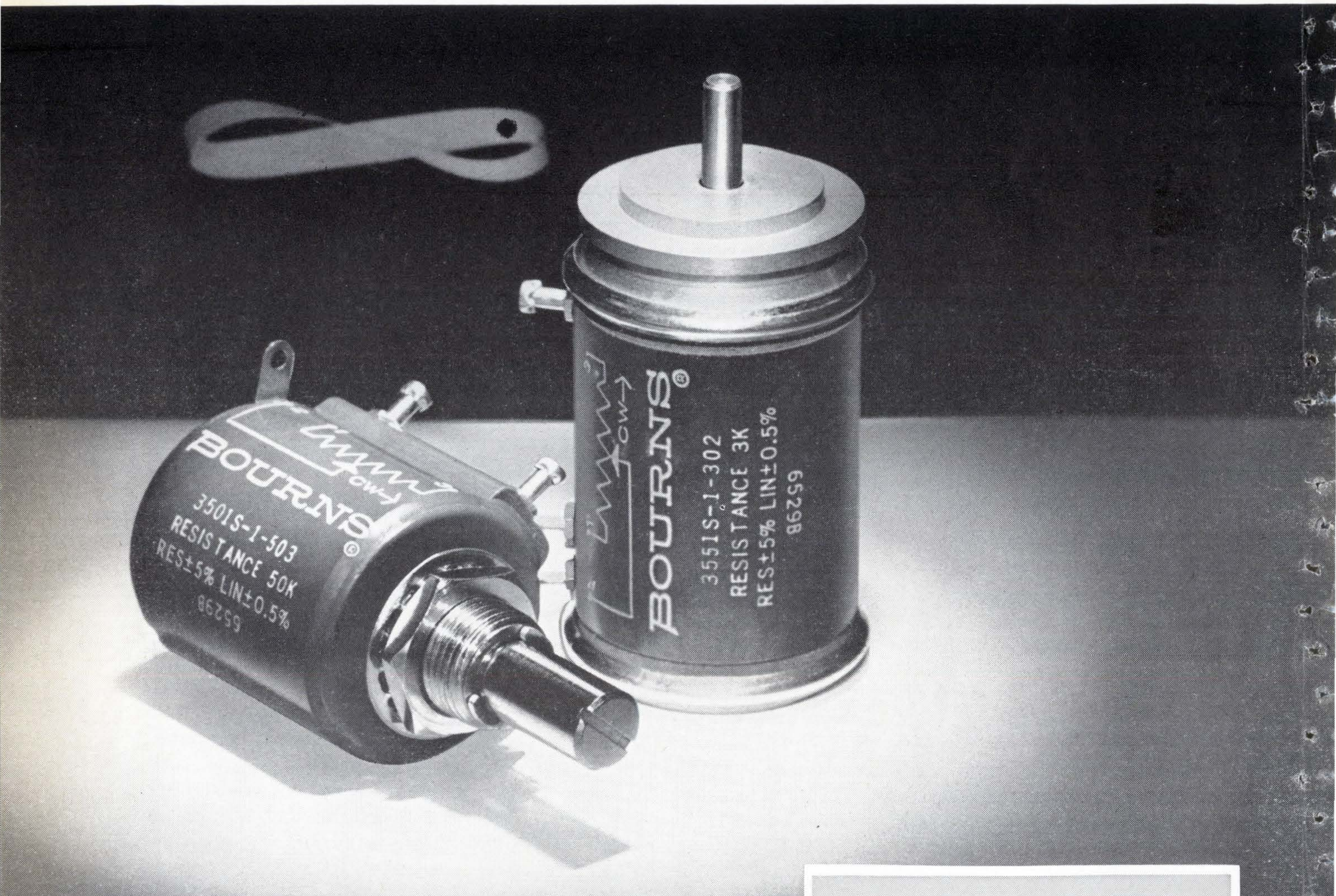
Here at last are multi-turn precision potentiometers that offer long life and essentially infinite resolution without asking you to compromise on your specifications. Noise in Bourns INFINITRON-element units is so low you can test them as if they were wirewounds. You don't have to hook up special filter circuits or contrive "output smoothness" tests. No need, either, to limit these potentiometers to voltage-divider applications or to guess where the resistance element starts and ends. Precise end-points make our linearity specification a reality in your circuits.

Convince yourself of the higher performance that Bourns INFINITRON-element 10-turn potentiometers can bring to your designs. Write today for product information and actual test data.

STANDARD SPECIFICATIONS
⅞" Diameter, 10-Turn, Bushing-Mount Model 3501
⅞" Diameter, 10-Turn, Servo-Mount Model 3551

Noise Performance:	100 ohms or 1% of total resistance, whichever is greater
Humidity Performance:	MIL-STD-202, Method 103
Independent Linearity:	±0.5%
Temperature Coefficient, All Resistances:	±300 PPM/°C
Total Resistance Tolerance:	±5%
Rotational Life:	Model 3501: 4,000,000 shaft revolutions Model 3551: 10,000,000 shaft revolutions
End Resistance:	1 ohm or .1% max., whichever is greater
Electrical Rotation:	3600° (+10°/−2°)
Power Rating:	2 watts at 70°C
Operating Temperature Range:	−65°C to +125°C
Environmental Stability:	Resistance shift < 5%
Approximate Weight:	1 oz.
Resistance Range:	1K to 500K
Price, 1-9 pieces:	Model 3501 (Bushing Mount): $14.00 Model 3551 (Servo Mount): $30.00

Long-life, ball-bearing shaft supports, standard in the servo-mount model, are also available in the bushing-mount unit.



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Electronics Newsletter

February 20, 1967

King-size pack for IC arrays

Fairchild Semiconductor plans to continue its "think big" approach to integrated-circuit packages **when it starts selling large-scale arrays of up to 200 circuits in a jumbo version of the popular dual in-line package.**

The standard dual-in-line package lead spacing of 0.1 inch (100 mils) will be retained, but each package will have 50 leads—25 on each side—instead of the usual 14. The package will be about 2½ inches long, instead of ¾ inch, and about 1 inch wide instead of 0.3 inch. **The 1-inch spacing between lead rows will allow up to 50 printed circuit interconnections to run between the lead rows when the packages are plugged into circuit boards.**

Rex Rice, the man responsible for keeping Fairchild IC packaging in tune with upcoming digital systems designs, says the package will permit building large digital systems without using multilayer circuit boards. He estimates system designers will be able to interconnect an average of 150 circuits per array with the 50-lead packages and double-sided circuit boards. **Rice calculates that up to 21,000 circuits can be interconnected in a volume of 702 cubic inches.** He recommends system packaging ground rules similar to those he worked out for the original dual in-line packages [Electronics, Feb. 7, 1966, p. 109].

Air Force seeks control towers

The Air Force has defined its needs for helicopter-transportable air traffic control towers **and will request bids this week on 22 of them to be used by the Tactical Air Command.** This will be the first production procurement of the towers. The request for proposals will come from the Electronic Systems division, with initial procurement—expected to reach $5 million—by the 407L program office at Hanscom Field, Mass.

The towers, designated TSW-7, will be the outgrowth of the TSW-6 tower developed for the Air Force by the Radio Corp. of America, which has been undergoing tactical field tests. Chu Associates, Harvard, Mass., is modifying the RCA version, incorporating a single mast for the various antennas.

AT&T to test compact radio telephones

Compact radio telephones will be field tested later this year in the Houston and Phoenix areas by the American Telephone and Telegraph Co. The "lineless" phones look like oversize Trimline handsets with an antenna. **Bell Telephone Laboratories, AT&T's research arm, is at work to further reduce the size of the portable units by designing integrated circuitry for them.**

Real-time tv from outer space?

Real-time television picture transmission from other planets is the goal of tests on a laser space-to-earth communications system at NASA's Goddard Space Flight Center.

The 20-watt carbon dioxide laser, built under a $100,000 contract by Sylvania Electric Products Inc., a subsidiary of the General Telephone & Electronics Corp., transmits data at 10^6 bits per second. At the present 8 bits-per-second transmission speed, on a narrow bandwidth, it took eight days to send pictures from Mars to earth.

Use of the CO_2 laser, which has a wavelength of 10 microns, overcomes one problem of a laser system, attenuation, by providing a window in the atmosphere. Another problem, that of cloud cover, hasn't been tackled but NASA says several solutions are available. Signals could be relayed by earth-orbiting satellites, sent to stations in cloud-free areas, or the data could be stored and sent when the clouds disappear.

In the tests at Goddard, coherent light is bounced off passive satellites, such as Echo 2, and received at Goddard.

Administration readies patent reform bill

The Johnson Administration's forthcoming bill aimed at modernizing the 129-year-old patent system **is generally backed by the electronics industry but is already under attack from powerful lobbies.**

The American Society of Inventors and the Patent Law Association oppose some of the 35 recommendations offered by a Presidential commission appointed to study the system.

Electronics companies support nearly all the proposals—especially those that would speed patent processing. **Some companies, however, criticize the first-to-file proposal, which would grant ownership to the first company applying.** They claim this would start a race to the patent office before an invention is developed and would penalize a company that invested heavily in time and money to develop a workable device. Other companies favor it, saying it would eliminate litigation over patent rights.

Another commission recommendation would drop all computer programs from patent consideration. Currently, programs can be copyrighted.

Broken-up memory slated for Illiac 4

Individual small memories instead of the single large capacity memory that was originally planned, will be built for each of the 256 processors in the University of Illinois' Illiac 4 computer. **The Burroughs Corp. will design and fabricate a thin-film memory containing more than 2,000 64-bit words and operating at a cycle time of 250 nanoseconds for each processor.** Originally one memory containing many 512-bit words was to serve all the processors simultaneously [Electronics, April 4, 1966, p. 36].

Contract negotiations are under way between Burroughs and the University's digital computer laboratory for the entire system; the contract is to be signed in four to six weeks. **For logic circuitry in the giant system, Texas Instruments Incorporated will make large-scale integrated circuits to Burroughs' specifications.** As high a level of integration as possible will be used in the completed system, according to Daniel L. Slotnick, project director at Illinois. The project is sponsored by the Advanced Research Projects Agency of the Department of Defense.

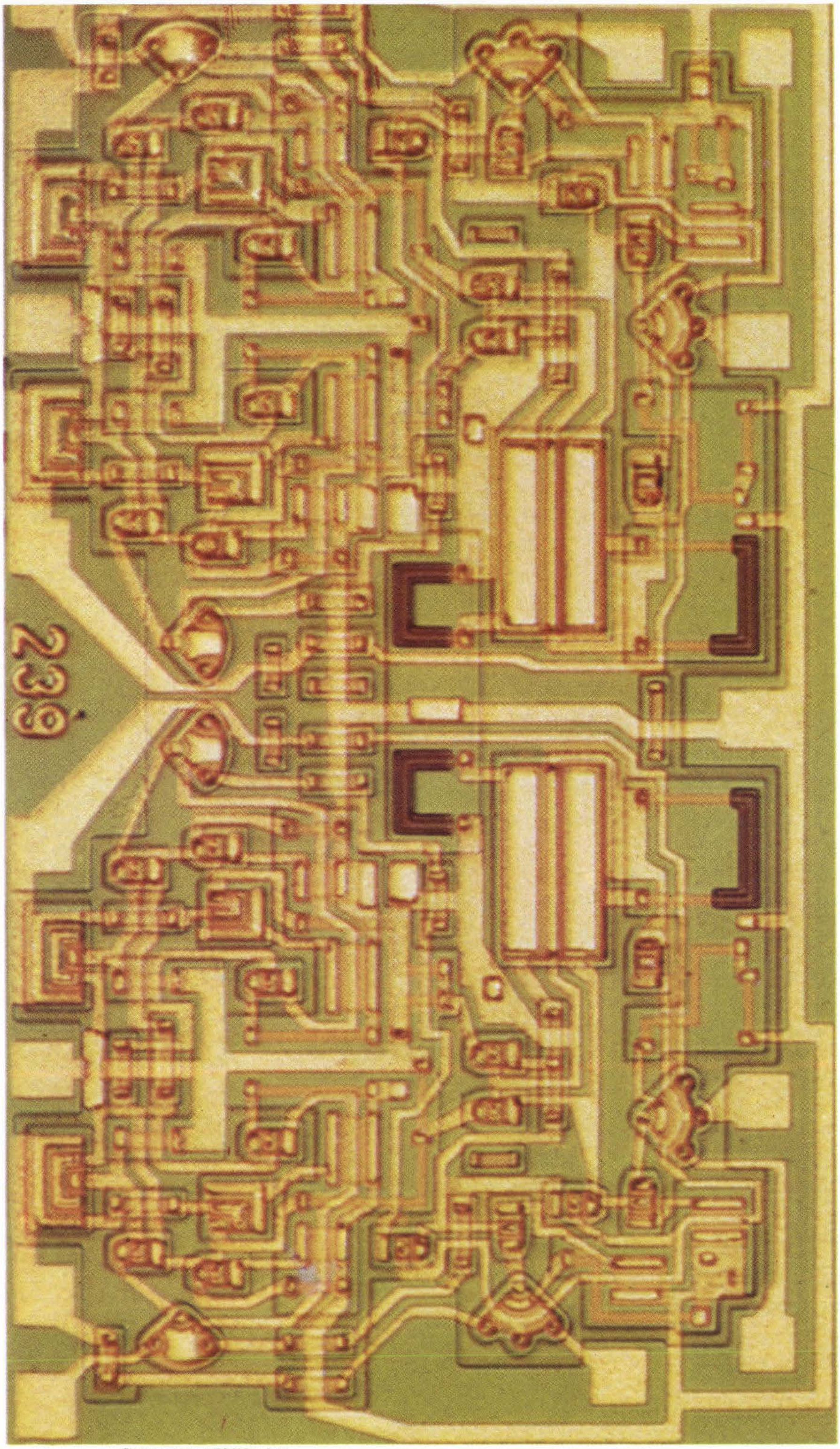
FAA evaluating superbright radar display

A radar display with a brightness of 1,200 foot-lamberts is being tested at airports in Atlanta and Washington where control tower personnel have difficulty seeing conventional displays rated at 50 to 100 foot-lamberts. The system, consisting of a monitor with a 5-inch cathode-ray tube and a television camera, was developed by the Federal Aviation Agency's experimental center in Atlantic City, N. J. Brightness is achieved by using a P-31 phosphor made from zinc, sulfur and copper on the tube, and by higher voltage—22,000 volts compared with 15,000—than is used with present radar display crt's.

Integrated Circuit IDEAS

SYLVANIA
Electronic Components Group

Build binary counters with fast (to 50 MHz) J-Ks



Sylvania's 50MHz J-K

Whether it's ripple or synchronous binary counting, Sylvania has the right J-K flip-flop. Ten types (single and dual) go to 50 MHz.

Flexibility provides the optimum design! That's the best description of how the wide range of J-K flip-flops available from Sylvania can solve your binary counting problems. Here's how two techniques, ripple and synchronous counting, can be implemented with Sylvania's J-Ks to get rates of 5.5, 7.5, 14, 15, 18, 25, 38 MHz in a binary counter.

Ripple type binary counters are sequential in nature: the designated clock pulse drives the first stage flip-flop with each subsequent stage being driven in turn by the preceding flip-flop. As seen in Figure 1, at the 8th clock pulse, the 4th flip-flop settles at a time $t_1 + t_2 + t_3 + t_4$ after the initial clock pulse. Also note, it is possible that the 4th stage flip-flop might not be settled before clock pulse #9 occurs.

The speed of a ripple counter, however, is limited because decoding can't begin until the last flip-flop in the counter has settled down. As a result, the maximum frequency is:

$$f_{max} = \frac{1}{\text{clock width} + t_1 + t_2 + t_3 + t_4}$$

For Figure 1, SUHL J-K flip-flops would be capable of the following typical decoding rates:

$$\text{SF-50 (20MHz)} = \frac{1}{35\text{ns} + (4\text{bits} \times 37\text{ns})} = 5.5\text{MHz}$$

$$\text{SF-250 (30MHz)} = \frac{1}{30\text{ns} + (4\text{bits} \times 25\text{ns})} = 7.5\text{MHz}$$

$$\text{SF-200 (50MHz)} = \frac{1}{12\text{ns} + (4\text{bits} \times 14\text{ns})} = 15\text{MHz}$$

(Continued on next page)

The semi-ripple counter in Figure 2 shows how SUHL SF-110 and 130 series dual J-K flip-flops can be used to obtain even higher decoding rates:

$$\text{SF-110, 130} = \frac{1}{[12\text{ns} + (4\text{bits} \times 14\text{ns}/2)]} = 25\text{MHz}$$

High-speed applications invariably call for synchronous binary counters. In a synchronous counter each flip-flop is triggered simultaneously and is driven separately by the clock. Therefore, all the counter's outputs occur simultaneously. This type counter must be designed so that each flip-flop is properly set ahead of clock time in order that the proper output appears when triggered by the clock. Therefore, each flip-flop must have a gate stage at its input end to set the flip-flop for triggering.

Figure 3 shows a four-bit synchronous binary counter using SUHL flip-flops which have input gate structures. Each flip-flop has the output of all previous flip-flops fed into its J and K terminals. The maximum time at any clock pulse is t_1. All outputs appear simultaneously and reading or decoding can be performed in t_1 nanoseconds after the clock trigger. Maximum frequency is: $f_{max} = \frac{1}{(\text{Clock width} + t_1)}$.

Typical SUHL J-K flip-flops would be capable of:

$$\text{SF-50 (20MHz)} = \frac{1}{(35\text{ns} + 37\text{ns})} = 14\text{MHz}$$

$$\text{*SF-250 (30MHz)} = \frac{1}{(30\text{ns} + 25\text{ns})} = 18\text{MHz}$$

$$\text{SF-200 (50MHz)} = \frac{1}{(12\text{ns} + 14\text{ns})} = 38\text{MHz}$$

With synchronous counters, the number of inputs increases as the number of bits increases. For example, a 5-bit synchronous counter requires 4 inputs at the last flip-flop stage and a 10-bit counter requires 9 inputs at the last flip-flop stage.

Figure 4 shows a synchronous counter greater than 4-bits in length. It is completely synchronous. Using SUHL J-K flip-flops, this counter can operate at:

SF-50 with SUHL I gates = 11.0 MHz
SF-250 with SUHL II gates = 13.5 MHz
SF-200 with SUHL II gates = 22.0 MHz

*For new designs, the SF-200, SF-210 series are recommended replacements for the SF-250, SF-260 series.

CIRCLE NUMBER 300

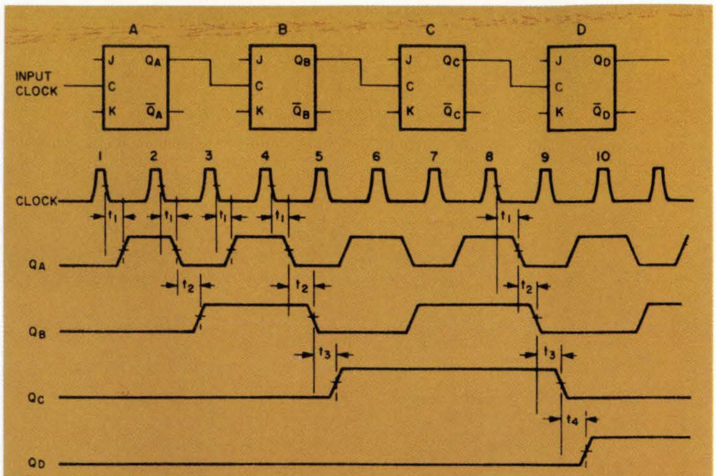


Fig. 1. Ripple Counter

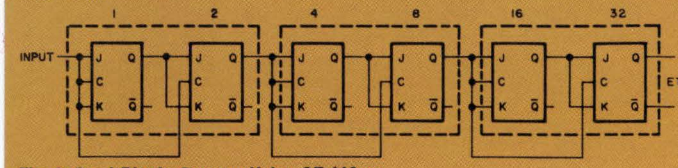


Fig. 2. Semi-Ripple Counter Using SF-110 or SF-130 Dual J-K F-F with Common Clock

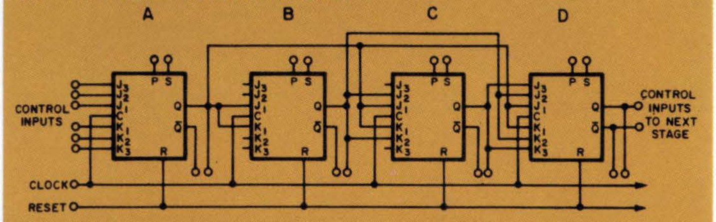


Fig. 3. Synchronous Binary Counter

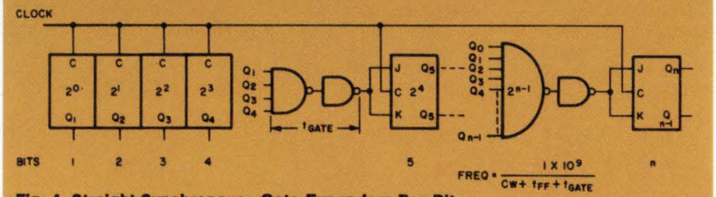


Fig. 4. Straight Synchronous—Gate Expanders Per Bit

100 MHz wideband amplifiers for video and pulse applications

Sylvania's high-performance, three-stage, direct-coupled linear amplifiers have low output, high signal voltage outputs, and excellent linearity.

While configurations of Sylvania's SA-20 and SA-21 wideband amplifiers are the same, the SA-20 is for applications requiring higher signal swing and tighter performance tolerances. Here's how you can use them.

Figure 1 shows the circuit diagram for the SA-20 series amplifier. Negative feedback is applied from output stage to first stage emitter through the divider consisting of R_4 and R_6. Typical voltage gain of the device is 21 db. An external capacitor connected from the collector to base of Q_2 provides local high-frequency feedback. This feedback shapes the roll-off of gain at high frequencies. Values ranging from 2.5 to 5.0 pF normally give the most uniform high-frequency response.

Tests with resistive loads show that a feedback capacitance (C_f) of 3.6 pF gives a voltage gain essentially constant to 50 MHz. Gain is down 3 db at frequencies approaching 100 MHz. Increasing C_f to 6.5 pF reduces the −3 db frequency by 30 to 50 MHz.

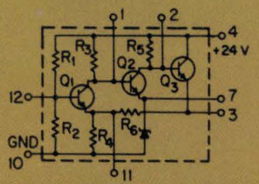


Fig. 1. Sylvania Wideband Linear Amplifier

SA-20 Typical Electrical Characteristics

Power Supply	+24 volts
Voltage Gain	21 db
Input Impedance	1.6K
Output Impedance	5 ohms
Max. Output Voltage Swing	14 volts p-to-p
3 db Frequency Response	100 mc: 17 db 30 mc: 20 db
2nd order Intermodulation Product, Po = 0 dbm	−65 db
3rd order Intermodulation Product, Po = 0 dbm	−75 db

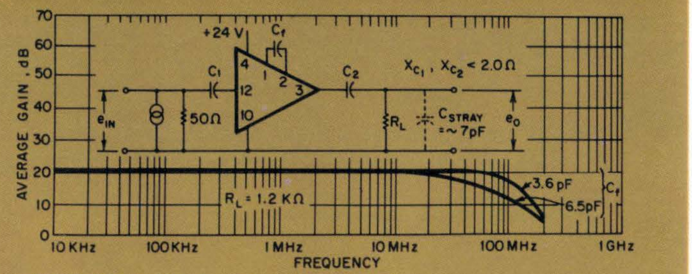


Fig 2. SA-20 Typical Gain vs. Frequency

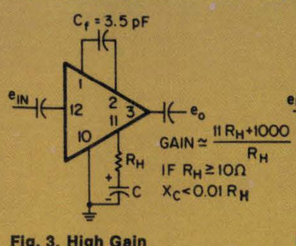


Fig. 3. High Gain Configuration

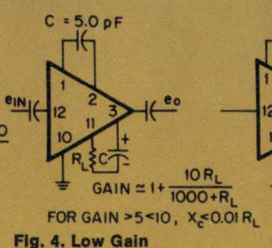


Fig. 4. Low Gain Configuration

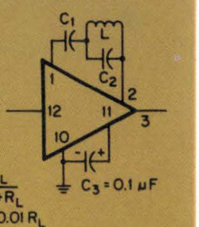


Fig. 5. Selective Amplifier

Figure 2 shows how the voltage gain varies with frequency.

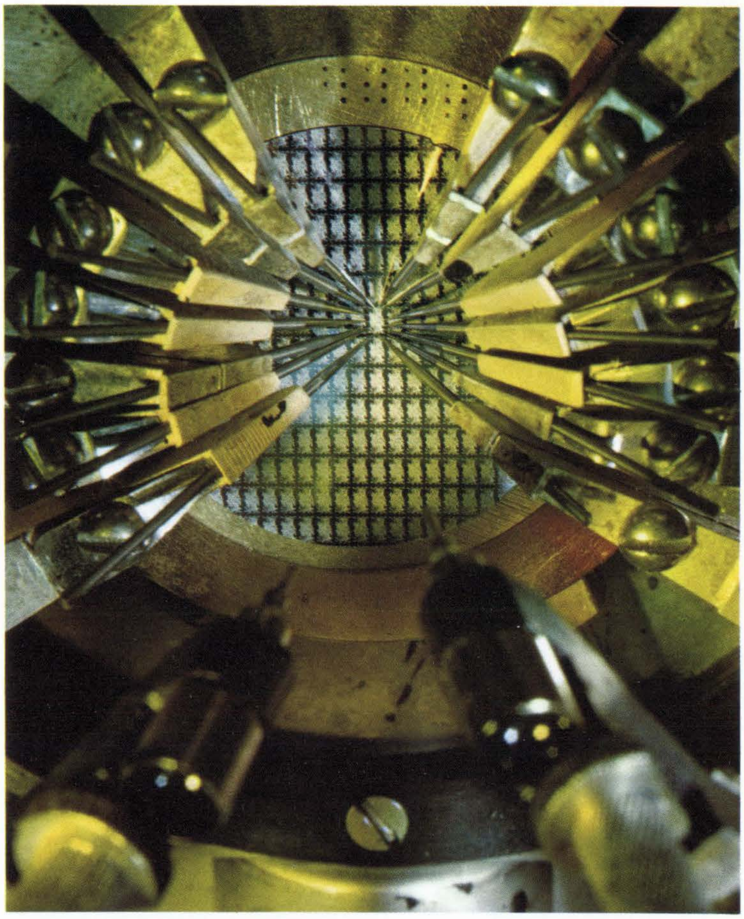
Amplifier gain can be changed by resistive shunting of feedback resistors (Figures 3 and 4). It is necessary to connect a dc blocking capacitor in series with the external resistor to prevent shifting of the normal quiescent voltages.

Maximum amplifier gain is realized when all forms of feedback are removed. This is done by not connecting a feedback capacitor between base and collector of Q_2 and by bypassing the emitter resistor of Q_1. In this configuration, the amplifier has a typical voltage gain of 60 db and a −3 db gain frequency of about 4.5 MHz with an R_L of 1.2K.

Connecting the circuit as shown in Figure 5 gives bandpass characteristics. Voltage gain at the resonant frequency of L and C_2 approaches the gain realized in the maximum gain configuration. Capacitor C_1 blocks dc and should be large enough to prevent series resonance with inductor L. A notch characteristic is obtained when C_2 is removed and L and C_1 are series resonant. Selectivity of bandpass and notch circuits can be improved by replacing the tuned circuits with piezoelectric crystals. CIRCLE NUMBER 301

Reliability: engineering superior circuits with superior packages

In short, the reliability of integrated circuits depends on how well the circuit chip is made and how well it is packaged.



Mechanized wafer-level dc testing

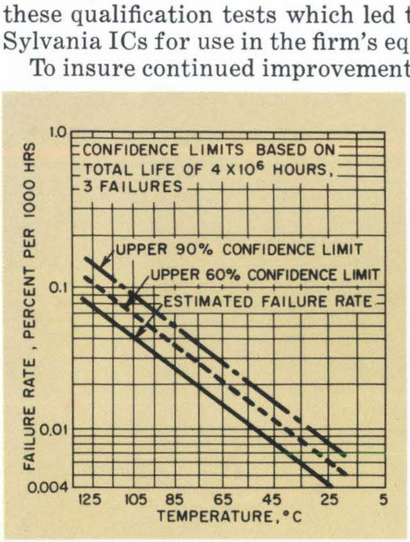
Sylvania's integrated circuit Quality Assurance and Reliability Department recently completed evaluation of data compiled on 400 four-input NAND gates after 10,000 hours of life test (a total of 4 million component hours). Failure rate was a low 0.009% per 1,000 hours at 25° C.

The circuits tested were basic SUHL four-input NAND gates produced throughout 1964 and early 1965. Thus, they do not represent the improved products made since either the completion of Sylvania's new facilities, or the introduction of newer integrated circuit processing improvements. The improved devices are now undergoing life tests.

The NAND gates were life tested in the ring counter configuration. Life test sockets were placed in an oven where ambient temperature was maintained at 125° C. The graph relates failure rates and confidence limits to temperature.

Sylvania's in-house life and performance tests are supplemented by users' testing programs. A leading manufacturer of aerospace equipment recently completed an extensive testing of Sylvania's TO-85 packaged ICs. The manufacturer performed these key tests per MIL-STD 750 and 202 on SUHL devices and their packages: (1) 10-day JAN moisture resistance, (2) Radiflo leak test, (3) Shock, (4) Centrifuge, (5) Vibration fatigue, (6) Vibration-variable frequency (7) Lead fatigue, (8) Lead bending, (9) Salt atmosphere, (10) Storage life at 150° C, and (11) Operating life at 125° C. The package passed these qualification tests which led to the selection of Sylvania ICs for use in the firm's equipment.

To insure continued improvement in reliability and maintain product quality levels, Sylvania has an extensive quality assurance test program. In addition to in-process testing of wafers, all Sylvania integrated circuits also go through a sequence of reliability tests after being sealed in packages. These tests insure that both the actual circuit and the package maintain their integrity.



Each IC first goes through five cycles of −65° C to +200° C cycling with a fifteen-minute soak time at each temperature extreme. A 20,000 G centrifuge test, while units are in the Y_1 plane, insures that the wire bonds are properly connected. Bubble-testing in 150° C glycerine points out leaks which may have resulted from the first two tests or from previous processing.

Next, units are baked at 300° C for 48 to 60 hours to stabilize them. Then all circuits must meet worst-case tests at the temperature extremes guaranteed in addition to all parameters called for on the Sylvania data sheet or in the customer's qualifications. Electrical capability of each IC is tested at 75° C, 125° C, −55° C and 0° C for dc parameters.

Finally, each unit is tested for all switching characteristics at 25° C. This is done by Sylvania's fully automatic test equipment at the rate of one circuit every two seconds. Only at this point is differentiation made between military and industrial capability.

This 100% testing program is in addition to extensive tests of random samples from each lot of circuits. These samples are subjected to electrical, environmental and life testing. CIRCLE NUMBER 302

SUHL I & II, the most efficient, most complete TTL lines

SUHL ICs are high-level TTL units and more. Designers get flexibility from a wide variety of functions without sacrificing performance.

Sylvania's IC pioneering has led to the highest quality and most complete lines of high-level TTL ICs in the industry. With each of 41 separate functions now available in four different versions (for a total of 164 types), SUHL I and II represent the largest high-level TTL lines on the market.

SUHL units combine propagation delay times as low as 6 nanoseconds with high noise margin, high logic swing, high fan-out, low power and high capacitance drive capability (see Table).

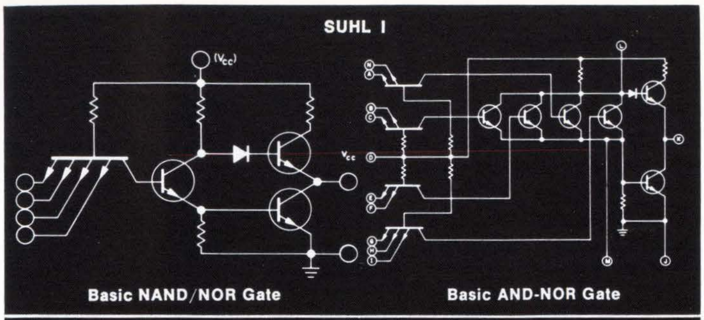
Advantages of SUHL integrated circuits are not limited to electrical performance characteristics. Because Sylvania provides more logic per package, you can build a computer, or other digital equipment, with 25% less packages. The savings in system cost which result from lower package count are not eaten up in higher initial costs because SUHL units are competitively priced.

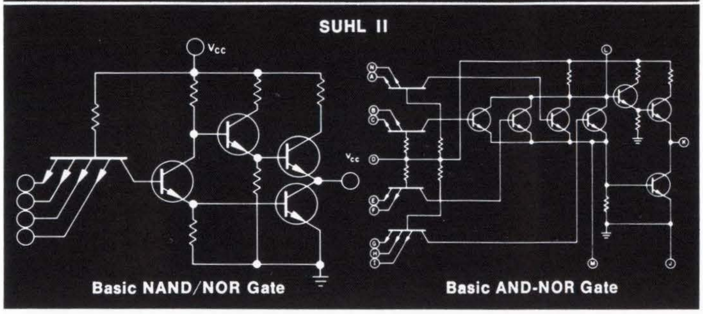
Sylvania's head start in TTL integrated circuit de-

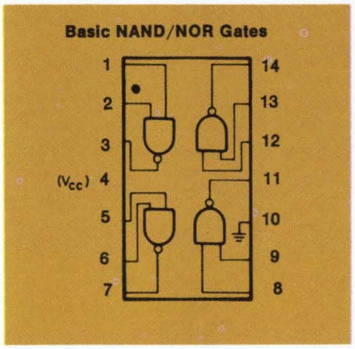
SUHL I TYPICAL CHARACTERISTICS (+25°C, +5.0 Volts)

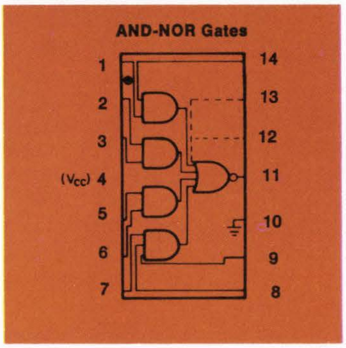
Function	Type Nos.	t_{pd} (nsec)	Avg. Power (mw)	Noise Immunity +(volts)	−	**Military (−55°C to +125°C) Prime FO	Std. FO	**Industrial (0°C to +75°C) Prime FO	Std. FO
NAND/NOR Gates									
Dual 4-Input NAND/NOR Gate	SG-40, SG-41, SG-42, SG-43	10	15	1.1	1.5	15	7	12	6
Single 8-Input NAND/NOR Gate	SG-60, SG-61, SG-62, SG-63	12	15	1.1	1.5	15	7	12	6
Expandable Single 8-Input NAND/NOR Gate	SG-120, SG-121, SG-122, SG-123	18	15	1.1	1.5	15	7	12	6
Dual 4-Input Line Driver	SG-130, SG-131, SG-132, SG-133	25	30	1.1	1.5	30	15	24	12
Quad 2-Input NAND/NOR Gate	SG-140, SG-141, SG-142, SG-143	10	15	1.1	1.5	15	7	12	6
Triple 2-Input Bus Driver	SG-160, SG-161, SG-162, SG-163	15	15	1.1	1.5	15	7	12	6
Triple 3-Input NAND/NOR Gate	SG-190, SG-191, SG-192, SG-193	10	15	1.1	1.5	15	7	12	6
AND-NOR Gates									
Expandable Quad 2-Input OR Gate	SG-50, SG-51, SG-52, SG-53	12	30	1.1	1.5	15	7	12	6
Expandable Dual Output, Dual 2-Input OR Gate	SG-70, SG-71, SG-72, SG-73	12	20/gate	1.1	1.5	15	7	12	6
Exclusive-OR with Complement	SG-90, SG-91, SG-92, SG-93	11	35	1.1	1.5	15	7	12	6
Expandable Triple 3-Input OR Gate	SG-100, SG-101, SG-102, SG-103	12	25	1.1	1.5	15	7	12	6
Expandable Dual 4-Input OR Gate	SG-110, SG-111, SG-112, SG-113	12	20	1.1	1.5	15	7	12	6
Non-Inverting Gates									
Dual Pulse Shaper/Delay-AND Gate	SG-80, SG-81, SG-82, SG-83	11	30/gate	1.1	1.5	15	7	12	6
Dual 4-Input AND/OR Gate	SG-280, SG-281, SG-282, SG-283	11	38/gate	1.0	1.5	10	5	8	4
AND Expanders									
Dual 4-Input AND Expander	SG-180, SG-181, SG-182, SG-183	<1	0.9/gate	1.1	1.5				
Dual 2 + 3 Input AND/OR Expander	SG-290, SG-291, SG-292, SG-293	7	15/gate	1.0	1.5				
OR Expanders									
Quad 2-Input OR Expander	SG-150, SG-151, SG-152, SG-153	4	20	1.1	1.5				
Dual 4-Input OR Expander	SG-170, SG-171, SG-172, SG-173	3	5	1.1	1.5				
Flip-Flops									
Set-Reset Flip-Flop	SF-10, SF-11, SF-12, SF-13	20MHz*	30	1.1	1.5	15	7	12	6
Two Phase SR Clocked Flip-Flop	SF-20, SF-21, SF-22, SF-23	20MHz*	30	1.1	1.5	15	7	12	6
Single Phase SRT Flip-Flop	SF-30, SF-31, SF-32, SF-33	15MHz*	30	1.1	1.5	15	7	12	6
J-K Flip-Flop (AND Inputs)	SF-50, SF-51, SF-52, SF-53	20MHz*	50	1.1	1.5	15	7	12	6
J-K Flip-Flop (OR Inputs)	SF-60, SF-61, SF-62, SF-63	20MHz*	55	1.1	1.5	15	7	12	6
Dual 35MHz J-K Flip-Flop (Separate Clock)	SF-100, SF-101, SF-102, SF-103	35MHz*	55/FF	1.0	1.5	11	6	9	5
Dual 35MHz J-K Flip-Flop (Common Clock)	SF-110, SF-111, SF-112, SF-113	35MHz*	55/FF	1.0	1.5	11	6	9	5
SUHL II TYPICAL CHARACTERISTICS (+25°C, +5.0 Volts)									
NAND/NOR Gates									
Expandable Single 8-Input NAND/NOR Gate	SG-200, SG-201, SG-202, SG-203	8	22	1.0	1.5	11	6	9	5
Quad 2-Input NAND/NOR Gate	SG-220, SG-221, SG-222, SG-223	6	22	1.0	1.5	11	6	9	5
Dual 4-Input NAND/NOR Gate	SG-240, SG-241, SG-242, SG-243	6	22	1.0	1.5	11	6	9	5
Single 8-Input NAND/NOR Gate	SG-260, SG-261, SG-262, SG-263	8	22	1.0	1.5	11	6	9	5
AND-NOR Gates									
Expandable Dual 4-Input OR Gate	SG-210, SG-211, SG-212, SG-213	7	30	1.0	1.5	11	6	9	5
Expandable Quad 2-Input OR Gate	SG-250, SG-251, SG-252, SG-253	7.5	43	1.0	1.5	11	6	9	5
Expandable Triple 3-Input OR Gate	SG-300, SG-301, SG-302, SG-303	7	36	1.0	1.5	11	6	9	5
Expandable Dual Output Dual 2-Input OR Gate	SG-310, SG-311, SG-312, SG-313	7	30/gate	1.0	1.5	11	6	9	5
AND Expanders									
Dual 4-Input AND Expander	SG-180, SG-181, SG-182, SG-183	<1	0.9/gate	1.1	1.5				
OR Expanders									
Quad 2-Input OR Expander	SG-230, SG-231, SG-232, SG-233	2	28	1.0					
Dual 4-Input OR Expander	SG-270, SG-271, SG-272, SG-273	2	6.7	1.0	1.5				
Flip-Flops									
Dual 50 MHz J-K Flip-Flop (Separate Clock)	SF-120, SF-121, SF-122, SF-123	50MHz*	55/FF	1.0	1.5	11	6	9	5
Dual 50MHz J-K Flip-Flop (Common Clock)	SF-130, SF-131, SF-132, SF-133	50MHz*	55/FF	1.0	1.5	11	6	9	5
50MHz J-K Flip-Flop (AND Inputs)	SF-200, SF-201, SF-202, SF-203	50MHz*	55	1.0	1.5	11	6	9	5
50MHz J-K Flip-Flop (OR Inputs)	SF-210, SF-211, SF-212, SF-213	50MHz*	55	1.0	1.5	11	6	9	5

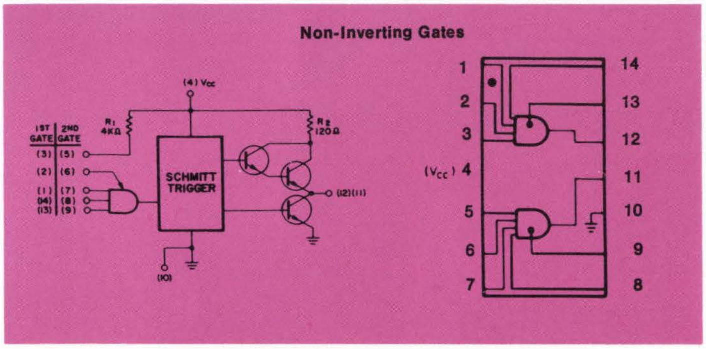
*Minimum toggle frequency **Minimum fan-out

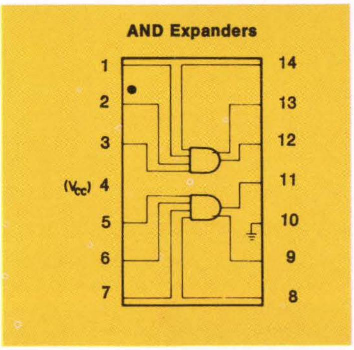


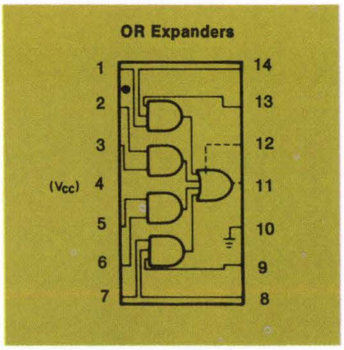


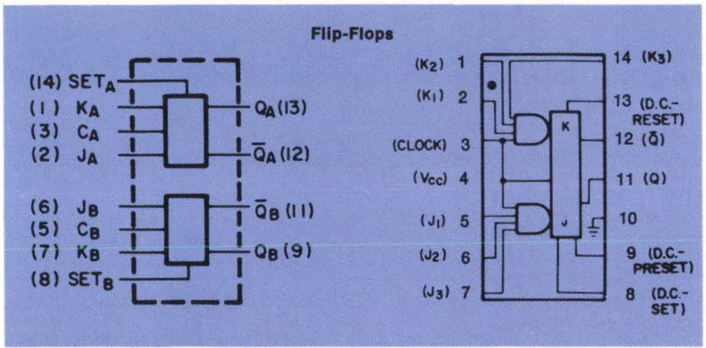












sign, manufacturing and testing is reflected in the superior quality of the SUHL lines. Patented active pull-up networks allow high output logic levels. Use of smaller device geometries not only gives better electrical characteristics, but also cuts device cost. Aluminum to aluminum ultrasonic bonding improves reliability two ways, better bonds and less heat applied to the silicon chip. Automatic testing by Sylvania's specially designed Multiple Rapid Automatic Test Of Monolithic Integrated Circuit (MR. ATOMIC) equipment insures that the units you get meet the specification to which they're bought. Tested here are all dc parameters at temperature and all switching parameters at 25° C.

The continuing leadership in TTL innovation and manufacturing exemplified by the SUHL lines makes Sylvania the prime source for high-level TTL devices.

CIRCLE NUMBER 303

This is Sylvania's DTL line

The 930 series of DTL ICs now available from your Sylvania distributor comes in flat and dual in-line plug-in versions.

Sylvania's DTL circuits are a low-power logic family with high noise immunity and moderate speed capabilities. Operating over a temperature range of −55° C to +125° C, these units are ideal replacements for similar units designed into digital systems already in production. They are electrically interchangeable and have pin for pin compatibility with other 930 series devices. Prices are competitive with those of other manufacturers.

Type*	Description
S9301/S9303	Dual 4-Input Expandable NAND Gate
S9321/S9323	Dual 4-Input Expandable Buffer
S9331/S9333	Dual 4-Input Expandable
S9441/S9443	Dual 4-Input Expandable Power Gate
S9461/S9463	Quadruple 2-Input NAND Gate
S9621/S9623	Triple 3-Input NAND Gate
S9311/S9313	J-K/R-S Flip-Flop
S9451/S9453	High Performance J-K/R-S Flip-Flop
S9481/S9483	Fast Rise Time J-K/R-S Flip-Flop

*A number ending in "1" indicates the MIL version (−55°C to +125°C temperature range); those ending in "3" are industrial types (0°C to 75°C).

TYPICAL CHARACTERISTICS

Parameter	Basic Gate	FLIP-FLOP
Supply Voltage	4.5 to 5.5V	4.5 to 5.5V
Temperature Range Series 9301 Series 9303	 −55° to +125°C 0° to +75°C	 −55° to +125°C 0° to +75°C
Propagation Delay	25 nsec	50 nsec
Power Dissipation at 4.5V Supply	5 mw	20 mw
Noise Margin	750 mv	750 mv
Input Unit Load "O" "I"	 1.1*mA 0.5μA	 1.1*mA 0.5μA
Fan-out	8	8
Output Logic Levels "O" "I"	 0.3V 4.65V	 0.3V 4.65V

*V_{IN} = 0V; 0.9 mA V_{IN} = 0.75V

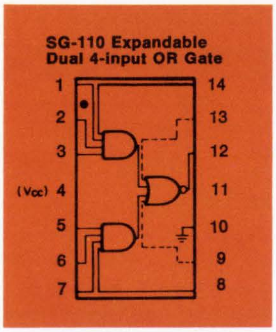
The added plus in this DTL line is the availability of devices housed in Sylvania's dual in-line plug-in package. With this package, designers get an extremely effective hermetic seal, circular leads with tapered shoulders, leads which can be flexed close to the package body, and a package of very small total volume.

CIRCLE NUMBER 304

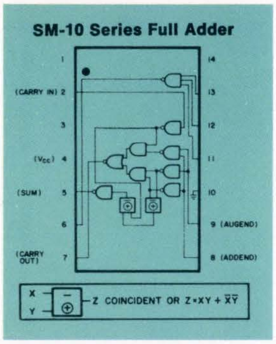
8-stage parallel add/subtract system uses only 17 ICs

Here's an example of compatible devices—a system using units from three Sylvania IC families: functional arrays, SUHL I and SUHL II.

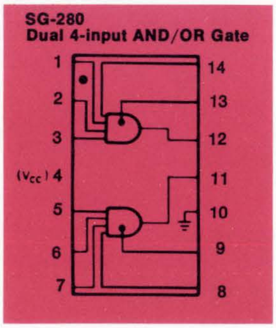
An eight-stage parallel add/subtract subsystem using ripple carry techniques can be made with 17 packages—eight SM-10 series full adders, eight SG-110 series expandable dual 4-input OR gates, and one SG-280 series dual 4-input AND/OR gate. The full adder is one of Sylvania's family of monolithic digital functional arrays. The SG-110 and SG-280 are SUHL family high-level TTL gates.



SG-110 Expandable Dual 4-input OR Gate



SM-10 Series Full Adder



SG-280 Dual 4-input AND/OR Gate

In the ripple adder configuration shown, control for the subsystem is represented by a mechanical switch. When the switch is in the SUBTRACT position, complement binary addition is performed. With the switch in the ADD position, straight binary addition is performed. It is assumed that only positive numbers will be added or subtracted, and that the most significant digit is the sign (0 = Positive, 1 = Negative).

The independent three-input NAND gate included in each SM-10 full adder package provides the complement of the SUM for subsequent operations. This includes such operations as complementing the answer in subtraction (depending on the sign bit in the answer). Enabling of the SG-280 AND gate during the subtraction process provides end around carry.

Typical propagation delay times are found by assuming that the number to be added or subtracted (the B inputs) is present in both true and complemented form, and that all A and B inputs are presented simultaneously. Then propagation delay times can be calculated with these equations:

Addition

Final Sum $= (N\text{-}1)t_{pd}carry + t\ sum + t_{pd}gate$
where N = Number of adder stages
$t_{pd}carry$ = one carry delay or 15 ns (typ.)
$t_{sum}carry$ = one sum delay or 25 ns (typ.)
$t_{pd}gate$ = propagation delay of SG-110 or 15 ns (typ.)

Subtraction

Final Difference $= (N\text{-}1)t_{pd}carry + t_{sum} + 2\ t_{pd}gate$ where $t_{pd}gate$ includes the propagation delay through the SG-280 (15 ns, typ.)

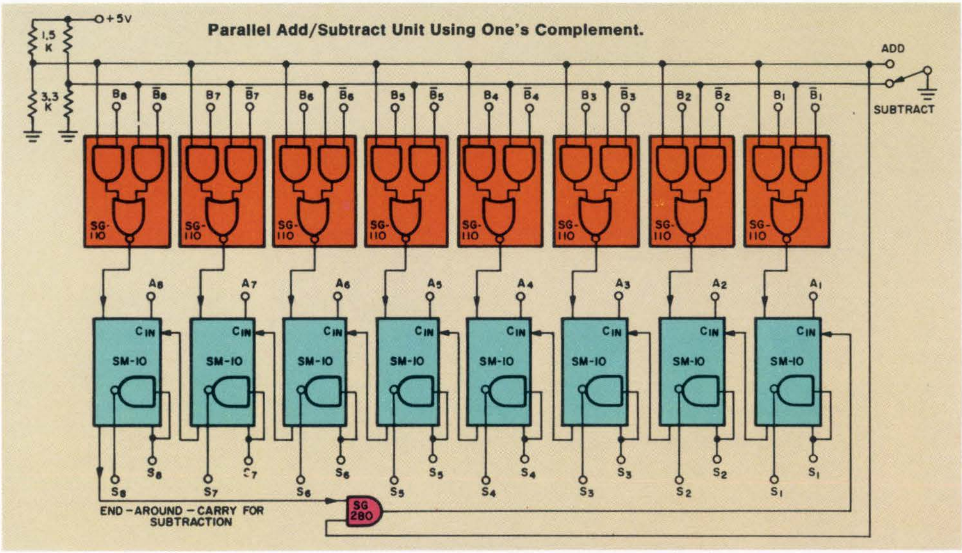
Thus, for an 8-stage add/subtract unit:

Final Sum $= [(8\text{-}1) \times (15)] + 25 + 15 = 145$ nsec
Final Difference $= [(8\text{-}1) \times (15)] + 25 + (2 \times 15) = 160$ nsec

Average Power Dissipation for a complete 8-stage unit is 880 milliwatts.

If a faster subsystem is needed, an eight-stage anticipated carry adder using SM-20, SM-30 and SM-40 digital functional array adders can be employed to replace the SM-10 devices.

CIRCLE NUMBER 305



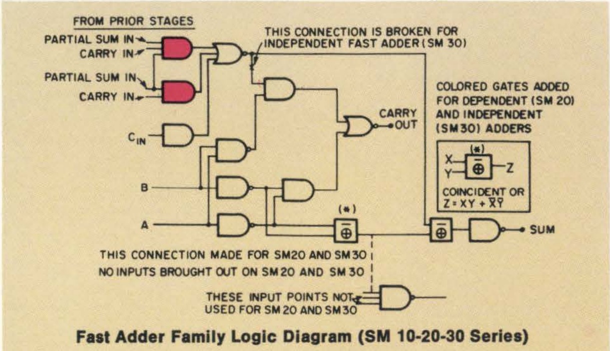
Parallel Add/Subtract Unit Using One's Complement.

These functional arrays reduce power, delay, and connections

This line of monolithic digital functional arrays provides computer and communications system designers with a powerful design tool.

Sylvania's line of monolithic digital functional arrays represents a significant advance over conventional integrated circuits. You can get typical computer subsystems such as adders, frequency dividers, registers, and memories which work at faster speeds, use less power and need fewer external connections.

For example, in a decade frequency divider with a frequency range of dc to 30 MHz, power can be reduced to one-fourth of that required by conventional



Fast Adder Family Logic Diagram (SM 10-20-30 Series)

MONOLITHIC DIGITAL FUNCTIONAL ARRAYS VS. CONVENTIONAL ICs

	Sylvania Monolithic Digita Functional Arrays					Conventional Integrated Circuits		
Typical Computer Subsystems	**Number of Packages**	**Number of Equivalent Discrete Components**	**Speed (nsec)**	**Power (Milliwatts)**	**Number of External Connect'ns**	**Equivalent Number of IC Gates**	**(A) Power (Milliwatts)**	**(B) No. of External Connect'ns**
Basic Single Stage Fast Adder With Anticipated Carry	1	73	14	120	14	18	180	64
Four Bit Anticipated Carry Adder	4	292	35	480	56	72	720	252
Four Bit Ripple Carry Adder	4	264	60	400	32	36	540	132
Eight Bit Anticipated Carry Adder	12	704	45	1040	168	172	1460	602
Eight Bit Ripple Carry Adder	8	528	120	800	112	72	1080	252
Decade Frequency Divider	1	116	DC to 30 mHz	150	6	40 (C)	600 (C)	140 (C)
Four Bit Register (Bus Transfer Output)	1	87	15	120	12	25	350	89
Four Bit Register (Cascode Pullup Output)	1	94	15	120	11	25	350	89

(A) Based on Average of 15mw per NAND/NOR and Average of 5mw per AND-NOR Expansion.
(B) Based on Average of 4 Gates per 14-Lead Package.
(C) Using 4 Sylvania JKs and a Pulse Shaping Gate, the Package Count would be 5 and Interconnections 37. Average Power Drain would be 190mw.

ICs while cutting external connections from 140 to 6. The table shows other examples—four-bit and eight-bit fast adders, and four-bit registers.

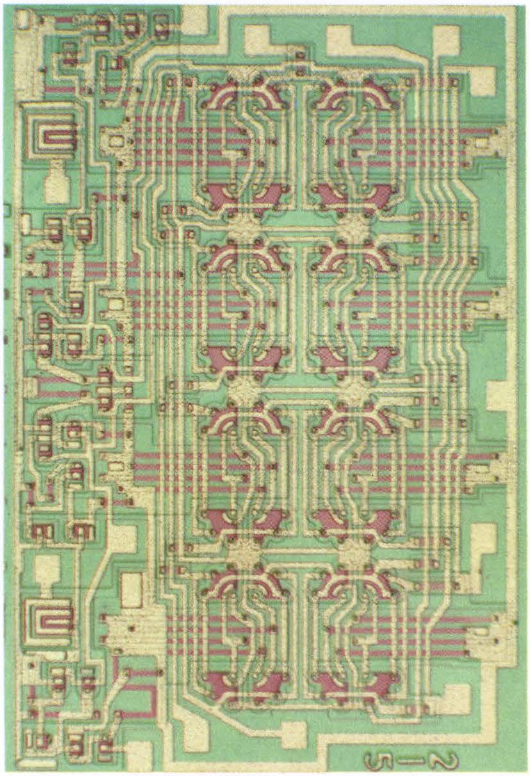
The functional arrays used in such circuits combine as many as 40 conventional integrated circuit functions in a single package while providing greater reliability and less costly system assembly.

The fast adder family of arrays contains the equivalent of 70 discrete components. Its basic integrated circuit is interconnected by three standard metal patterns to form the SM-30 single-stage independent fast adder, the SM-20 single-stage dependent fast adder, and the SM-10 single-stage full adder. The independent and dependent fast adders, in conjunction with the SM-40 carry decoder, can form parallel anticipated-carry fast-adder subsystems of any size.

Sylvania's SM-50 series decade frequency divider accepts both analog and digital inputs and produces a symmetrical square wave output. Digital signals from dc to 30 MHz and analog signals from 5 Hz to 30 MHz can be processed. This frequency divider is a six-stage circuit with the first a buffer which shapes the input. The following three stages perform a synchronous division by five. The next divides by two to complete the decade division. An output buffer in the final stage provides high ac and dc fan-out.

Four-bit storage registers, Series SM-60 and SM-70, are used as high-speed storage elements in con-

(Continued on next page)



SM-80 16-bit scratch pad memory

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trol and arithmetic sections of computers. The SM-60 series has clock input as well as clock output. Further, SM-60 output has wired-OR capability which means outputs can be tied together to perform the logic OR function. The SM-70 series is similar to the SM-60 but has a SUHL type output network and is not clocked with an enable signal. This means information set in the device is available at the output after a delay of 20 nanoseconds.

The SM-80 series 16-bit memory is for high-speed scratch pad memory systems with cycle times in the 100 nanosecond range. This single chip memory consists of 16 solid-state set/reset flip-flops arranged to form an addressable four-by-four memory matrix. This structure permits nondestructive readout of all 16 bits. Reading and writing is through four X and four Y lines which are brought out to eight external terminals, one for each line. Read and write control is by four internal amplifiers. Each flip-flop in the four-by-four matrix is logically connected to its own X_M, Y_N address combination and to the sense and write amplifiers.

All these monolithic digital functional arrays are compatible with SUHL ICs. The arrays are rated for operation in the temperature ranges up to −55° C to +125° C and are available in the standard Sylvania 14-lead dual in-line plug-in package and the TO-85 flat pack.

CIRCLE NUMBER 306

MARKETING MANAGER'S CORNER

Sylvania's commitment to IC upgrading

Fifty years of manufacturing electronic components has taught us that it pays to give our customers what they want.

Five years ago, when we started our integrated circuit facility, we polled our customers and, based on their reaction, initiated design on transistor-transistor logic to meet their need for faster integrated circuits. When this new line was introduced, some of our customers asked for buffered outputs to handle higher capacitive loads. The result was a development of a line of high-level transistor-transistor logic which we called SUHL, for Sylvania Universal High-level Logic.

These high-level TTL circuits were originally available in a limited number of logic configurations. However, customers required a wider variety of circuits to implement their logic designs. Our various solutions to their requests resulted in our present SUHL lines; one operating at 20 megahertz, the other at 40 megahertz with some 40 different logic configurations available to designers.

The next step was to develop functional arrays such as storage registers, counters, and adder circuits which satisfied customer requirements for more logic per package and for complete interfacing capability with SUHL circuits.

Our production philosophy was equally customer-oriented. We met the requirements for a dual in-line plug-in package with a ceramic/Kovar 14-pin enclosure using the same construction as was proven out in the TO-85 flat pack. The dual in-line package was developed and met customer needs including stringent military requirements. In conjunction with such development, Sylvania decided the best way to produce highly reliable integrated circuits was to concentrate on a single process. This included a series of 100% production tests and final 100% testing of all dc parameters at temperature extremes and ac parameters at room temperature.

We did this and now we're able to state that all our circuits, regardless of grade, are identical in construction. Any improvements are always immediately incorporated in the total line. Further, such upgrading is an intrinsic part of our manufacturing process. For example, when we added a Kovar base plate to the flat pack to improve its heat dissipation capabilities, we made a similar change in our dual in-line plug-in package.

We intend to continue pursuing this philosophy which permits us to assure all our customers that our circuits, regardless of grade, represent the best in performance and construction available.

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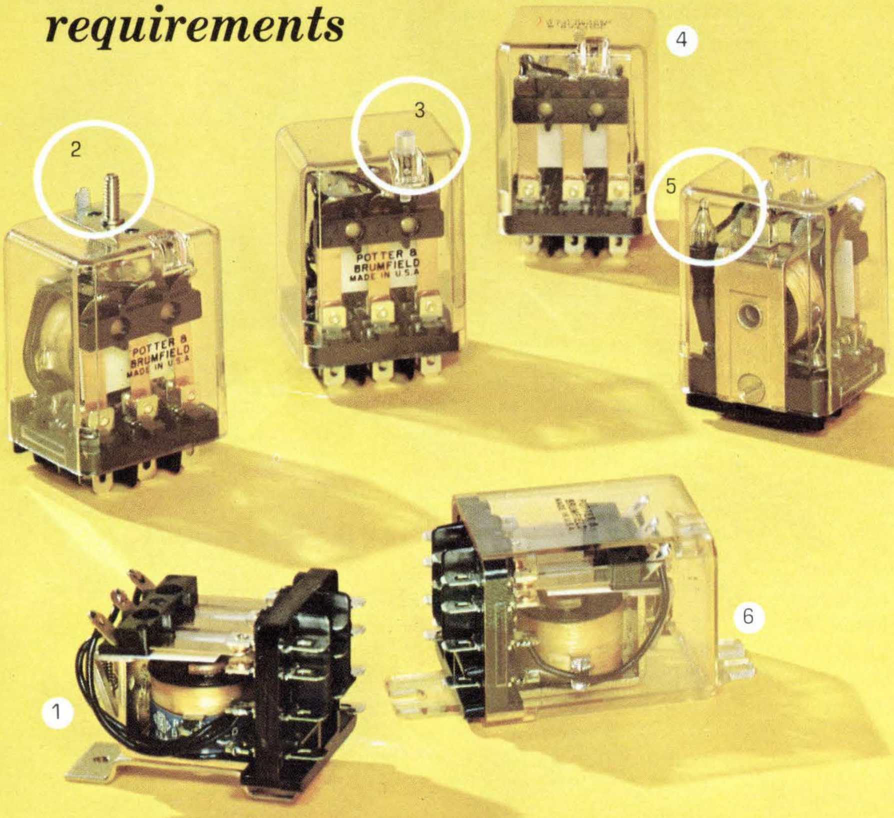

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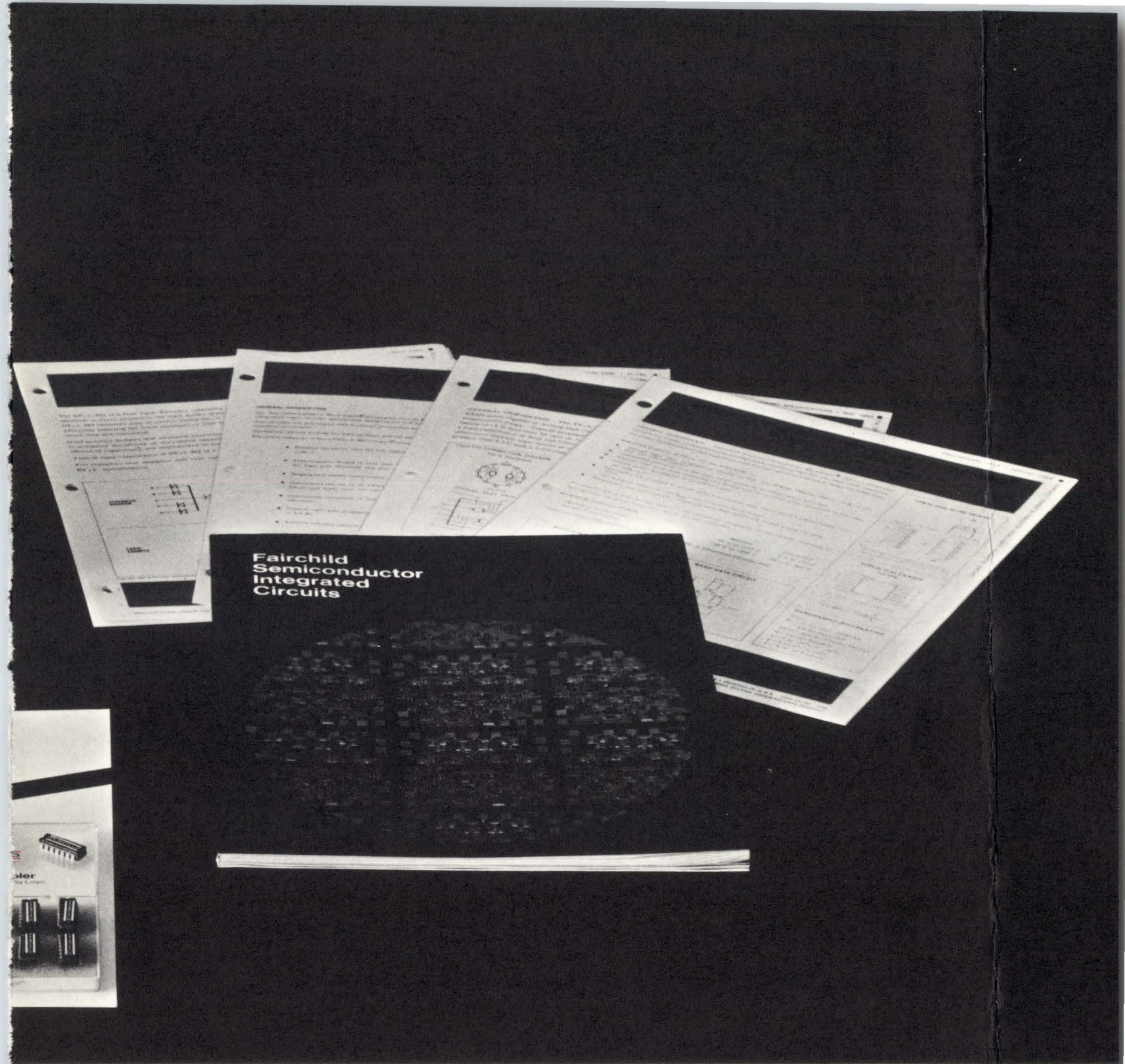

and LPDTμL (Low-power diode-transistor Micrologic) integrated circuits. By crossing family boundaries within the compatible logic group, you can optimize your system design. Here's how:

How compatible logic helps you: TTμL is the fastest of the three families and also the one that dissipates the most power. LPDTμL dissipates the least power, but is slower than the others. DTμL is right in between, both in speed and in power dissipation. There are clearly some functions in your system that require all the speed you can get. There are other functions where the speed of TTμL, for example, is wasted, because it is waiting for slower system elements. So you can use a slower logic family and optimize your power dissipation without sacrificing overall system speed. When you design with Fairchild's current sinking logic group, you are assured that all the families within the group are fully compatible.

What we mean by compatibility: All three families use NAND logic, and all basic NAND logic functions are available in any of the three forms. All three families use a single 5V power supply, and all three are guaranteed to perform compatibly when the specified fan-out and fan-in rules for inter-connecting between logic forms are observed. Pin configurations for the same functions are the same, and all three families come in the same two package configurations (maximum-density ¼″ x ¼″ Flatpak, and easy-to-handle Dual in-line). Finally, all three families are manufactured using the same technology, so that within the same working environment they will maintain a uniform stability over a period of time.

Get our product sampler: We want you to get acquainted with Fairchild's compatible current-sinking logic group at first hand, so we have prepared a special product sampler you can get. The sampler contains a 90-page book describing Fairchild integrated circuits; a guide to current sinking logic; data sheets on individual products and families; and actual product samples (see listing on back). Our complete product sampler kit sells for $51.00, which is the over 100 price of the samples alone. But quantities are limited, so act now.

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Integrated circuits are conventionally classified by family, and within each family by function. This method of classification restricts you to a single family within a system. Now Fairchild allows you to cross family boundaries and to design by function, selecting circuits from compatible logic families. This permits you to choose the best circuit for each function, and to optimize the system as a whole.

What is compatible logic? Fairchild classifies all digital integrated circuits into compatible logic groups: current sinking logic, current sourcing logic, and current mode logic. A current sinking logic gate (for example, a DTL gate) draws current into its output ("sinks" current) when in the low state, and draws virtually no current when in the high state. A current sourcing gate (for example, an RTL gate) drives current out of its output in the high state and, except for minor leakage, drives no current in the low state. Current mode logic can draw or drive current.

Compatible current sinking logic: There are three families within the Fairchild current sinking group: TTμL (Transistor-transistor Micrologic), DTμL (Diode-transistor Micrologic®)

Compatible Current Sinking NAND Logic Summary

Number and function	Typical Specifications at 25°C Free Air Temperature			
	Noise Immunity	Propagation Delay	Power Dissipation	Fan-out
TTμL				
9000 Clock-gated J-K flip-flop	1 volt	25nsec.	45mW	10
9001 Clock-gated J-K flip-flop	1 volt	25nsec.	45mW	10
9002 Quad 2-input gate	1 volt	10nsec.	12mW	12
9003 Triple 3-input gate	1 volt	10nsec.	12mW	12
9004 Dual 4-input gate	1 volt	10nsec.	12mW	12
9005 Dual AND/OR/NOT gate	1 volt	12nsec.	12mW	12
9006 Dual 4-input extender		4nsec.		
9007 8-input gate	1 volt	10nsec.	12mW	12
9008 Quad 2-input AND/NOR gate	1 volt	12nsec.	12mW	12
9009 Dual 4-input buffer	1 volt	15nsec.	22mW	30
DTμL				
9111 Parallel-gated clocked flip-flop	1 volt	40nsec.	48mW	8
9930 Dual 4-input gate	1 volt	25nsec.	8mW	8
9931 Clock-gated flip-flop	1 volt	50nsec.	20mW	7
9932 Dual 4-input buffer	1 volt	35nsec.	35mW	25
9933 Dual 4-input extender				
9936 Hex inverter	1 volt	25nsec.	48mW	8
9937 Hex inverter	1 volt	20nsec.	72mW	6
9941 Monostable multivibrator	1 volt	25nsec.	35mW	10
9944 Dual 4-input power gate	1 volt	40nsec.	20mW	27
9945 Clock-gated flip-flop	1 volt	50nsec.	42mW	9
9946 Quad 2-input gate	1 volt	25nsec.	32mW	9
9948 Clock-gated flip-flop	1 volt	40nsec.	48mW	8
9949 Quad 2-input gate	1 volt	20nsec.	48mW	5
9950 High speed gated flip-flop	1 volt	20nsec.	50mW	10
9951 2-input monostable multivibrator	1 volt	25nsec.	35mW	10
9961 Dual 4-input gate w/extender	1 volt	20nsec.	24mW	6
9962 Triple 3-input gate	1 volt	25nsec.	24mW	8
9963 Triple 3-input gate	1 volt	20nsec.	36mW	6
LPDTμL				
9040 Clocked flip-flop	1 volt	180nsec. (Output going positive) 90nsec. (Output going negative)	4mW	10
9041 Dual 3-input gate	1 volt	65nsec.	2mW	10
9042 Dual 3-input gate	1 volt	65nsec.	2mW	10
9043 Three and 4-input gate w/extender	1 volt	65nsec.	2mW	10
9044 Dual 4-input gate w/extender	1 volt	65nsec.	2mW	10
9046 Quad 2-input gate	1 volt	65nsec.	2mW	10
9047 Triple 3-input gate	1 volt	65nsec.	2mW	10

Contents of Sampler Kit

Qty.	PART No.	Description	PRICE 1-99 each
4	9000	J-K flip-flop	$ 5.10
2	9002	Quad 2-input gate	$ 3.65
2	9946	Quad 2-input gate	$ 3.65
2	9046	Quad 2-input gate	$20.00

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A very short course for engineers engaged in testing and evaluation of resolvers and synchros as components or as system transducers.

Selecting a resolver/synchro test instrument for any engineering, production or system requirement is remarkably simple from North Atlantic's family of resolver and synchro instrumentation. Because this group has been developed to cover every area of need in both manual and automatic testing, obtaining the desired combination of performance and package configuration usually demands no more than 1) determining what you need and 2) asking for it.

Remote Readout of Angular Position

For remote indication of resolver or synchro transmitters in system testing, North Atlantic's Angle Position Indicators (Figure 1) provide the advantages of low cost and continuous counter or pointer readout. These high-performance instrument servos are accurate to 4 minutes of arc, with 30 arc seconds repeatability and 25°/second slew speed. Dual-mode capability, multi-speed inputs, integral retransmit components and other optional features are available to match application needs. Priced from $895.

Figure 1. Angle Position Indicators are available in half-rack, quarter-rack and 3-inch round servo packages.

High-Accuracy Testing Of Receivers And Transmitters

Measuring receiver and transmitter performance to state-of-art accuracy is readily accomplished with North Atlantic's Resolver/Synchro Simulators and Bridges (Figure 2). Each of these dual-mode instruments tests both resolvers and synchros, and provides direct in-line readout of shaft angle, accurate to 2 arc seconds. Simulators supply switch-selected line-line voltages from 11.8 to 115 volts from either 26 or 115 volts excitation, and so can be used to test any standard receivers. Bridges have constant null voltage gradients, making them ideally suited for rapid deviation measurements. Simulators and Bridges each occupy only 3½ inches of panel height and are available in a choice of resolutions. They are priced in the $1500 to $3000 range.

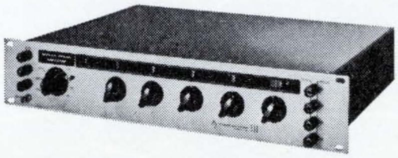

Figure 2. Resolver/Synchro Simulator provides ideal source for receiver testing.

Automatic Measurement And Conversion

Where systems require continuous or on-command conversion of resolver or synchro angles to digits, North Atlantic's Automatic Angle Position Indicators (Figure 3) handle the job without motors, gears or relays. These solid-state automatic bridges accommodate all standard line-to-line voltages and provide both Nixie display and printer output, accurate to 0.01° and with less than 1 second update time. Many variations, including 10 arc second accuracy; binary, BCD or decimal outputs; multiplexed channels and multispeed operation, are available for specific requirements. Ballpark price: $5900.

Figure 3. Model 5450 Automatic Angle Position Indicator. It measures shaft angles, converts them to digital data.

Measuring Electrical Characteristics

Combine a Resolver/Synchro Bridge and a Simulator with a North Atlantic Ratio Box, a Phase Angle Voltmeter and a test selection panel and you have an integrated test facility for determining all electrical characteristics of resolvers and synchros in component production or Quality Control. An example is the North Atlantic Resolver/Synchro Test Console shown in Figure 4. It measures phasing, electrical zero, total and fundamental nulls, phase shift and input current, as well as angular accuracy. Standard North Atlantic instruments are used as modules, making it a simple matter to fill the exact need. The unit shown sells for about $7500.

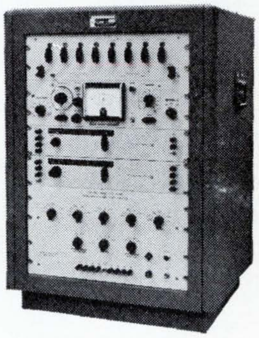

Figure 4. Model RTS-573 Test Console is a complete facility for the production line or in quality control.

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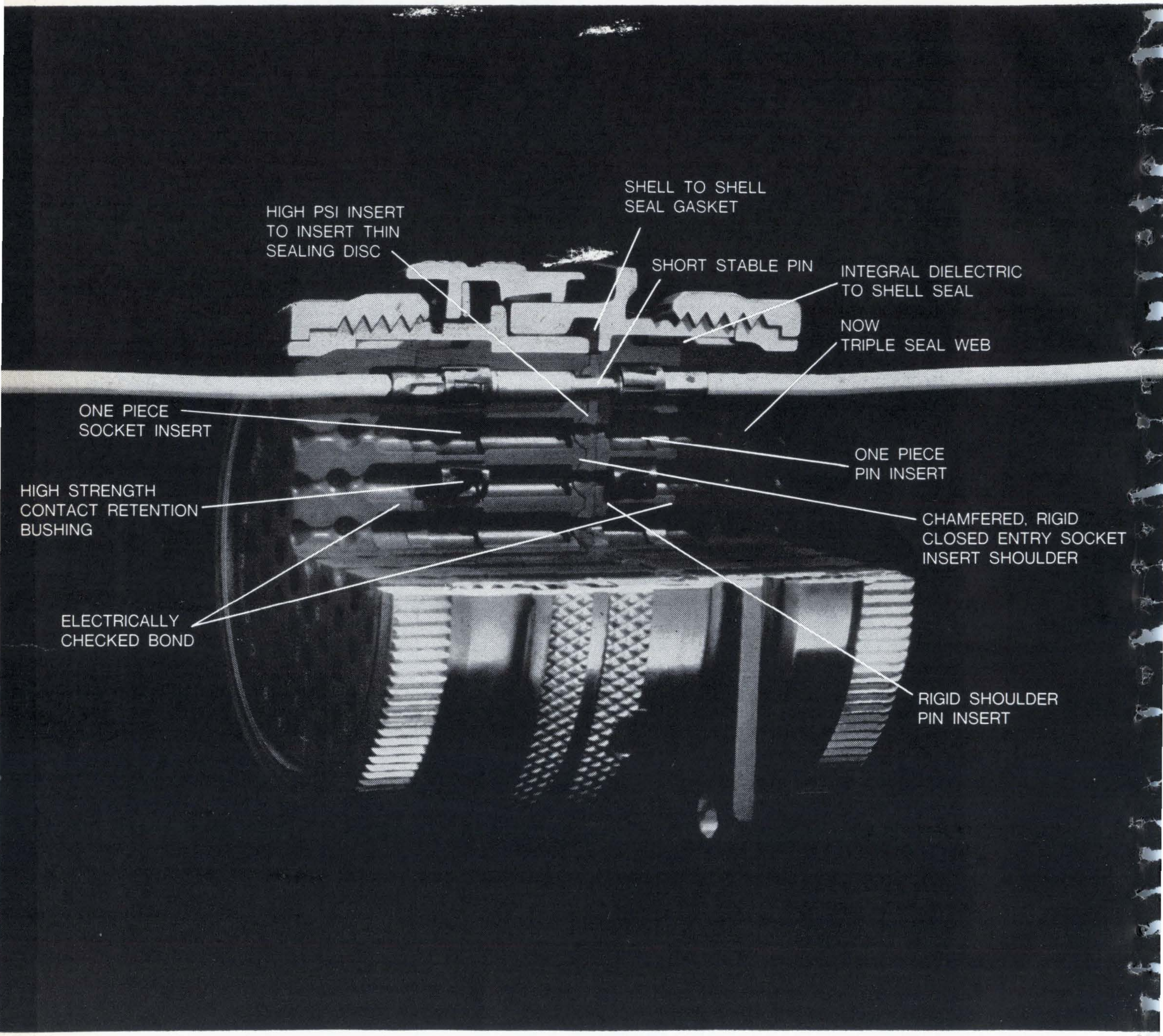

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Bendix Electronics

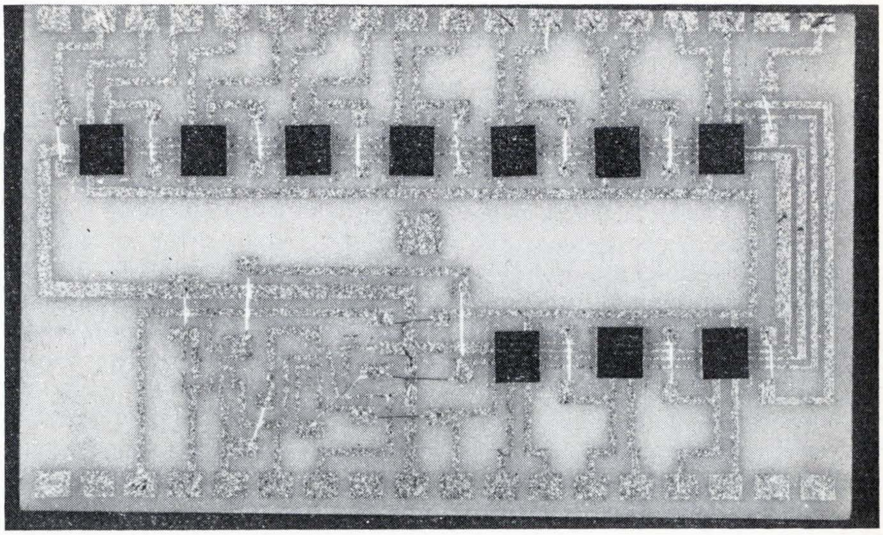
Circle 48 on reader service card

Electronics Review

Volume 40
Number 4

Solid state

Flip-chips emerge



One of Amelco's two microelectronics modular assembly packages has 18 leads on each side or 24 on one side.

The integrated-circuit package that goes by the sprightly name of the flip-chip has long been considered one of the best ways to match the low cost of the plastic package without sacrificing the hermetic seal. At least two companies have now solved some of the knottier problems of flip-chip technology and have put the devices on the market.

The Fairchild Semiconductor division of the Fairchild Camera & Instrument Corp. will announce at the Institute of Electrical and Electronics Engineers convention in New York next month that it is offering off the shelf four types of diode-transistor-logic circuits in ceramic dual in-line packages. And the Amelco semiconductor division of Teledyne Inc., is building and shipping 16-and 20-bit shift registers in a ceramic IC array package called the microelectronics modular assembly.

The Amelco assembly consists of up to 20 individual IC's that normally would be connected by bonding wires from their pads to a metalized interconnect pattern on the ceramic base of the package. With flip-chip techniques, in which the IC's are bonded face down on aluminum bumps, Amelco lost the interconnect flexibility provided by wires. It has therefore developed a multilayer ceramic sandwich with metalized holes connecting two layers of interconnects, a design it considers as significant as the flip-chip itself.

Bumping along. Flip-chip techniques save money by eliminating the tedious process of individually bonding each of the 14 IC pads to a lead running outside. Instead, a gold interconnect pattern is laid out on the ceramic substrate and aluminum bumps are formed in alignment pads.

Like most semiconductor processes, this one isn't as simple as it sounds. If the bumps aren't exactly the same height, the IC will tilt like a table with a short leg, and some of the connections won't be made. If pressure is exerted to bond the chip, it may break. This problem doesn't exist with flip-chip transistors, because their three leads always lie in the same plane, like the feet of a three-legged stool.

"A large part of our success lay in making the bumps high enough," says Joseph Welty, who heads Amelco's integrated helicopter avionics system program under which the arrays were developed. "There has to be enough room for a 'cold flow' of the metals so that the bump can be squeezed out a little and the aluminum oxide on the surface broken up." Amelco found that five microns was too short and had to build 15-micron pyramids to get the desired cold flow.

Making the aluminum bumps is also difficult. Electroplating is a touchy process, and etching away unwanted aluminum as is done in laying interconnect patterns a half-micron thick, would be uneconomical for a high bump. Amelco turned to evaporation, depositing the bumps through a metal mask.

The problem here is to peel away the mask, which would naturally tend to bond itself to the bumps the way an angel food cake bonds itself to the funnel in the middle of the pan. A baker can grease his pan to prevent the bonding; Welty will say only that Amelco changed the metal composition of the mask to prevent sticking.

Hot sandwich. Amelco likens the multilayer ceramic to a microminiature, hermetically sealed, multilayer etched circuit board, and thinks that it will be a direct competitor to discretionary wiring for complex integrated circuits. "Nobody had ever been able to bury a conductor in a ceramic before, because the metal was oxidized when the ceramic sandwich was fired," Welty says. As with the masks, Amelco experimented with new materials, and finally settled on a refractory metal (one which has a melting point higher than 4,000° fahrenheit) for the conductor to be buried in the aluminum oxide ceramic. The company won't say which metal or combination of metals it chose, but common refractory metals are molybdenum, tantalum tungsten and columbium.

Crossovers in the microelectronics modular assembly package are thus made in the ceramic itself. An interconnect pattern one mil thick is printed on the lower layer, the two layers are fired together fusing them, and a second interconnect pattern is printed on the top. The whole sandwich is 24 mils thick.

James F. Battey, general manager of Amelco, says the company will extend the flip-chip techniques to any product with healthy volume. "I would expect a substantial flip-chip production in the second half of 1967," he says. Besides the microelectronics modular assembly, Amelco is working on a dual in-line package and a flatpack. It began offering the two shift registers when procedural improvements brought costs down to the level of conventional methods.

Fairchild Semiconductor says its flip-chip dual in-line package, called "Fairpak," pairs industrial and consumer IC prices with military-level reliability.

IC price slash

Costs and speeds of ferrite-core and integrated-circuit main memories for computers appear to be converging, although cores are still less expensive per bit stored and IC memories are still much faster.

The Memory Products division of Fairchild Semiconductor, the first company to produce all-IC main memories as a standard line, plans to cut prices on a new line of IC memories to about one-tenth the present levels.

Fairchild's current IC memories contain 256 32-bit words per module, have a cycle time of 100 nanoseconds and cost $1 to $2 per bit. The larger but far slower core memories generally used in computers rarely cost that much, and the biggest and slowest types are priced at only pennies per bit.

Compromise. Each module in the upcoming Fairchild IC line will contain at least 1,000 words and will cost 10 to 20 cents per bit. As a trade off, speed will be reduced to a 200-to-300-nsec cycle time.

This will still make them at least twice as fast as the high-speed core memories that Fairchild is also producing. The latter have a cycle time as fast as 550 to 650 nsec, according to the company. This speed, two to three times that of conventional core memories, is the result of 2½-D organization [Electronics, Oct. 31, 1966, p. 83] and small, low-inductance packaging. Five or six other companies have also been making 2½-D memories with submicrosecond cycle times. Modular design allows the manufacture of memories with as many as 2,350,000 bits.

Fairchild has just started designing a line of faster core memories, with speeds of less than 500 nanoseconds the goal. It hopes to achieve this by cutting core size from 22 mils to 16 or 18 mils and by further reducing package induction. However, it hasn't been decided whether to retain the 2½-D structure or go to a different organization, according to Jack Schmidt, engineering manager of the Memory Products unit.

Schmidt declines to estimate per-bit prices on the planned memories, except to say that they will be competitive.

Ahead of demand. Schmidt indicates that computer designers have been slow in accepting high-speed, all-IC main memories. There is no ready made market for them, he explains, because existing computers weren't designed to employ main memories with such speed. Very fast IC scratchpad or register-type memories are being used in computers now, but the capacities of the scratchpads are tiny compared with the storage of the Fairchild memories.

Instrumentation

All in the family

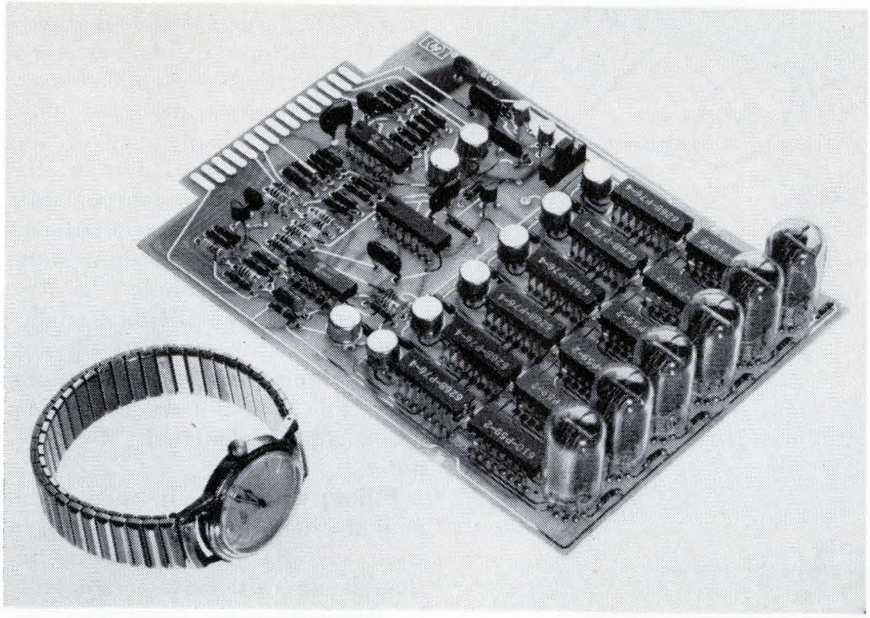
On the lower level of the sprawling Palo Alto, Calif., headquarters of the Hewlett-Packard Co. is an integrated-circuit facility whose capabilities have kept both semiconductor and instrument manufacturers guessing for more than a year. At the Institute of Electrical and Electronic Engineers international convention next month in New York, Hewlett-Packard will lift the veil a little when it introduces three electronic counters—its first products built with homemade IC's. The scope of the company's IC operation is indicated by its intention to continue making the circuits for the production line while maintaining its IC research and development.

"We expect to take care of our market predictions," declares Ed Hilton, manager of the IC facility. That means the company will be producing dual in-line packaged circuits for:

- The 12.4-megahertz model 5216A, a seven-digit multipurpose counter that measures frequency, period, period average, multiple period average, and time interval, draws only 6 or 7 watts of power so that it may be offered with self-contained batteries, fits in half a rack panel, and is priced below $1,300.
- The 12.4-Mhz model 5221A, a frequency counter 6¼ by 5¼ by 8 inches, available with four, five or six digits, priced at "well under $600."
- The 12.4-Gigahertz 5240A, an eight-digit hybrid unit that combines a counter and a divider and gives an unambiguous readout, with no further calculation necessary. It will sell for less than $5,500.

Each of the instruments has all of the counter circuitry, plus new miniature Nixie tubes on one printed circuit board.

Self-sufficiency. Hewlett-Packard reportedly has a fourth instrument in the wings. The design philosophy behind all of them bears out a statement made by company president David Packard almost a year ago [Electronics, April 4, 1966, p. 23] that to maintain its market position, Hewlett-Packard would make its own custom circuits. "If we go into a store and buy a lot of parts which we then assemble, someone else can go into the store, buy the same



Integrated-circuit counter from Hewlett-Packard puts counter circuitry and new miniature Nixie tubes on one circuit board. It costs under $600.

parts, and produce the same thing. If we do our own design and engineering, then we can make products that other people cannot make."

The 5216A, for example, will have 34 IC packages, 29 of which were developed at Hewlett-Packard. (The other five are Texas Instruments Incorporated logic functions.) "We optimized those 29 circuits for use in the kind of instrument we make," says Dexter Hartke of the company's frequency and time division. "In the case of the time base, a chain of decades, we have added extra circuitry, in the form of gating, that reduces the number of IC packages. Without that circuitry, we would have had to use three more packages; the $9 we saved pays for the crystal oscillator."

Proximity is bliss. "We could tailor those decades to our needs," Hilton explains, "because we didn't have to worry about different end-use; we didn't have to be concerned with a large fan-out capability, for instance." Hilton's domain is just across a corridor from Hartke's, which makes for close cooperation between instrument designers and IC designers. "We have freedom of design, with more control over design, and shorter turnaround time for design changes," Hilton says.

The hybrid 12.4-Ghz counter is only a cousin to the other two. Project manager Robert Allen says the division wanted to make an X-band frequency meter to combine the functions of two other Hewlett-Packard instruments—a counter and a divider. "We found that the IC people had developed a decade counter that we could use, so we took it," Allen says. "I would have gone to TI or Fairchild if ours hadn't been available, because it was obvious that we had to go to IC's. We did use Texas Instrument's TTL in the logic to get the speed we needed, but put our own RTL circuits in the drivers."

The competition. Hewlett-Packard is not alone in the IC counter field. Aerometrics, a subsidiary of the Aerojet-General Corp. introduced a 10-Mhz counter last year and now has plans to push it as high as 28 Mhz with Micrologic circuitry developed by the Semiconductor division of the Fairchild Camera & Instrument Corp. Aerometric's unit measures only 3¼ by 9¼ by 11 inches, and weighs 8 pounds. Its 114 IC's replace 1,768 discrete components. At $1,250 to $1,925, (with from four to eight digits), it is competitive with the 5216A.

The Systron-Donner Corp. will introduce at the IEEE meeting a series of seven counters that range from 5 Mhz to 12.4 Ghz, with direct counting up to 100 Mhz. The counters are designed exclusively with IC's.

Fairchild's own electronic instrumentation division is reportedly ready to market an instrument that uses an automatic transfer oscillator to count up to 15 Ghz. It will have an aging rate of one part in 10^9 a day. Fairchild promises some surprises in the scope and price of the new instrument.

But Hewlett-Packard's own series has quite a span. The 5221A has the capabilities of five counters now in the company line, and the 5216A can do as much as two of its discrete ancestors. Hewlett-Packard is really counting on its own IC's.

Space electronics

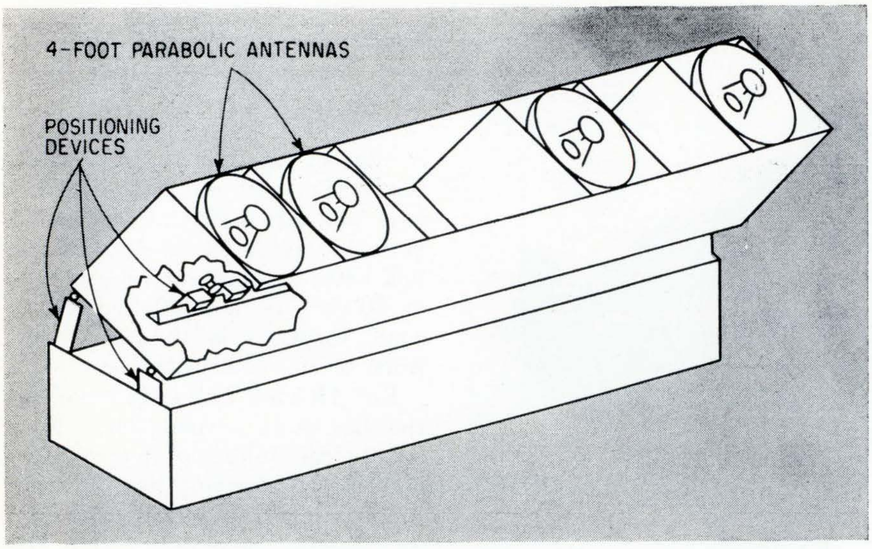
Fewer dishes . . .

High angular resolution at millimeter-wavelengths is the goal of an experimental antenna being built for the Air Force's Cambridge Research Laboratories, Bedford, Mass. This move into relatively unexplored antenna frequencies is aimed at increasing capabilities for ground identification of satellites, secure communications, and satellite-to-satellite measurements and observations.

Also, in using four paraboloid dishes to do the work of seven, the antenna will represent an experiment in "thinned array" design. "If you have to pay a lot for dishes, you don't buy as many," explains Allan C. Schell, a physicist at the Air Force labs and the designer of the antenna.

Aim for January. Operating as a multiple-element interferometer at a wavelength of 2 millimeters, the antenna will explore the 140-gigahertz frequency band. It is slated to begin operations next January.

The array consists of four 4-foot paraboloid reflectors coupled by a low-loss wideband feed and mounted side by side on a 28-foot-long structure slotted for seven reflectors. Various combinations of outputs from the four dishes will



Four dishes do the work of seven in thinned array being built for the Air Force's Cambridge Research Laboratories.

provide measurements of all spacings up to six, and the spatial frequency responses will thus be equivalent to those obtainable with seven dishes. The technique is similar to the one employed by Stanford University in building an array of five dishes to do the work of 10 [Electronics, Sept. 19, 1966, p. 48]. Schell concedes that basically "the method is a way to skimp on an antenna and still get your data."

Down the waveguide. The four-dish interferometer will be mounted on a tiltable frame and will be steerable along that axis only. The reflectors will be fed by a beam-waveguide structure that will combine optical and microwave techniques to provide power division among the dishes and individual phasing. The signal will move down the waveguide structure like a light beam, being refocused by lenses in the structure. It will, however, be varied in amplitude and will phase like a microwave signal.

The TRG division of the Control Data Corp. is building the $150,000 antenna system, including a temperature-controlled structure to house it, on Katahdin Hill overlooking the Air Force Labs. After the interferometer is used to explore millimeter-wave antenna techniques, it will probably be turned over to radio astronomers to be used as an atmospheric research tool. The design may be useful at microwave frequencies, Schell notes, "but first we have to prove it can be implemented at 2 mm."

. . . and better discrimination

A few miles away, on 90 acres in Maynard and Sudbury, Mass., Schell's group has built an interferometer that operates near the other end of the radio spectrum. This high-frequency array may also prove to be a prototype for a new class of antennas yielding high-angular-resolution data on satellites, and may be particularly useful in handling the problem of discrimination among simultaneous multiple targets.

The $80,000 antenna consists of 103 elements—wire dipoles strung on utility posts—arranged in a circular pattern whose diameter is 2,040 ft. It will have a 3-degree beam, which will be used only as a receiving antenna.

Almost ready. First tests will be conducted in early spring, with the antenna operating initially at 6.5 megahertz but tunable between 5 and 7.5 Mhz. The Air Force Labs assert that it will be the first high-resolution radio telescope operating at such low frequencies.

In a van parked near the perimeter of the array, a control console with 103 knobs can be used to vary the antenna pattern as desired. "The targets will do the moving. Our patterns will be set," says Schell. If this design concept works out, future antennas could have real-time display and beam-switching capabilities, but for the experimental system, output data will be sent back to a computer at the Cambridge labs for processing, while the scan angle can be changed only by individual adjustments at each of the 103 dipoles, an operation requiring about one hour. The adjustments have to be previously calculated by computers.

Filling in points. In the experimental program, data will be taken from celestial radio sources, although aircraft may occasionally be flown over for some measurements. "We hope to see the spectral output of radio sources at lower frequencies than now available," says Schell, pointing out that scientists have voluminous data on emissions from celestial bodies at microwave and optical frequencies, but hardly any at h-f.

Information derived will also be of interest to communications researchers since the ionospheric cutoff point, or maximum usable frequency, is often in the 5- to 10-Mhz band. The program's principal problem will be the signal-to-noise ratio.

According to Schell, the dipole pattern plus computer processing of output data will give the antenna a resolution equivalent to that of a 2,000-ft. aperture dotted with 1,000 separate dipoles. The phase and amplitude of signals reaching pairs of dipoles will be compared, and these in turn will be correlated with the phase and amplitude of signals reaching other pairs, resulting in a high resolution—or separation—of targets.

Medical electronics

Sound eye

A team of scientists in Cleveland has developed a surgical technique, using high-frequency sound waves, to push a detached retina back into place and to "weld" it securely against the eyeball. The group, at the University Medical Center, has performed the operation on animals only.

Test results encourage the developers, Adnan Sokollu, associate professor of biophysics, and Dr. Edward S. Purnell, assistant professor of ophthalmology, to believe that ultrasonic retina welding can be used on humans soon. The center is part of Western Reserve University's School of Medicine.

Retina detachment—caused by disease, accident or shock—results in serious impairment of vision or in blindness, unless it is sucessfully treated.

Lean on gravity. Eye surgeons long have depended primarily on gravity to get the retina back in place because the eye is too delicate for more direct surgical methods. A patient might be confined to bed for weeks until the retina eventually settles back into place. Or the patient might be whirled around on a turntable to let centrifugal force push the retina back.

Recently, retinas have been welded with a laser beam. However, the light can only pass through transparent media to reach the retina. The laser can't be used with a clouded cornea, a cataracted lens or a bloody vitreous humor.

Electric sparks have been used for retina welding, with the sparks applied from behind the eyeball to form a blister that will adhere to the eyeball. But small incisions are required to place an electrical probe behind the eye. All the techniques used heat to effect the weld but the spark method produces a slow-healing burn.

The ultrasonic method, on the other hand, is directly and immediately effective and does not produce any tissue trauma. Ultrasound is focused on the patient's eye through a cone-shaped nozzle. A few drops of liquid lubricator placed in the eye serve as a conducting medium. Ultrasound will not pass through an air gap but travels easily through liquids or solids.

A little push. The short, high-frequency sound pulses enter the eye, pass through, but do not affect the intervening tissue and exert a gentle pressure on the detached retina. The sound beam can be focused on a spot as small as $\frac{1}{16}$ inch in diameter.

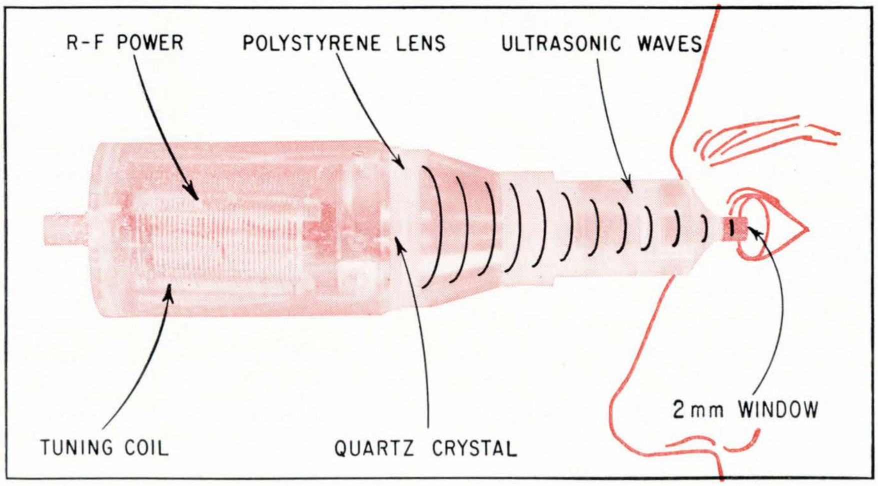
To produce focused ultrasound a quartz-crystal energy converter is used to develop low-power sound waves at about 7 megahertz. Interchangeable lenses and cones vary the beam's convergence.

Coupled by a 50-ohm coaxial cable to a radio-frequency power generator, the transducer can be excited with up to 40 watts of radio-frequency power to deliver 6 watts of sonic power. Efficiency in transduction is low because the sonic wave has to travel through a polystyrene lens in the transducer and the liquid media in the eye.

The focal intensity averages up to 250 watts per square centimeter for retinal welding. For pushing the retina back into place, a lower-power convergent beam is used, with an average intensity of 0.1 to 2 watts per sq. cm. All cases were treated with pulsed ultrasound at 3 to 7 Mhz.

The whole operation, performed experimentally several hundred times, takes only a fraction of a second.

Some five years have been spent in establishing proper levels for the process. Too much power would cause cavitation of the eye fluids, damaging the eye; too little would not produce a lesion, and the retina would not be welded.



Results of tests to relocate and "weld" detached retinas of animals hold promise that the process may be used on humans.

Scanning sleuth

An electronic scanner display system developed in a Massachusetts Institute of Technology study of cognitive processes is now being turned to research on blood cells and the elusive chromosome.

Chromosomes, the rod- or loop-shaped bodies that the protoplasm of a cell nucleus divides into before cell multiplication, have proven difficult to classify, because they exist in many combinations. Also, their pairings and structural changes during cell growth are extremely complex. Since they carry genes, the units of heredity, chromosomes are believed to hold some of the keys to inherited tendencies toward certain diseases.

Identification. MIT's new scanner display system, called Scad, links pictures and a computer. As a fallout from the data processing study, it's hoped that the system can help researchers categorize and pair chromosomes and identify various kinds and stages of development. The alternative for a researcher would be to manually examine millions of electron micrographs, keep a file and try to remember the correlations himself.

While the immediate goal calls for computer scanning of chromosomes and blood cells for the purpose of classification and correlation, the head of the program, Oleh J. Tretiak, says his personal goal is to get a "fingerprint" of a chromosome during a cell's splitting process. The longer-range objective of the project is automatic scanning of X rays of cell sections.

Says Tretiak: "Medical people can ask us for certain kinds of information they want to know about chromosomes or about blood cells and we will try to get this with the scanner. We will also try to ferret out certain correlations in the pictures—information, for example, about the center of gravity in a chromosome spread or about moments of inertia—and ask the medical people if these offer any useful clues."

How it works. The scanning system can accept transparencies, measure transmission of light at various points and convert this data into digital numbers for storage and retrieval. It can also accept digital data and produce pictures from it. Tretiak says Scad can delineate in a micrograph a part of one chromosome lying under another chromosome.

Scad measures display data and brightness over a raster of discrete points. When a transparency is placed in the scanner, the picture may be viewed on a monitor or photographed with a display unit. In the scanner, a spot of light from a cathode-ray tube is imaged on a transparency. The light passing through the transparency is collected by a condenser and sent through a sequence of dichroic mirrors that split the light spectrum into three bands. Each band is sent to a different photomultiplier; signals from the photomultipliers control the crt drive.

Color. Scad can measure color as well as brightness—an important feature in both chromosome research and in studies of red and white blood corpuscles. To scan color pictures, light passed through the transparency is split into three spectral bands and the amount of light in each band is measured by photomultiplier tubes. Color pictures are obtained from the display by photographing three separate pictures through three color filters.

Military electronics

SAM-D surfacing

An advanced development contract for the Army's SAM-D system, which incorporates the first tactical phased-array radars for the battlefield, is slated for award sometime this spring. Work on the project should be under way by the summer.

More than $2 billion will be spent on SAM-D (Surface-to-Air Missile — Developmental) during the next six years and most of the money is ticketed for electronics. The price tag includes the $300 million needed to get the system through engineering development, a process that should be finished by the early 1970's. Planners hope to have units ready for operation in 1972.

Triple threat. Originally designed to protect troops in the field against aircraft and short-range missiles, SAM-D — which also incorporates sturdy battlefield computers and solid-fuel missiles—has two other prospective applications. Besides replacing the Hawk as a mobile air-defense system, it may be used for continental defense, replacing the Nike-Hercules and complementing Nike X if that system is deployed around cities and fixed installations. And SAM-D subsystems may also be adapted for shipboard use to replace all or parts of the Navy's Talos and Standard missile systems.

In the three-way competition for the contract, the Radio Corp. of America, which is teamed with the Beech Aircraft Corp., is reported to have a slight edge. Also in the running are the Hughes Aircraft Co., working with the FMC Corp., and the Raytheon Co., which heads a group that includes the Martin-Marietta Corp. Raytheon, once eliminated from the SAM-D bidding, was reinstated when requests for proposals were reissued.

Evaluation of the proposals submitted to the Army last month will be complete by mid-Spring. These studies, along with recommendations will be forwarded to the Pentagon for action.

Three units. The system's final design won't be determined until a contractor is chosen because each group takes a slightly different approach. However, plans call for SAM-D to be divided into three separate units—radar, launcher and computer command. The continental defense system will be installed in fixed vans and the battlefield version in trucks. No specifications have yet been issued for the shipboard system.

Phased-array radar will be a key element of SAM-D [Electronics, Jan. 9, p. 172]. Continental defense units may be able to sweep 360°, while mobile defense systems will be equipped with more-limited arrays that can be angled to cover likely attack approaches. Calibration, normally a problem with phased-array apparatus, will present no special difficulties in the field since the system requires data only on the relationship between the bearing of the target and itself.

Compact digital computers able to handle a number of targets simultaneously will direct the fire of the missile batteries. A terminal-guidance system will assume control when the missile reaches mid-course.

The missile, said to be about the size of the 1,275-pound Hawk, will carry either a conventional or a nuclear warhead. Its range is classified but it's estimated to be about 60 miles. No decision has been made on how many SAM-D batteries will be deployed, but the projected number is said to range from 75 to 150.

Space-link probe

An Air Force investigation into alleged improprieties associated with the upcoming award of a multimillion-dollar set of contracts for a secret communications link between satellites and ground stations is essentially complete [Electronics, Dec. 26, 1966, p. 49], and a source close to the probe says the results will definitely not affect the selection of contractors.

A prototype of the communications link, called the space-ground link subsystem, was developed for

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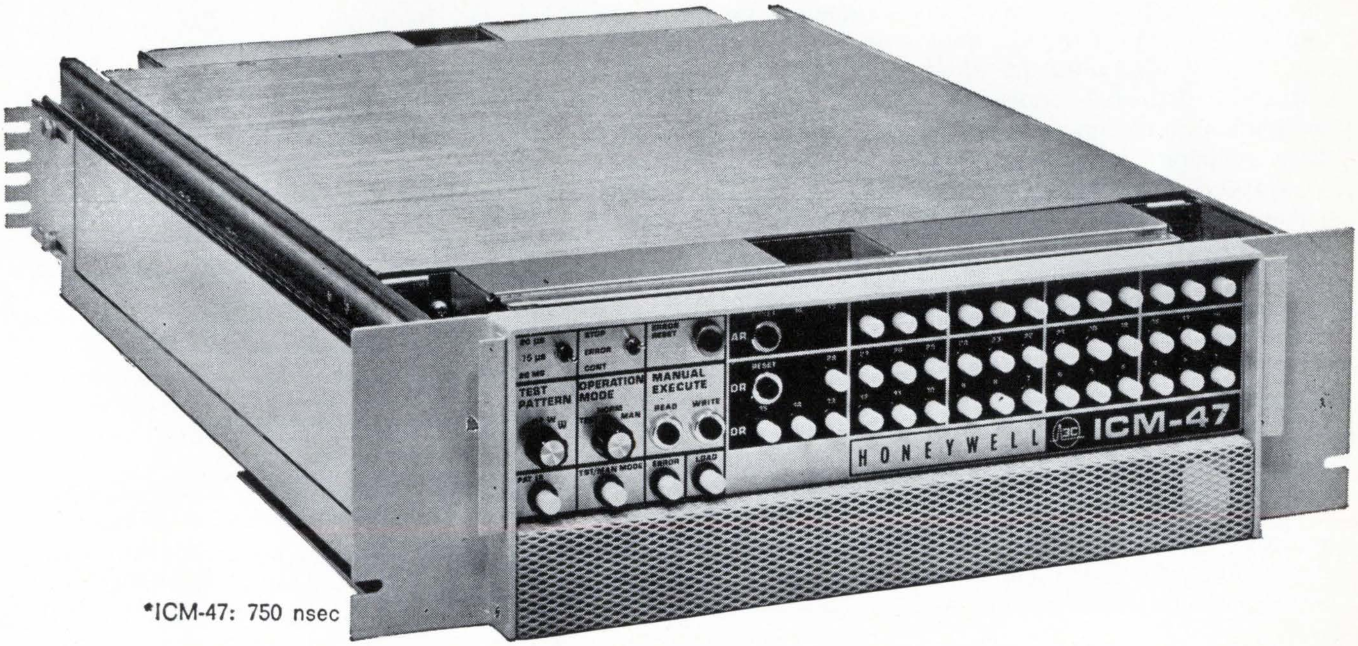


*ICM-47: 750 nsec

Honeywell

COMPUTER CONTROL DIVISION

Circle 55 on reader service card

the Air Force's Space Systems Division by the systems group of TRW Inc. The link was tested in orbit recently, TRW has just disclosed; the results were described by the concern as highly successful.

The investigation, it was reported, confirmed that gratuities were accepted by an individual connected with the program from a company interested in a development contract. But the source says there's no doubt that the gratuities did not represent an effort by the company to influence the Air Force's decision.

Awards pending. The Space Systems Division is currently studying bids for work on the project, and the award of the contracts is a few months away. A report on the investigation will be made before the orders are let.

The contracts are broken down into three parts: integration, installation and check-out; ground stations; and telemetry. The major bidders are the Philco-Ford Corp., TRW, the General Dynamics Corp. and Radiation Inc.

The aim of the program is to standardize and consolidate all the various tracking, telemetry and command functions of Air Force satellites. By using ultrawide bandwidth and high-speed pulse code modulation techniques, at least three separate communications links—very high frequency for telemetry, ultrahigh frequency for command and S band for tracking—are to be integrated into a single multiplexed S band channel.

Compatibility. The system is understood to be able to handle 1 million bits per second. The digital techniques that were designed for it are compatible with the Air Force's real-time computer data processing and with NASA's S band tracking system. The system could also handle voice communications between satellites and ground stations.

The plan calls for 10 space-ground link stations to be in operation next year; eventually, stations would be peppered all over the world.

A typical space-ground link spacecraft unit, the Air Force says, weighs about 25 pounds and consumes about 50 watts.

Communications

Tactical transceiver

A solid state transceiver that combines a high antijam capability with security and multiple-access and discrete address features has been developed for tactical military use by the Autonetics division of North American Aviation Inc.

Called Rascal (random access secure communication antijam link), it has an anti-jam margin of 22-25 decibels. This means an enemy would have to put into the band 200 to 300 times the power Rascal uses in order to jam it.

The line-of-sight transceiver operates with a 10-megahertz transmission band over the ultrahigh-frequency range from 225-400 Mhz. It is a frequency-hopping system operating in a pseudo-random manner. Both voice and digital data are transmitted in digital form.

Unique breed. The principle is not limited to uhf, says Dr. Robert W. Parkinson, engineering manager for Autonetics' electro sensor systems operation. "We could go to S band or X band, but above uhf we would probably have to use tubes," he notes. The significance of the system, according to Parkinson, is that it is the only one that combines the antijam property with such features as:

- Multiple access with discrete address. Each unit has its own address and can call another unit without getting the wrong party.
- Tight security. Since the signal is wideband, it would be difficult for an enemy to demodulate it.
- Reliable synchronization of transmitter and receiver. Synchronization time is one to two seconds.
- Efficient use of the spectrum. About 800 addresses could be assigned to the 10-Mhz band and about 200 could be on the air at the same time without appreciable degradation of the antijam capability and without crosstalk.

Each unit has a bell to signal incoming calls, an acknowledgment signal to advise the caller that the bell on the other end is ringing, and a busy signal. Further, there is provision for an override capability in case a third party wants to break in. To contact another station, the operator selects the code of the day, then punches in the numerical four-digit address of the other station on the push-buttons of the address panel.

Demonstration. Autonetics recently demonstrated four units under simulated tactical conditions before representatives of all the services at the Coronado, Calif., base of the Navy's Pacific Fleet amphibious force. Rascal units were set up to link a trailer at the base, a bunker at an electronics laboratory in Point Loma, five miles away, and a ship 220 miles out to sea.

Solid power

Until recently, the highest very-high-frequency output generated by solid state amplifiers has been about 100 watts. Now the Collins Radio Co. of Dallas has built a unit that achieves 500 watts continuous-wave power by linking high-power transistors in parallel and summing their outputs. Collins says the 500-watt output for frequency modulated signals is the highest yet delivered without the use of vacuum tubes.

Linking the transistors in hybrid-type summation networks provides isolation and assures that the failure of one transistor will not short out the others. In a tube amplifier, a tube failure would put the entire unit out of service.

In the unlikely event that three modules failed, the amplifier would still operate on about half power, says Tom Dennis, head of the Collins department that developed the device.

Collins developed the amplifier for its standard 618 series radio transmitter, which the firm supplies to commercial airlines. The solid state unit was made expressly for use in last December's tests of vhf voice communications between

airliners and ground terminals via the Applications Technology Satellite (ATS-1) of the National Aeronautics and Space Administration [Electronics, Nov. 28, 1966, p. 121; Jan. 9, p. 52]. Collins provided the radio for American Airlines Inc., which used it on a Boeing 707 jet airliner.

Fledgling market. The firm is building additional models for use in later tests with satellites in the ATS series, and is also producing another version for satellite control applications in NASA ground stations. But Collins expects its biggest customers to be the airlines after the carriers begin regular use of communications satellites.

The amplifier can also put out 125 watts when transmitting amplitude modulated signals for troposcatter. The input signal is the 25-watt output of a standard 546 transceiver.

Bandwidth of the two-stage amplifier is 20 megahertz. Collins has operated it with this bandwidth at frequencies from 116 to 152 Mhz. The low impedance level of the transistors permits this broad bandwidth operation.

The first stage is the driver amplifier, which uses two transistors. The second stage, the final amplifier, has 16 transistors in parallel. These transistors (ITT type 3TE225) are set up in eight modules. Each pair produces 100 watts. However, Collins has been operating the unit so that the modules actually run at about 70 watts, bringing the total output to around 560 watts. Some 60 watts are lost in the amplifier's low-pass filter, hybrid coaxial networks, and antenna switching relays.

Efficiency and cost. Dennis claims the amplifier is as efficient as a tube amplifier (around 59% in f-m mode). Gain is 9 decibels per stage.

Thin-film resistors are used in the attenuators and the hybrid coaxial connections.

Collins could make a smaller package, Dennis says, but so far the firm is putting the unit in a standard air transport rack.

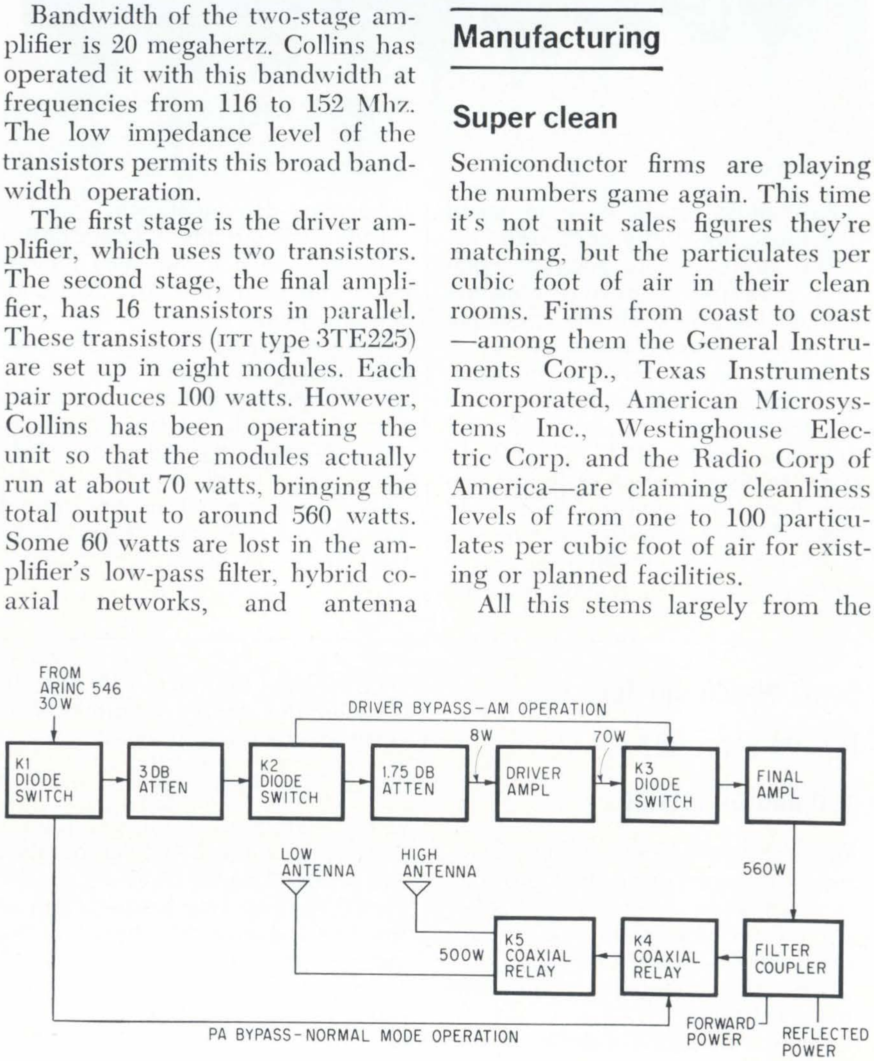
No price has been established for the amplifier, but Dennis expects it will be close to that of a tube unit. He contends that while the transistor cost is about triple the tube cost, a savings is effected by the elimination of tuning and servomechanism elements.

Manufacturing

Super clean

Semiconductor firms are playing the numbers game again. This time it's not unit sales figures they're matching, but the particulates per cubic foot of air in their clean rooms. Firms from coast to coast—among them the General Instruments Corp., Texas Instruments Incorporated, American Microsystems Inc., Westinghouse Electric Corp. and the Radio Corp of America—are claiming cleanliness levels of from one to 100 particulates per cubic foot of air for existing or planned facilities.

All this stems largely from the



Solid state amplifier used in aircraft-to-satellite-to ground voice link.

This is a triode?

This *is* a triode?

This is *a* triode?

This is a *triode*?

This is a triode*?*

RCA's new 40461 N-channel, depletion-type, insulated full-gate (MOS) transistor may not be a triode... but it works like one in critical audio and wideband amplifier applications from DC to 100 MHz...with solid state reliability!

RCA's new *M*etal-*O*xide-*S*emiconductor transistor makes it easy to design solid state devices into your high impedance control and instrumentation circuits. Unlike bipolar transistors, the 40461 has an extremely high input resistance (10^{15} ohms typical) which is relatively insensitive to temperature, at any gate polarity.

Further, this RCA MOS transistor features high transconductance and low input capacitance. Long-term stability is assured by a metallized gate which covers the *entire* source-to-drain channel. The 40461 is hermetically sealed in a TO-72 4-lead metal case.

With these features, the 40461 can do the job done by conventional triode devices and you gain the extra advantages of transistors! And this new MOS transistor can be used where conventional bipolar semiconductor devices were not previously applicable. You can also use two of these MOS transistors in cascode for greater versatility in your circuit design.

FOR YOUR CRITICAL CHOPPER APPLICATIONS *use the new RCA 40460 solid state chopper. It eliminates problems associated with mechanical choppers. The full-gate construction permits symmetrical operation and assures long-term stability. Offset voltage is virtually zero. And you can use the new RCA 40461 triode in the chopper amplifier's high impedance second stage.*

Design these devices into your existing circuits. Check your RCA Field Representative for complete information on both the 40460 and 40461 MOS transistors. Write RCA Electronic Components and Devices, Commercial Engineering, Section CN2-2, Harrison, N.J. 07029, for data sheets.

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trend to large-scale integration. The technique requires multilayer interconnections, and the associated crossovers can be short-circuited during fabrication by particles in the atmosphere. TI has found that work in a normal clean room—one containing about 100,000 particulates per cubic foot of air—results in a rate of around 100 defects per 100,000 crossovers; the company figures that large scale integration isn't feasible if the level is above 10 defective crossovers per 100,000.

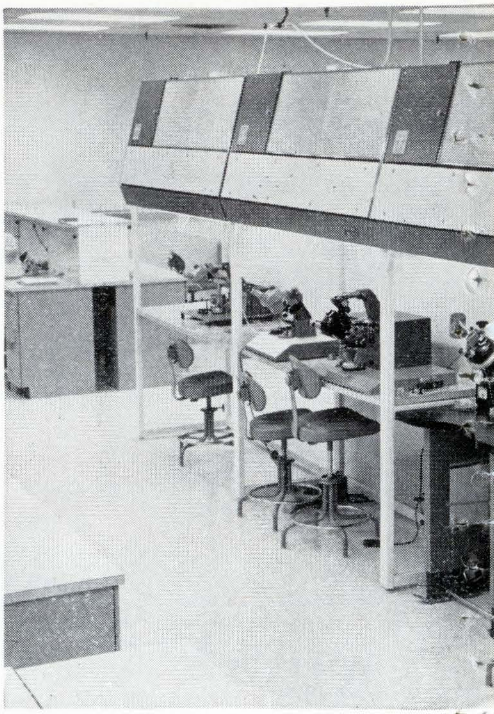
TI has already achieved a rate of only one defect per 100,000 crossovers by cutting the air contamination level over the workbench area to one particulate per cubic foot in a clean room rated over-all at 100 particulates. And it is now building a plant in which the clean rooms themselves will contain only one particulate per cubic foot of air.

This new TI facility is an example of the general trend in semiconductor production. The entire operation will be built around two ultraclean clean rooms, each of 10,000 square feet. A new vertical laminar system will keep air flowing from the ceilings of these rooms down to gratings in the floors to maintain the slated one-particulate-per-cubic-foot level.

Others in the industry aren't far behind in this business of counting particles.

"We're providing a really benign atmosphere for the chip," says Val Valandingham, operational vice president of American Microsystems, a company formed only last summer by a group formerly associated with the old General Micro-Electronics Inc. The goal of this benignity is increased yield, and the concern feels its investment in cleanliness is paying off.

More than 20% of the $1.5 million that American Microsystems Inc. spent on its new 24,000-square-foot production facility for the manufacture of metal oxide semiconductor integrated circuits went toward making the plant one of the cleanest in the business. Every process except final assembly is carried out in class-10,000 clean rooms and every bench inside



Work stations at American Microsystems are rated class 100.

these rooms is under a laminar-flow hood that gives the actual work area the environment of a class-100 clean room.

Designer's dream. The plant, in Sunnyvale, Calif., is a semiconductor designer's dream. The air in each room is passed through absolute filters and is changed every 45 seconds. Absolute filters theoretically pass no impurities. Epoxy paint, which won't flake or oxidize, is used throughout. Exhaust ducts are polypropylene rather than aluminum, which might flake. Humidity is controlled within ±5% and temperature is ±2%.

Stewart-Warner Mircrociruits, a subsidiary of the Stewart-Warner Corp., has been operating for more than two years in a clean plant specifically designed for the advent of large-scale integration.

The failures associated with contamination are random—that is, they may occur anywhere on the silicon wafer. As the size of individual chips increases to accommodate the complex circuitry of large-scale integration, the percentage of failures attributable to contamination is bound to rise.

Frances B. Hugle, who designed the Stewart-Warner plant when she and her husband William ran it, explains that the necessity for clean facilities was impressed on her when the couple was at Siliconix Inc. "We were making a series of four field-effect transistors that were exactly the same except for the area; they increased in size as they went up in power. We found that we got good yields for the smallest two, almost as good for the next largest, and no yield at all for the biggest. If you plotted random failure against device size, the curve was exponential."

Computers

Good housekeeping

The General Services Administration — the Government's housekeeper—is discovering that it's just as difficult to get Federal agencies to share their computers as it would be with a group of competing private companies.

For this reason, it has earmarked $10 million of fiscal 1968 funding to get into the computer service center business. It would rent computer time to agencies that periodically have either too much work for their own electronic data processing systems or don't have enough to warrant buying their own.

The agency is concerned over the growing number of digital computers used by Government and is seeking better use of existing equipment. It wants to set up regional centers to handle excess loads that can't be parceled out to other agencies. Los Angeles and New Orleans are being considered as sites.

Profits. Operating like a private data processing center in renting time and billing user agencies, General Services would maintain a $10-million internal revolving fund for the purchase and leasing of equipment, and would plow profits —income over that sum—back into the Treasury's coffers. Plans also call for the service centers to handle their own electronic data processing maintenance. Officials regard equipment maintenance as a high profit area for computer manufacturers and believe the Government could cut its data processing costs by training its own maintenance men.

The agency, as the Government's central purchasing agent, is also asking Congress for an additional $1.1 million to study centralized buying, leasing and use of all Government computers. Federal agencies operate about 3,000 computers —half of them are leased. The head of General Service's supply operation, H.A. Abersfeller, says the agency wants to determine how it can get rid of unnecessary equipment and add to existing systems while still saving money. In calling for computer pools as well as service centers, General Services officials believe many small Federal agencies now clamoring for their own computers could be fitted into the scheduling of equipment owned by larger agencies.

Program proliferation. Also to be included in the $1.1 million study will be methods to increase computer programing efficiency. Abersfeller says "there is vast duplication that we might pull together— such things as payroll programing, for instance."

The agency wants to identify the equipment that can be kept up to date and that can pay for itself fairly quickly if purchased rather than leased. In its funding request, General Services said that in many cases a piece of equipment being leased might pay for itself in three or four years if its usefulness could be extended. But first, Abersfeller notes, it must be determined how adaptable existing gear is to new features and whether there are agencies with less complex problems that can use older equipment being phased out by another agency.

Consumer electronics

Holographic static

H.M. Siegel, one of the strongest proponents of holographic television for both consumer and military applications, resigned as president of Conductron Corp., Ann Arbor, Mich., in a policy dispute over the commercial potential of the three-dimensional photographic technique in tv. [Electronics, Nov. 28, 1966, p. 25]. Siegel had wanted to buy a consumer electronics company that produces television and stereo sets so that he could lead Conductron into the holographic tv business before the end of the decade. But the company that controls 83% of Conductron, the McDonnell Co. of St. Louis, objected to the plan.

"The powers that be said 'no'— that's all; so I quit," said Siegel. "There were no arguments, just an honest difference of opinion."

McDonnell, currently negotiating to acquire the financially troubled Douglas Aircraft Co., was too heavily committed to the Douglas transaction to consider his proposal, Siegel explained.

Pioneering. Siegel, one of the founders of Conductron, had been pushing the company's research divisions to develop techniques for shrinking the bandwidth needed for 3-D television. "The techniques are within reach," he says. In fact, only a few months ago he claimed that a prototype system would be in operation this year.

As much a promoter as a researcher and teacher (he holds a professorship at the University of Michigan in Ann Arbor), Siegel had an "academic spat" with such holography experts as Emmett N. Leith, also a professor at the University of Michigan, and Dennis Gabor, the man who invented holography but could not demonstrate it at the time because the laser hadn't been invented. Both felt then that holographic tv was beyond the state of the art.

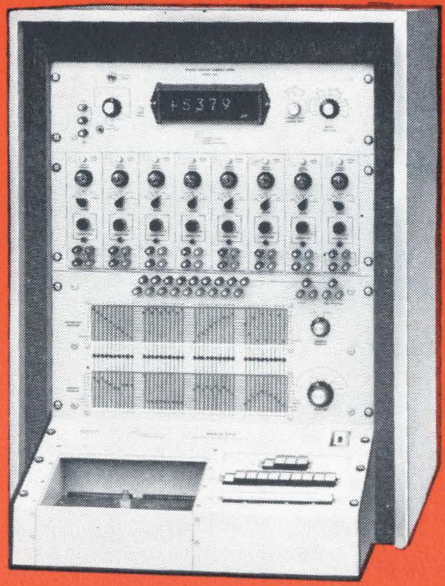
The company that Siegel wanted to buy was the old Trav-ler Industries Inc., which Hoffman Electronics Corp. and Montgomery Ward & Co. jointly acquired in 1964. Under the now-defunct plan, Conductron was to purchase a 51% interest in Trav-ler.

The move would have given Conductron some diversification. The firm produces fine-resolution radars and is doing operations research on missile penetration aids for the military.

NEW

semi-automatic integrated circuit analyzer

MICA 150



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Now the integrated circuit user can get all the flexibility and performance of an expensive, large scale IC test system in an accurate and reliable DC bench top analyzer.

The new MICA-150 Modular Integrated Circuit Analyzer tests all IC configurations of up to 40 pins with unique programming, fast pushbutton sequencing and built-in DVM readout.

Fast, Versatile Programming Two independent 10x40 crossbar switches and rapid pushbutton sequencing provide up to 40 tests on a single device without re-programming. For example, it's now quick and easy to check a 10 pin device using four completely different test programs without resetting any switches to advance the test from pin-to-pin or program-to-program. Additional flexibility allows the built-in DVM to measure current on one pin of the device and voltage on another—all pre-programmed.

Universal Test Adapters Through use of universal test adapters, the MICA-150 is designed to check ICs according to the number of pins of a particular package, not device or circuit type. Adapters are available for diode, transistor, TO-5, flat-pack, dual in-line and other package configurations, and can also be provided for Kelvin connections.

Accurate Digital Readout Specifically designed for the MICA-150 analyzer, the built-in Digital Volt/Ammeter has a conservatively rated readout accuracy of 0.1% with a four digit display. Other features include automatic ranging and polarity selection, self-calibration, automatic voltage or current readout selection. Measures currents as low as 1 nanoamp, voltages to 1 mv.

Modular Design Modular construction allows users to select an economical, customized tester without obsolescence problems. Maximum capacity of eight function generators permits later expansion, including modules for AC and pulse testing, without additional modifications.

Variable Soak Time Marginal device operation can be easily detected through use of an adjustable test time control which provides a period for thermal stabilization prior to measurement. A continuous position on the control allows parameters to be varied while observing results.

Precision, Wide Range Power Supplies Highly precise supplies utilize multi-turn calibrated potentiometer controls with high resolution and repeatability. Constant current supplies are continuously variable from 0-100 ma with voltage compliance adjustable to 100v. Constant voltage supplies are variable from 0-100v with automatic current limiting to 100 ma to provide device protection.

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Detailed technical literature on the MICA-150 will be mailed immediately upon receipt of this request.

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For the record

Delayed action. The launch date for the third Intelsat 2 communications satellite has been set back one month—to March 15—because of problems with the Delta booster. The satellite—built by the Hughes Aircraft Co.—is to be placed in stationary orbit over the Atlantic Ocean to supplement the Communications Satellite Corp.'s Early Bird satellite. It is also slated to become part of NASA's Apollo communications network.

Destination Mars. An engineer at Hughes, Thomas P. Van Horne, has outlined plans to redesign the Surveyor spacecraft to enable it to make a soft landing on Mars and survey the planet with its tv cameras. Another Hughes engineer, Harold S. Braham, suggested that a synchronous satellite be orbited around Mars to relay signals from a Surveyor spacecraft. The proposals were made at the IEEE's winter convention on aerospace and electronic systems in Los Angeles.

Trial run. The first population census by mail—a dress rehearsal for the 1970 census—is scheduled to take place in New Haven, Conn., in April. Robert F. Drury, assistant director of operations for the Bureau of Census, says the study will evaluate new data collection procedures. Every household will receive a short-form questionnaire coded to be read by high-speed optical scanning devices. A long-form questionnaire will go to every fourth household.

Education. Cornell University's College of Engineering in Ithaca, N.Y., is using a "blackboard-by-wire" system to teach a course in physical metallurgy to a group of Sylvania research and development specialists in Towanda, Pa., 55 miles away. The lecturer's voice and any graphics he uses are transmitted from a console in the Ithaca classroom to a television monitor and speaker system at Towanda.

Merger. The proposed merger between the International Telephone and Telegraph Corp. and the American Broadcasting Co. may be stalled for several months. The Justice Department threatens court action against the Federal Communications Commission if the agency refuses to reopen hearings on the merger.

Marketing. The General Electric Co. is marketing a frequency-modulated two-way radio using integrated circuits. The integrated circuit oscillator module is a thimble-sized device containing components smaller than a pinhead.

Programing. General Electric also has added a new software capability to its GE-400 computer series. Called the direct access programing system, it provides multiprograming and communications capabilities.

New system. The Federal Aviation Administration has awarded a $44.8 million contract to the Raytheon Co. for a compact display system that will replace four subsystems currently needed to keep tabs on aircraft: alphanumeric generator, data filters, radar bright displays and computer entry and readout equipment. Using IC's almost exclusively, the new system will increase the control air traffic personnel have over data inputs to a central computer.

Longevity. A new argon laser providing 1,000 hours of operation —more than three times the life of previous units—has been developed by the Radio Corp. of America. The laser will be used in data processing, space communications, satellite tracking, earthquake detection and surgery.

Firing up. The Zirconium Corp. of America is making furnace furniture with an inert refractory material that reduces impurities in the production of ceramic capacitors. The material, zirconium oxide, is effective at temperatures up to 4,600°F. Melting point is 4,800°F. Capacitors are usually fired at temperatures from 2,000°F to 2,600°F.

Education. The Philco-Ford Corp. is building an education development center in Ft. Washington, Pa. The computerized facility, which is expected to be completed in April, will give the company a high-level base for entering the field of academic education.

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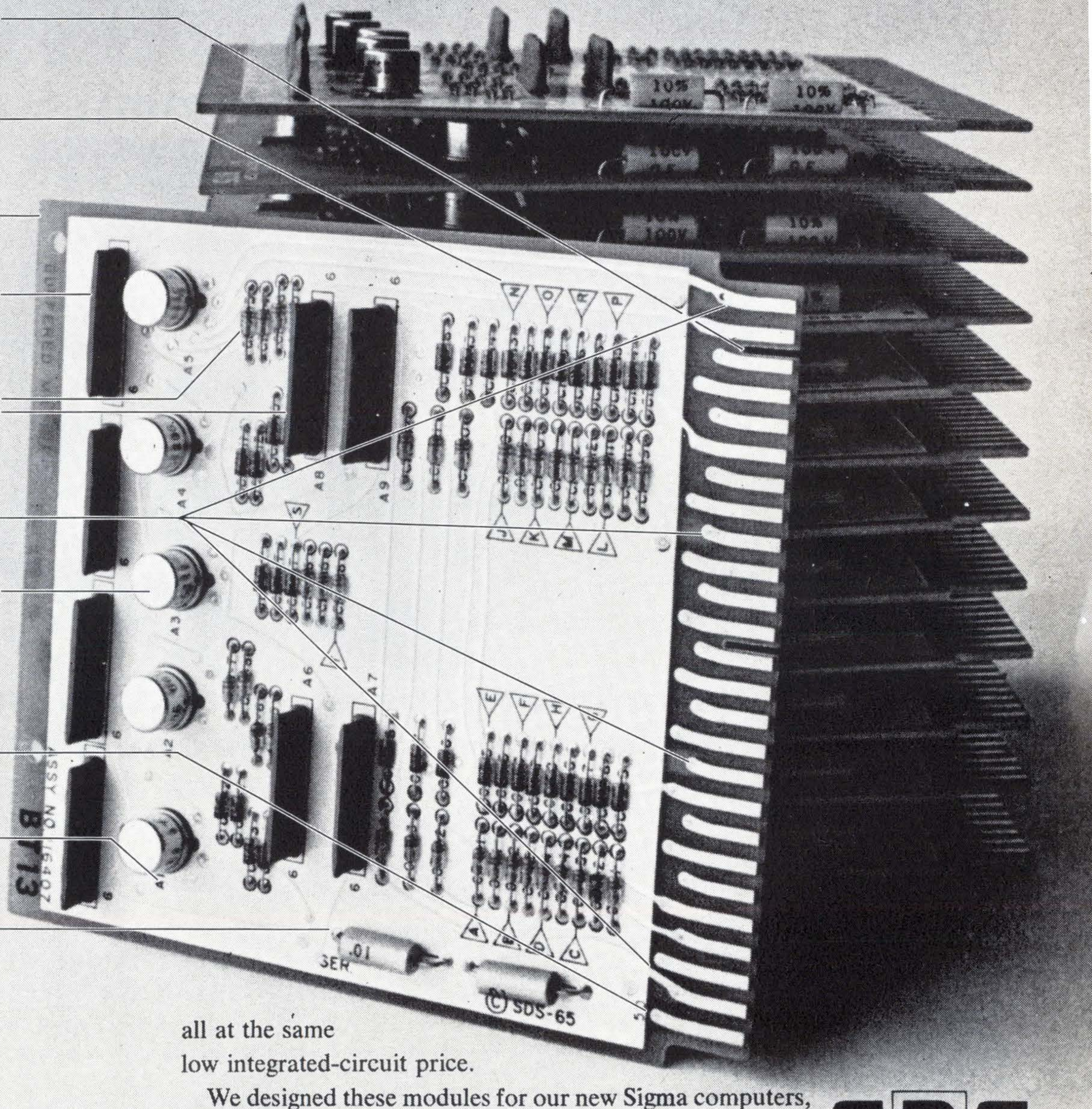

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SDS

Scientific Data Systems, Santa Monica, California

Washington Newsletter

February 20, 1967

Systems approach seen coming on like gangbusters

The role of the electronics industry in the Johnson Administration's assault on crime will involve a total systems approach and the implementation of military-style command and control techniques rather than the production of two-way wrist radios and other Dick-Tracy-style devices that some in the industry had expected [Electronics, Aug. 8, 1966, p. 52]. S.I. Gass of IBM, a consultant to the staff of the science and technology task force on crime, says one proposed study **would determine if emergency calls and the dispatching of police cars could be best handled by real-time computer response.** Envisioned by the task force is a system in which a switchboard operator would feed the location of an emergency call directly into a computer. A dispatcher would immediately read out on a cathode-ray-tube display such data as the location and number of the police car and hospital nearest the scene of the call.

Weigh new uses to save Ilaas

Two new jobs may save the integrated light attack avionics system. **The Navy is considering using Ilaas displays in its F-111B aircraft and the Air Force may use technical inputs from the system in the F-X advanced tactical fighter.** Being developed by the Sperry Gyroscope Co., the system was originally earmarked for the A-7 attack aircraft, but was dropped because it would have added $230,000 to the plane's cost [Electronics, Oct. 3, 1966, p. 75]. The Air Force is also considering using technology from the Mark II avionics system for the F-X.

Walkie-talkie firms unruffled by FCC band-change plan

Neither Japanese nor U.S. manufacturers are fretting much over the Federal Communications Commission's proposal to ban unlicensed walkie-talkies from the 27-megahertz Citizens Band. **Most feel sure that no action will be taken for several years, perhaps as many as five.**

The proposed changes in regulations covering unlicensed walkie-talkies—operated mainly by children—were prompted by growing complaints by licensed Citizens Band users about interference from the toys. **The FCC proposal would shift the walkie-talkie allocation to a channel in the 40-kilohertz region and at the same time lower the permissible power limit for the radios from 100 milliwatts to 60 mw.**

New designs to accommodate the shift to the higher frequency would force toy walkie-talkie producers—there are more than 80 in Japan alone—to raise their retail prices by about $2 to $3 a unit. Thousands of the walkie-talkies, some priced as low as $10, are sold each year.

Apollo changes may undercut other programs

The division of NASA funds is up in the air pending a report by a board of inquiry on the Jan. 27 disaster that killed three astronauts.

There is some worry among officials of the space agency's unmanned programs that fiscal 1968 budget funds earmarked for such projects as Apollo Applications and Voyager may be diverted to the manned Apollo program in the wake of the space capsule fire.

Pressure in Congress to pare NASA's $5.1 billion budget request appears to be easing, but if costly Apollo changes are required, the unmanned programs may be undercut. However, NASA officials hint that the investigators will call for procedural revisions rather than more expensive hardware modifications; such findings could also enable the agency to hold to its schedule of landing a man on the moon by 1970. Meanwhile, NASA will proceed with the launching of three unmanned Apollo flights this year.

FAA tests system reporting weather every two minutes

A system to provide aircraft preparing to land with continuous reports on weather conditions above the runway is being tested by the Federal Aviation Agency at Atlantic City, N.J. In the trial program 13 observation points around the airfield, each equipped with rain, temperature and pressure gauges, rotating-beam ceilometers to measure cloud height, and transmissometers to measure visibility, are queried every 24 seconds. Analog outputs from the equipment are converted into digital signals and fed into a computer that checks the data and puts the information in forecast form.

Incoming pilots will receive updated weather reports every two minutes. The FAA hopes to eventually install the system at 25 major U.S. airports.

Comsat requests bids on terminals

The Communications Satellite Corp. has asked for bids on three more satellite ground terminals. To be jointly owned by Comsat and international-communications common carriers, the stations will have fully steerable 85-foot antennas. Estimated cost: about $5 million to $6 million each.

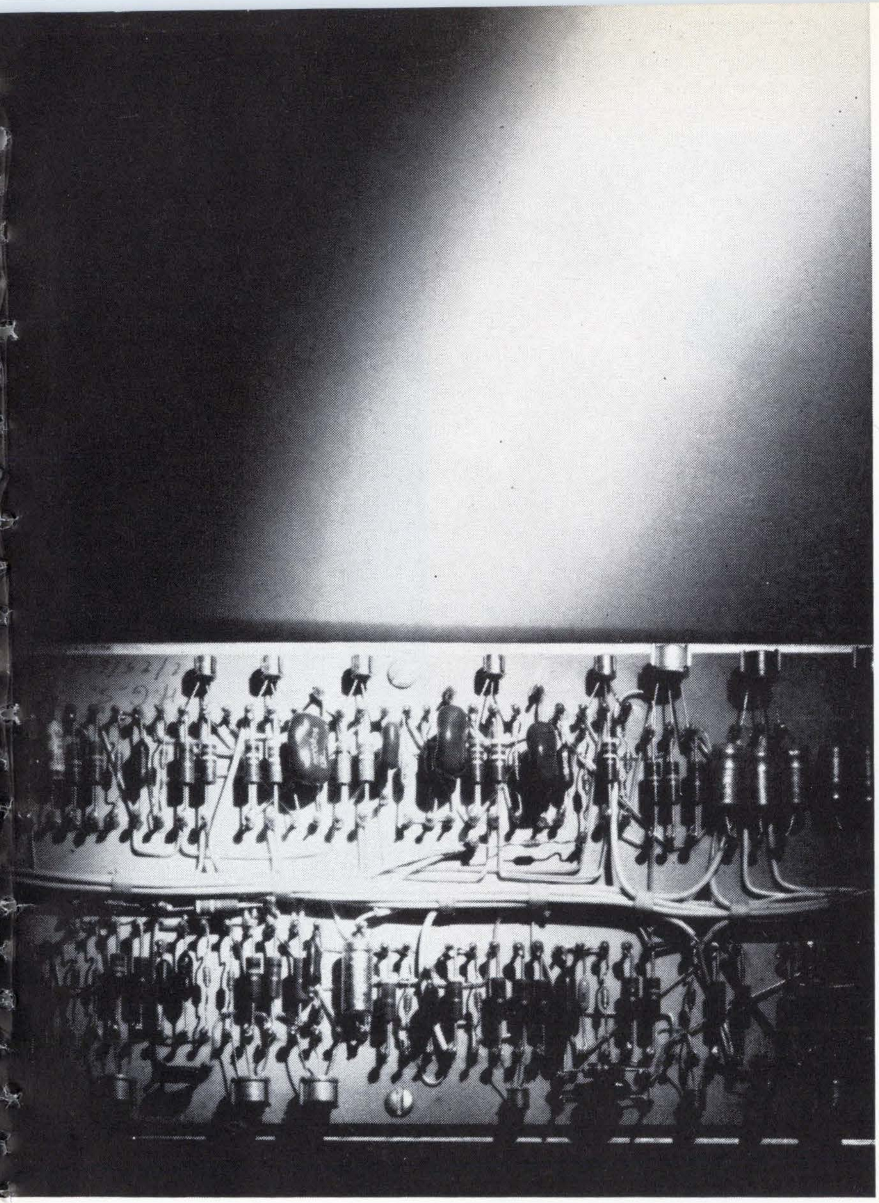
One station will be built near King City, Calif., the second at one of four sites now being considered in West Virginia and the third in Puerto Rico where two sites are under study. The proposals, for architectural and engineering services, were sent to 35 firms. Comsat also has plans to add another antenna at its Hawaiian terminal.

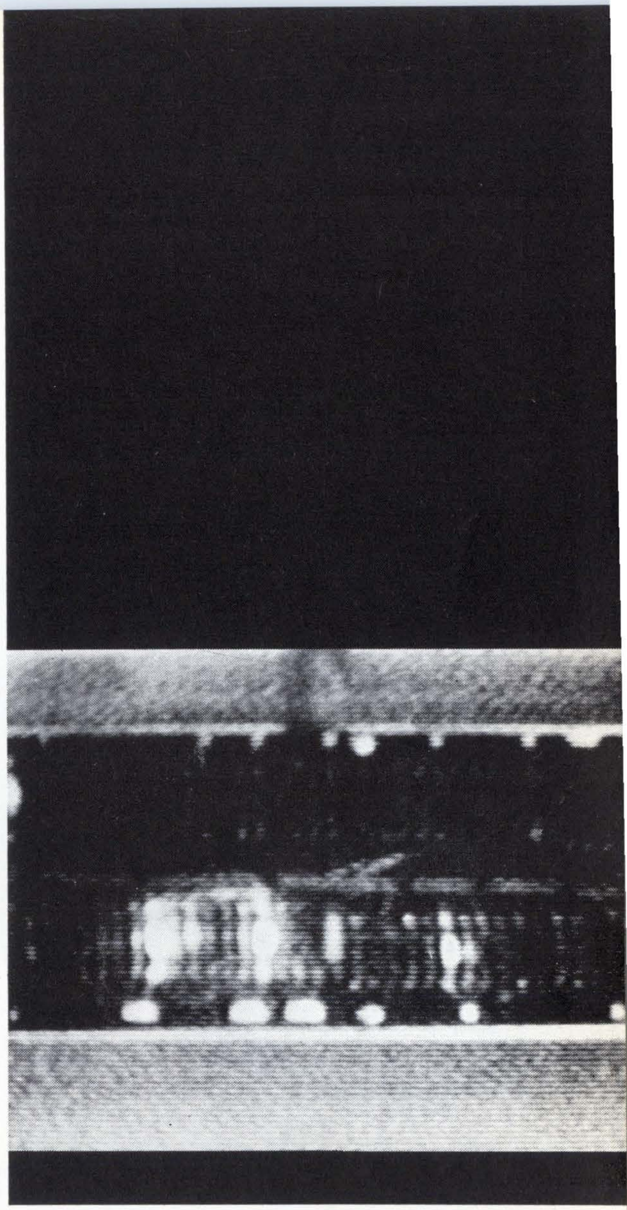
U.S. copter system is studied by Bonn

West Germany may be a customer for the Navy's integrated helicopter avionics system, which is nearing the production stage at Teledyne Inc. in Hawthorne, Calif. **Some of the project's subsystems, such as stationkeeping radar, are being suggested for use in German military helicopters;** Pentagon and Teledyne representatives are briefing Bonn officials in Germany this month.

Addenda

The Internal Revenue Service **is seeking $1 million next year for optical scanner research and $2 million for electronic direct data entry equipment** . . . The Food and Drug Administration will set up an **automatic laboratory in St. Louis to increase testing of drug samples from 40,000 annually to 1 million.** A computer will tie together a modular complex of sorting, testing and evaluation equipment . . . Electronics companies spent $122 million of their own money in 1965 on basic research, up $10 million from 1964, and $304 million on applied research, up from $280 million. **Company-funded development hit $1.487 billion, up from $1.445 billion in 1964,** according to figures released by the National Science Foundation . . . **Industry meetings may have to scratch policy briefings by Federal Communications Commission officials** from their programs unless they can pick up the travel and per diem tab. The FCC has already spent all of its fiscal 1967 funds for these items.





What defect lurks in the shadows of this PC board?

. . .The Scanner knows!

Faulty diodes, overheating resistors, cold solder joints give themselves dead away under the searching eye of Sierra's Model 710B Infrared Scanner. And fast! The scanner puts the heat on hidden problem makers in as little as five seconds.

Model 710B functions as a closed-circuit television system that sees heat instead of light — an ideal setup for nondestructive testing. Point the scanner at an object, such as our PC board above, and seconds later a detailed thermal map appears on the scope (photo above right). Cool components remain relatively dark. Flaws show up as hot spots. By running a scan line you can measure absolute temperatures across the board. Model 710B lets you stop the scan at any point to study individual segments.

The scanner resolves thermal detail down to 0.03 inch at 3½ inches, discriminates gradients of 0.6°C. You can vary optical attenuation from 2°C to 1200°C black-to-white. The instrument scans a complete raster in five seconds, forming an image containing approximately 15,000 picture elements.

Model 710B consists of a precision scanner, tripod, power supply, dual-scope console, and Polaroid camera with special scope mount. For further data and detailed applications information, write Sierra, 3885 Bohannon Drive, Menlo Park, California 94025.

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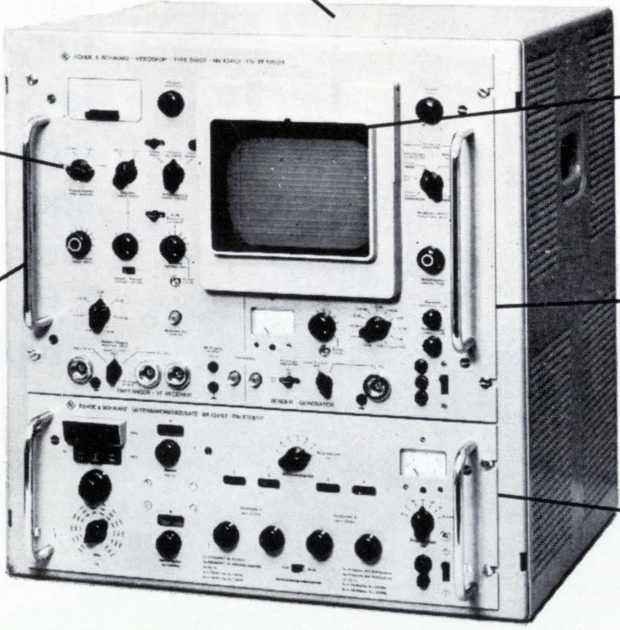

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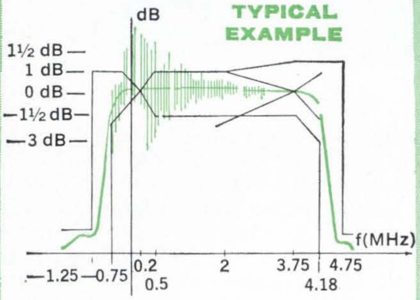
SWEPT FREQUENCY SYSTEM

FEATURES:

- Complete test system: Sweep Signal Gen., Selective Tracking Receiver, Large Display Unit
- Frequency range: 20kHz — 20MHz
- Sweep width: 1-16MHz
- Sweep rate: .2 to 20 sweeps/sec.
- Selective tracking receiver: 3kHz bandwidth
  - Permits measurements in presence of sync. and blanking pulses
  - Use as spectrum analyzer
- Separate audio and video inputs
- Use as Sweep Source and Plotting Detector with R/S Type LFM Group Delay Test Set

MEASURE:

- Absolute and relative amplitude-frequency response
- Return loss
- Transmission characteristics of TV units
- Amplitude characteristic of TV Test Demodulator



Vestigial sideband characteristic of a TV channel signal generator (SBTF). Test condition: Sweep component in composite picture signal 10% of picture, set-up at picture white. Combination of analyzing and sweeping methods permits the sideband characteristic to be studied between the pulse spectrum lines.

Videoskop is a complete visual display sweep frequency system covering the range of 20kHz to 20MHz. An optional sideband adapter ($5,605) extends the range to 1,000MHz and permits measurement of sideband characteristics to within 50kHz of TV picture carrier. Type SWOF Videoscope provides an automatic display of the amplitude response of a test item instantaneously, thereby eliminating point-by-point measurements. Level meter, calibrated input and output attenuators, and crystal marker generator (0.5, 1.0, 5.0MHz, EXT.) permit absolute measurements. Selective tracking receiver makes possible plotting of characteristics of TV systems in the presence of sync. and blanking pulses. It further eliminates errors due to harmonics and can be used as a spectrum analyzer. Measuring range is 40dB dynamic and 100dB overall. By substitution attenuation or gain as small as 0.1dB can be easily measured. Accessories available: single sideband adapter, camera adapter, graticules in accordance with FCC TV-transmission standards and custom graticules to your specifications.

Get The Extra Capability, Greater Reliability, and Longer Useful Life Of . . .

ROHDE & SCHWARZ

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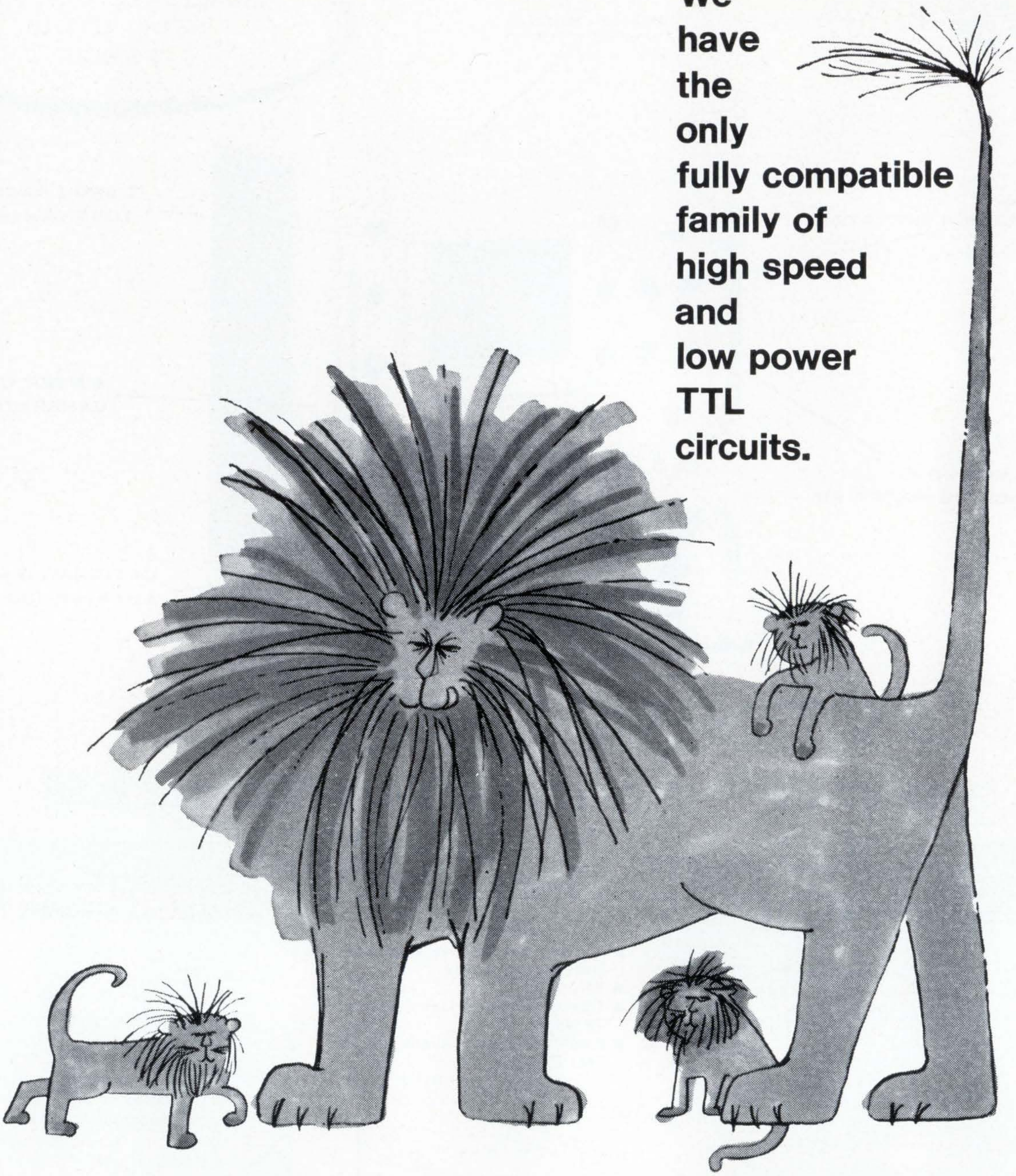
Inquiries outside the U.S.A. should be directed to Rohde & Schwarz, Muehldorfstrasse 15, Munchen 8, West Germany

Circle 67 on reader service card

We have the only fully compatible family of high speed and low power TTL circuits.



You can go wild with Signetics new Designer's Choice 8000 Series: it gives you the widest selection of design trade-offs in speed, power, noise immunity and price ever offered in a TTL family. The family consists of a very high speed set (the 8800's) and a fully compatible but slower low power set which offers very high AC noise immunity. Now TTL system designs can be optimized without laborious calculations, unusually expensive and time-consuming special ground-plane designs, or extensive use of outboard discrete components in areas where the highest possible speed is not required. All you do is follow the published S8000-series usage rules. All circuits are compatible over the full MIL temperature range of −55°C to +125°C and are available off-the-shelf in Signetics 14-lead glass-Kovar flat pack. Hunt up your local Signetics distributor. For further information on the Designer's Choice 8000 Series, write Signetics, at 811 E. Arques Avenue, Sunnyvale, California 94086. ■ At the IEEE Show, be sure to check into Rooms 3000A & B at the New York Coliseum, for latest Signetics news.

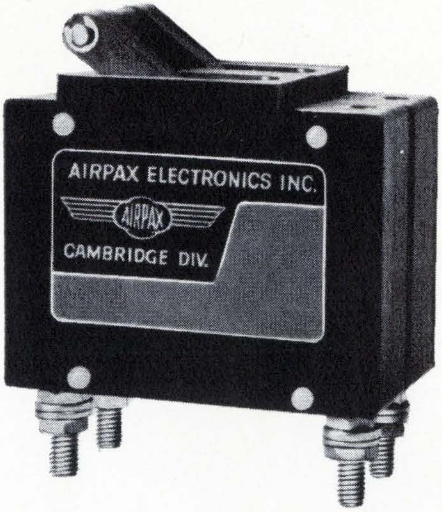
TYPE	DESCRIPTION		
S8416	Dual 4-Input Nand Gate	S8816	Dual 4-Input Nand Gate
S8417	Dual 3-Input Nand Gate	S8825	DC Clocked J-K Binary Element
S8424	Dual AC Binary Element	S8826	Dual J-K Binary Element
S8440	Dual Exclusive-Or Gate	S8840	Dual 4-Input Exclusive-Or Gate
S8455	Dual 4-Input Buffer/Drive	S8855	Dual 4-Input Power Gate
S8480	Quadruple 4-Input Expander	S8870	Triple 3-Input Nand Gate
S8806	Dual 4-Input Expander	S8880	Quadruple 2-Input Nand Gate
S8808	8-Input Nand Gate		

SIGNETICS INTEGRATED CIRCUITS

A SUBSIDIARY OF CORNING GLASS WORKS

Circle 69 on reader service card→

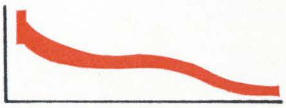
MATCH PROTECTOR TO HARDWARE



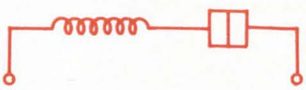
An APL Circuit Protector–

will rupture a fault of 5,000 amperes at 240 volts!

provides a time delay for every demand!

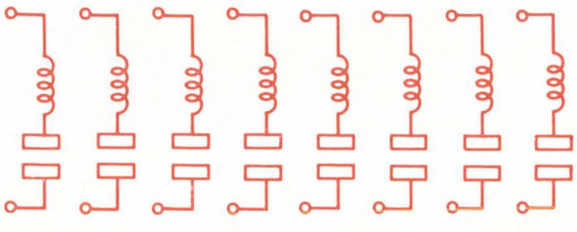


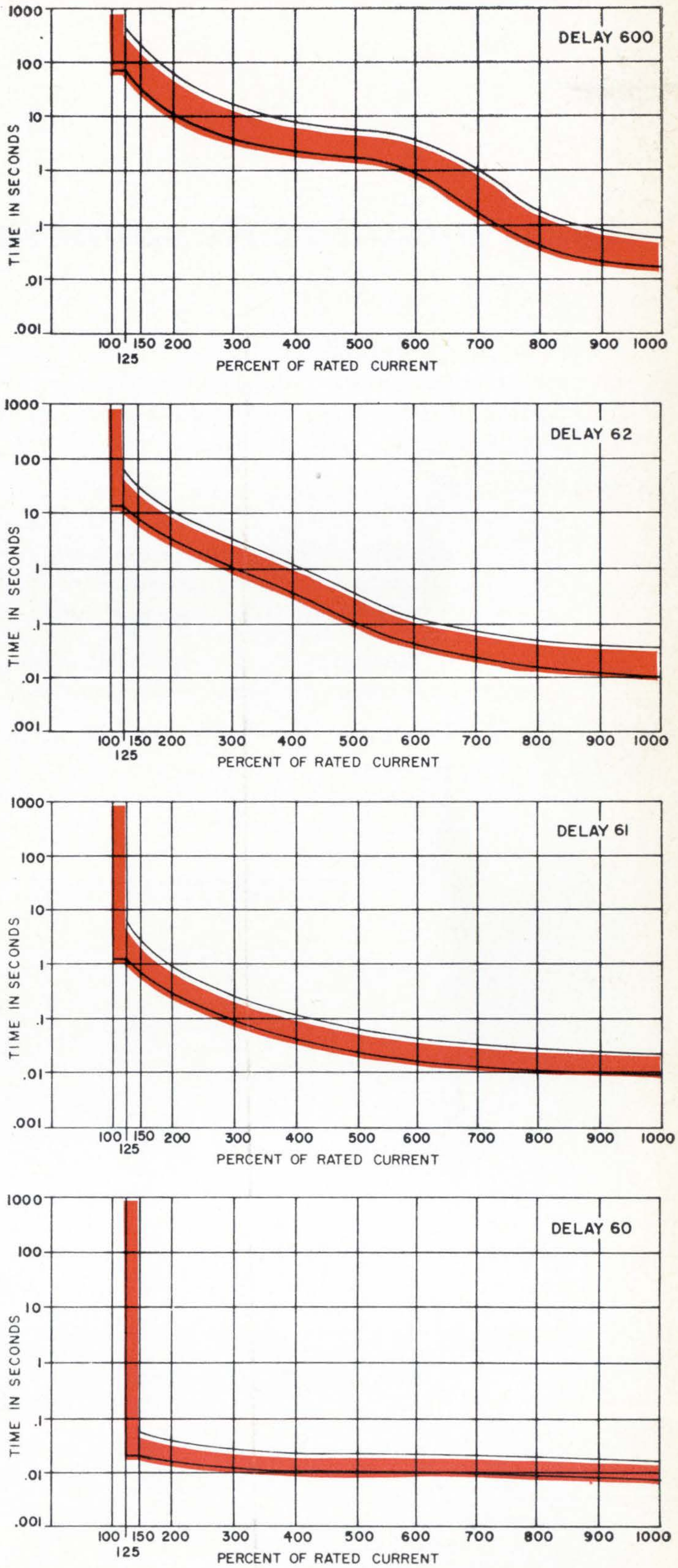
is entirely magnetic — no heater elements!



Tripping coils can be completely isolated!

Gang every circuit together!

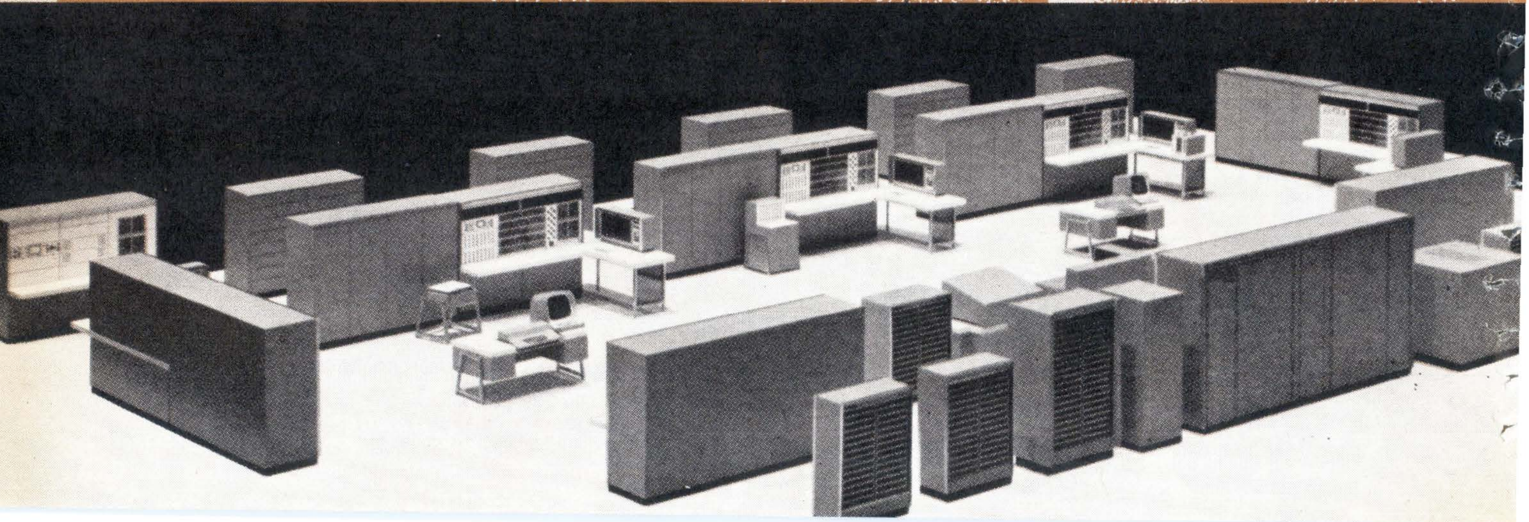




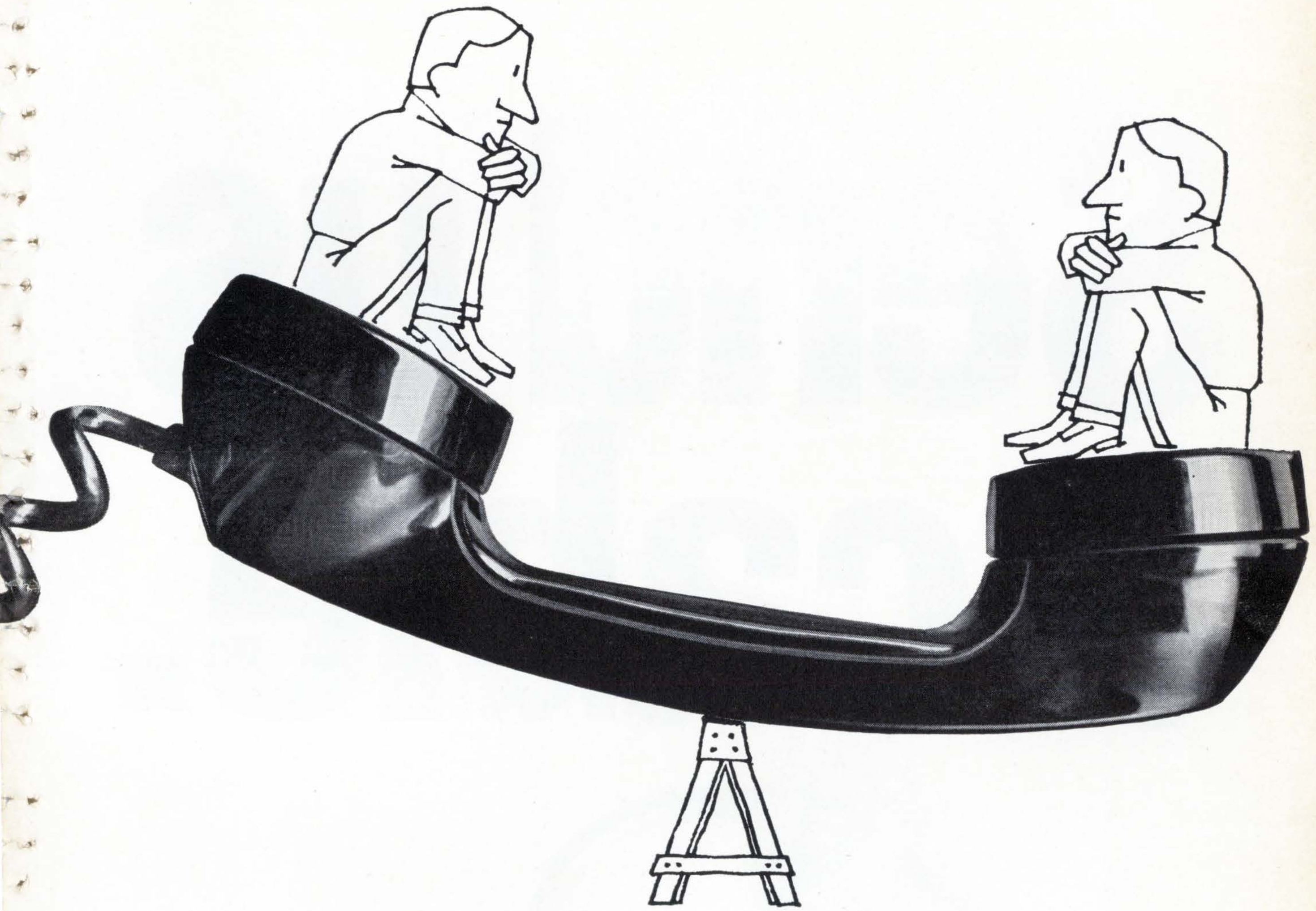
TYPICAL 60 CYCLE DELAYS

AIRPAX ELECTRONICS

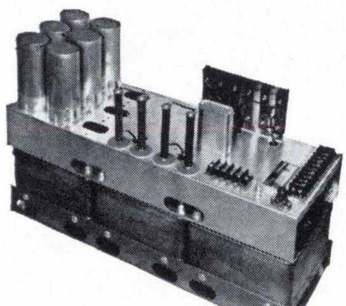
CAMBRIDGE, MARYLAND 301-228-4600



can't decide to make or buy your power supplies?



call 312 439-2800



Sola quotes both ways.

First, we'll quote an entire custom-built Sola power supply—designed to your specs by power supply specialists. Second, we'll tell you the cost of a custom Sola CV® transformer. And give you the ratings of other components, too, so you can build your own power supply.

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Send us a cable.

Send us a small sample, at least one foot, of the coaxial cable you're using and tell us what you're using it for. Then we'll install the Burndy crimp removable coax contact that'll do the job best. Guaranteed.

A tough job? Not really.

Remember, crimp removable contacts began at Burndy. As a result Burndy offers the most complete line of coaxial connectors for standard, miniature and sub-miniature coaxial cables. And they're available for all rectangular, rack and panel and terminal block configurations.

Send your sample along to Mr. M. Elkind, Product Manager, Burndy, Norwalk, Conn. He'll see that the job is done and returned quickly. You'll receive our latest coax connector catalog, too.

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INTERNATIONAL SALES HEADQUARTERS AND MANUFACTURING FACILITIES:
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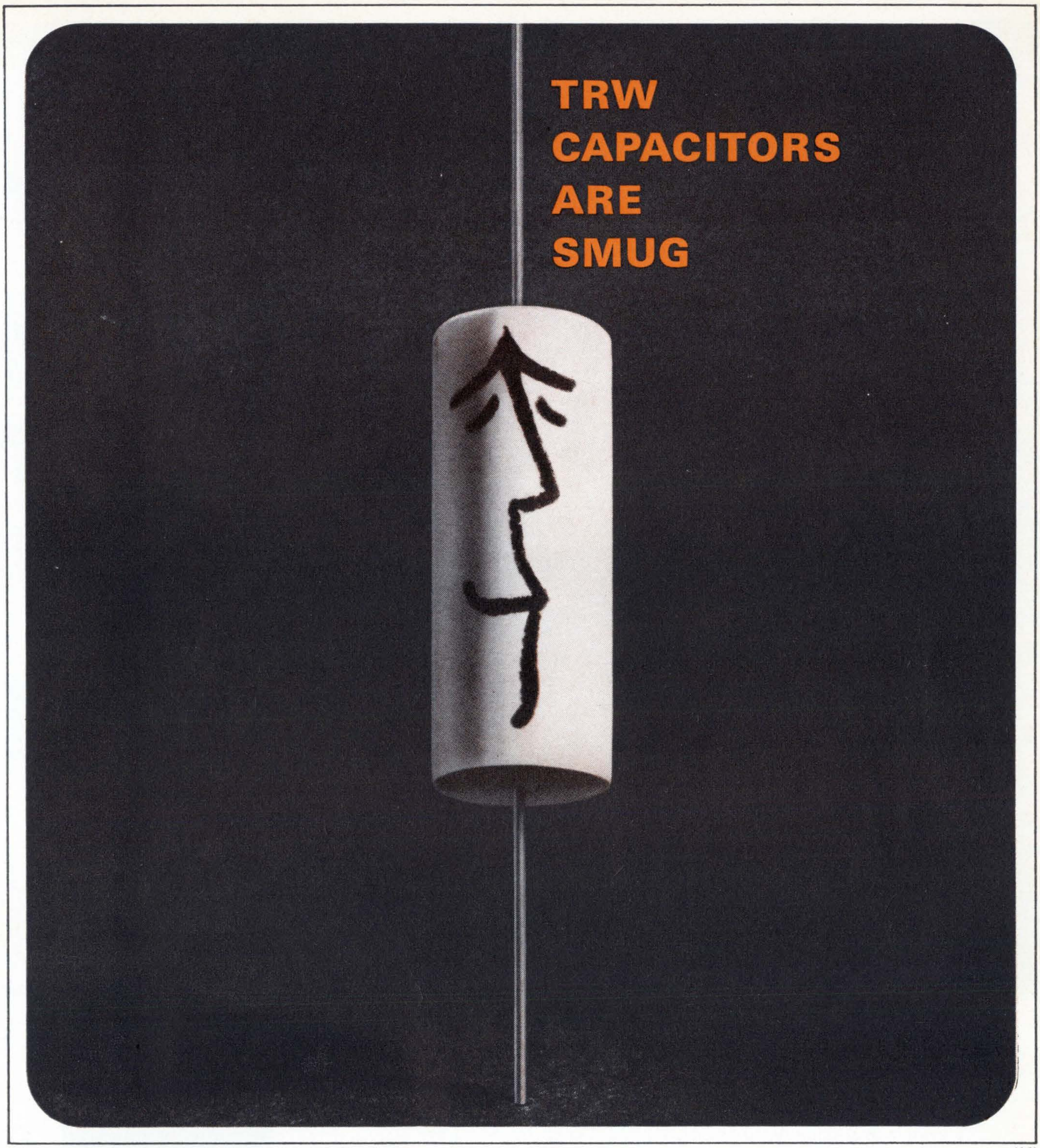


14-61

. . . especially our new metallized polycarbonates!

TRW has now extended its leadership in film capacitors to include metallized polycarbonate types. Two features of the X463UW are outstanding. Precise processing assures low TC through temperature ranges to 125° C. Metallized construction reduces size to less than one half that of film-foil designs. Other features of the line include:

- Capacity range from .01 to 10.0 mfd
- Low dielectric absorption
- Available in tolerances to ± 1%
- Humidity resistance per MIL-C-27287

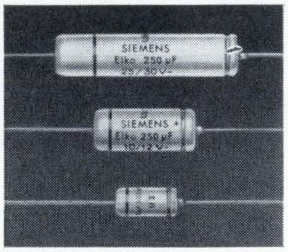
For full information contact: TRW Capacitors, Box 1000, Ogallala, Nebraska. Phone: 308-284-3611 • TWX: 910-620-0321.

TRW CAPACITORS

Circle 77 on reader service card

durability

Performance tests of up to 64,000 hours (approx. 8 years) show that Siemens electrolytic capacitors can operate as long as all other types of capacitors. This is achieved through an optimum balance of dissipation and corrosion. Siemens electrolytic capacitors feature minimum size along with maximum performance, and are available out of stocks in White Plains, N.Y. Tell us your application, we'll be glad to show you how adaptable they are. It's child's play.



SIEMENS ELECTROLYTIC CAPACITORS

99.99% pure aluminum for the anode makes it possible for Siemens to project performance capability accurately for usage up to 100,000 hours (approx. 12 years). Special sealing technique and choice of materials assure longest possible operational span of electrolyte. Siemens components include ferrite materials, metallized polyester and polystyrene capacitors, all electronic and microwave tubes, rectifiers and a complete line of semi-conductors.

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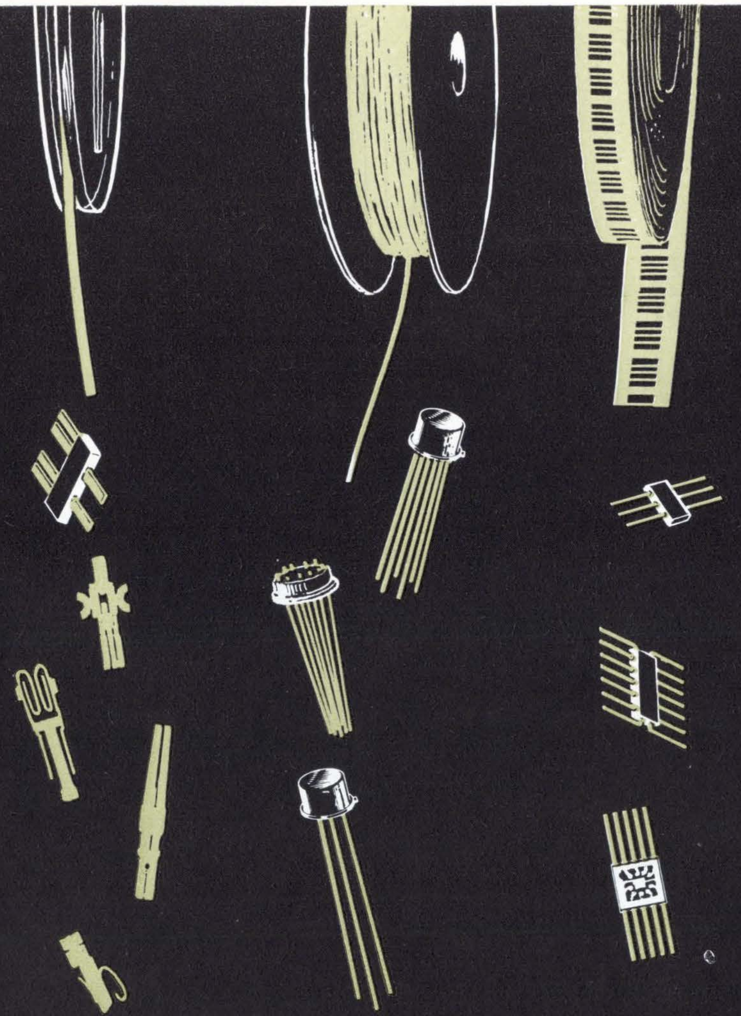
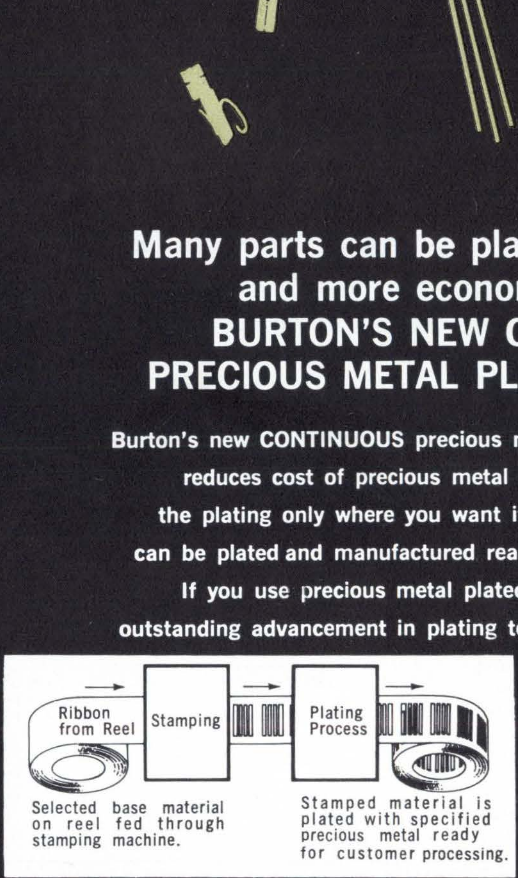


Many parts can be plated better, faster, and more economically with BURTON'S NEW CONTINUOUS PRECIOUS METAL PLATING PROCESS

Burton's new CONTINUOUS precious metal plating process normally reduces cost of precious metal substantially by putting the plating only where you want it. In addition, some parts can be plated and manufactured ready for your use (see inset)! If you use precious metal plated parts of any kind this outstanding advancement in plating techniques may save you time and money while greatly improving quality. Why not find out about it? We'd be glad to send you complete information.



BURTON RESEARCH LABORATORIES, INC.
11240 PLAYA / CULVER CITY, CALIFORNIA / (213) 391-6325
A Division of Burton Silver Plating Company

NEW

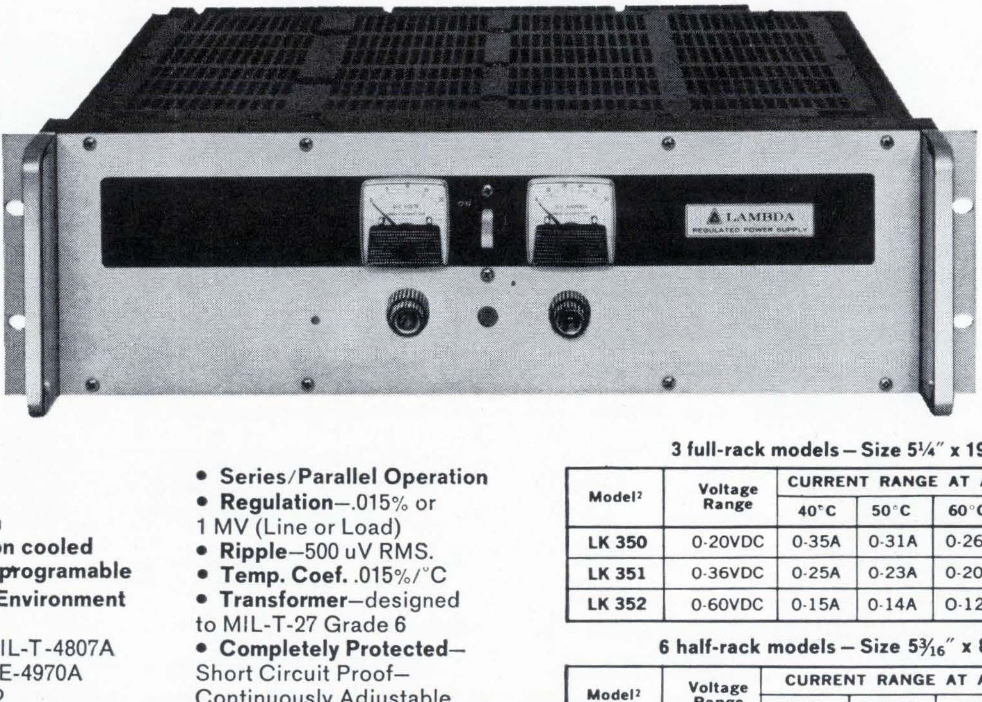
Lambda high current LK Series power supplies

0-20, 0-36, 0-60 VDC • up to 35 amps • 5¼" height • starting at $330.

5¼"

HALF RACK

5¼"



FULL RACK

5 Year Guarantee

Features

- **All Silicon**
- **Convection cooled**
- **Remotely programable**
- **Meet Mil-Environment specs**
  Vibration, MIL-T-4807A
  Shock: MIL-E-4970A
  - Proc. 1 & 2
  Humidity: MIL-STD-810
  - Meth. 507
  Temp. Shock: MIL-E-5272C
  - (ASG) Proc. 1
  Altitude: MIL-E-4970A
  - (ASG) Proc. 1
  Marking: MIL-STD-130
  Quality: MIL-Q-9858
- **Remote Sensing**
- **Series/Parallel Operation**
- **Regulation**—.015% or 1 MV (Line or Load)
- **Ripple**—500 uV RMS.
- **Temp. Coef.** .015%/°C
- **Transformer**—designed to MIL-T-27 Grade 6
- **Completely Protected**— Short Circuit Proof— Continuously Adjustable Automatic Current Limiting
- **Constant I./Constant V.** by automatic crossover
- **No Voltage Spikes or Overshoot** on "turn on, turn off" or power failure
- **Wide Input Voltage and Frequency Range**—105-132 VAC, 47-63 cps

Rack or Bench use—rubber feet included for bench use.

3 full-rack models – Size 5¼" x 19" x 16½"

Model[2]	Voltage Range	CURRENT RANGE AT AMBIENT OF:[1]				Price[2]
		40°C	50°C	60°C	71°C	
LK 350	0-20VDC	0-35A	0-31A	0-26A	0-20A	$675
LK 351	0-36VDC	0-25A	0-23A	0-20A	0-15A	640
LK 352	0-60VDC	0-15A	0-14A	0-12.5A	0-10A	650

6 half-rack models – Size 5³⁄₁₆" x 8⅜" x 16½"

Model[2]	Voltage Range	CURRENT RANGE AT AMBIENT OF:[1]				Price[2]
		40°C	50°C	60°C	71°C	
LK 340	0-20VDC	0- 8.0A	0- 7.0A	0- 6.1A	0-4.9A	$330
LK 341	0-20VDC	0-13.5A	0-11.0A	0-10.0A	0-7.7A	385
LK 342	0-36VDC	0- 5.2A	0- 5.0A	0- 4.5A	0-3.7A	335
LK 343	0-36VDC	0- 9.0A	0- 8.5A	0- 7.6A	0-6.1A	395
LK 344	0-60VDC	0- 4.0A	0- 3.5A	0- 3.0A	0-2.5A	340
LK 345	0-60VDC	0- 6.0A	0- 5.2A	0- 4.5A	0-4.0A	395

[1] Current rating applies over entire voltage range.
[2] Prices are for non-metered models. For metered models add suffix (FM) to model number and add $30.00 to price.
[3] Overvoltage Protection: Add suffix (OV) to model number and add $70.00 to the price for half-rack models; $90.00 for full-rack models.

LAMBDA ELECTRONICS CORP.
515 BROAD HOLLOW ROAD • MELVILLE, L. I., NEW YORK • 516 MYRTLE 4-4200
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LA-173

Name your failure rate

this G-E sealed relay will give it to you

But you have to let us establish:

- level of confidence
- operating conditions
- what constitutes a failure

By varying these conditions, we can give you any failure rate you want.

Doesn't make sense, does it? You're supposed to set the conditions. Not us.

That's why we don't establish failure rates till you give us application information.

If we did, we'd hurt you. And us.

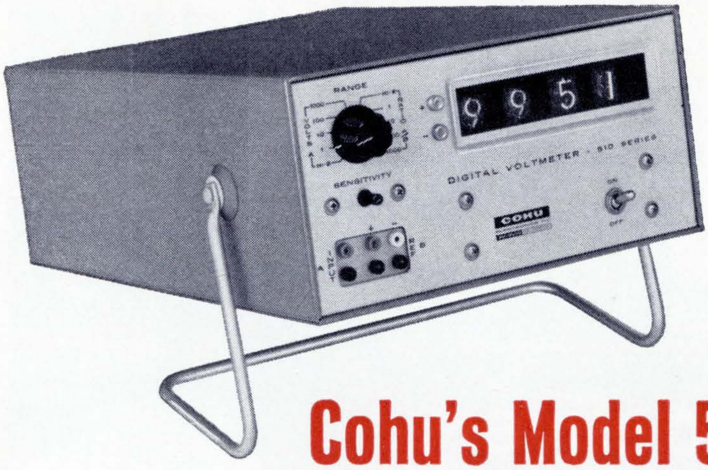
You, because you might buy the wrong relay.

Us, because we might hurt our reputation and lose you—a valued customer.

Want realistic failure rate data and the best relay for your next project? Contact your G-E Electronic Components Sales Engineer. Or for latest catalog information, write General Electric Company, Section 792-40, Schenectady, New York 12305.

GENERAL ELECTRIC

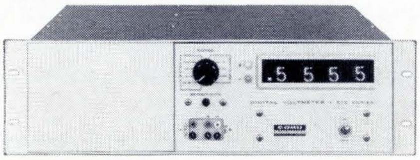
Now available in 16 different configurations – all with 0.01% accuracy –



Cohu's Model 510 Series Digital Voltmeter-Ratiometer!

This highly reliable and stable instrument is now being delivered in models to meet virtually every application–laboratory, bench and assembly line. The basic cabinet model weighs only 12 lbs. and sells for $995, while the basic rackmount model is $1050. Both prices are FOB San Diego. Additional export charge.

The 510 series is available either with manual ranging only or optionally with both manual and automatic ranging of the four voltage ranges. Electrical output options are biquinary, 1248 BCD, or 1224 logic level outputs, enabling this DVM to drive most types of digital recording devices. An optional accessory probe is also available.



These features are common to all models in the 510 Series:

- 0.01% ±1 digit accuracy
- automatic polarity indication
- 4-place reading on all ranges
- 4 manual ranges, 2 functions (1V to 1000V, 1:1 to 1000:1 ratios)
- single control, range and function
- front panel sensitivity control
- high input resistance
- solid-state reference and circuitry
- bidirectional tracking logic

For full details, contact Cohu engineering representatives in major cities throughout the world.

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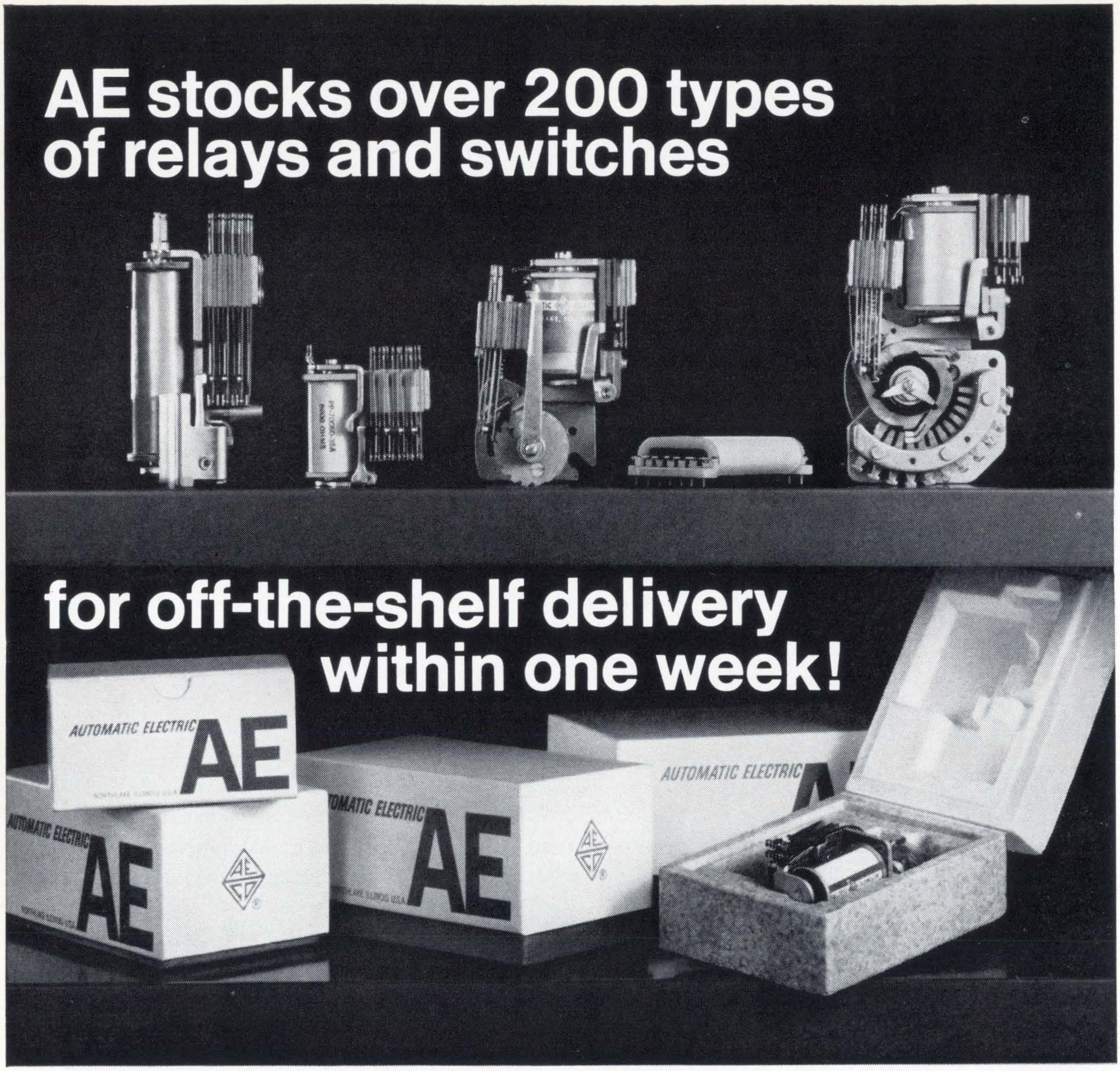

Get fast, direct delivery—at no extra charge. Thanks to the Automatic Electric Stock Program.

This program keeps growing. Now, we stock over 200 kinds of relays, switches, and accessories. In large enough quantities to fill your normal prototype requirements within 7 days.

That means fast delivery on many of the most popular types from AE's broad line. EIN (integral socket) relays with power contacts; mercury-wetted-contact relays; PC Correeds; rotary stepping switches with gold levels for dry- and low-level circuits; ERM (magnetic latching) relays; Class E relays with four different wire termination methods; and many more.

Send for a free copy of Circular 1053, our newest "Stock Letter." It's the latest listing of items you can get quickly. Just write to the Director, Relay Control Equipment Sales, Automatic Electric, Northlake, Illinois 60164.

AUTOMATIC ELECTRIC

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Here's an engineer's magazine even your wife will love

It's the *portable* chart paper magazine from our new Mark 250 Strip Chart Recorder. Now you can take the record home with you, or any place for that matter! Manual turning knobs let you roll the chart forward and back. Later, you can re-record on the same chart for side-by-side comparison. Chart take-up is automatic. And you can reload the magazine in seconds. (Many users get an extra magazine . . . study one while the other is in the recorder.)

But the world's slickest chart magazine is just one of the Mark 250's great new features. Step response over the full 4½-inch span (10% to 90%) is 40 milliseconds . . . records up to 100 cps . . . flat to 10 cps full scale! Choice of 21 interchangeable preamps. Pushbutton selection of 12 chart speeds. Crisp, clear, rectilinear presentation. Patented, pressurized inking system. Owners say there's no other strip chart recorder in the same league.

Words just don't do it. You have to *see* a Mark 250 to understand why it's called "the first strip chart recorder for the perfectionists of the world." A call to your local Brush Sales Engineer brings a Mark 250 right to your office or lab. Go ahead. Even *our* wives will love you for *that*. Clevite Corporation, Brush Instruments Division, 37th & Perkins, Cleveland, Ohio 44114.

CLEVITE

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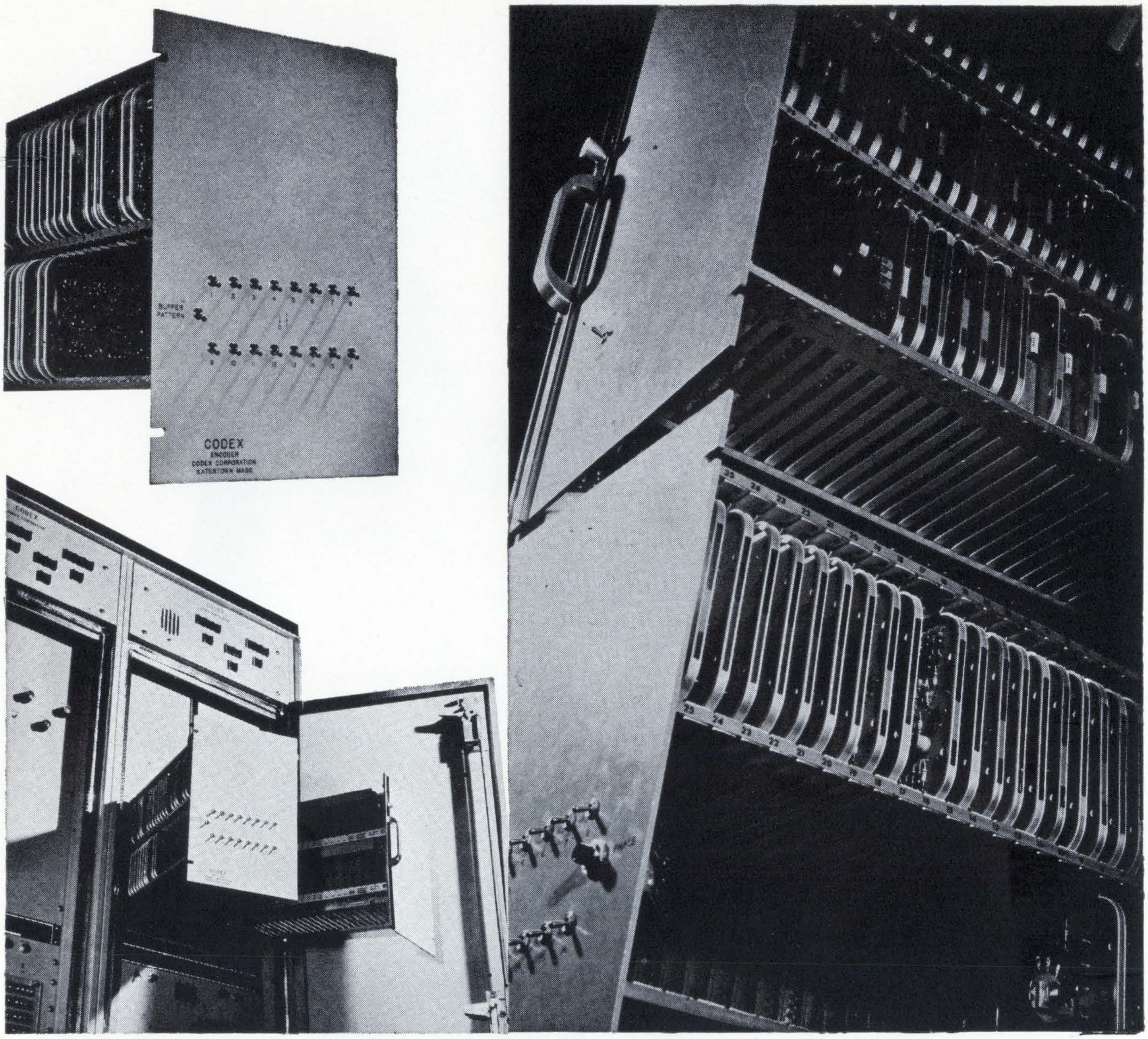


DATA HEADACHE REMEDY!

The Codex CT-1A Digital Communications Terminal is not coding theory. Quite some time ago we made forward-acting error correcting equipment a fact. Daily on-line service in operational systems proves that Codex equipment does transmit high-quality data through low-quality, substandard voice channels.

The CT-1A Terminal is a complete dc in-audio out digital communications terminal. It transmits 1200 bps data with low error rates over any nominal 4 KC circuit except HF radio. The CT-1A Terminal was designed to work over long haul circuits which include one or more tropo scatter hops, but if HF radio is your problem, we have equipment which will handle that too. Three of the terminal's six transmission modes are compatible with the maximum allowable delay of the Autodin system.

For additional information, and our new CT-1A brochure, write, phone, or Telex Codex — the company with the headache remedy for data transmission.

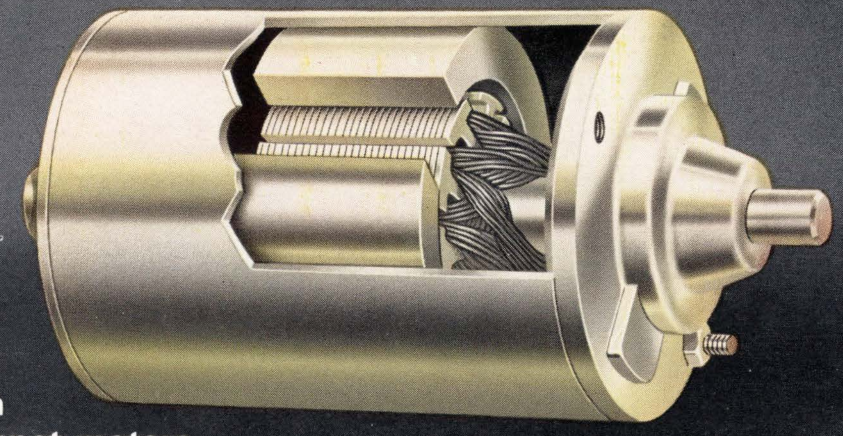
CODEX CORPORATION • 222 ARSENAL STREET, WATERTOWN, MASSACHUSETTS • ZIP CODE 02172 • (617) 926-3000 • TELEX 094-6332 •

Circle 89 on reader service card→

American Bosch

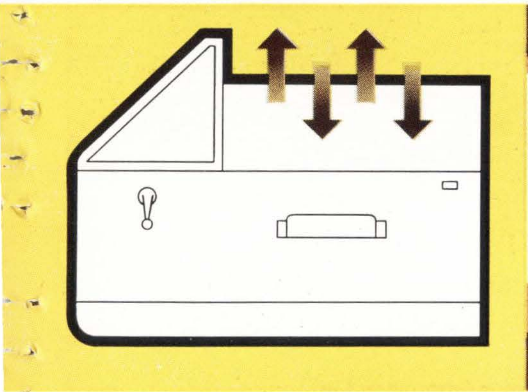
uses Allen-Bradley Oriented Ceramic Permanent Magnets...

because of their uniformity in staying within specifications, and delivery schedules—though tight—are kept!

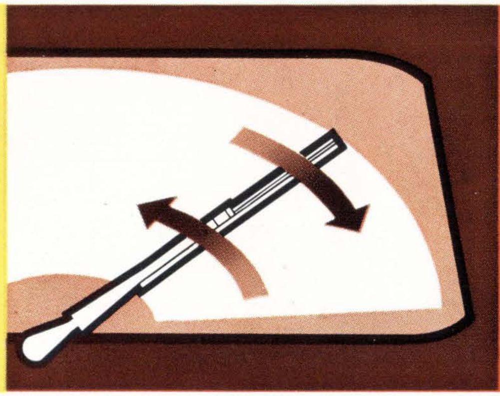


American Bosch permanent magnet motors are used for...

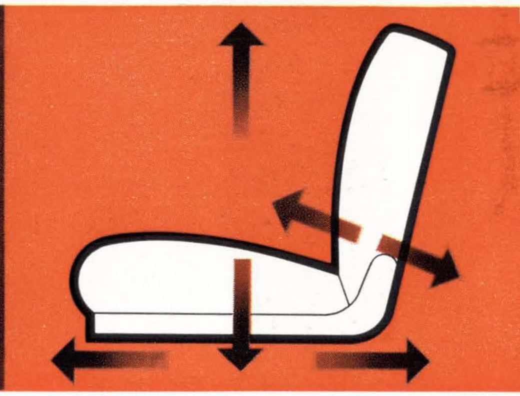
power windows



electric windshield wipers



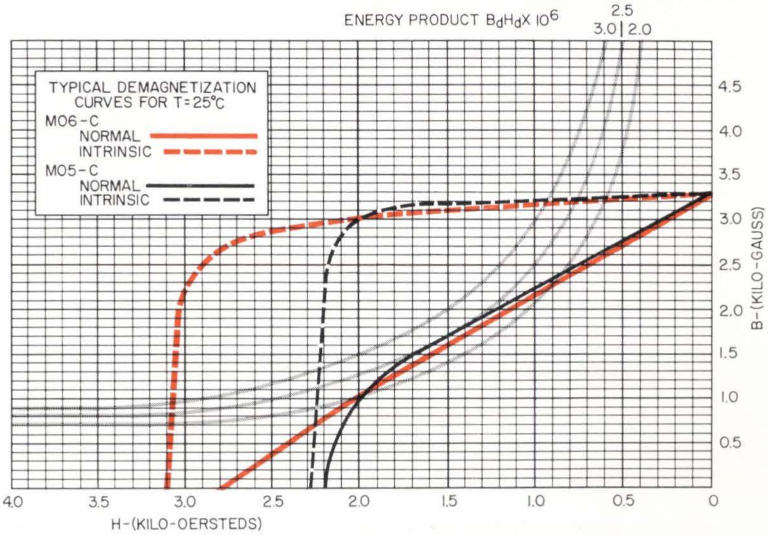
power seats



■ Allen-Bradley's quality control procedures assure the continuously uniform properties—both electrical and physical—that are essential to profitable large volume motor production. The most modern manufacturing facilities in the hands of technically experienced craftsmen produce the highest quality, radially oriented ceramic permanent magnet segments that are presently available.

Allen-Bradley ceramic permanent magnets can be furnished for a wide range of motor sizes—from ¾" diameter up to a 10 hp motor rating. They are available in a variety of types—having different properties—to satisfy your specific requirements. A-B application engineers will be happy to consult with you in developing your dc motors for maximum motor performance. Allen-Bradley Co., 1316 S. Second St., Milwaukee, Wis. 53204. In Canada: Allen-Bradley Canada Limited. Export Office: 630 Third Ave., N.Y., N.Y., U.S.A. 10017.

Properties of typical Allen-Bradley ceramic permanent magnets



ALLEN-BRADLEY

QUALITY MOTOR CONTROL
QUALITY ELECTRONIC COMPONENTS

68-11-6CE

Yes—Allen-Bradley hot molded potentiometers cost more, but—

for critical applications they prove themselves far superior—and well worth the price

■ When a potentiometer in your equipment does not provide the kind of service expected of it—or fails completely—it is only natural for the user to blame you, the manufacturer of the respective instrument. After all, you selected the lower cost component, and your engineer or your purchasing agent decided that "it was good enough." Correcting the mistake usually runs into real money—it does not necessarily eliminate your customer's dissatisfaction. However, you can protect yourself and your customers against such potentiometer failures by joining the ever growing list of the nationally recognized equipment manufacturers who are standardizing on Allen-Bradley potentiometers.

The resistance track of all Allen-Bradley potentiometers is hot molded—a process developed and used only by Allen-Bradley. Resistance adjustment is always smooth—never an abrupt change. Though the initial noise level is very low, it is still further improved with use. The long life of all A-B potentiometers is a fact, established by performance during the many years that these controls have been on the market. For instance, on "speeded up" tests this "life" will exceed 100,000 complete operations, with less than 10% resistance change. And during the 30-year history of this control there has never been recorded a single catastrophic failure.

Protect your reputation as a quality equipment manufacturer by having your purchasing specification call for Allen-Bradley hot molded potentiometers. They are available in single, dual, and triple units. Can be equipped with a 2 ampere 125 volt line switch. Dual units can be supplied with vernier control that provides 20 times finer setability than obtainable with a single control. Units for T, L, and Bridged T and H attenuators are also available. Yes—Allen-Bradley controls *cost slightly more*, but they are *worth much more*. For more details please write: Allen-Bradley Co., 222 W. Greenfield Ave., Milwaukee, Wisconsin 53204. In Canada: Allen-Bradley Canada Ltd. Export Office: 630 Third Ave., N.Y., N.Y., U.S.A. 10017.

62-04-6E

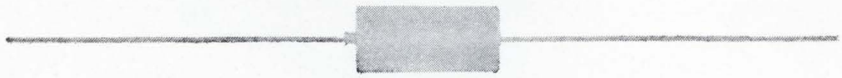
A-B QUALITY

ALLEN-BRADLEY

QUALITY ELECTRONIC COMPONENTS

ELECTRONIC INNOVATIONS IN ACTION

small



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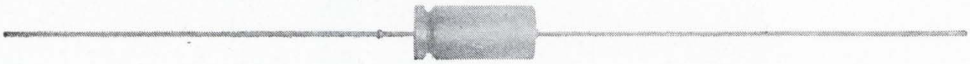


smallest

G.E.'s new wet slug tantalum capacitor gives you the performance of the CL64 in only ½ the case size

Get the highest volt-microfarad product per unit weight and volume of any capacitor you can buy with General Electric's new 69F900 wet slug tantalum capacitor. How? General Electric reduced the case size of the military type (CL64) wet slugs by ½ (it's even smaller when compared to solids). Electrical characteristics and performance remain essentially the same. G.E.'s new 69F900 answers the need for a commerical wet slug capacitor with the high volumetric efficiency demanded by modern high density applications.

G.E.'s new addition to its complete line of tantalum wet slug capacitors has excellent high capacitance retention at low temperatures and can be stored to —65°C. Its wide operating range is —55°C to +85°C. And it meets the parameters of larger military wet slugs: vibration to 2000 Hz, 15g acceleration!

RATING	CASE SIZE	VOLUME
50V, 30μf		
solid (CS12)	.341 x .750	100%
wet slug (CL64)	.281 x .681	58%
69F900	**.145 x .600**	**15%**
15V, 80μf		
solid (CS12)	.341 x .750	100%
wet slug (CL64)	.281 x .681	58%
69F900	**.145 x .600**	**15%**
6V, 180μf		
solid (CS12)	.279 x .650	100%
wet slug (CL64)	.281 x .641	100%
69F900	**.145 x .600**	**25%**

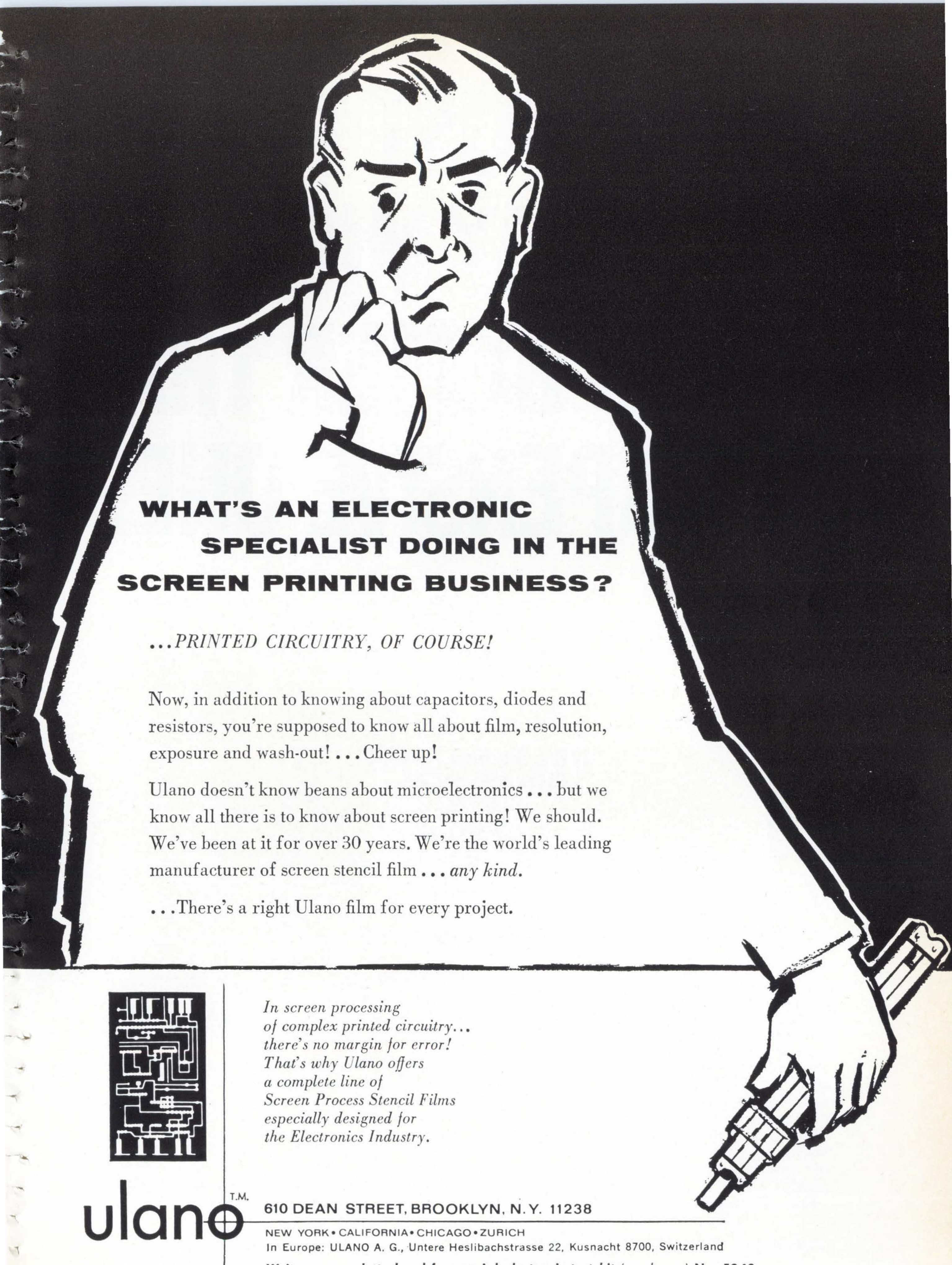
The new sub-miniature 69F900 capacitor is fully insulated and has a low, stable leakage current. Voltage ratings are available from 6–60 volts; capacitance ranges from 3.3–450 microfarads.

Choose from a complete line of G-E wet slug tantalum capacitors to fill your slim, trim circuit needs. Write for GEA-8369 for details about the 69F900 and the other capacitors in General Electric's complete wet slug tantalum line, or ask your G-E sales engineer. **Capacitor Department, Irmo, South Carolina.**

ELECTRONIC COMPONENTS DIVISION

GENERAL ELECTRIC

430-28A



Circle 93 on reader service card

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New Sigma Series 65 miniature relays are specifically designed for low-level DC switching applications where economy is of major importance. Available in quantity for 75 cents, these general purpose relays include extra design benefits:

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Greater Mechanical Strength: Glass-filled nylon, not ordinary phenolic, is used to support contact members assuring long-term mechanical life and stability.

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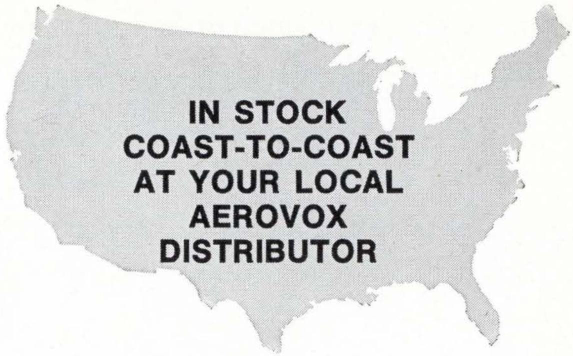
if you're developing prototype hybrid circuits you need this...



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ATTACK INDIVIDUAL MISTAKES
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AEROVOX—the industry's leading supplier of ceramic chip capacitors offers this Engineering Kit to facilitate your prototype development of hybrid circuits. The kit contains 125 chip capacitors in values from 1 pf to 100,000 pf in three basic temperature characteristics (stable, semi-stable and Hi-K) to permit the user to select the smallest chip for any given temperature and capacitance requirement.

The CERALAM capacitor featured in this kit is a rugged, monolithic block of ceramic dielectric and noble metal plate laminated into an extremely dense unit. Because of their unique structure, these units are impervious to moisture and organic solvents. They can be soldered or welded directly into the circuitry. The high ratio of capacity-to-volume inherent with Ceralam capacitors permits significantly smaller sizes suited to hybrid circuitry.

The Chip Capacitor Engineering Kit is available from your local Aerovox Distributor at $59.95. For the name of your nearest distributor or further information write or call. . . .

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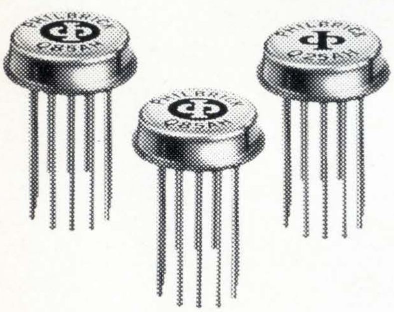
Philbrick's NEW BREED Micro-Hybrid Operational Amplifiers Obsolete Monolithics



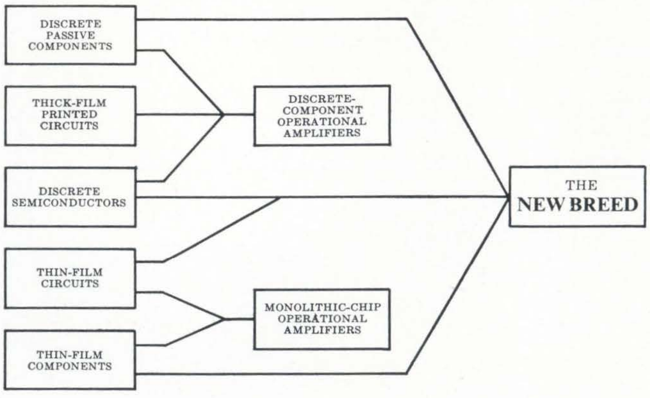
If you are still using monolithic-chip operational amplifiers, your system may be on its way to obsolescence — perhaps even before it gets off the board. A full year of industry-wide evaluation has proved it.

Philbrick's NEW BREED of "micro-hybrid" operational amplifiers combines the best of the linear-monolithic and discrete-component technologies. The result: a line of "micro-hybrid" operational amplifiers unequalled in reliability and performance. You'd expect premium amplifiers like these to cost more. They do — but your total system cost, *including design, development, materials, and production,* is usually substantially *lower* when you use NEW BREED Operational Amplifiers.

You can bid, win, and build highly superior "third-generation" systems with the NEW BREED — systems with an order of magnitude better performance, and absolute immunity to overloads, shorts, and supply-voltage stresses. *Without* the NEW BREED, your analog Aerospace/Weaponry designs are no longer competitive — technologically *or* economically.

More than 200 systems organizations have evaluated (and many have already approved) the NEW BREED. The facts are all assembled in our report entitled *"THE NEW BREED MICRO-HYBRID — A STATUS REPORT."* Write, wire, or phone for your copy. Philbrick Researches, Inc., 000 Allied Drive at Route 128, Dedham, Massachusetts 02026. TWX (617) 326-5754. Telephone (617) 329-1600.

GENETIC EVOLUTION OF THE NEW BREED HYBRID



ELECTRONIC ANALOG COMPUTING EQUIPMENT for MODELLING, MEASURING, MANIPULATING and MUCH ELSE

PHILBRICK

Specification Summary
Model 2936
Universal SSB Test System
10 Hz–30 KHz/1-40 MHz

Model 2736 LF Analyzer and Display Module:

Low Frequency Input Range (Center frequency, digitally read out)	10 Hz to 30 KHz (with calibrated dispersions from 150 Hz to 30 KHz)
IF_1 / IF_2	500 KHz / 1750 KHz — Other IF's on special order request
RF Input Range	1 to 40 MHz (Useable to below 100 KHz and to over 100 MHz)
Low Frequency Sensitivity	100 μV RMS — For full scale logarithmic display. Tangnetial sensitivities are respectively 1 and 10 μV
IF, RF Sensitivity	1 Mv RMS
Manual Sweep	Over full dispersion range
Dynamic Range	All intermodulation products more than 80 db down
Vertical Display:	
Linear	10 to 1 voltage (20 db)—accuracy ± 3%
Log	40 db plus 20 db step for 60 db dynamic range accuracy ± 2 db
Power	Square law (10 db)—±0.25 db
Display	5½ by 4½ inch rectangular CRT with scale illumination
Outputs	Standard X-Y recorder
Dispersion	Six fixed, calibrated dispersion ranges with automatic optimum resolution as listed below

Dispersion Ranges	150 Hz	300 Hz	1 KHz	3 KHz	10 KHz	30 KHz
Resolution Rate	7	7	18	32	100	173
Second/Scan	10	10	3	3	1	1

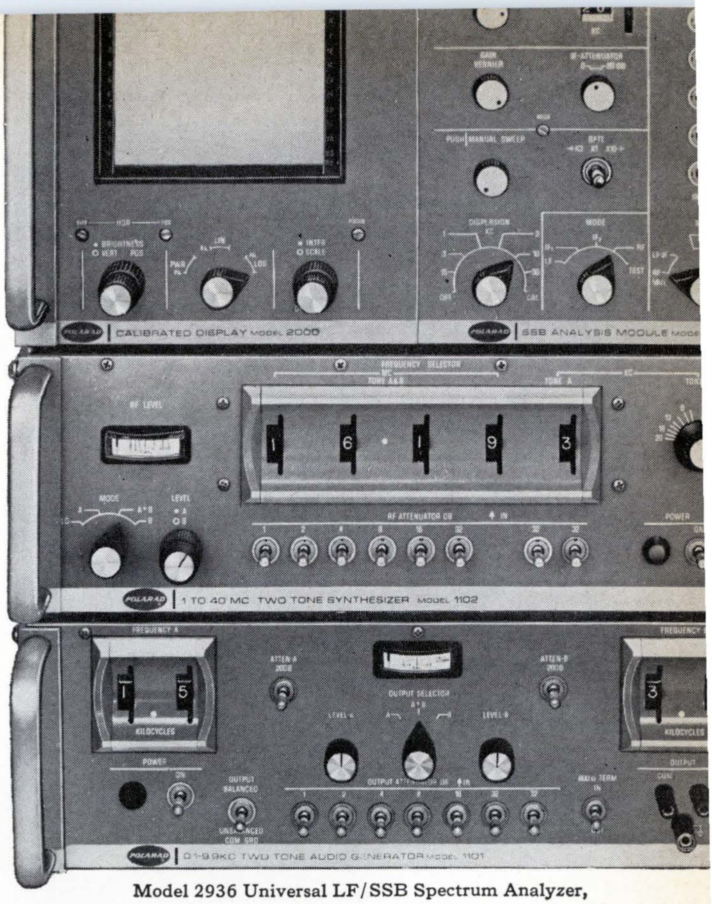
Calibrated Rate Override	X3 and X10, for all dispersions
Low Frequency or Intermediate Frequency Attenuators (100 kΩ input impedance)	80 db in 20 db steps (100 volts maximum input) plus 20 db in one step
Intermediate Frequency or RF Input Attenuators (at 50 Ω input impedance)	63 db in 1 db steps, accuracy 0.1 db/db 20 db in one step

Model 1102 Two-Tone RF Signal Synthesizer:

Frequency Range:	1 to 39.999 MHz with digital tuning in 1 KHz steps. Useable from below 100 KHz to 1 MHz
Frequency Modes	Tone A, Tone B, Tones A+B, L.O. output
Two-Tone Difference	0 to 20 KHz continuously tuned
Frequency Accuracy	0.08% at 10 MHz 0.02% at 39.999 MHz
Output Impedance	50 ohms
Output Level	0 to —127 dbm, calibrated, independent metered vernier output control for each tone
Local Oscillator Output for Analyzer	1.0 Volt, 300 KHz frequency offset
Harmonic Distortion	More than 30 db down
Non-Harmonically-Related Spurious signals	More than 70 db down
Intermodulation Distortion	More than 60 db down

Model 1101 Two-Tone Audio Generator:

Frequency Range	100 Hz to 9.9 KHz with digital tuning in 100 Hz steps
Frequency Accuracy	+2%
Frequency Modes	Tone A, Tone B, Tones A+B
Power Output	+ 10 dbm per tone into 600 ohms
Output Impedance	600 ohms (balanced and unbalanced)
Attenuation Range:	
Each Tone	0 or 20 db in one step independent metered vernier output control for each tone
Combined-tones	9 to 95 db in 1 db steps
Harmonic Distortion	Less than 0.1%
Hum	60 db below output voltage
Intermodulation Distortion	More than 60 db down



Model 2936 Universal LF/SSB Spectrum Analyzer,

It Stands Alone . . .
at the top

the Only *truly* Universal SSB Spectrum Analyzer

The Model 2936 is unique. It is the only spectrum analyzer providing pure, two-tone RF *and* two-tone AF, for accurate, anomaly-free frequency-domain display and measurement of low-frequency and single-sideband signals.

Because it contains independently useful AF and RF signal generators, in addition to the LF analysis module, it is a Universal/AF/RF/SSB Test Set. It will check a complete communications system, from transmitter microphone to receiver loudspeaker, at every point of interest; yet it costs no more than a conventional, limited, pseudo-two-tone spectrum analyzer.

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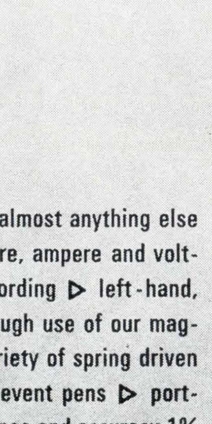

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Technical Articles

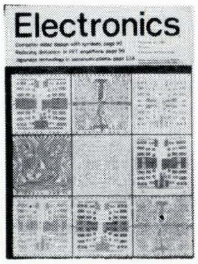
Digital phase shifter tests navigation system
page 104

Like a watchdog watching a watchdog, a new kind of signal generator checks out the monitors that are constantly checking a new VOR aircraft navigation system. An interesting feature of the generator is the way the phases of the output signal are shifted—digitally. The low-frequency phase shifting technique could be used in other applications such as servoanalyzers.

Norad's computers get all the facts
page 113

Although the computers installed in Cheyenne Mountain are not new—in fact their design is at least five years old—unique interface equipment has been developed, along with endless programing, to guarantee that no message is lost. The computer complex is the forerunner of the giant information systems that soon will screen data in other government operations and help run industrial organizations.

Special report: Large scale integration
pages 123 to 182



Large scale integration—putting hundreds and thousands of components on a single slice of silicon—is the next step in integrated electronics. Technically, it brings together important new developments like monolithic technology and computer-aided design. Although some people are saying LSI is a long way off, the evidence in this special report shows it is much closer. Prototype equipment is already being built; commercial production of pioneering items will start within 18 months. For the cover, art director Saul Sussman arranged some of the masks required to make a large integrated array.

Coming March 6

- **New product development at IEEE**
- **Computer-aided design: nonlinear analysis**
- **Selecting digital IC's**
- **Airborne computers**
- **Lunar television**

Digital phase shifter tests navigation system

Logic system in a signal generator simulates operation of new very-high-frequency omnirange system by creating two sets of sine waves whose phases are shifted in hundredths of degrees

By Edwin M. Drogin
Airborne Instruments Laboratory, Cutler-Hammer Inc., Deer Park, N.Y.

Like a watchdog watching a watchdog, a new kind of signal generator is checking out the monitors that are checking out a new VOR aircraft navigation transmission system. The generator digitally generates two sets of low-frequency sine waves and then digitally shifts the phases of the output signals with a resolution of 0.01°.

The prototype of the generator is calibrating new high-precision digital receivers that, in turn, are being used to test an experimental navigation transmitter, called the precision multilobe VOR. The transmitter, a version of a conventional very-high-frequency omnirange navigation system, is being tested by the Federal Aviation Agency at Lake Ronkonkoma, N.Y.

Two versions of the generator have been developed, both built mostly of off-the-shelf monolithic integrated circuits. The first generates signals at 30 and 53 hertz; the phase shift at the higher frequency is 13 times greater than the shift at 30 hz, as a digital "gear changer" in the signal generator multiplies the phase shifts. The second type of generator puts out only 30 hz signals.

Beyond the immediate application of calibrating VOR receivers, there is a good chance the signal generator will be built into automatic checkout equipment. In the near future, large facilities for repairing and testing aircraft navigation systems—such as those operated by major airlines and the FAA—are expected to turn from manual to automatic digital checkout systems.

The basic low-frequency phase-shifting technique of the signal generators could also be adapted to such applications as servoanalyzers. The technique, however, is restricted to low frequencies because high resolution can only be achieved at a clock frequency hundreds of times that of the basic phase-shifted sine wave. If the sine wave frequency were increased significantly, the clocks would require a greater stability and accuracy than is currently possible to maintain the same degree of resolution, probably ruling out such applications as phasor generation in radar systems.

Standard signal generator

Standard 30-hz VOR receivers measure phase changes between two 30-hz sine waves transmitted by a ground station. The phase difference indicates an aircraft's position in relation to the VOR ground station, with each variation in phase of 1° corresponding to 1° of azimuth. In a standard VOR system, both the ground station and aircraft depend on analog equipment.

In the digital signal generator that simulates the standard transmitter, J-K flip-flops generate two 30-hz square waves—one of fixed reference and the other variable—that are converted to sine waves and used to modulate a standard VOR carrier wave. The phase relationship between the reference and variable-phase waves is controlled in the signal generator by a set of five thumbwheel switches that the operator sets between 000.00° and 359.99°. The thumbwheel switches are 10-position rotary mechanical switches whose output is a binary-coded decimal code. The BCD signal controls the operation

The author

Edwin M. Drogin is a consultant in the radar systems department at the Airborne Instruments Laboratory of Cutler-Hammer Inc. He has assisted in the development of systems to evaluate ground navigation equipment for the Federal Aviation Agency.

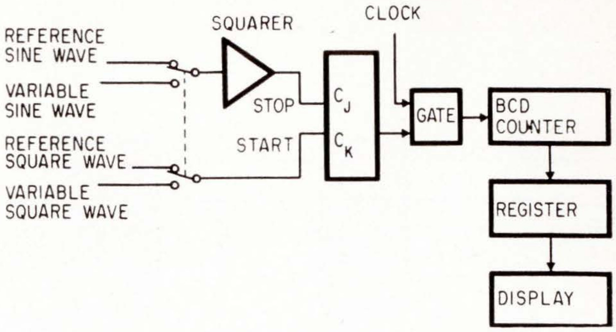
of comparators that set up the phase differences.

After the phase relationship between the two 30-hz square waves has been established, the waves are converted to sine waves by two narrow-band filters at the counter's output. These filters are very stable and do not reduce the 0.01° accuracy of the thumbwheel settings. When the phase-shifts through the reference and variable-phase filters are identical no relative bearing errors occur, and the system accuracy of 0.01° is maintained by a built-in calibration circuit. The calibrator measures the phase shift through the filters by picking off a portion of the sine wave output and converting it back to a square wave, allowing the sine wave's zero crossing time to be accurately measured.

The precision multilobe VOR ground station radiates two sets of waves instead of one. The first set contains the standard VOR signals, while the second set theoretically will allow the special receivers to be 13 times more accurate in determining a plane's bearing. The standard 9,960-hz subcarrier in the second set is frequency modulated at a 53-hz rate, and radio frequency carrier is amplitude-modulated by a 53 hz sine wave which changes in phase by 13° for each degree of azimuth; the larger phase change is expected to provide the greater bearing resolution, while the standard phase change prevents ambiguity in the bearings measured.

Aircraft equipped with the older receivers could still obtain bearing measurements from the first set of signals even if the FAA decides to replace its standard VOR transmitters with the new precision system. Receivers equipped with 53-hz adapters are set up on the ground around the experimental system at Lake Ronkonkoma to monitor the operation of the experimental VOR.

In both versions of the signal generator, the 30-hz signals are derived from a BCD counter driven by a crystal-controlled oscillator. The counter counts repeatedly from 0 to 35,999. Since each count cycle represents 360°, each clock period represents 0.01° of phase; the clock frequency is



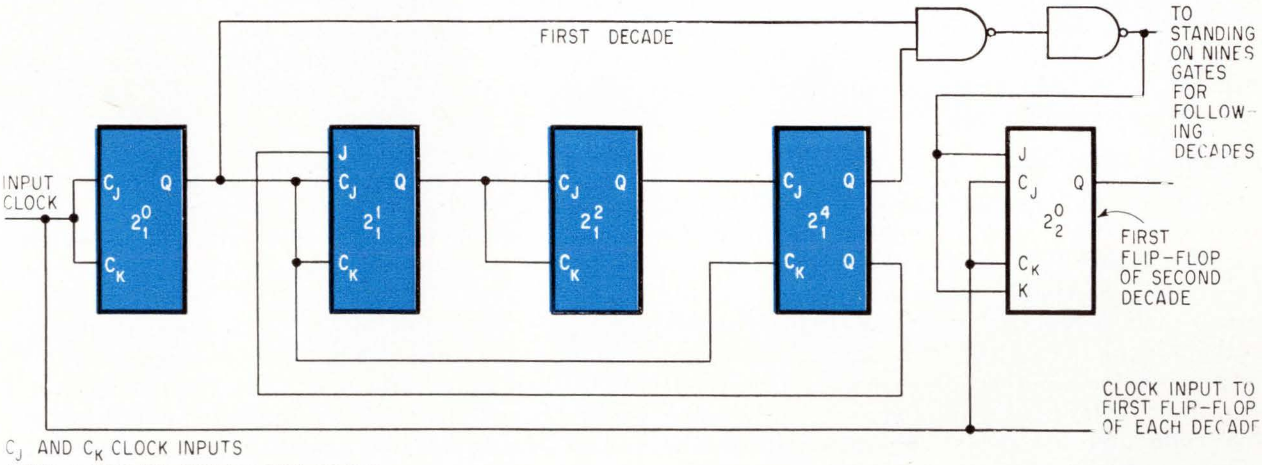
Squarer converts sine waves into square waves so that the zero crossings of the variable-phase and reference signals can be measured accurately by the digital counter.

1.08 megahertz so the counter cycles at 30 hz.

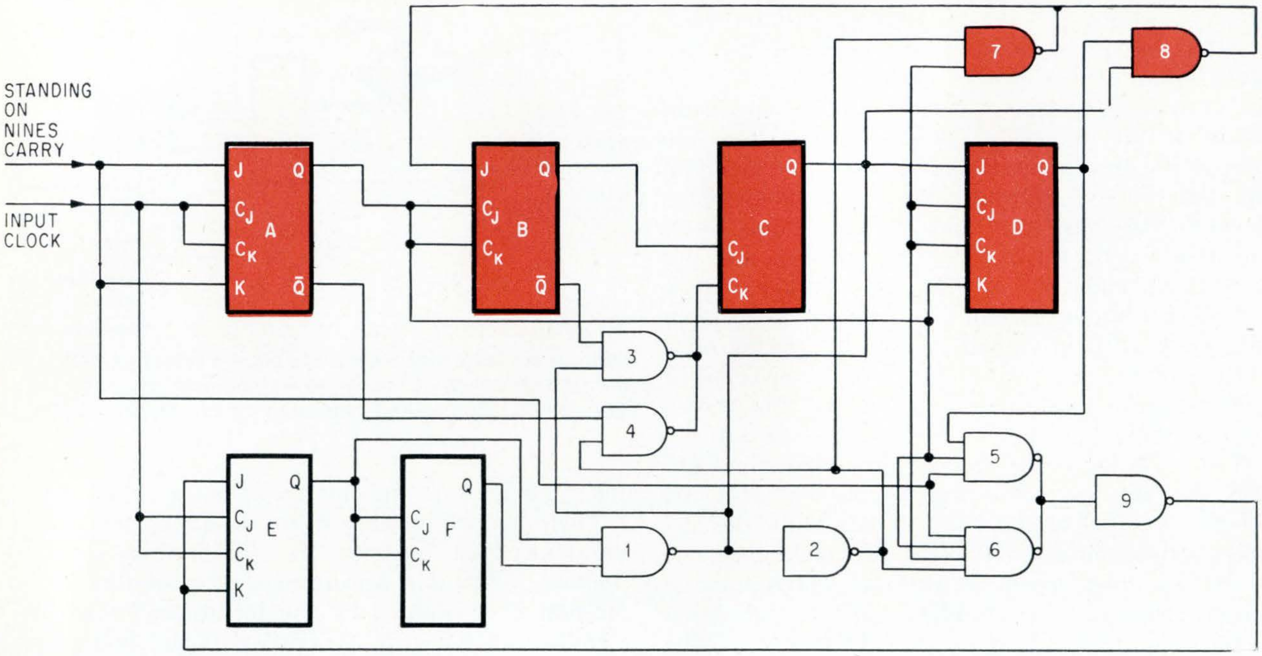
There are 18 flip-flops in the counter chain, with the first four forming the hundredths decade (below). When this decade reaches a count of nine, flip-flop 2^0_2 is enabled by the technique known as standing on nines. This flip-flop is the first stage in the second decade, which counts tenths. When it reaches nine tenths, a similar third decade counting units is enabled.

The tens decade, flip-flops A through D in the drawing on page 106, is of special design because it must be changed from a decade counter to a modulo-6 counter when the two flip-flops in the hundreds counter have counted to three. Hundreds are counted by flip-flops E and F; this counter has only two flip-flops because it must only count up to three, which is 11 in binary notation.

The change in modulus is accomplished as follows: At the count of three in the highest decade, NAND gate 1's output equals $\overline{EF}$ and gate 2's output is EF. NAND gate 7 is therefore enabled and NAND gate 8 disabled. At the count of 5 (represented by the Boolean expression D′ C B′ A, or in binary code as 0101) the outputs of gates 7 and 8 go to logic 0. When the outputs of these digital transistor logic NAND gates are tied together, they perform



Four flip-flops in color make up the first (hundredths) decade in the BCD counter. The flip-flop 2^0_2 at the far right is the first in the second (tenths) counter, and is enabled when the count in the hundredths decade reaches nine.



Tens counter operation is changed from modulo-10 to modulo-6 by the gates in color when flip-flops E and F of the hundreds decade are both at logic 1 (BCD 3). This prevents phase shifts greater than 359.99° in the output signal (an impossible VOR output). Otherwise, the tens decade can count to nine.

an AND function, preventing flip-flop B from going to logic 1 at the next switching of flip-flop A because the J input of flip-flop B is held at 0.

At the same time, NAND gate 4 is enabled so that the change of flip-flop A from logic 1 to logic 0 will pulse flip-flop C. Thus the tens decade resets from 0101 to 0000, never going over 5 when the hundreds counter is at 3. Note that the D flip-flop is prevented from going to logic 1 when C is reset because the clock inputs are 0.

For other states of flip-flops E and F—hundreds count of 0, 1 and 2—the logic is in the standard decade configuration. NAND gates 5, 6 and 9 ensure that flip-flop E will be pulsed to start a new hundreds count when the tens decade is reset from a count of five to zero and when E and F are both at logic 1. When E or F are not at logic 1 and the decade changes from 9 to 0, gates 5, 6 and 9 enable the clock. The 30-hz reference square wave is provided by an additional flip-flop. This flip-flop is triggered when the counter output passes through a count representing 0° and 180°.

Generating the trigger

When the counter output agrees with the thumbwheel settings, a trigger is generated to drive the variable phase flip-flop. Most computers use exclusive OR logic circuits to generate triggers at the correct time. A typical comparator circuit is shown at the top on page 107. This method, however, is unsatisfactory in the VOR generator because it needs three gates per bit and requires that both the true code and its inverse be provided by the thumbwheels. For example, if the outputs of the counter chain are labeled 1, 2, 3 . . . n, and the outputs of the thumbwheel switches are labeled A, B . . . n, coincidence between the counter output and thumbwheel input pulses occurs at (A1 + A′1′) (B2 + B′2′) and so on. When the counts in the BCD counter chain agree with the switch settings, one term in each of the above logic groups will be "true," or at logic 1. Therefore, the over-all expression goes to logic 1. This method thus requires two coded BCD wafers per digit on the thumbwheel or an extra inverting gate per bit in the counter because both A and A′, B and B′ and so forth are needed.

The coincidence circuitry of digital VOR generator's BCD counter only looks for an agreement between the logic 1's in the counter chain and the binary code 1's from the thumbwheels. The logic 0's can be treated as "don't cares" and the following expression used:

coincidence = (A1 + A′) (B2 + B′)

which can be simplified to

coincidence = (1 + A′) (2 + B′)

This is illustrated in the lower part of the drawing, which shows the NAND outputs tied together to implement an AND function.

If one of the NAND gate inputs is at ground, the transistor in that DTL circuit is cut off and at logic 1; that is, if flip-flop 1 is ON or A′ is ON, A is at ground and the first logic gate will have its output transistor cut off. This implements the first term in the coincidence expression (1 + A′). Similarly if all the transistors in the chain are cut off, the common line stays at logic 1. If it weren't possible to tie these outputs together, the NAND gate outputs would have to be fed into a separate multiple-input NAND logic circuit that would drive a second NAND gate to invert the signal and give the correct output.

With this logic circuitry, coincidences will occur as soon as the logic 1's in the counter chain are in the same positions as the logis 1's on the thumbwheels. However, there will be additional coincidences at counts higher than the count set on the thumbwheel. For example, if thumbwheel input A is at logic 1, and B through R are at logic 0 (thumbwheel bearing setting is 0.01°), the first term 1 + A′ will equal logic 0 when the counter chain is at zero. All the remaining terms are always at logic 1 regardless of the state of the counter.

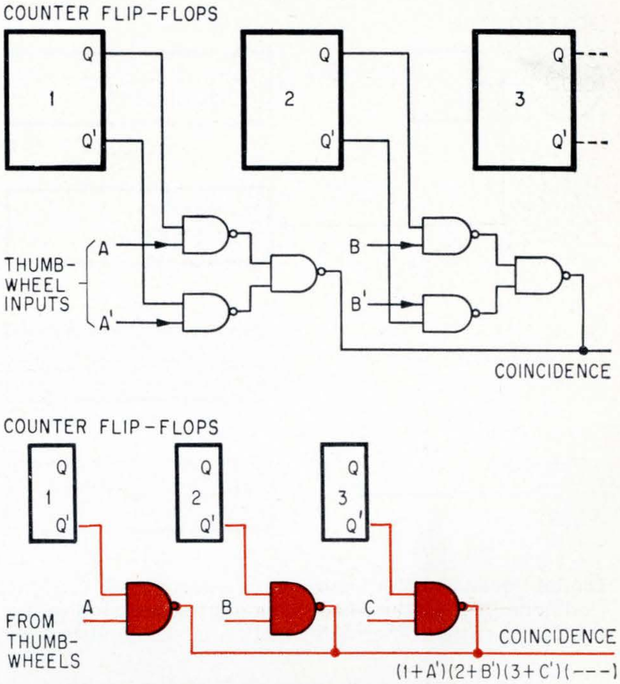
As soon as the counter goes up one count, flip-flop 1 will go to logic 1 and coincidence occurs. However, at every odd count after this—three, five, seven and so forth—the first flip-flop will be at logic 1 and additional undesired coincidences would occur. This is easily prevented, however, by a flip-flop latching circuit set at the first coincidence and not cleared until the next cycle. The extra latching circuitry is worth its cost because the comparison process requires only one gate and one input wire per bit.

Adding angles

To generate the 30-hz variable square wave, triggers must be provided at some phase angle, θ, and $\theta + 180°$, the zero crossing points. It's impossible to provide these triggers by running the BCD counter at a 60-hz rate because the thumbwheel's phase steps would be twice the amount needed. For example, if a 20° phase step were indicated on the thumbwheel and the counter were running at 60 hz, the actual phase step would be 10°. This would cause the triggers to fall at the wrong point and would result in an incorrect bearing output.

Fortunately, providing the $\theta + 180°$ trigger is not too difficult, as indicated by the table that shows the BCD codes for θ and $\theta + 180°$ trigger positions. Only the first five bits of the bearing code are shown because the low-order bits, to the right of the fifth bit, are unchanged when 180° are added to the bearing. There are therefore only 18 codes (0 to 340° in 20° steps) that must be listed. In the θ group, the Boolean expression RQ represents the two lower bits of the hundreds digit and PON represents the three highest bits of the tens digit. Likewise, the hundreds and tens digit in the $\theta + 180°$ group are represented by the Boolean terms rq and pon.

The reason for dropping the excess codes is the commonality between the two columns. Suppose, for example, that θ is an angle 325°. The hundreds digit 3 in BCD code is 11, and numeral 2—the tens digit—in BCD code is 0010. The units digit 5 is 0101 in BCD code, but the last five bits are not shown because they do not change if 180 is added to a bearing. At $\theta + 180°$, the angle of interest is 145° degrees (325° + 180° − 360°). Here the numeral 1 is represented by 01, the numeral 4 by 0100, and the numeral 5 by 0101, the duplicate of the previous number. The Boolean equations r′ through n′ show how the angle $\theta + 180°$ is derived from angle θ.



The output signal is triggered by coincidence between thumbwheel settings and internal count. Conventionally, coincidence is detected by exclusive OR logic (top) requiring three NAND gates per flip-flop. In the signal generator, the coincidence is detected by a comparator (bottom) with only one gate per flip-flop (color) and one input from the thumbwheel.

Conversion of θ to $\theta + 180°$

θ	RQ	PON	θ+180°	rq	pon
0°	00	000	180°	01	100
20°	00	001	200°	10	000
40°	00	010	220°	10	001
60°	00	011	240°	10	010
80°	00	100	260°	10	011
100°	01	000	280°	10	100
120°	01	001	300°	11	000
140°	01	010	320°	11	001
160°	01	011	340°	11	010
180°	01	100	0°	00	000
200°	10	000	20°	00	001
220°	10	001	40°	00	010
240°	10	010	60*	00	011
260°	10	011	80°	00	100
280°	10	100	100°	01	000
300°	11	000	120°	01	001
320°	11	001	140°	01	010
340°	11	010	160°	01	011

Given θ, the Boolean expression for θ + 180° is:

$r' = R + QP + Q'P'O'N'$

$q' = R'Q'(P + O + N) + R'QO'N' + RQ'P'$

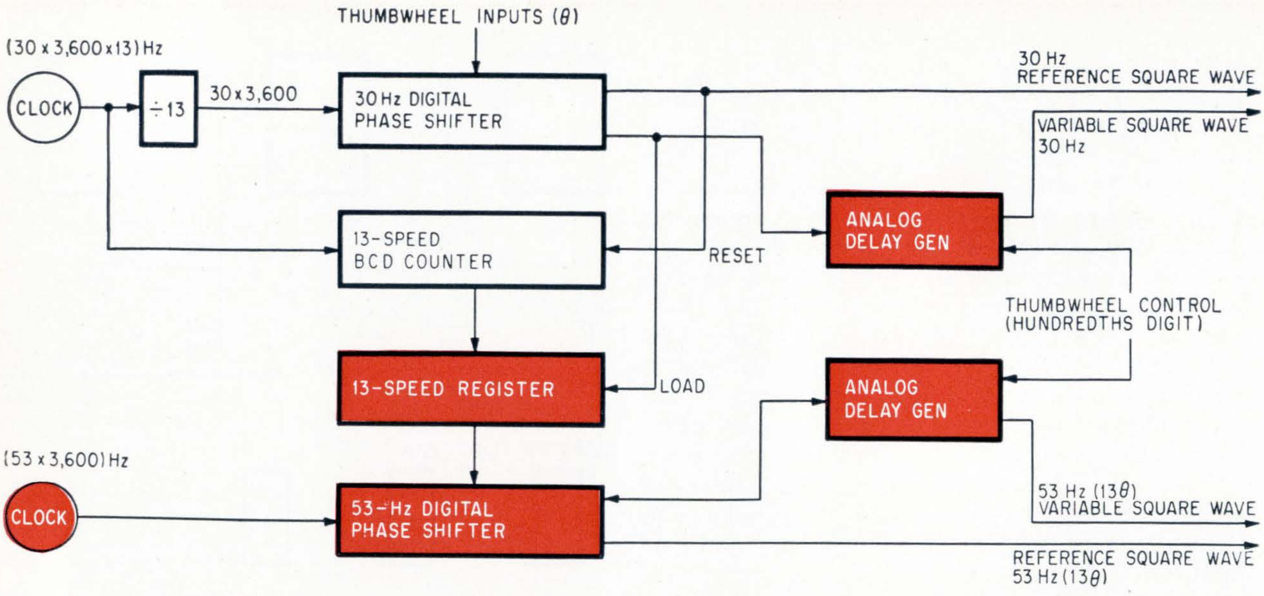
$p' = R'(P + O + N) + R(O' + N')$

$o' = R'P'(O' + N') + R'Q(O' + N') + RO'N' + RQ'ON$

$n' = RQ'P + RN + R'P'(O' + N') + R'Q(O' + N)$

Comparator output

The NAND-gate circuitry on page 108, which compares thumbwheel outputs with the outputs of the BCD counter stages, is an extension of the basic comparator circuitry. The comparison results in a set of triggers at θ and $\theta + 180°$ that are fed in turn to the upper flip-flop in the diagram. The flip-flop generates a square wave at the instant required for it to represent the variable-phase square wave.

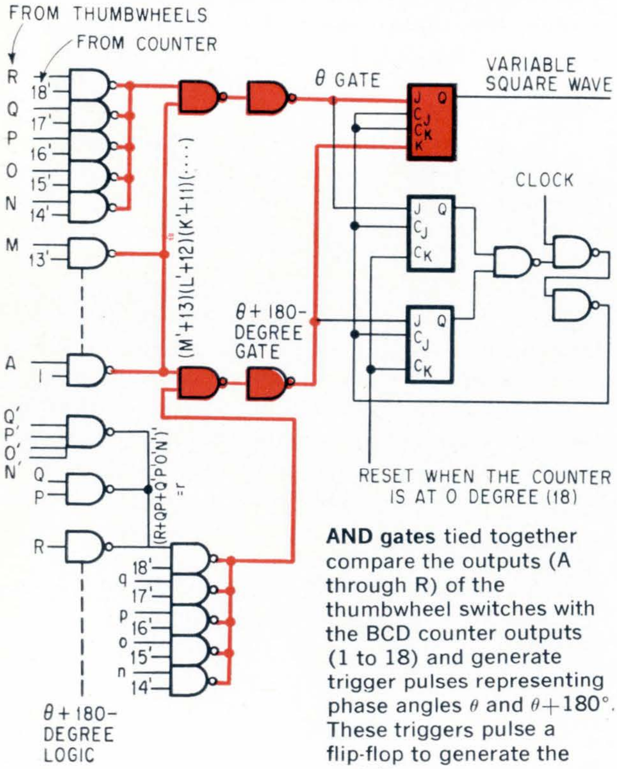


Digital "gear changer" provides the second set of signals in the signal generator that simulates the precision multilobe VOR system. Each degree of phase shift in the standard 30-hertz output becomes 13° of phase shift in the 53-hz output. The multiplication is accomplished with the 13-speed counter.

This will be the selected point in the clock cycle from 0 to 35,999.

Complementary and uncomplemented code disks on the tens and hundreds thumbwheels provide the Boolean terms—R and R′, Q and Q′, and so on—that are needed. Also, only two bits are required on the hundreds thumbwheel to coincide with the two bits, from flip-flops E and F on page 106. This thumbwheel is an octal wheel with the numbers 0 to 3 repeated twice.

The highest bearing that can be set on the thumbwheels is 399.99°. However, if a bearing larger than 359.99° is set, the output of the variable square wave flip-flop drops to zero since no coincidences can occur. It would therefore be helpful to the operator if a simple mechanical arrangement could be devised to prevent the thumbwheels from being set at useless bearings.



AND gates tied together compare the outputs (A through R) of the thumbwheel switches with the BCD counter outputs (1 to 18) and generate trigger pulses representing phase angles θ and $\theta+180°$. These triggers pulse a flip-flop to generate the variable square wave.

Precision VOR generator

In the version of the generator that tests the precision multilobe VOR receivers, a set of 53-hz square waves must be provided in addition to the 30-hz signals. At 53 hz, the relative phase shifts are 13 times that of the 30-hz square waves because a 13-speed counter and other circuits are added to the 30-hz signal generator.

The clock in the standard VOR generator runs at 1.08 Mhz, but the precision generator's clock oscillates at 1.404 Mhz. This signal is divided by 13 before it enters of the 30-hz counter section so that the 30-hz counter output represents 0.1° instead of 0.01° as in the standard unit. To obtain the required 13-to-1 phase shift ratio in the 53-hz section, the 13-speed counter runs 13 times faster than the 30-hz counter as reset line keeps the two counters synchronized. At the time the 30 hz variable square wave passes through zero, the contents of the 13-speed counter (which is 13 times the number of counts in the 30-hz section) are loaded into the 13-speed register. The register then controls the 53-hz phase shifter in the same manner as the thumbwheels did in the standard 30-hz unit.

Bearing resolution is restored to 0.01° by analog delay generators in the variable square wave output circuits. The generators are controlled by the hundredths thumbwheel, which is built as a decade switch and delays the clocks in 0.01° steps (1/10 clock periods). This technique saves flip-flops and gates and has little effect on accuracy. A delay generator that is linear to within 5% will have a maximum error of .005° at a 0.9° setting.

Circuit design

Designer's casebook

Designer's casebook is a regular feature in Electronics. Readers are invited to submit novel circuit ideas, packaging schemes, or other unusual solutions to design problems. Descriptions should be short. We'll pay $50 for each item published.

Instant commands trigger monostable tunnel diode

By R.C. Garavalia and E.B. Daly*

Automatic Electric Co., Northlake, Ill.

Output pulses are obtained instantly from the monostable multivibrator at the right because the input pulses automatically discharge the timing capacitor and reset it to zero. Access to a monostable is usually delayed until the circuit executes the previous command and has had time to recover.

The no-waiting feature enables successive commands to generate an output pulse of indefinite duration by continually discharging the timing capacitor. A missing pulse is also detected in an incoming pulse train since the capacitor has time to charge, thus terminating the output pulse.

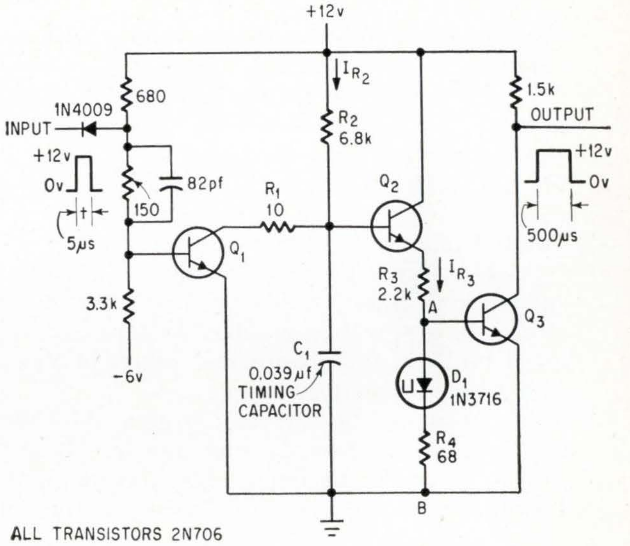
An emitter follower isolates the timing circuit from the output so that long time constants (and long output pulse durations) are possible; output switching by a tunnel diode circuit assures compatibility with high-speed logic without a separate pulse shaping circuit. Since millisecond pulse durations with nanosecond transition times can be achieved, flexible pulses can be generated.

When the circuit is quiescent, the input voltage is at ground potential, holding Q_1 off. Transistor Q_2 is held on by base current I_{R2}. Emitter follower Q_2 generates an emitter current, $(h_{fe2} + 1)\ I_{R2}$, large enough to operate tunnel diode D_1 in its high voltage state at point S and saturate Q_3 at point S′ as illustrated in the graph. With Q_2 and Q_3 on, C_1 charges to the sum of the voltages across R_3 and the base-emitter diodes of Q_2 and Q_3.

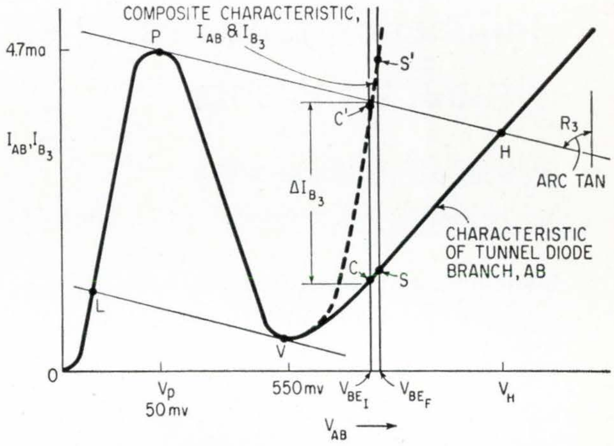
An incoming positive pulse triggers the circuit by driving Q_1 into saturation thus providing a discharge path for C_1. As C_1 discharges, the base voltage at Q_2 approaches ground so that Q_2 gradually cuts off and I_{R3} decreases to a very small value.

With its current source removed, Q_3 starts to turn off and discharges its stored charge through D_1 and R_4. The discharging continues until Q_3's base-emitter voltage reaches valley point V on the composite characteristic. At point V, D_1 snaps to point L where the resistance of D_1 is much lower.

* Authors now with Bell Telephone Laboratories, Naperville, Ill.



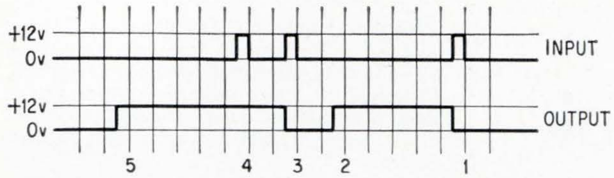
Input pulses turn on Q_1 to provide a discharge path for timing capacitor C_1.



Composite characteristic shows the additional current, ΔI_{B3}, switched into the base of transistor Q_3.

Thus, the stored charge of Q_3 is quickly drained to ground. As Q_3 turns off, its collector voltage jumps to 12 volts, initiating the output pulse.

The input pulse must stay positive long enough to discharge C_1 through Q_1. When the input voltage drops to ground, Q_1 turns off and the timing capacitor, C_1, begins to charge. Because the input impedance to the base of emitter-follower Q_2 is at least 10 times larger than R_2's impedance, C_1 charges essentially through R_2. The charge of C_1



Third input pulse initiates a new 5-unit output pulse.

approaches the positive supply voltage with a time constant R_2C_1.

As the voltage across C_1 increases, Q_2's emitter current I_{R3} increases. Since Q_3 is in cutoff, the entire current I_{R3} flows through D_1. Current I_{R3} increases until the peak tunnel diode current is reached at point P, and D_1 attempts to switch to point H in its high voltage state.

As D_1 is switching, the voltage V_{AB} across the tunnel diode branch is in transition from V_P to V_H. When the V_{AB} voltage reaches the turn-on level for Q_3, it turns on and clamps the voltage at V_{BE_I}, the initial base-to-emitter voltage.

In turning on, Q_3 diverts a large amount of current, ΔI_{B_3} away from D_1 and into Q_3's base very quickly. When C_1 becomes fully charged, quiescent conditions are again established with the tunnel diode current at S, Q_3 saturated at S′, and Q_3 base-emitter voltage clamped at its final value, V_{BE_F}.

The waveforms demonstrate the operation of the no-waiting feature. The first input pulse triggers the circuit and the operation takes place as previously described.

The duration of the output pulse (shown as 5-time units) is a function of the time constant R_2C_1.

A second input pulse at point 3 triggers the circuit in a similar manner. Two time units later, a third input pulse at point 4 triggers the circuit and starts a new 5-unit output pulse by turning on Q_1 and discharging all of the charge placed on C_1 after the end of the second input pulse. The resulting output waveform is a 7-unit pulse terminating near point 5; the third triggering pulse causes no interruption of the output pulse because D_1 stays in its low voltage state.

Millisecond output-pulse durations are possible because time constant R_2C_1 can be made very large. The size of C_1 is limited only by the duration of the input pulse which must hold Q_1 on until C_1 has been discharged. A large value can be chosen for resistor R_2 since Q_1's base current will be multiplied by the current gain, $(h_{fe2} + 1)$.

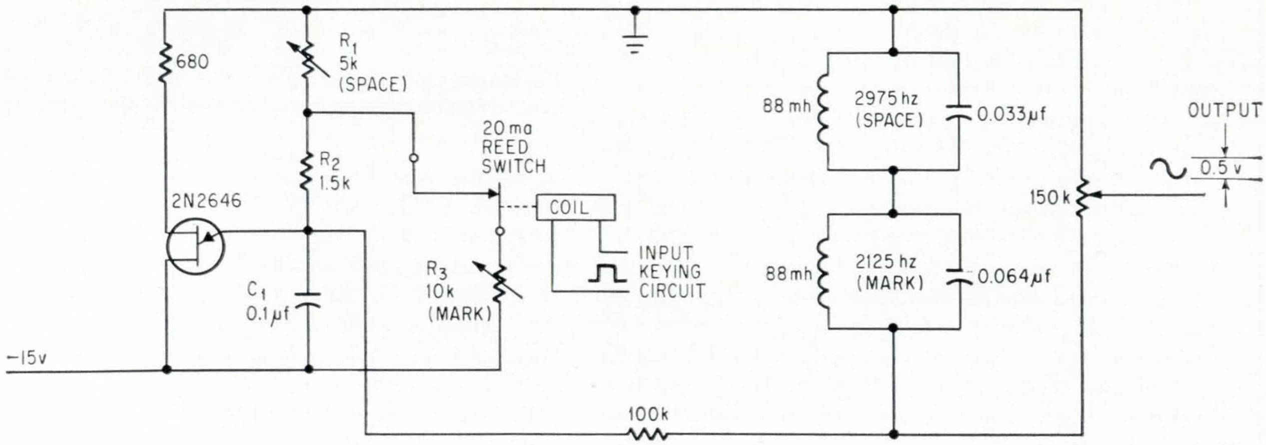
Unijunction switches tones without transients

By Michael G. Mladejovsky

Ajax Presses Division, McGraw-Edison Co., Salt Lake City

Switching audio tones instantly without large transients can be accomplished simply with a unijunction relaxation oscillator.

The circuit converts d-c pulses to audio tones that modulate the amplitude of a carrier for transmission of radioteletypewriter signals on the very high frequency amateur bands. Every character on the teleprinter keyboard is represented by a corresponding seven-bit code transmitted as a train of seven, 22-millisecond pulses. When the pulse train is applied to the keying relay's driving coil each pulse opens the normally closed relay contacts. As the contacts open, resistor R_3 is removed from the tuned circuit. Therefore, the presence of a pulse is signaled by a 2,125-hertz audio tone



Input pulses from the keying circuit of the teleprinter switch R_3 into the network, making the frequency 2,125 hz.

called a mark and the absence of a pulse is signaled by a 2,975-hertz audio tone that is called a space.

The relaxation oscillator is well suited for this application since it shifts instantly from one tone to the other, generates an equal output at both frequencies and has good long-term stability. However, the sawtooth output of the relaxation oscillator must be filtered to produce a desired sinousoid. Two parallel-resonant LC tank circuits with high-Q toroidal inductances perform the filtering and insure a good output waveform that represents a perfect sinousoid.

With the reed switch open, the frequency of the relaxation oscillator is dependent on the value of C_1 ($R_1 + R_2$), so R_1 is adjusted for an output of 2,975 hz, the space tone. When the reed contacts are closed, resistor R_3 is shunted across R_2 and C_1; the additional current path slows the rate at which C_1 is charged, lowering the frequency. Therefore, R_3 is adjusted for an output of 2,125 hz with the contacts closed. With the contacts closed the circuit generates a mark tone.

The LC filters should be adjusted for resonance at 2,125 hz and 2,975 hz. If the output at one frequency is greater than the other, the outputs can be equalized by detuning the appropriate filter or padding it with resistance.

Negative inverter simplifies symmetrical level detection

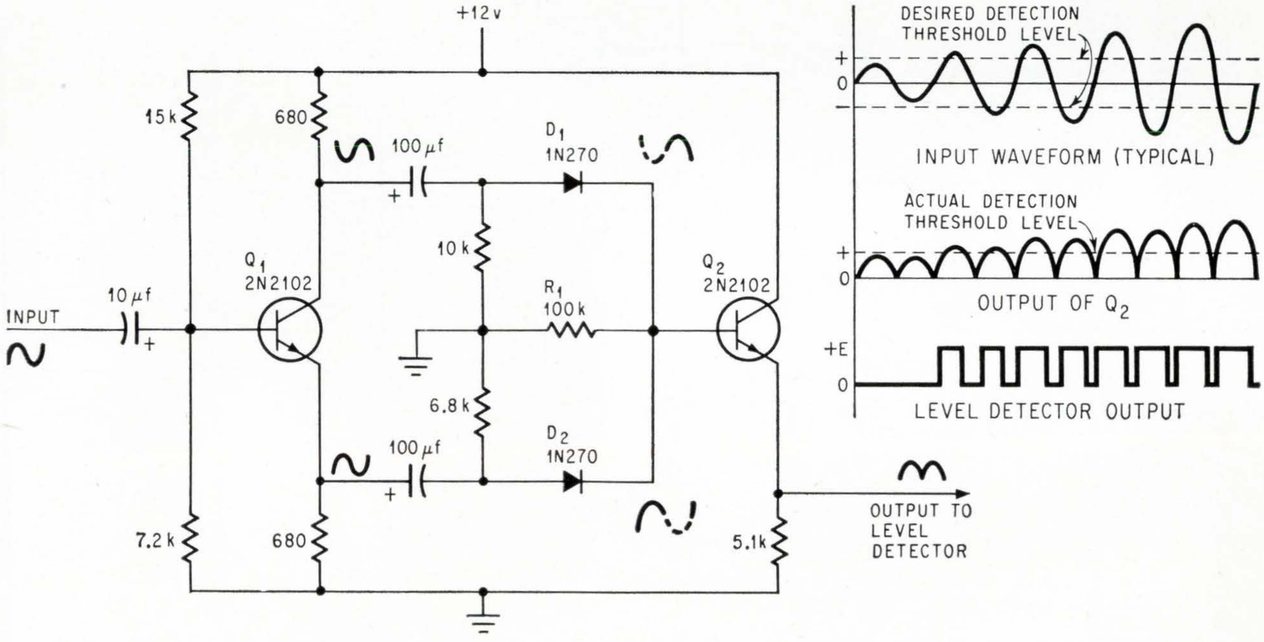
By Phil Salomon

Hycon Manufacturing Co., Monrovia, Calif.

By inverting the negative portion of input waveforms, a Schmitt trigger can detect both positive and negative amplitude peaks. The circuit simplifies symmetrical level detection because it attains the accuracy of circuits with separate level detectors, but without their tracking problems. When only single-polarity bias voltage is available, as in the space vehicle for which the circuit was designed, the circuit achieves symmetrical level detection without cumbersome, sign-inverting power supplies.

The circuit is essentially a full-wave rectifier. A transistor provides the isolation and the 180° phase separation usually provided by a center-tapped transformer. Elimination of the transformer substantially improves the circuit's frequency response while reducing its cost.

A-c input signals appear intact at the emitter of Q_1. The negative portion of the a-c input is inverted and appears at the collector of Q_1. Both waveforms are then applied to a full-wave rectifier, diodes D_1



A-c input signals at the emitter of Q_1 and their inverted images are inputs to the full-wave rectifier formed by D_1 and D_2. The fully rectified signals appear at the output of emitter follower Q_2.

and D_2, working into load resistor R_1. The diodes clip negative portions of the signals, and yield full-wave rectification of the a-c input. The rectified signal appears at the output of emitter follower Q_2.

By employing a conventional level detector at the output of transistor Q_2, symmetrical detection of both positive and negative peaks of the input waveform is obtained.

Zener diodes convert signals from digital to analog

By P.P. Tong*

Systems Development Division, International Business Machines Corp., Rochester, Minn.

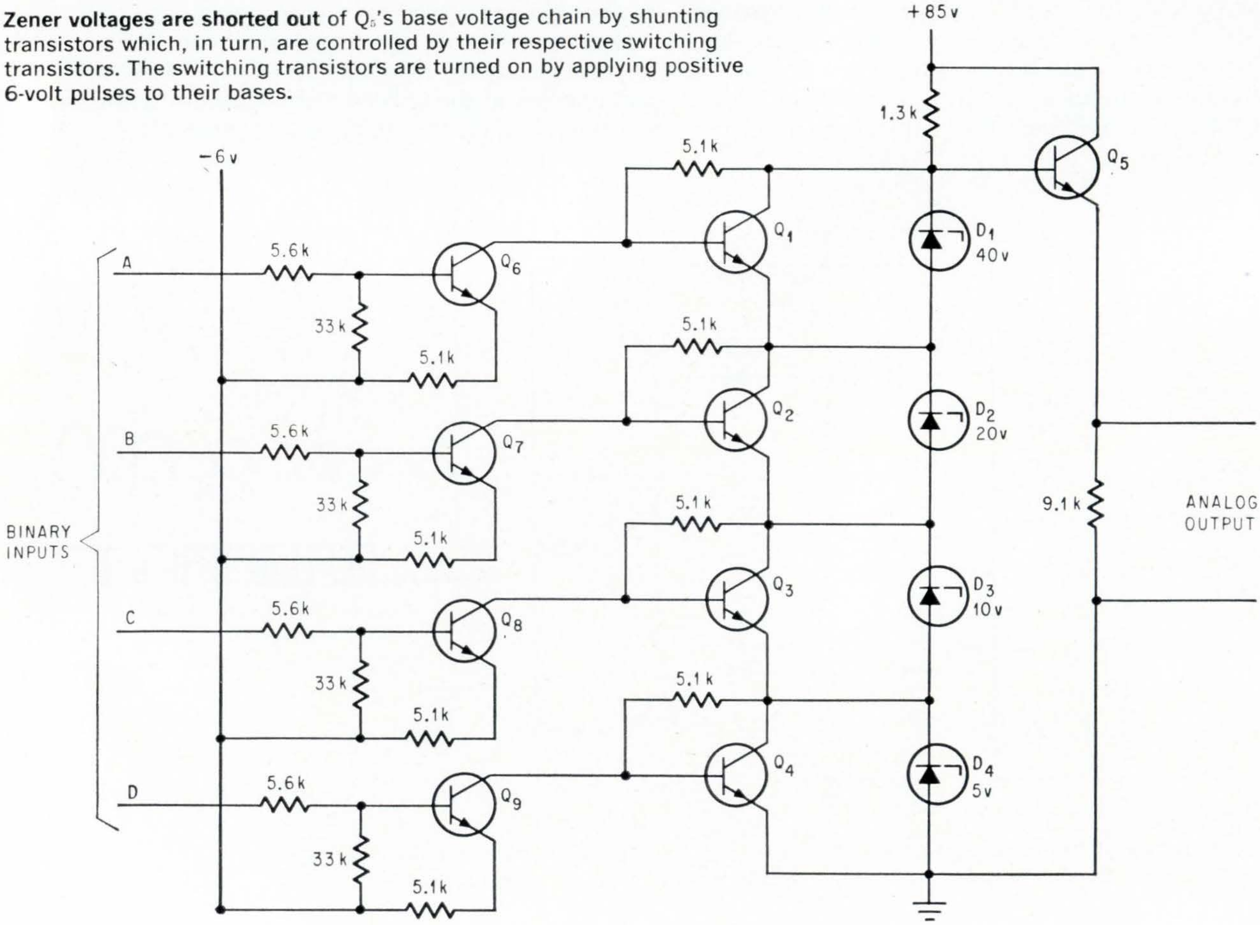
Where high accuracy and high resolution are not required, digital commands can be converted into equivalent analog signals by summing the voltages of back-biased zener diodes. The zener conversion circuit produces a high output voltage at low output impedance and is much simpler than similar circuits using operational amplifiers.

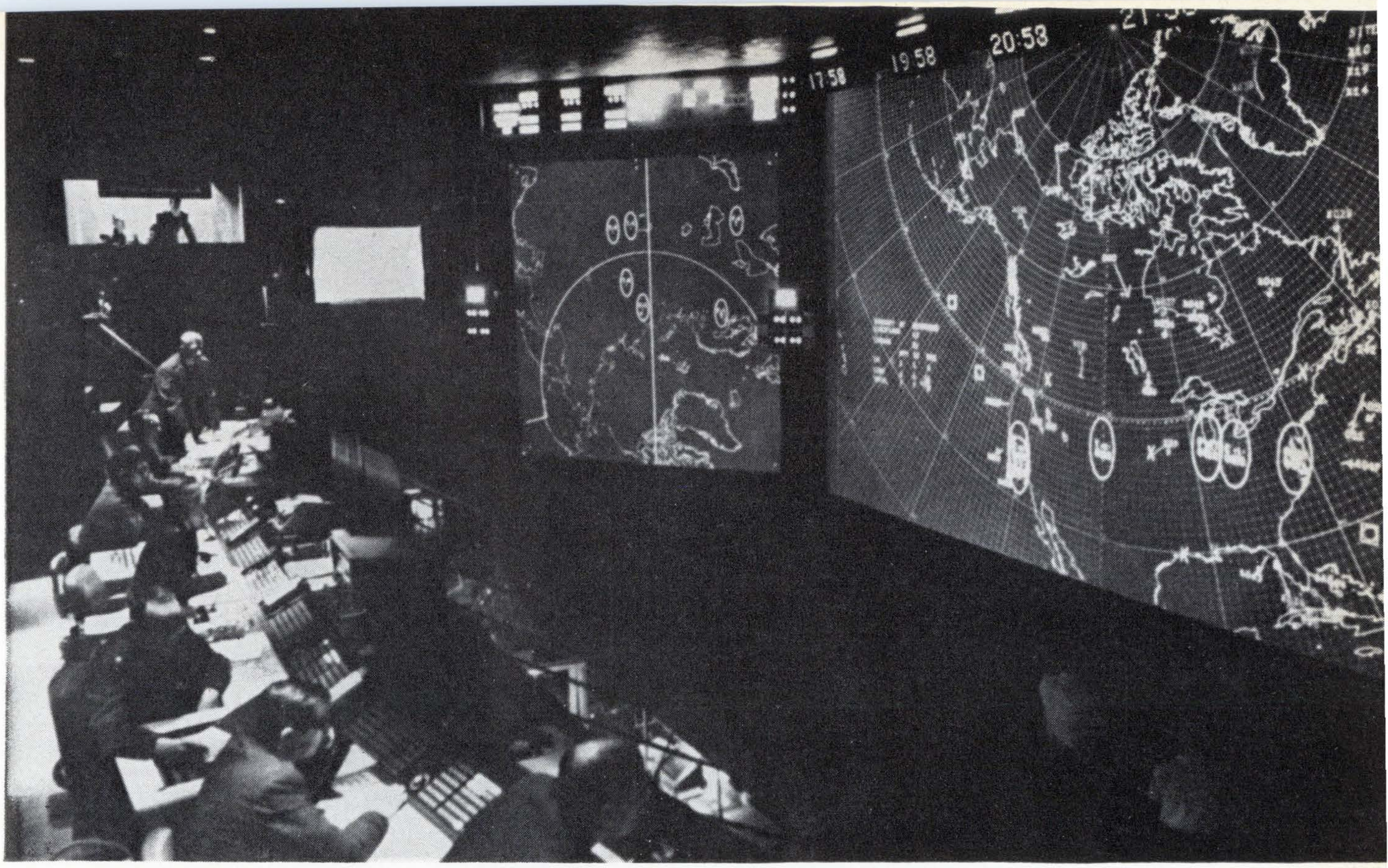
* Now with the University of Wisconsin, Madison

The analog output taken from the emitter of Q_5 (2N1310), equals the base voltage of Q_5 except for the negligible base-to-emitter-diode drop. The base voltage at Q_5 is determined from combinations of zener voltages. The combinations are formed when the shunting transistors short certain zeners from the base voltage chain in response to digital commands.

Zener diodes D_1, D_2, D_3 and D_4 are shunted by transistors Q_1, Q_2, Q_3 and Q_4 (2N1305), these transistors are, in turn, controlled by switching transistors Q_6, Q_7, Q_8 and Q_9 (2N1306) which are normally off, but can be turned on by positive 6-volt pulses on base lines A, B, C, and D. For example, a positive pulse on input line A turns on Q_6 which then turns on Q_1, shorting D_1 out of Q_5's base voltage chain and reducing the analog output signal by 40 volts.

Zener voltages are shorted out of Q_5's base voltage chain by shunting transistors which, in turn, are controlled by their respective switching transistors. The switching transistors are turned on by applying positive 6-volt pulses to their bases.





The large group display dominates the command post of Norad's combat operations center. Battle-staff personnel also monitor real-time displays on the screens of small display consoles.

Military electronics

Norad's computers get all the facts

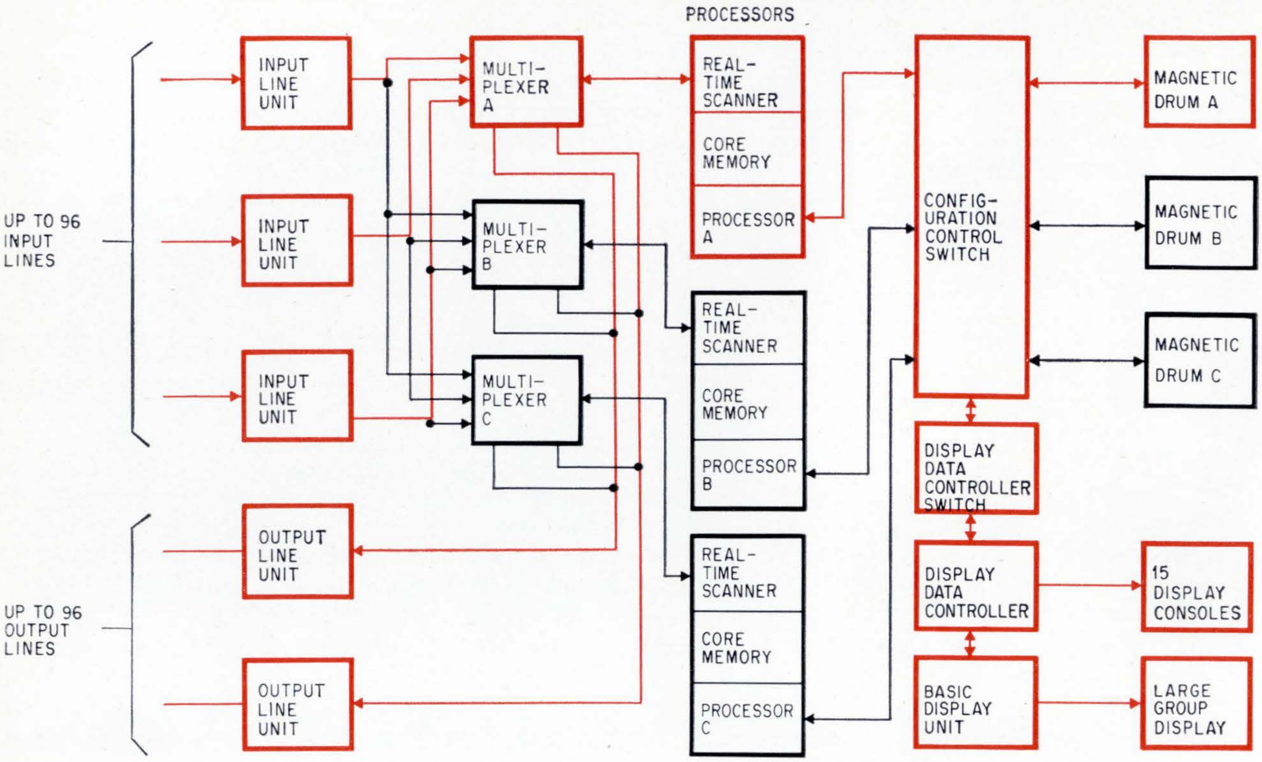
Unique interface equipment and endless programing guarantee that no vital message is lost by the commercial computers of the command and control system that guards against nuclear attack

By Rogert T. Stevens
Mitre Corp., Bailey's Crossroads, Va.

If North America were attacked, the alarm would be flashed to the nerve center of the North American Air Defense Command buried deep inside the solid granite of Cheyenne Mountain, near Colorado Springs, Colo. Half-a-second or less after the first warning was received, the information would be displayed for the Norad commander and his battle staff in the Combat Operations Center.

Aircraft activity over the continent, predicted missile impacts, actual nuclear detonations and the status of all defense facilities would be reported by teletype, high-speed data links and other specialized communications lines and radio. Counterattack commands and alerts to all important military and Government centers would go out through the communications channels.

At the heart of the center's complex command and control system—probably the Western world's most important military data processing installation—are three standard commercial digital com-



Command and control system is triply redundant. Normally, the configuration shown in color would process and display incoming messages and transmit messages to remote commands. If processor A should fail, the B or C subsystems are put into operation through the configuration control switch. The line units and their controllers (not shown) and multiplexers form the input-output data control set.

puters, more than five years old in design. Two computers were originally installed. Recently, a third computer was added to provide the increased reliability of triple redundancy.

The basic computers have been left unchanged in their functioning. They were adapted to their vital role by special peripheral equipment and the programing, designed to make it impossible for a computer to lose a single bit of message data. Even when thousands of messages are arriving every minute at different transmission rates over many separate communications links, the computer cannot be overloaded.

The general-purpose computers selected for Norad were the only suitable high-speed, large-scale digital computers available at the time the system design was frozen in 1963.

Messages, messages, messages

Even in peacetime, a constant stream of information is processed and displayed in the operations center. Messages flow to and from eight Norad regions, Ballistic Missile Early Warning System (Bmews), Distant Early Warning (DEW) and coastal radar networks, picket planes and ships and other information sources and field commands. In addition, there is two-way communication with Washington and Ottawa—Norad is jointly operated with Canada—and such agencies as the Federal Aviation Administration.

Each message normally relates to a single event. The Norad system must process the messages to update stored information on names, locations and status of aircraft, airbases, command centers and major cities and, in case of war, predicted missile impacts and tracks of hostile aircraft. In peacetime, tracks of unknown aircraft and Strategic Air Command flights are displayed.

Triple redundancy

Incoming data is combined with the stored information in the computers, called the data base, to calculate the importance of attack threats, match duplicating reports and tally tracks and predicted impacts. Displays requested by the battle staff are taken from memory files and updated by the fresh inputs. The system must display information in immediately usable form, either in English or in easily understood symbols on maps and in tables.

Any of the three digital computers can be switched into the attack-alert on-line system, while another is used for Norad's second responsibility, space surveillance. Norad keeps track of every detectable object in orbit, including dead satellites and other "space garbage." The third computer is ready as a standby, undergoing maintenance, or processing off-line data. The three main computers are Philco 2000/212's. A fourth computer, a Philco 1000, performs routine off-line data processing for the center.

Originally, the Norad system called for only two computers, with automatic switching of the second to replace the on-line computer if it failed. Automatic switching has been abandoned in favor of manual switching, because any system failure requires a command decision.

A highly significant message, such as a missile attack warning, may never be repeated. Automatic switching could conceal the failure of the on-line computer, and the message would unknowingly be lost. The commander must know of the failure and evaluate the possibility of data being missing and its importance. His decisions will depend on the whole North American defense posture and the world political situation. They are too important to be left to a machine.

If the commander switches to an alternate computer, the data in the first computer's drum memory is transferred to the second computer's drum memory. All significant information in the data base is stored on the drum of the computer in use every 60 seconds. For example, the data base would include special combinations of displays that had been "assembled" with the display control consoles. These displays would not be stored as safe data on the drum, but they could be reassembled after startover. To guard against drum failure, essential data is also stored in the tape memory every 15 minutes and can be transferred to the second drum. Less data is stored on tape than on the drums.

A commercial real-time system, such as an airline reservation computer, can make do with a single computer since an occasional failure would cause only inconvenience. A system whose task is more critical, such as the one that will control airliner spacing in the airlanes, requires higher reliability. The Mitre Corp., which designed the Norad system, is also systems engineer for the FAA's National Air Space Enroute system.

Each computer module has a spare that will go into operation automatically if an on-line module fails. It doesn't matter if some of the radar data indicating aircraft position is lost during such reconfiguration, since the data is frequently updated, but it is essential that the air traffic controller have uninterrupted use of the system.

Always room at the input

Since a vital message might also be lost if the computer became overloaded and could not accept it, the Norad system program makes it virtually impossible for the computer to lose a single piece of incoming data. The only exception is if the equipment were saturated and then failed, but this would be known immediately. As messages are fed into and cleared from the computer memory there is always a specific assigned station available for any arriving message.

In conjunction with the system program, the special interface equipment called the input-output data control set allows the unmodified commercial computers of the Norad command and control system to handle this highly demanding mission. A control set, designed by the Philco-Ford Corp. for the Norad system, can address the computer core memory without computer program intervention. It transfers incoming data directly into the computer's memory.

Most large-scale digital computers are designed to accept input data in large batches that can be processed almost instantly. However, inputs to the Norad system usually arrive in serial form at widely differing data rates. If the on-line computer attempted to accept the serial messages directly, each bit of each message would require a distinct program action. It would take as long to process a single bit as it would to handle a complete message. At peak loads, there wouldn't be enough time to handle the data on a bit-by-bit basis, even if the computer stopped all other processing. The data control set allows the computer to process peak loads of data, perform all its other processing jobs and still have time available for contingencies.

The data in outgoing messages is transferred from the computer's core memory to the output line units without program intervention. The line unit then controls the serial transmission at the correct rate and in the correct form for the communications link selected. This, again, avoids tieing up the computer program in bit-by-bit processing of each message.

Program without end

The Norad program is probably the most extensive and complex command and control system program in use. A command and control system program, unlike other large digital computer data processing programs, does not have a definite end. Once it starts, it continues to operate—in theory—forever. Incoming data arrives continually throughout the life of the system and results must be displayed at once. In contrast, a typical computer program, consisting of addresses and instructions for processing data, begins with the raw data and ends when the results are obtained.

The command and control program may be indefinite, but it isn't formless. It can be broken up into discrete segments. Each segment consists of all the instructions for processing one particular

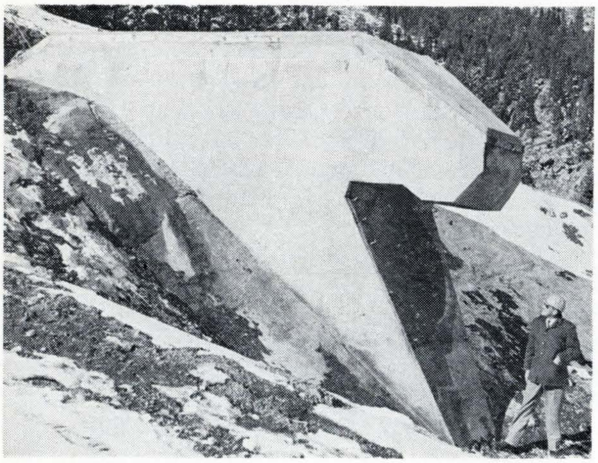
Computer capacities

Model	Philco 2000/212
Word size	48 bits
Memory capacity	
core	32,768 words
drum	512,000 words
Memory access time	
core	1 microsecond
drum	17.5 milliseconds
Fixed-point add time	0.6 microseconds
Floating-point times	
add or subtract	1.5 microseconds
multiply	5 microseconds
divide	12.5 microseconds

type of message or to create one specific display. The complete program, in the usual computer sense of the term, contains an endless sequence of such tutorial segments. Their real-time order is determined by incoming messages and display requests.

The complete set of segments making up the command and control program is stored on magnetic tape. It is initially read into the on-line computer, then stored in its assigned drum memory. The complete program can be read into either of the alternate computers almost instantaneously. An executive-control subprogram held in a reserved section of the computer core memory examines the interrupt signals from the data control set and display consoles. It selects the specific program segment needed for processing each message or request.

The program also allows the system to be used for training exercises, with simulated inputs. While the exercises are carried out, a portion of the system continues to record and display live inputs in an isolated portion of the data base. If a significant real-time event occurs, the live display console issues alarms that permit the entire system to return to live operation.



Blast-resistant microwave antenna provides one of many communications links to the combat operations center.

Message traffic commissioner

Message flow into and out of the on-line computer is governed by an input-output data control set, diagramed on page 114. In the set are a multiplexer attached to the on-line computer, the input and output line units and their input or output controllers. All the line units are connected to each of the three multiplexers, but the line units handling tactical messages address and are addressed by the on-line multiplexer only. Messages referring to space surveillance automatically go to the second computer's multiplexer. An input or output controller controls data flow and computer addressing for up to three input and output line units. There are now a total of 42 such units, but the system can handle as many as 96 input and 96 output line units.

Each line unit terminates a single incoming or outgoing line and provides temporary storage for its data. A line unit's circuitry is tailored to match the input of each line. Messages from Norad regions and DEW sites arrive on standard teletype lines at data rates of 40 to 100 words a minute in several standardized formats. Each character is defined by a start and a stop pulse. The teletype line units strip these pulses from each character as they appear and store the characters in their own shift registers for later transferal to the computer memory.

Data from the Ballistic Missile Early Warning System comes in on digitally modulated 1,500-hertz sine wave carriers, accompanied by an unmodulated reference sine wave. The data is demodulated in the line units and stored serially in the registers. Bomb alarm data arrives in parallel, needing only to be stored in a line unit register until time to pass it to the memory. Other data, called "fieldata," in codes at 600, 1,200 or 2,400 bits a second, require a locally generated synchronizing signal for processing. The control bits are stripped from the signal by the fieldata units that also check character parity and generate the synchronizing signal to gate the characters into the shift register.

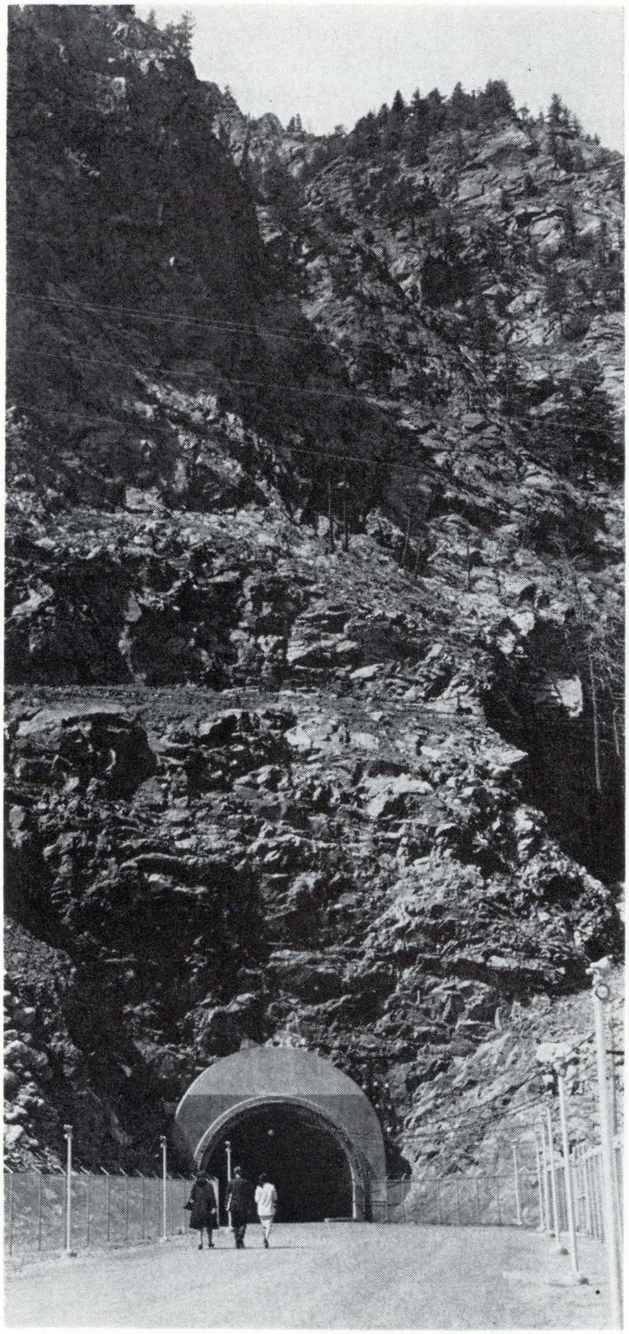
Line units handling serial data store the incoming bits of each character in six-bit character shift registers. As each character is assembled, it is shifted to a 48-bit word register. When the word register is filled, the contents must be transferred to the computer core memory before the character register fills again. Otherwise, when the new character is transferred to the word register, one character already in the word register would be lost.

Slots of memory

Messages received by the line units run up to 32 words long. Each unit is assigned a unique location in the computer core memory known as a "slot," which is exactly twice the length of the maximum message that can be received by that unit. The slots are divided into halves whose functions are similar to those of the shift registers in a line unit. When one half-slot is filled, it must be cleared before the other half is filled to avoid loss of data. The computer supplies the initial slot address to the line unit, which adds the address to each completed word. The line unit increments the address after a word is transferred to the memory, so the next word takes the adjacent address.

When a line unit has assembled a word, it notifies the multiplexer. The multiplexer scans all its line units according to a priority system based on rate of data transmission, not data importance.

Line units are guaranteed processing within 1.66 milliseconds under A priority, in 3.33 msec under B priority, 9.9 msec under C priority and within 60 msec under D priority. The priorities insure processing of an assembled word before the line unit character register refills. Even if all line units are receiving messages at their maximum rates, no data will be lost, because of the priority transfer



Norad's hideaway

Visitors to the combat operations center enter through a tunnel, one-third of a mile long. At the end of the tunnel are two steel doors, 50 feet apart. Each door weighs 30 tons. Beyond the doors is a complex of two- and three-story welded-steel buildings mounted on massive steel springs. The buildings are in a cavern hewed from the granite of Cheyenne Mountain.

The buildings house the Norad staff and the command post of Air Force Gen. Raymond J. Reeves. The center was designed to be impervious to the blast effects of nuclear warfare and to be self-sufficient for several weeks. Electromagnetic pulses from a nuclear explosion would be attenuated to safe levels before reaching the electronic equipment in the center.

system and the dual half-slot memory locations.

The input controller that services a particular line unit keeps track of the number of words transferred to a slot. It changes the address by one count for each successive word so that the message enters the half-slot in proper sequence. When a message is completed or a half-slot is full, an interrupt signal is sent to the computer which notifies it that a message is ready for processing. Up to this point, the message has been handled without any computer program action.

From drum to core

The computer, under the executive-control subprogram, now selects the program segment needed for processing this message and moves the segment from the magnetic drum into its internal core memory. A storage area, twice the size of the largest program segment, is reserved for the active program segments. Meanwhile the computer schedules processing action for the message. There is one restriction on computer action: while a word transfer into a memory half-slot is taking place, the computer is denied access to the memory section containing that slot. However, the transfer only takes 1.5 microseconds per millisecond of operation, so there is ample time between transfer cycles for computer access. Under simulated battle conditions, when message traffic is at its peak, the time between completion of a message and display of the data is less than 400 μsec. In peacetime operations, delays are much less.

While one message is being processed, other actions are taking place concurrently. The executive control subprogram is selecting the program segment for processing the next message and reading it into the other half of the core memory segment storage area. The line units are forming words from incoming data and the control set is transferring them into the empty half-slots in the memory. Messages are being completed and scheduled for processing by the computer.

As processing of a message is finished, its half-slot in the core memory becomes free to accept message words again, and the stored program segment goes to work on the next scheduled message. This parallel-series functioning of the command and control system will continue as long as data continues to feed into it.

Let's see it now

The role of the command and control system in the over-all functioning of the Norad combat operations center is to supply the commander and his battle staff with up-to-the-minute displays of the tactical situation. The center is manned 24 hours a day by personnel in the command post and at the center's four divisions. The divisions are:

- Missile warning, which is responsible for the integrity of Bmews communications and for alerting the command post to missile attack threats.
- Operations, which maintains Air Force resources records and is responsible for detection and

tracking of unknown, hostile or special aircraft.

- Logistics and damage analysis, which assesses damage and reassigns the defense forces according to the situation.
- Communications, which takes care of all the data links and the operation of the command and control system itself.

The Norad commander watches a large group display, measuring 12 by 16 feet. His staff operates 15 cathode-ray-tube console displays measuring 10.8 by 14.4 inches. Each display operator can select the combination of data he looks at and modify the data base.

Display consoles and the unit that drives the large display are supplied with data from the display data controller. Each block of data words is transferred through the controller as a single computer program action.

Combinations of the data and maps shown on the smaller displays are combined in the large group display and projected in three colors. The large display is first assembled on a console display, then switched over to the large group display. Data to be displayed in each color is generated in turn on a small, intense crt and photographed as three adjacent frames on a roll of 35-millimeter film. The pictures are projected through color filters and a lens system so that they are superimposed on the screen.

Film processing takes 14 seconds. Under battle conditions, the group display can be updated in 14 seconds, but it would usually be updated every minute or 30 seconds. Normally, the updating cycle is 5 minutes. Although the commander's display is not in real time, the crt displays are, so the staff can instantly alert the commander to any significant event.

Display consoles

Map backgrounds of Norad regions and North America, category displays that are superimposed on the maps, tabular information and inputs and outputs through an electric typewriter are stored in each display console in a 2,048-word core memory.

The category display section of the memory contains 120 nine-word slots. Each slot contains one word representing a symbol, such as an aircraft track, an airbase, or a nuclear detonation, plus four pairs of feature words, Each pair describes some characteristic of the symbol, such as altitude or speed of a track. The capacity is normally ample, since 120 symbols with four features each are more than an operator can normally discern. If more than four features per symbol are required, each must be assigned a second slot, reducing the total to 60 symbols.

If the operator requests more data from the data base than the slots can hold, data arriving after the slots are filled will not be displayed. An alarm will ring and the word "Saturation" will be printed on the display. The console also checks parity of incoming data and gives an alarm if it is not correct.

Each display word contains coordinate data which are converted to the analog voltages that control deflection of the crt's electron beam. This establishes the location of the symbol or vector on the crt screen. Each word also contains character-indication and vector-generation bits. These activate character and vector generators that cause the beam to draw symbols, alphanumeric characters and tracks on the crt screen.

Planning ahead

Five years ago, when the system design was just beginning, it required advances in the state of the art in hardware and software. The hardened site is, in itself, a significant advance in mechanical engineering. The system is sometimes criticized as being obsolete because recent advances have not been adopted. The critics overlook the fact that by the time more advanced electronic equipment could have been integrated into the system, that equipment would also have become out of date. Meanwhile, the Norad system has become fully operational.

For the future, more sophisticated systems are envisioned. The volume and speed of input data may in time exceed the extra capacity of the data control sets. Being considered is the use of medium-speed mass-storage devices such as input-output buffers, with perhaps a small computer exclusively for message processing.

A second look is being taken at command and control programing. For example, the central data processor operates at only 10% of its capacity during routine peacetime operation. A more efficient, second-generation program might allow time-sharing of many routine computations without degrading performance of the command and control system.

Real-time operation of a large group display is still beyond the state of the art, but several promising methods are being studied. The Eidophor system and thermoplastic recording are two possibilities [Electronics, May 30, 1966, pp. 80-89, and July 25, pp. 143-146]. In its present form, the Eidophor system is not suitable for display of random data.

Acknowledgment

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The author

Roger T. Stevens earned his master's degree in mathematics at Boston University. Before joining the Mitre Corp. in 1965, he worked with computer-driven displays, among other things, at Sanders Associates Inc.

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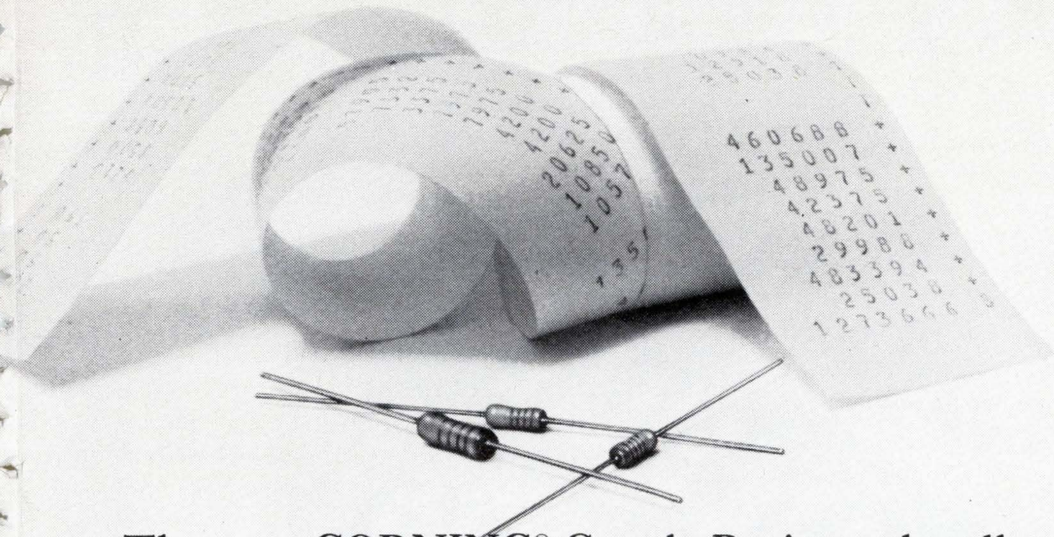

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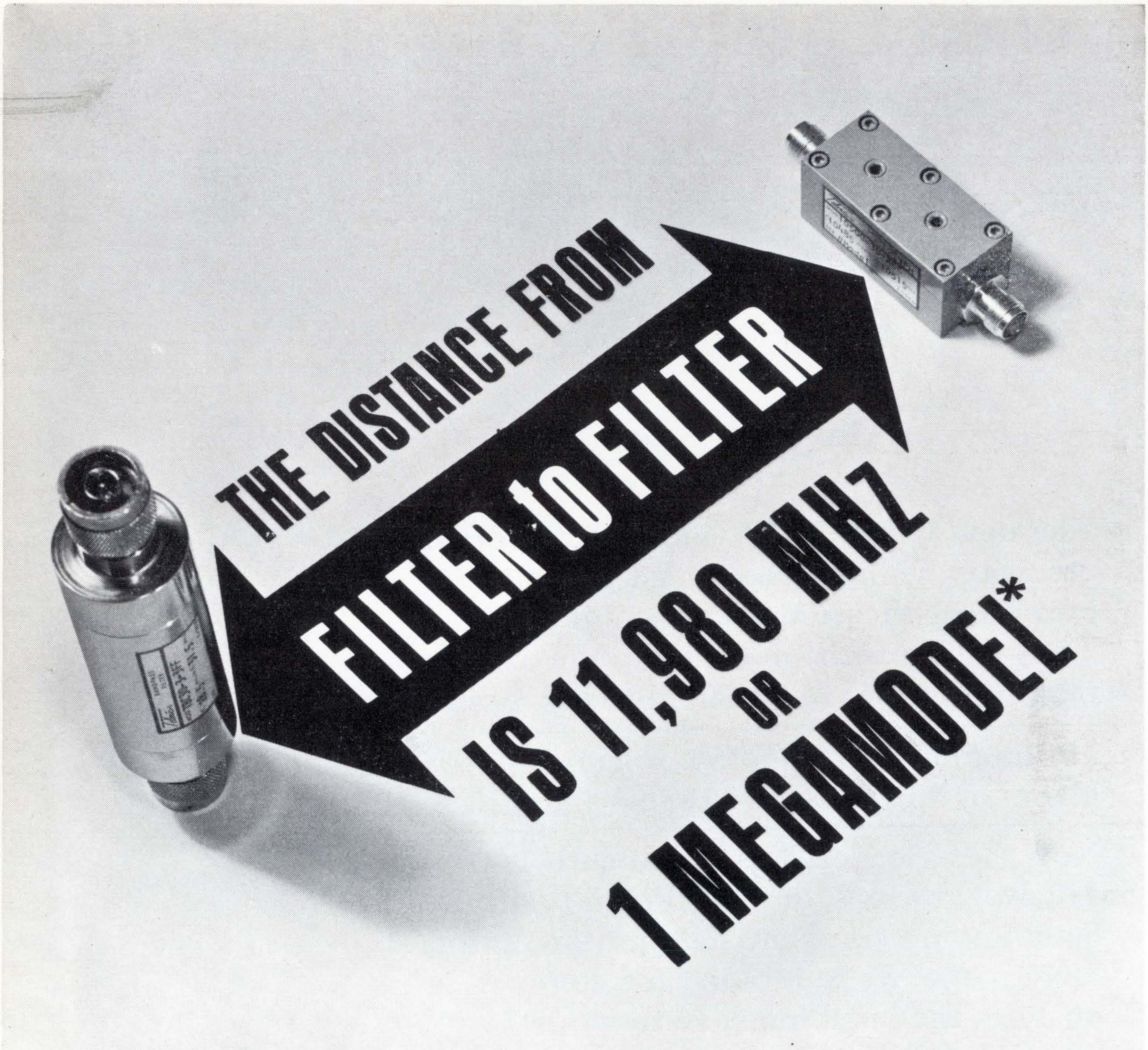

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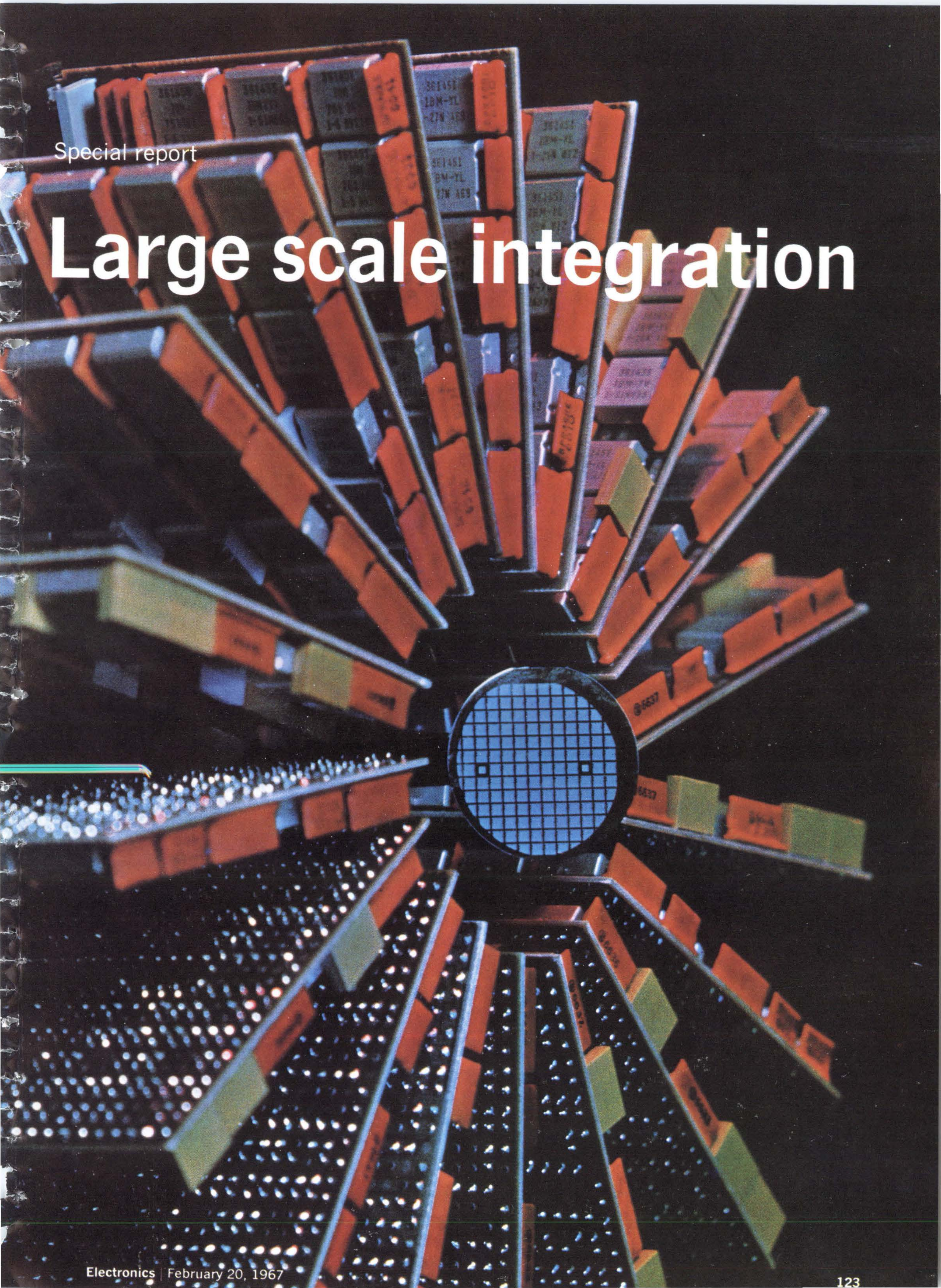
Special report

Large scale integration



LSI: the technologies converge

Economic and technological pressures are forcing device and systems manufacturers toward an intimate, though unwilling, partnership

By Samuel Weber
Associate managing editor

Discussions of large-scale integration these days are marked by a kind of majestic sweep that stirs and disturbs the mind. Descriptions of the potential rewards afforded by LSI, and the drastic penalties for failure to exploit it, as depicted by its proponents, are characterized by a brand of rhetoric unmatched since the discovery of the laser. Typical discussions of LSI bring emotional responses ranging from awe (". . . more impact on circuit design engineers than the discovery of the transistor") to panic ("LSI means LSD for circuit designers").

LSI is being hailed on the one hand as making possible, at last, the achievement of that Holy Grail of the more mystical designers—the computer on a chip—and on the other is decried as heralding the end of the electronics industry as we know it.

Not all talk

The cynical observer of the electronic scene might point out that the only products being turned out on a large scale are words, not arrays. It's easy, in this kind of climate, to dismiss all the ballyhoo as another case of overreaction to a new development, another publicity ploy by the innovation-loving technical press.

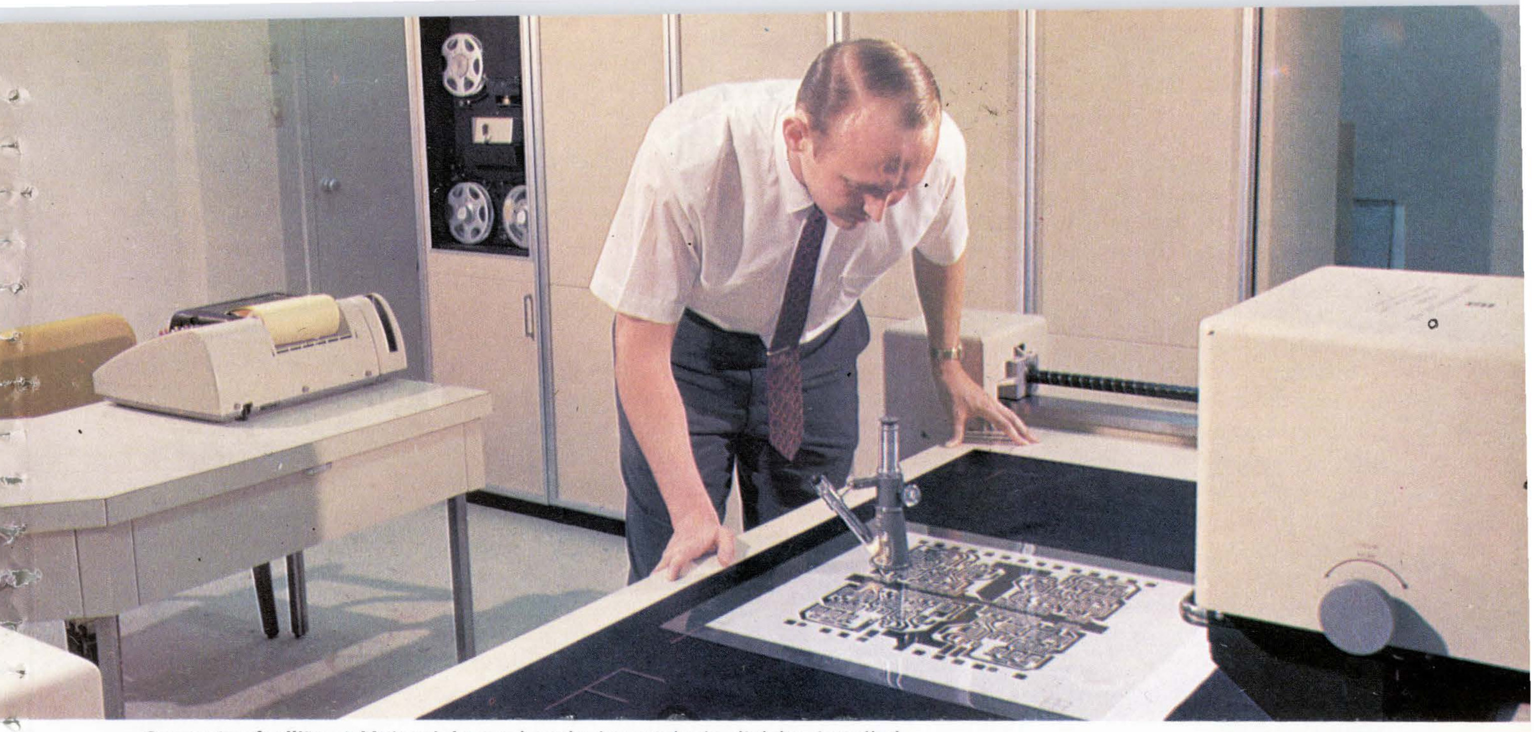
But LSI cannot be dismissed so easily.

While it is true that few products legitimately classified as large-scale arrays have left the laboratory, the magnitude of the efforts by digital systems and semiconductor manufacturers alike to get into LSI, the amount of manpower being devoted to it and the piles of hard cash being laid out for the required sophisticated equipment testify to the fact that LSI is indeed here, and will soon be a way of life for semiconductor manufacturers, system producers, circuit designers and process engineers. In point of fact, with the newly developed capability of putting 100 gates on a chip, semiconductor manufacturers are now assuming responsibility for the design and fabrication of subsystems instead of merely circuit functions. And as always, new, unaccustomed responsibilities bring uncomfortable and disturbing problems.

Converging forces

LSI is the result of a convergence of a number of technological and economic forces that have been gathering since Texas Instruments Incorporated's Jack Kilby produced his first crude, lumpy integrated circuit. Foremost is the improvement of integrated circuits under the impetus of the drive for higher reliability, higher speed and low cost in digital systems. In the last five years, the realization of these goals has been amply demonstrated and exploited, and in fact progress has been more rapid than anyone had anticipated. The era has been marked by improvements in fabrication methods, reduction in the size of components and circuits and the trimming of manufacturing costs. With these substantial gains, it wasn't difficult for both device and systems designers to extrapolate their results and envisage further improvements in performance and cost reduction as a result of higher component densities.

But merely increasing the number of components on a chip does not produce lower cost in itself. The total cost per function of a monolithic IC depends on a complicated relationship of several parameters that include engineering cost, processing cost, assembly cost and testing cost. Thus while it is true that to a point, the manufacturing cost per component decreases as the number of components rises, beyond a certain number the component cost increases again due to circuit complexity which tends to reduce the yield. According to Helmut Wolf and Kenneth Greenough of the research and development laboratories of Signetics Corp., a division of Corning Glass Works, there is, in any given point of time, an optimum number of components per IC, which will produce minimum cost



Computer facility at Motorola's semiconductor products division is called on to produce artwork in a hurry for large scale arrays.

per component.[1] At the present time, they say, the optimum number is about 70 from a fabrication cost standpoint. The cost per component has been reduced by a factor of 30 from the level of 1962 where 10 components per circuit represented the optimum.

Wolf and Greenough predict that the optimum number will increase from 70 in 1966 to 1,000 in 1970, and to about 5,000 in 1972. This increase in optimum number of components will be accompanied by a commensurate reduction in the price level. R.A. Henle and L.O. Hill of the International Business Machines Corp. predict that in the early 1970's, interconnected arrays of circuits (presumably gates) will be available at a cost of less than five cents per circuit, for moderate performance.[2]

Incentive for LSI is also coming from the system manufacturers who are seeking not only lower cost but more performance per dollar. The higher densities of LSI will reduce the time delays introduced by wired interconnections in today's machines, and thus speed up operation. Furthermore, transferring much more of the circuit interconnection wiring to the chip will increase system reliability.

As the economic benefits of LSI accrue, the technical benefits will probably multiply. As the cost and density of logic keeps going down, it will be possible to try new ideas in designing computer systems or ideas that weren't economically feasible when first proposed. For example, there will probably be more software functions built into the hardware, in an effort to mitigate mounting software costs. There may be a trend toward more parallel processing systems as a way to get more speed. There will surely be a growth of memory capacity, and the use of more memory and logic in peripheral equipment.

Computer aid essential

All of these developments would be impossible without some form of computer-aided design—the influence of which is another of the converging forces referred to earlier. Without the computer as an engineering tool LSI would be science fiction. In actuality, all the major semiconductor manufacturers are committing large capital investments to computer-aided design in anticipation of LSI. There are a number of reasons for this—most of them relate to the complex relationship that exists between the semiconductor manufacturer and his customers. With the advent of LSI, this relationship must become more intimate than ever.

To be practical, a semiconductor supplier must be able to furnish LSI arrays quickly, and at reasonable cost. According to Robert Noyce, vice president and general manager of the semiconductor division of the Fairchild Camera & Instrument Corp., the start-up costs associated with making a custom circuit are about 30% of the total outlay. Unless some way of reducing this critical cost is found, Noyce says, LSI is doomed to oblivion, even if manufacturing expenses are reduced to zero. At Fairchild, it has been estimated, on the basis of the demands imposed by some 100 design programs initiated in a year, that approximately 320 different arrays would have to be designed per week.[3] The design work, bookkeeping and testing associated with that rate of array engineering just aren't feasible without a computer.

Another reason the computer is essential to LSI is that, to be efficient from a system point of view, arrays must be designed with a high gate-to-pin ratio. Designers will shun packages bristling with a hundred or so pins to be connected to the outside world. This means that the computer logic must be partitioned in such a way that most of the interconnections can be committed internally on the chip to provide a given subsystem function. (The partitioning problem is discussed in greater detail in an article starting on page 130.) For this reason, most of the initial efforts in LSI are directed toward memories, which is apparent from the programs described in the following pages. Memory design is an area where it is relatively easy to interconnect an array of repeatable cells with a high gate-to-pin ratio.

Resistance to standardization

But as partitioning efficiency gets higher, the designer's flexibility in other parts of the system will be severely limited, and as a result, many different kinds of arrays will be needed to satisfy the requirements of all the equipment manufacturers. In other words, the need for off-the-shelf standard arrays will be small, if present conditions prevail, and the trend will be away from industry-wide array standardization—something dear to the hearts of the semiconductor firms, but inimical to the interests of the system makers. Nonstandardization means more start-up problems, larger catalog inventory and difficulty in making engineering changes. From the fabricator's point of view it would be much more advantageous to encourage all his customers to build systems from a limited selection of standard off-the-shelf arrays. Unfortunately, the facts of commercial life being what they are, it is not likely to happen.

On the other side of the coin, the system manufacturer must find ways to standardize the arrays inside his own new computers. (See the article beginning on page 130). For economic reasons, he will want to use the same LSI chip over and over again, either in one system, or over a whole line. This will help to increase the volume of any one LSI chip design, but whether the user will permit semiconductor firms to market proprietary designs as off-the-shelf units is questionable. Systems people are notoriously jealous of their proprietary prerogatives and are not wont to turn them over to the device makers.

To offset this, semiconductor firms will aim to expand the market for LSI into a broad range of equipment products, and will probably turn their own unique designs, or obsolescent proprietary designs, into off-the-shelf units, to be used outside the realm of digital computer systems. Richard L. Petritz, director of TI's semiconductor research and development laboratories, considers this a major challenge in the era of LSI: to find new ways to use integrated equipment components, as he calls LSI arrays, and to persuade a variety of equipment makers to use them.

Computer aid a must

In the meantime, to satisfy the requirements of this decade, semiconductor people are turning to computer assistance to achieve the fast engineering turnaround and flexibility that will be required.

How the computer will be used specifically is a subject of some controversy. One way is the so-called discretionary wiring approach advocated—but by no means to the exclusion of other approaches—by TI. Its application of discretionary wiring to the design of a memory is described in the article starting on page 143. In this approach, many unit cells consisting of gates or flip-flops are constructed on individual wafers. Each cell is tested, and only those which are good are interconnected by alternating metal and insulating layers to form the desired function. The interconnection masks are designed by computer, based on the test data fed into it. The advantages of this system include increased yield because only the good cells are used, while providing the necessary artwork in fairly short order. One disadvantage is that the necessity for probing each cell imposes a requirement for providing contact pads for the probe, which substantially reduces the available real estate on the chip that can be used for circuit cells.

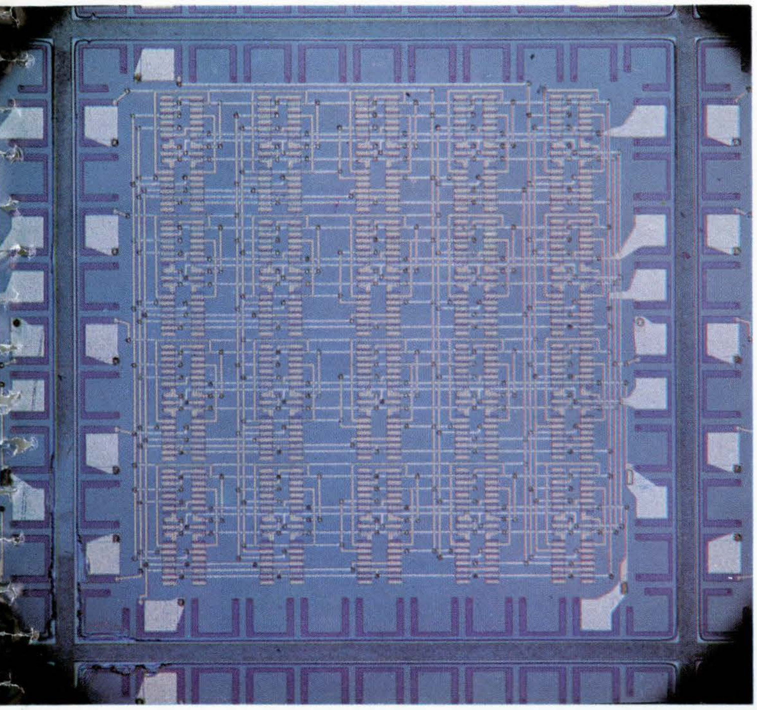
An alternative, favored by Fairchild and Motorola Inc. is the so-called "100% yield" approach to LSI. Here, the fabricator assumes that all the cells on the wafer are good, and testing is left until one of the final steps, after metalization. Because probing is not required, more devices can be put on the chip, with additional gains in array complexity and speed.

The computer's role

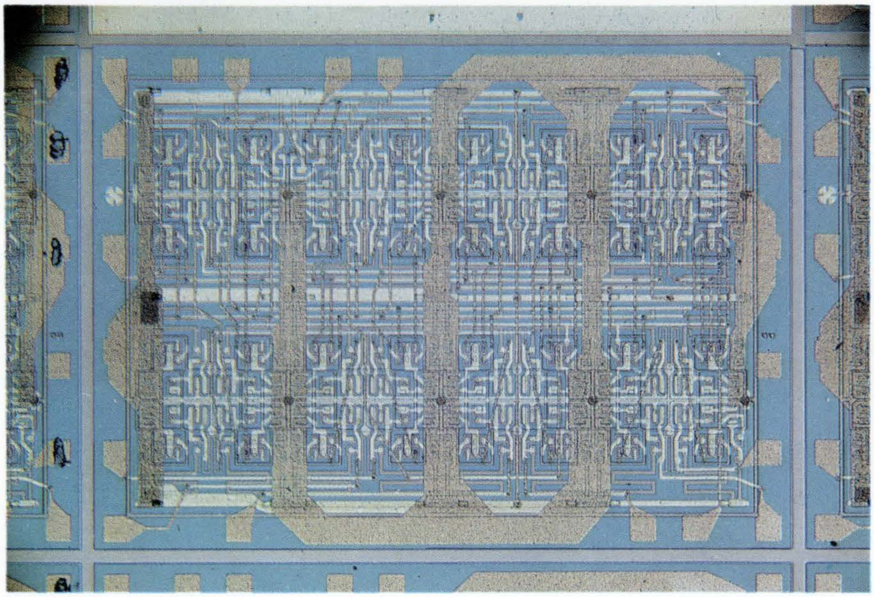
C. Hugh Mays[3] of Fairchild and W. Raisanen of Motorola[4] have both described concepts of a computer-aided facility for LSI production that are remarkably similar. In both cases, the design begins with the customer's logic diagram and test specifications. The array designer will have available to him a terminal consisting of a cathode-ray tube display, a light pen and a keyboard. On file in the computer memory will be a library of gate designs, cell designs and test sequences. The designer will be able to call up, by means of the keyboard, any combination of gates and cells that he requires to fulfill the customer's logic diagram. With the light pen he will be able to change interconnections at will, rearrange cell designs and check out the design's conformity with specifications without ever actually building the circuit. When he's satisfied with the array design, the computer will determine wire routing and test routines, and on command will generate the artwork necessary for producing the array pattern.

Raisanen estimates that with such a system, a vendor will be able to produce prototype arrays to customer specifications within two weeks to a month, at a cost not above a few thousand dollars.

It should be apparent that LSI will call for an unprecedented degree of sophistication on the part of designers—those who work for fabricators as well as users. One of the major problems will be communication between those involved in systems design, and those engaged in semiconductor technology. With LSI, device designers will be working at the subsystem level, and will necessarily be working much more intimately with systems designers. Because many more people are involved in systems design and systems definition than in semiconductor technology, says R.D. Lohman of



Bipolar array by Fairchild Semiconductor is composed of eight cells in a 4 by 2 pattern. Each cell is a four input diode-transistor NAND gate. Cells are interconnected to produce function desired by customer.



Higher density of MOS arrays is demonstrated by this Fairchild 20-cell chip, which provides the equivalent of 80 three-input gates. For examples of versatility of these arrays, see page 163

the Radio Corp. of America, there is a tremendous need for a common language that can enable these two groups to translate system needs into viable products. Here again, the computer will be required to bridge the gap.

The many roads to LSI

Already, before the first large-scale arrays reach the marketplace in any volume, some choices available to the designer are beginning to take shape. These are explored in some depth in this special report. In addition to the choice between discretionary wiring and 100% yield, there is the choice of metal-oxide-semiconductor or bipolar technologies, a matter of how much you want to pay for how much performance. There is the choice of materials technology—which make available the benefits of heteroepitaxy with its inherently high but more costly isolation characteristics, as described on page 171. The articles in this special report do not provide all the answers to the problems imposed by LSI, but they do reveal that there are many roads that can be taken, and that all of them are busy thoroughfares at the moment.

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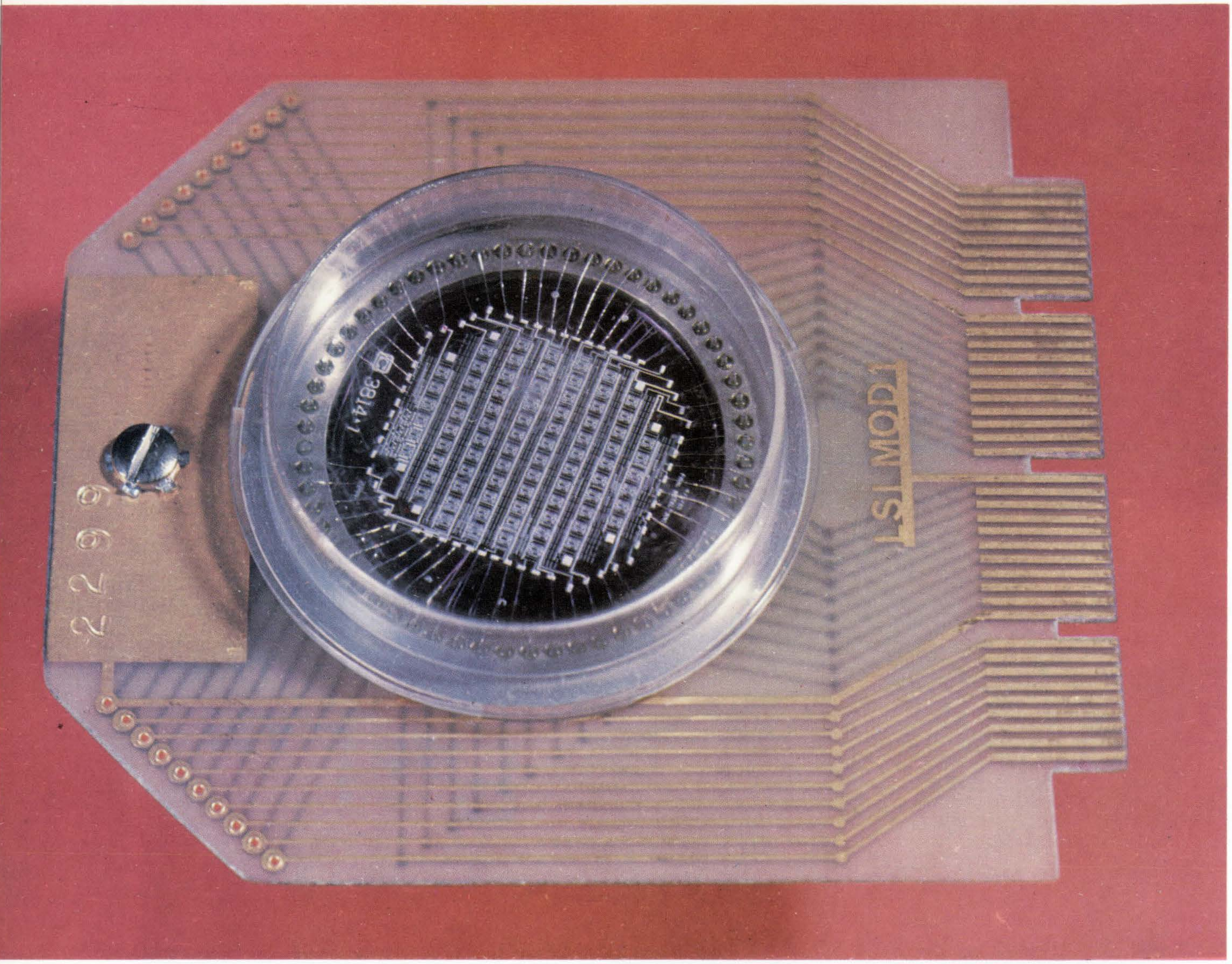
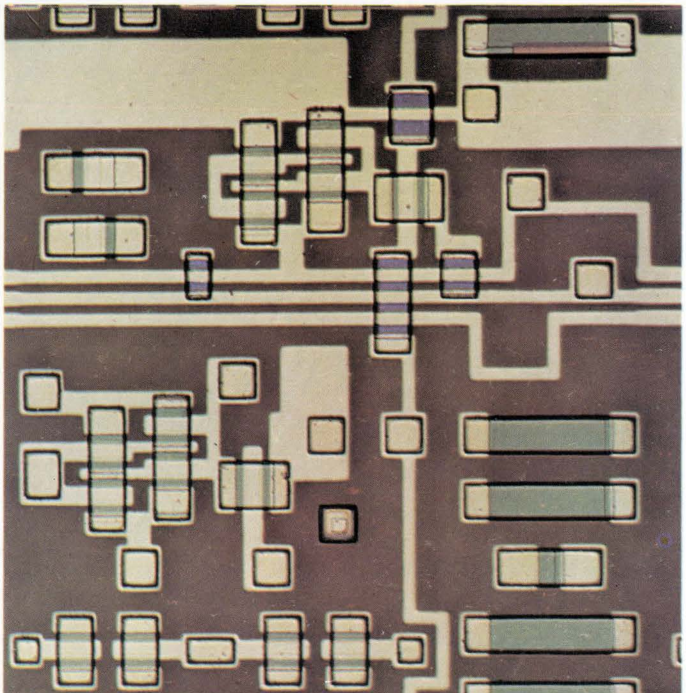
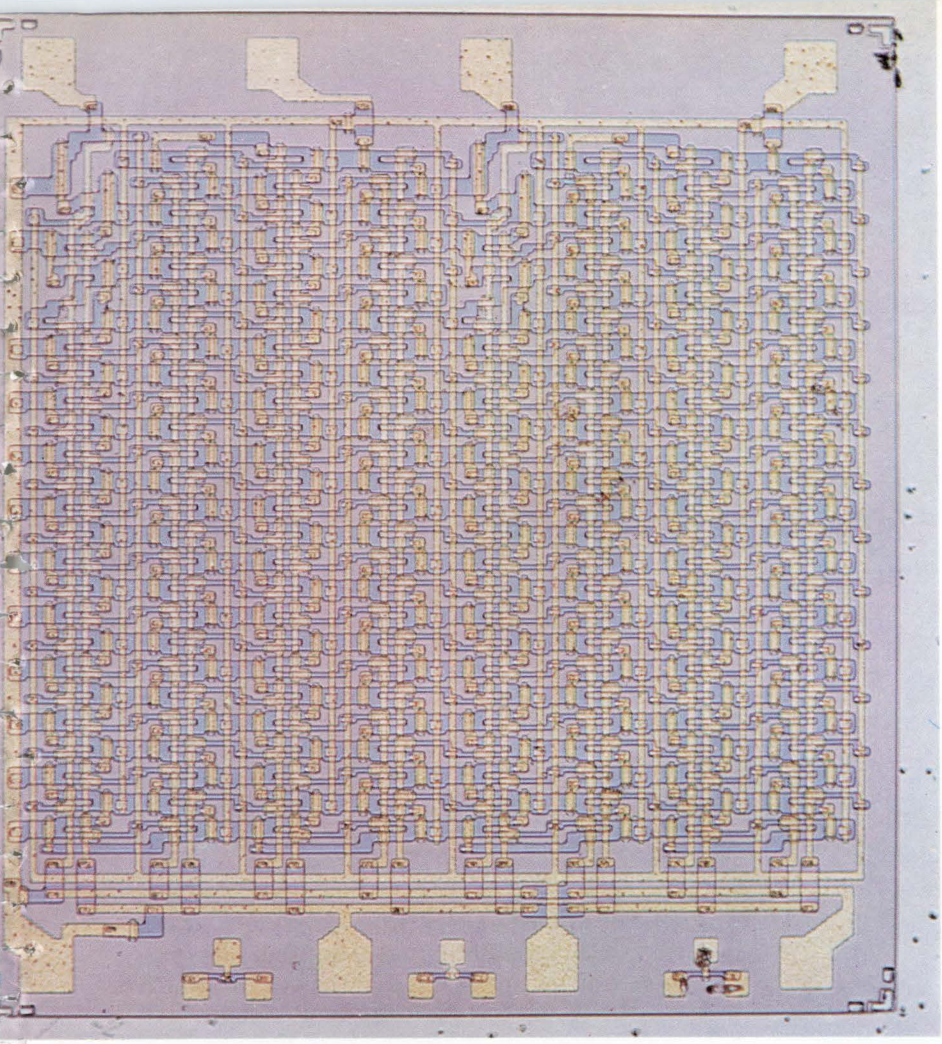
Five approaches to large scale integration



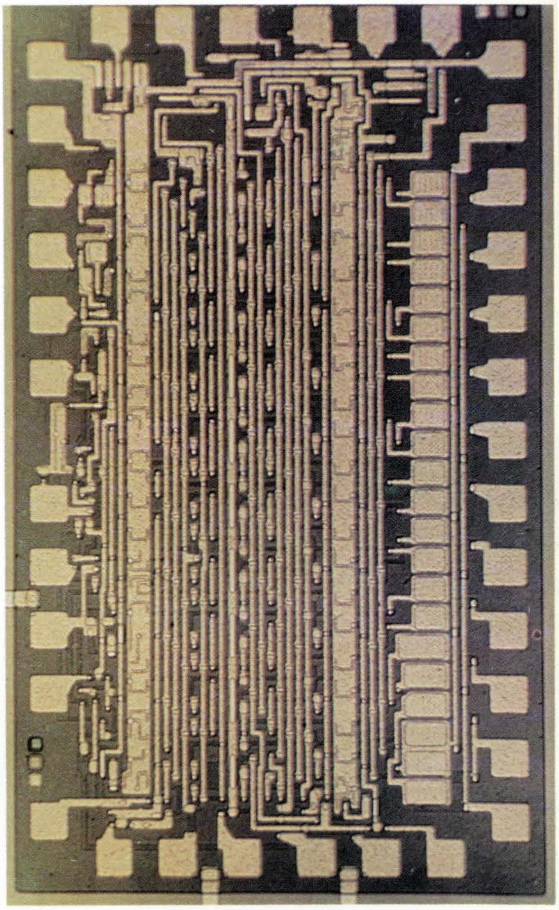
Early version of an experimental array developed by the International Business Machines Corp. Eighty standard circuits in fixed locations on a silicon slice have been interconnected by discretionary wiring to give the array an individual "personality."



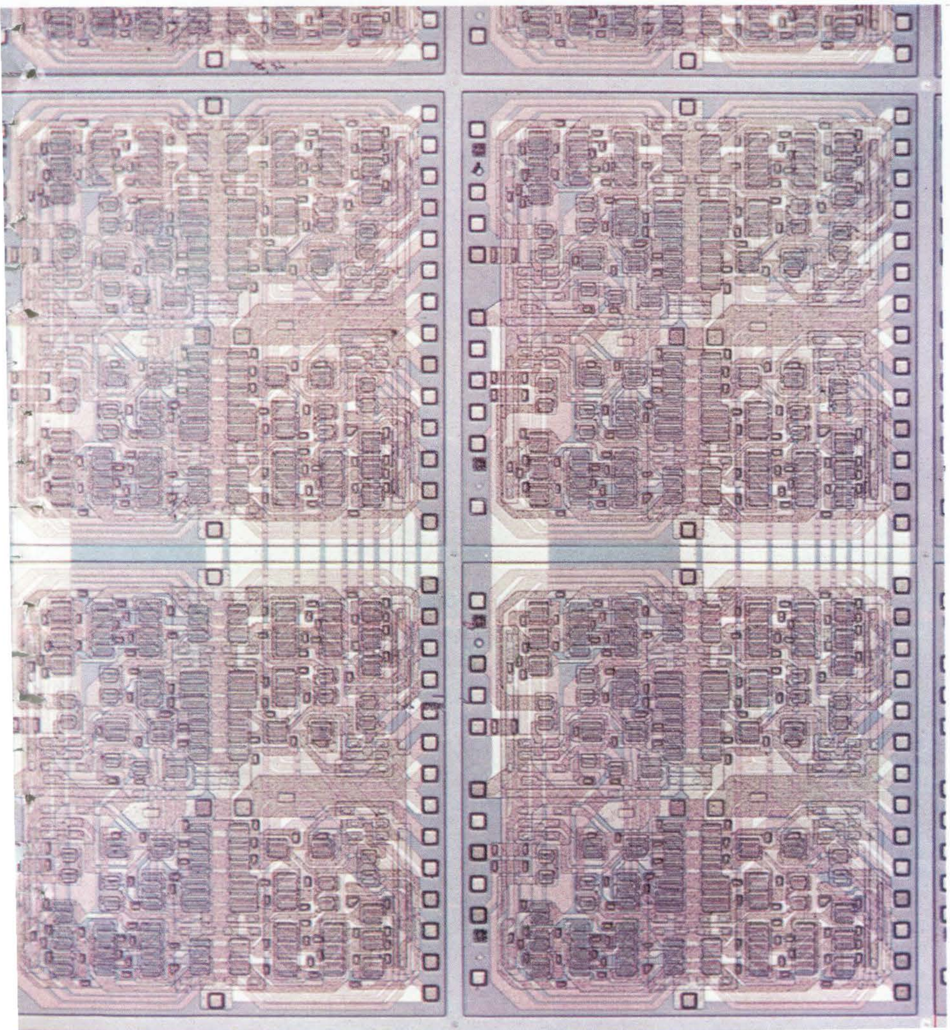
Versatility of silicon-on-sapphire technology is demonstrated by this nondestructive readout memory array from the Autonetics division of North American Aviation Inc. Memory is made up of complementary p- and n-channel MOS transistors arranged in cells, single p- and n-channel field effect transistors and resistivity-checking structures.



Isolation afforded by SOS permits design of high-density arrays such as this 100-bit, two-phase shift register from Autonetics' advanced electronics technology laboratory.



Approximately 300 MOS transistors are interconnected on this General Instrument Corp. array to provide three modes of operation: a 10-bit analog to digital converter, a 10-bit digital to analog converter, or a 10-channel analog multiplexer.

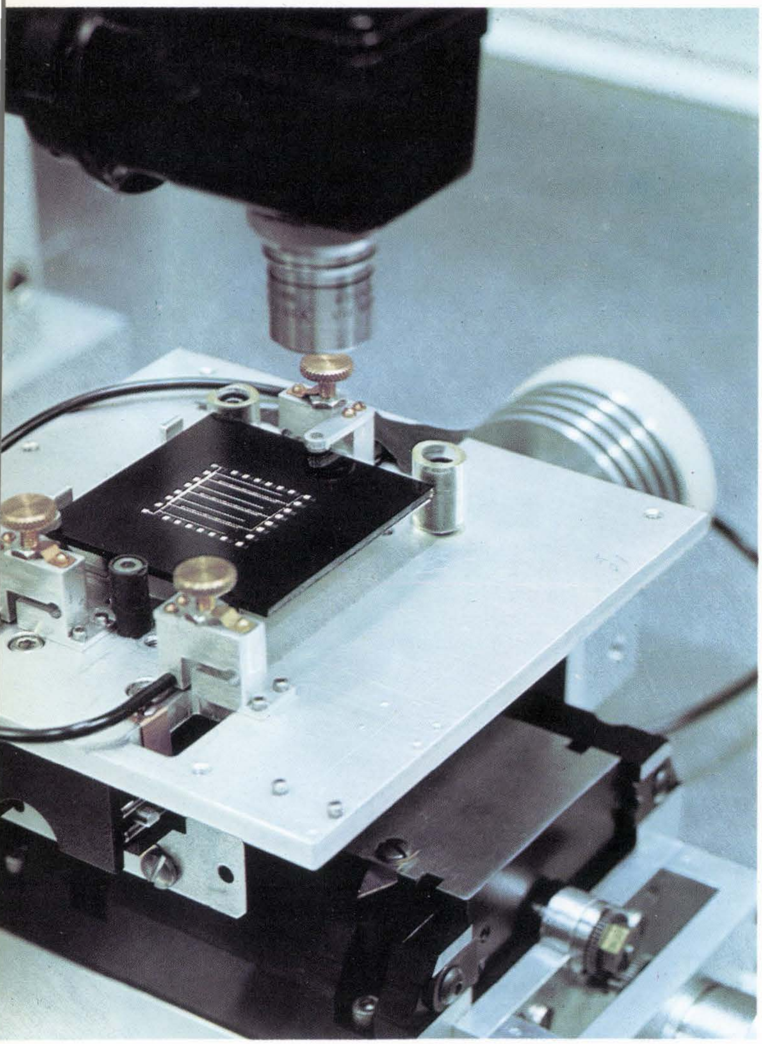


Each cell on this chip is a four-bit content-addressable memory array connected internally by two metalization layers. Motorola Inc., which developed this approach to LSI, calls them Polycells. Cells shown here are interconnected in groups of two by a third layer of metal to form a16-bit memory. A final metal layer will complete the memory, which includes 524 diffused components.

Benefitting the system designer

Although LSI promises substantial improvements in performance and reliability at lower cost, the system designers must first examine the complex trade offs that are required

By William A. Notz, Erwin Schischa, J.L. Smith and Merlin G. Smith
Thomas J. Watson Research Center, International Business Machines Corp., Yorktown Heights, N.Y.



Interconnection mask for large scale array is generated on computer-controlled optical table.

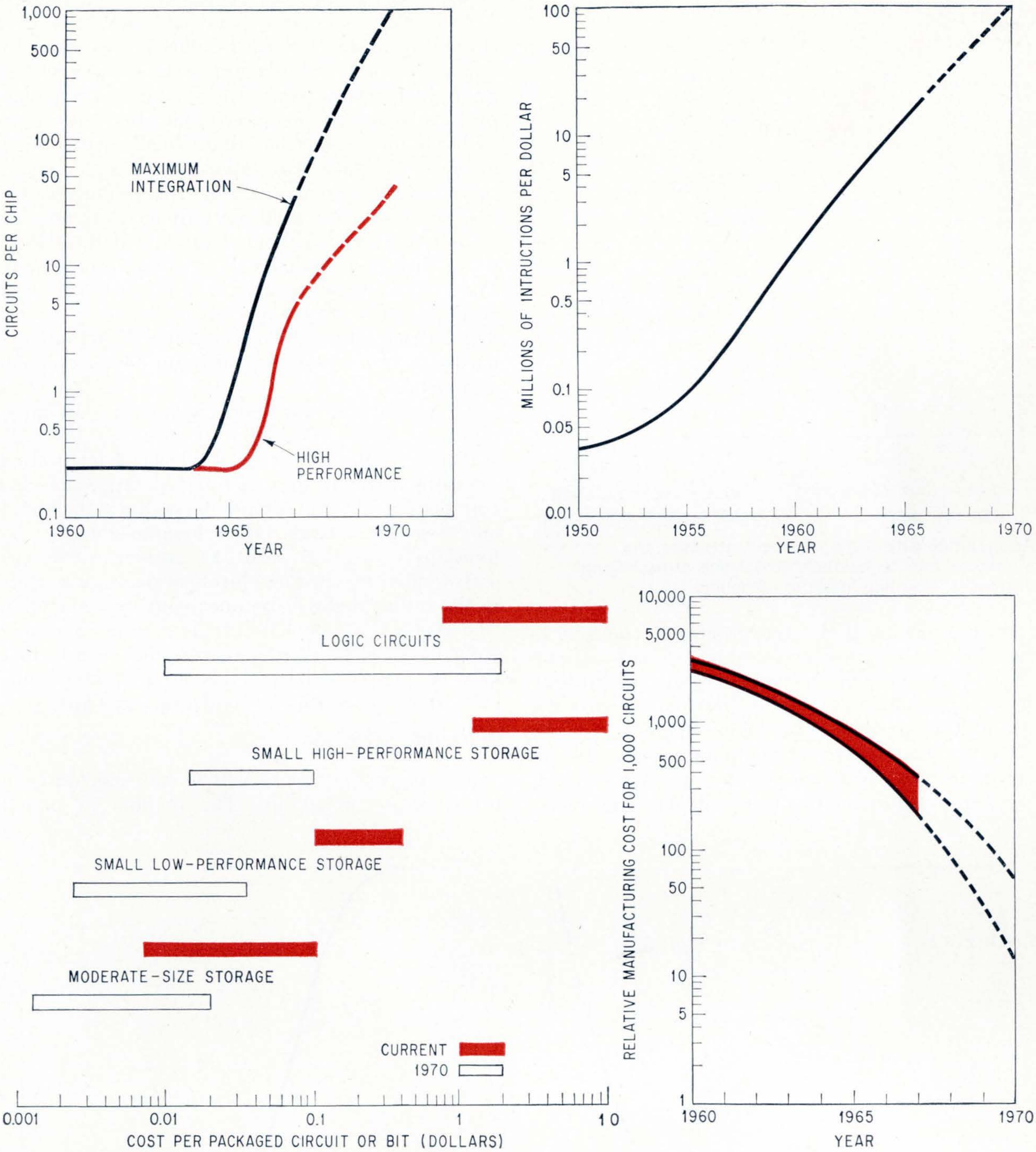
The advent of large-scale integration will have a major impact on the design of data processing machines, and significant changes in the system design process will occur. But radically new systems will not appear until more is known about the economic and technological trade offs inherent in LSI.

System designers will have to approach LSI cautiously, applying it first in areas offering the fewest constraints and the greatest economic advantages. System organization won't change drastically until over-all LSI circuit costs are reduced substantially below those of other means of implementation. Although LSI promises to offer cost reductions, improved reliability, better performance and use less power, the technology does impose some restrictions on the system designer. Mainly it forces him into a design before he may be able to test it thoroughly.

What is LSI?

There is no fixed definition of LSI when practical machine designs are considered because the level of integration offered to the machine designer varies as a function of circuit performance. Higher performance circuits are fabricated to closer tolerances so that the number of circuits that can be integrated at the chip level with reasonable yield will be lower than those designed for more modest performance. This is one of many trade offs to be considered in planning machine organization.

LSI also depends on the choice of device technology and hardware implementation. Since it isn't convenient to deal with all the alternatives each time numbers are used in the discussions that follow, a handy rule of thumb is that integration levels are typically two to four times higher for storage over logic, insulated-gate field effect tran-

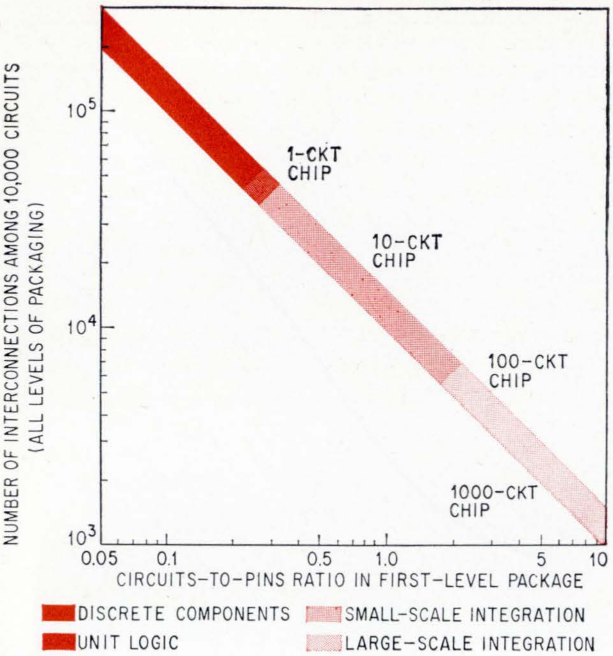


Improvements in integrated-circuit technology are generating a steep uptrend in performance, while costs are going down dramatically, as these curves indicate. At upper left, the number of circuits on an individual chip is increasing from one in 1965 to about 1,000 by 1970. At the same time, computer versatility is also expanding (top, right). This curve shows the gain in the ability of computers to handle instructions for problem-solving (not in real time) in relation to cost. Logic and storage costs will be reduced by large-scale integration (lower curves) as chips begin to carry more and more circuits. The range indicated by color in the curve at lower right reflects variations between the products of different manufacturers.

sistors (IGFET's) over bipolar transistors, and for custom-made over master-slice approaches. [See the article starting on page 157.

One of the major benefits to be gained from LSI is lower cost. LSI will permit many systems and system functions to be introduced which otherwise would be economically marginal or prohibitive, and this is vital; however, it will not necessarily mean dramatic reductions in the total system cost of existing designs.

For example, in some typical systems where logic costs are only a small fraction of the total price, an order-of-magnitude reduction in logic-circuit costs would appear inconsequential. Fur-



As circuit density at the first level increases, the number of interconnections at all levels of packaging decreases, resulting in better reliability.

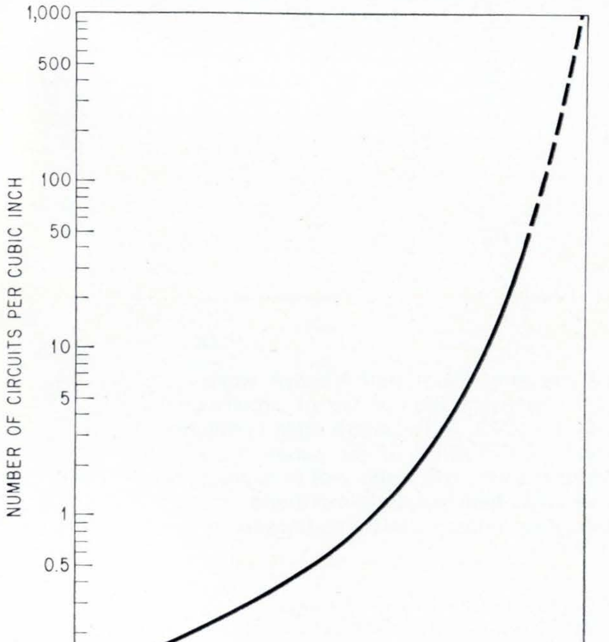
ther, the impact of this reduction may continue to be blunted by other costs which cannot be similarly reduced. On the other hand, significantly more logic circuitry can be provided at little or no additional cost. Thus, logic capability can be added to achieve greater computing power, higher reliability, improved system interfaces and reduced software requirements. This will be one major impact of LSI on the evolution of computers.

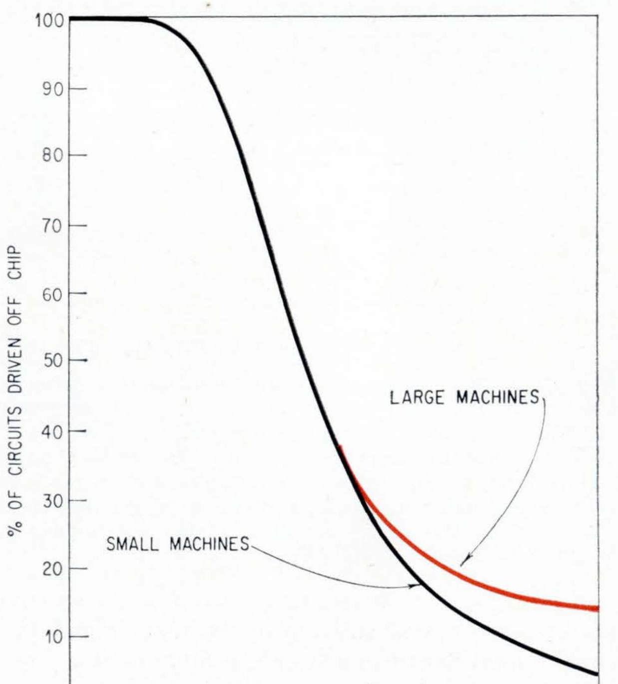
From the customer's point of view, the best over-all measure of these benefits is expressed by system performance per unit cost. A curve of the trend that relates system cost and performance, projects that the net performance-to-cost ratio will continue to increase dramatically with LSI. A machine designer can either produce a higher performance system without increasing system cost, if he chooses high-performance circuits, or a low-cost system without degrading performance, if he chooses a high level of circuit integration. The trend towards system performance and cost improvement can be expected to accelerate as integrated circuit technology is refined. Within the hardware of a computer the trade off in cost will also change.

At present the cost per logic circuit in computers is about 100 times as large as the cost per bit of main storage. As the level of integration increases, the cost per circuit will approach the cost per bit of storage and be within a factor of only 5 or 10 as large. Other logic-to-storage relationships change as well. At present, 1,000 circuits require two or three levels of packaging while in the future this will be one semiconductor chip. The cost for a 1,000-circuit unit, with improving technology, including the cards and boards that may be used to package this number of circuits will decline markedly, as shown on page 131.

Reliability gains, too

A second important benefit to be expected from LSI is greater reliability. The number of circuit





Benefits expected from LSI include increased circuit density (left), which reduces power and results in higher speeds due to lower circuit loading (right).

failures per 1,000 hours has been decreasing by a factor of 10 every five years since about 1950. LSI may be the principal means for continuing this decrease. Although marked improvements in both system reliability and maintainability are expected, an exact quantitative measure of these advantages is as yet not available.

The impact of LSI on reliability may be mainly in the reduction of interconnections. It is an accepted fact that the more interconnections integrated on the chip, the more reliable the system. If no new failure mechanisms intrinsic to LSI arise, then a considerable increase in system reliability will occur. This increase can be traded off in several ways. A given system will run longer, or if the system failure rate is adequate the system can be made larger. In some cases error checking and correcting circuits can be removed or extra circuits can be added to take over the functions of less reliable electromechanical equipment.

Other important and related benefits to be gained from LSI are lower power per circuit and higher speed. Much of the improvement will come from the decrease in the load imposed upon circuits by their environment as a function of the increase in circuit density.

As the number of circuits on a chip is increased, more of them will have the load they are driving on the same chip. In these cases, the transmission delays or reactive loads will be decreased significantly, often more than an order of magnitude. This cut in circuit loading can be cashed in for either higher performance or lower power or some trade off between these factors. This is especially significant in the IGFET technology.

LSI introduces very few truly new constraints to the system designer but the limits can be much more severe and impose a strong influence on design. Important among these are the potentially high costs and longer turnaround times associated with producing a new part or making changes. These costs are sensitive to both quantity and performance. Without careful partitioning, intermediate levels of integration can also produce enormous numbers of unique parts. In addition, the proliferation of larger systems and more complex parts will increase the susceptibility to these factors.

Trade off relationships will reflect more significant interdependences among more diverse factors. For example, the yield (and cost) of a specific level of integration may not be known until chips have been produced in a manufacturing environment, yet by this time the system hardware design may be frozen to prevent product obsolescence.

Changing the system design process

The aim with LSI is to minimize the number of chips in a system, while increasing their versatility and reducing interconnections

Limitations inherent in LSI have to be circumvented throughout the computer system's design process before the technique can be applied extensively. Because large-scale integration affects all the traditional steps in the design process and the interaction among them, its application demands a more unified approach to systems design than is currently taken. In other words, a new set of ground rules is needed.

The systems design process has always involved the following steps:

1. The drawing up of over-all specifications. These include functions to be executed by the system, performance objectives and cost projections.
2. Definition of system architecture. Functions are allocated to hardware and software, and the organization of the system is determined. At this point, machine instructions and formats for data and instruction are established, performance levels are set, circuits and equipment are selected and packaging is specified.
3. Design of the logic for the machine. Detailed algorithms are developed for machine functions, synchronization techniques are defined and microprograms to describe the execution of instructions are developed. Detailed logic for the machine is expressed in terms of the selected logic circuits.
4. Partitioning of machine logic and storage into packages. Logic signals are allocated to package pins.
5. Assignment of packaged logic and storage to locations within the machine framework.
6. Specification of wire routes interconnecting the packages for logic, storage, input-output equipment and console.

In modifying his approach to this process to accommodate LSI, the designer must bear in mind that large-scale integration will increase the capability of logic and storage per unit cost in those parts of the system that can use it.

New approach to logic design

Current techniques of logic design aren't adequate for LSI. The logical structure of a machine has traditionally been expressed as a set of Boolean equations that has then been transformed to achieve minimum circuit count through such techniques as Karnaugh maps, Veitch charts or Quine-

McCluskey tables. Sometimes computer programs have been used to carry out the design process. These techniques were developed in the days of discrete-component technology and are still being used to advantage with unit-logic monolithic circuits.

With LSI, however, the development of a minimum-circuit system may not result in minimum product cost. Extra circuits may be justified by the need to reduce pin requirements, to allow package testing and to create part repeatability. Where previously one attempted to design an optimum set of elementary logical building blocks and then proceeded to implement the logic in a straightforward manner, one is now faced with the much larger task of designing the optimum hardware implementation of a complex logic structure (100 or more gates) while at the same time optimizing many other design criteria. Well-defined systematic design techniques aren't currently available to cope with this problem.

The basic effect of LSI is to increase the amount of logic and/or storage in the most elementary building blocks of a system to the point where a single chip carries a significant fraction of the total logic in a small system or represents a major functional unit of a large system.

In machine organization, the application of LSI will force the designer to consider hardware constraints to an unprecedented degree. Cost objectives, intended applications and production volume will, of course, affect these considerations. For example, if a machine is being designed for high-volume and low-cost output, the organizational objective may be to minimize the total number of parts even though all the parts are different. On the other hand, if the machine's projected sales volume isn't high but low machine cost is still important, a considerable effort may be made to achieve part repeatability.

Heretofore, standardization has generally stopped at an integration level of two or three logic decisions in first-level packaging (modules) and at levels of 5, 10 and 20 interconnected modules, corresponding roughly to 15, 30 and 60 circuits in second-level packaging (cards). Extrapolation from statistics on part repeatability at the level of 100 circuits per part, representative of a large collection of machines that have been designed for unit-logic modules, would indicate that on the average, a 100-circuit part would only be used twice. This need to standardize larger and larger sections of a system presents the greatest current challenge in LSI machine organization and LSI chip design.

The partitioning problem

The selecting of portions of a system (carried through the logic-design stage) capable of being implemented on LSI chips without violating hardware constraints is called partitioning.

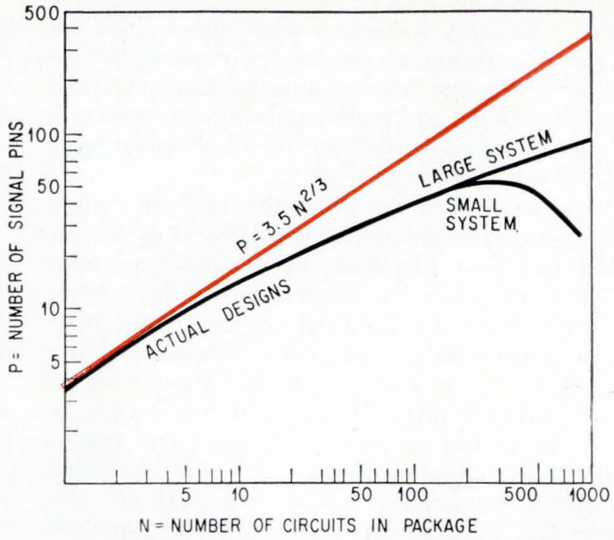
The criteria one attempts to satisfy in partitioning are numerous, and the relative weight of each depends on the final application of the system. In partitioning to the chip level, a designer is usually given a ceiling on the number of circuits and on the possible values for the number of input-output pins. The criteria that must be optimized to achieve a minimum system cost with LSI include: the number of first-level packages required (chips or parts); wiring on the second-level package; part repeatability; testing; ease of maintenance; reliability; performance; engineering-change capability; and requirements for special applications.

A close examination of these factors indicates that efforts to optimize some of them will conflict and that compromises must therefore be made. Furthermore, the techniques of achieving some of these criteria aren't well developed, although designers have gained some experience in satisfying the first three criteria and have come up with some preliminary measuring tools.

There are two principal objectives in organizing a system for LSI:

▪ Minimize the total number of chips and the interconnections between chips.

▪ Minimize the number of different chips to achieve a high degree of standardization.



As package complexity increases, the number of pins required departs radically from figures derived from empirical data (color) and valid for low-density integrated circuits.

Actual partitions compared with Equation 1

No. of circuits in partitions	No. of pins according to Eq. 1	No. of pins according to actual designs
1	3.5	
8	14.0	
27	31.0	12–24
64	55.0	24–41
125	87.0	39–52
216	125.0	
343	170.0	
512	220.0	45–96
729	285.0	45–92
1,000	350.0	62–120

The first objective must be met no matter what the production volume of the system is to be. If the second objective is met satisfactorily, means must be found to successfully interconnect the various chips.

Pin-package trade offs

If one can pare the number of chips without increasing the total number of input-output pins, then the wiring on the second-level package will be reduced. The trade off here presents a choice between either increasing the unit package cost at the first level or cutting the cost of the second-level package. In the past, when first-level packaging had a small degree of functionality, an empirical relationship could be stated to indicate the number of input-output pins needed for a given number of circuits. The equation representing this early circuit-to-pin relationship is

$$P = kN^{2/3} \qquad (1)$$

where P = Number of input-output pins required
N = Number of circuits in package
k = Average fan-in of circuits plus 1

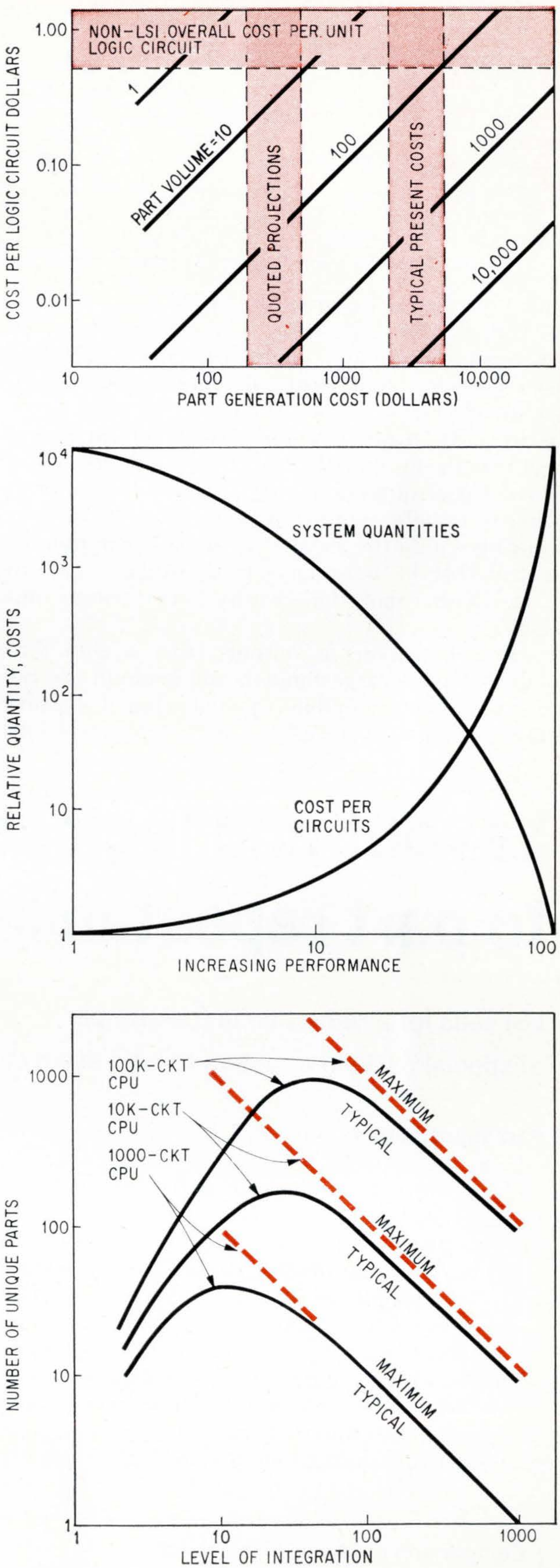
The table and chart on page 134 show typical calculations based on equation 1 and compare them with actual designs in which high circuit-to-pin ratios were primary objectives.

It's quite clear that the empirical relationship drawn by equation 1 is not valid for optimized circuit partitions with more than about 40 circuits. It should also be recognized from this data that wide variations can be obtained in circuit-to-pin ratios, depending primarily on the degree of effort, the techniques employed and the basic objectives of machine partitioning.

To achieve a minimum first-level package count while at the same time reducing the second-level package wiring, a new set of rules has been developed to augment those in general practice, which are applied at low levels of integration to partition logic into small units with few interconnections.

The usual objective in partitioning (except where the functionality of parts is of overriding importance) is to cut as few signal lines as possible so as to have the least number of interconnecting pins on the first-level packages. Rule 1 of the new set is rather general and aims at achieving minimum package count. Rule 2 touches upon the benefits to be gained through the addition of supernumerary circuits. Rule 3 has as its basis the fact that, at the outputs of bit storage cells (latches, flip-flops, etc.), one usually finds nonindependent information compressed to the fullest extent, usually for the sake of minimizing the number of stored bits. This compressing of logical information, whether it be for actual data or for the stable states of a collection of sequential control circuits, is usually called "encoding."

Rule 1. In general, to reduce the number of first-level packages and at the same time achieve high circuit-to-pin ratios, simply begin looking at larger collections of logic circuits as candidates for the partitions, or organize the logic into units with



Constraints imposed by large-scale integration must be weighed against benefits. To produce a new part or make a change in an old one may be very costly with LSI, as these curves show. Moderately dense chips will result in large numbers of unique parts (lower curve) in central processor.

Partitioning study for small system		
	Partition I	Partition II
Chips	8	7
Circuits	656	740
Average circuit/chip	82	106
Total pins	309	255
Average pins/chip	39	36
Average circuit/pin ratio	2.1	2.9

high circuit-to-pin ratios in mind.

Rule 2. Where possible, add supernumerary circuits to encode all nonindependent signals leaving the chip and to decode those signals at the destination chips.

Rule 3. Partition at the outputs of bit storage cells both in data-flow sections and sequential-circuit control sections, because here the information is usually completely encoded. Try to avoid cutting within the sections of signal-combining circuitry that lie between sets of storage cells; the intercircuit connection density here is often quite high.

Rule 4. Choose as outputs from a chip those signals having large fan-out, and keep all the destination points together—on one chip if possible. The signals with large fan-out can be replicated on the destination chip as required.

A study of a small system was conducted to demonstrate the efficacy of these partitioning rules. The system studied was complete, encompassing storage, arithmetic processing, control functions and input-output interface. The table summarizes the results of a partitioning study of the logic of this system.

The over-all study showed that with a 29% increase in circuit density and a 12.5% increase in total circuits, one could achieve an 8% decrease in the average number of pins used per chip, a 17% decrease in the total number of pins used and a 12.5% decrease in the number of chips. These results are believed to be sufficiently general to validate the following projections: an extra 10% of circuitry can free enough pins so that an additional 10% of logically useful circuits can be placed on each chip, while maintaining the same pin count. Furthermore, a 10% reduction in the number of chips per system can be expected. Also, if IGFET technology is utilized, this boost in circuitry doesn't result in a proportional increase in chip area or power dissipation. If the number of pins is reduced, so is the number of drivers, which, in IGFET technology, are relatively large and dissipate considerable power.

Layout and logic: two roads to part repeatability

LSI calls for a reduction in the number of special parts in a system to hold down costs

Part repeatability is a prime factor in any consideration of system design and partitioning. The larger the number of unique parts, the higher the costs of producing, servicing, field stocking and documenting them. The cost of conventional designs is generally linked to production volume, and the application of LSI proves no exception.

In cases where cost is a prime design objective, the optimum part volume lies in the flat portion of a cost-volume curve. If the system being designed isn't going to be produced in large volume, the number of different parts to be turned out must be pared during chip layout, logic implementation or system organization in order to hold down costs.

Three different layout schemes are being proposed for LSI, each taking a different route to part repeatability. The fixed interconnection pattern approach (ad hoc FIP) utilizes a special set of masks to define each logical structure. As the layout maximizes the utilization of chip area to implement a specific logic function, the masks resulting from this approach are useful only in producing that part. The volume of the part must therefore be large enough to sustain the cost of mask-making as well as the other costs that are

Comparison of layout efficiencies

	Circuit alone (Circuits/in.^{2})		Circuits+pad+scribe loss (Circuits/in.^{2})	
Integration level	Ad hoc	Master slice	Ad hoc	Master slice
50–100 circuits	27,000	9,800	16,300	8,900
100–150 circuits	23,000	7,700	17,000	6,800

related to generating that part.

Sharing the masks

If the part volume is small, some way must be found to spread the mask-generating cost among different parts and reduce the inefficiency that a large quantity of low-volume parts creates in a production facility. In one approach to this, called the master-slice technique, parts share all the masks except those involved in metalization—the last step in the fabrication process. The production facility thus handles only one high-volume part until the metalization step. The sketch shows a way of implementing the master-slice approach by fabricating circuits in a standard array with horizontal and vertical wiring tracks left between circuits, and then mass-producing this configuration. The designer has only to specify the wiring (metalization) to produce the logic required. [For a more detailed description, see page 157].

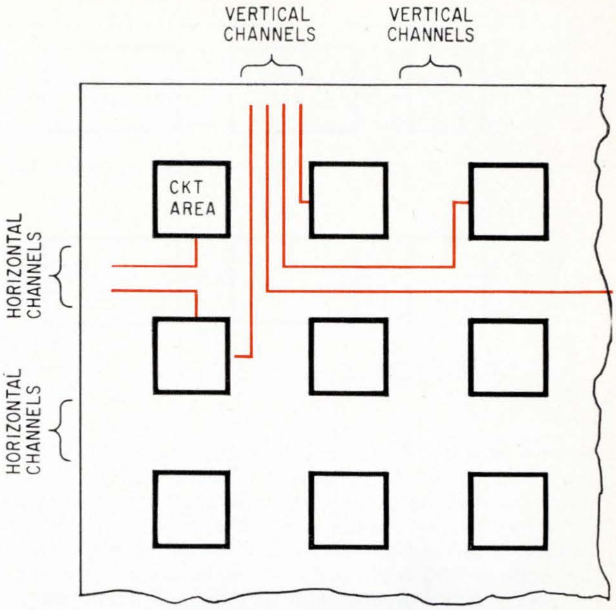
A comparison of the relative layout efficiencies of the ad hoc and master-slice FIP approaches leads to the conclusion that the ad hoc technique achieves more than twice the area utilization of the master-slice approach, and that this advantage becomes more pronounced as the integration level increases. The question of master-slice versus ad hoc, therefore, comes down to a choice between lower mask-making costs and greater utilization of silicon areas.

The master-slice concept can be applied efficiently, for example, to a read-only store (ROS). For such functions, monolithic versions become impractical for addresses (source code) greater than about six or seven bits, because the number of circuits increases exponentially with the number of source code bits. For this reason, the design would combine a number of elementary sections looking superficially alike and differing only in the decoded functions to be furnished—in other words, in "personality." Increased versatility would be afforded by the extender input connected externally to other similar elementary sections.

Applying the master slice

A particular application of this principle is the code translator shown on page 138. This chip, containing 78 circuits (558 IGFET devices), would provide up to four bits of the output, and could flexibly extend its logical capabilities. Quantities of such chips, differing only in the personalities of their AND-gate blocks, can be interconnected to provide any kind of code translation with a source code having no more than eight bits.

A third method of chip layout and fabrication is the programed interconnection pattern (PIP) or discretionary wiring approach [see page 143]. This technique is similar to the master-slice except that each chip produced has a different interconnection pattern, though the same logic is implemented. Since this method also permits the use of identical masks and processes up to the final fabrication stage, the unique-part cost is concentrated in one step. This technique may be economically feasible



Master-slice technique permits addition of metalization to mass-produced wafer to implement logic.

at certain levels of integration, device and interconnection yield, and density, but as circuit yield exceeds a certain level the fixed interconnection pattern becomes less expensive.

Attacking cost through logic

Another means of increasing the volume of standard parts is through logic implementation. One technique involves the deliberate introduction of redundancy or superfluity on one chip to make it useful for several applications. The table shows the estimated increase required in the circuit density of various functions to standardize them for use in a typical medium-performance application.

The amount of extra logic one can afford to add in order to reduce the number of different parts can be evaluated in terms of the advantages of part repeatability within one particular system. The cost of an LSI part of a given type can be expressed as

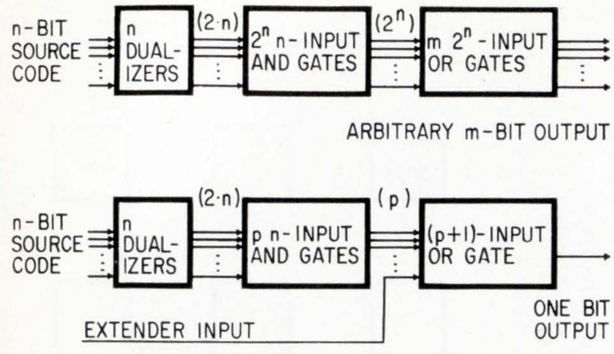
$$C_P = C_M + C_T = \frac{C_G}{V} = C_{MF} \quad (2)$$

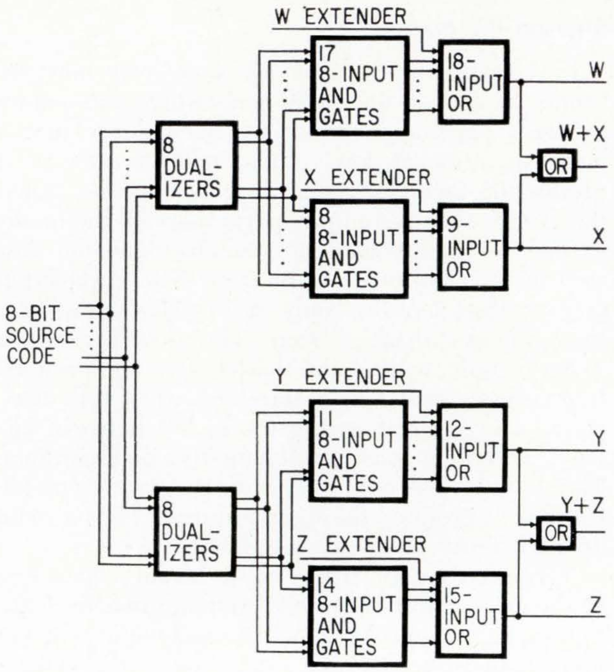
where

C_M = manufacturing cost per part (processing plus first-level packaging)
C_T = test cost per part
C_G = generating cost per part number (masks,

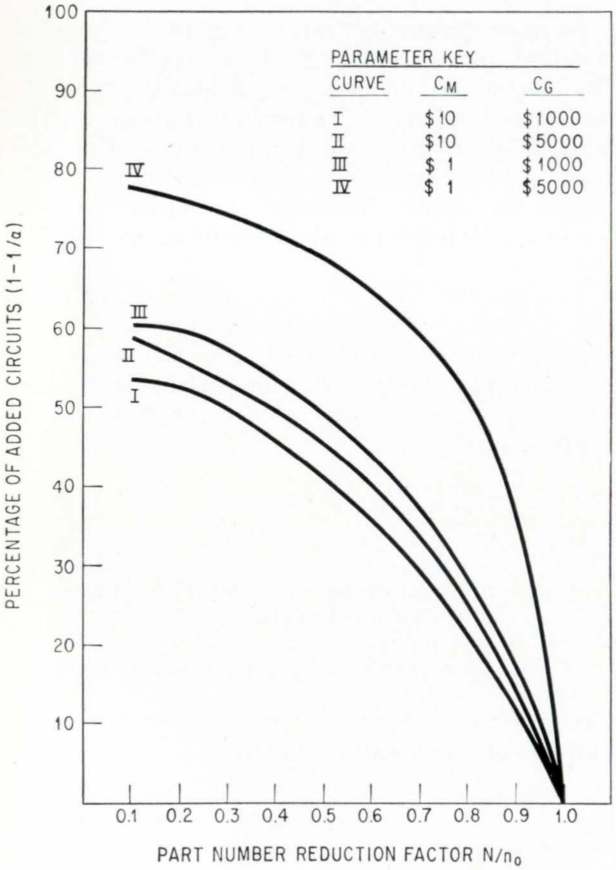
Effects of standardizing functions

Functional part	% increase in circuit count	Relative weight in medium size system
Adders	Up to 50%	0.10
Buses	Up to 100%	0.25
Registers	100 to 400%	0.25
Control (ROS)	500 to 1,000%	0.40





Read-only store (ROS) can be formed on one chip with the master-slice technique by the interconnection of dualizers, AND gates and OR gates (top left). The dualizer furnishes the signal and its logical inverse (resembling two out-of-phase signals), as required by the AND gates. Generalized ROS is difficult to implement monolithically for source codes greater than six bits, so the unit cell would be somewhat simpler (lower left), with increased versatility provided by an extender connection. Eight-bit code translator (right) is formed by interconnecting combinations of such unit cells.



The number of different part types can be reduced by adding extra circuits. These curves show results of analysis of four different combinations of fabrication and packaging costs (C_M) and costs of design, test and documentation (C_G).

test patterns, documentation)

V = parts per part number (volume = useful volume + stock volume)

C_{MF} = field maintenance cost per part

The cost of a system is the summation of all the parts' costs, expressed as

$$C_S = \sum_{i=1}^{\alpha n_0} \left(C_{M_i} + C_{T_i} + \frac{C_{G_i}}{V_i}\right) + BC_{MF} + C_{PK} \qquad (3)$$

where

C_{PK} = cost of the higher levels of packaging plus cooling plus power supply, etc.

B = the manner in which the maintenance cost varies as a function of the number of different part numbers, the number of systems in a given user location, stocking philosophy, etc.

N = the number of different part numbers in a system

n_0 = the number of unique parts needed in the system (the ratio of total circuits in a system to the integration level).

$$\alpha = \frac{1}{\text{utilization factor}} \geq 1 = \text{increase in}$$

system parts to allow for a decrease in system part numbers.

$1 - \frac{1}{\alpha}$ = fraction of circuits on a chip that are extra, or supernumerary.

Equation 3 can now be solved with C_S kept constant to find the relationship of α to N. The results shown above were determined under the following assumptions:

$C_M = C_T = C_{PK}$

C_{PK} varies directly with α

$\begin{pmatrix} C_{PK} = C_{PKO} \text{ for } \alpha = 1 \\ C_{PK2} = 2C_{PKO} \text{ for } \alpha = 2 \end{pmatrix}$

On-site stocking

One machine per location

$$C_{MF} = 2\left(C_M + C_T + \frac{C_G}{V}\right)$$

Increase of V due to $N \neq n_0$ has a second order effect on C_M and C_T.

Results applicable to any size machine as long as the same distribution of system parts in a part number is used.

In general, the analysis shows that:

- The higher the values of C_M, C_{PK} and C_T, the fewer the supernumerary circuits that can be added to achieve a given part-number reduction.
- The larger the ratio of C_G/C_M, the larger the number of supernumerary circuits that can be added to achieve a given part-number reduction.
- More supernumerary circuits could be added if C_M and C_T are reduced significantly with volume.
- Fewer supernumerary circuits could be added if a more optimistic stocking and system distribution philosophy were used.

Even for the wide range of parameters considered, the maximum number of supernumerary circuits indicated by the analysis doesn't appear to allow a practical one-part-type system—all chips in a system alike—at least in terms of conventional thinking. However, further significant reduction is possible.

Organizing for processing power

With LSI, low-cost logic and storage hardware can be used to tackle software problems

Most general-purpose commercial computing machines are organized on the basis of the von Neumann concept: a single central processor that executes sequentially a single stream of instructions, a main memory, and input and output facilities. The current trend toward more complex machine organization is principally spurred by a need for greater system capability.

Parallel data processing has been increased within the von Neumann concept by: boosting the parallel computation capability of such arithmetic processing functions as adders and multipliers; expanding the number of bits in the primary instructions of the machine to include several microinstructions, each to be executed in parallel by semiautonomous functional units of the system; and increasing the types of processing units that execute microinstructions ranging from arithmetic functions to logical, shift, editing and machine monitoring and control functions.

These efforts have put more hardware to work to improve total system capability, and they point to further steps that can be taken to exploit the cost reductions expected from LSI. The increased parallelism in machine structure provides the opportunity for a high order of part repeatability, so necessary for LSI.

Entire system affected

The standardization of chip types affects all facets of system organization—the arrangement of storage units, the manner of system control, the degree of sophistication in the central processing units (CPU), the variety and degree of autonomy of peripheral equipment (input-output), and the trade off between hardware and software for the over-all system.

One way to achieve part repeatability in small machines is to find some area of commonality among several different machines, such as some shift-register storage, an adder, some counters, etc. A common part might then be built using only three or four chip types in an efficient manner. The remaining parts would be peculiar to each different system and could be implemented through the master-slice technique or other more conventional technologies.

In the large-machine category, the use of parallelism in the organization could doubtless achieve considerable commonality of parts, though the picture here is less clear.

Main and functional storage

From the standpoint of system organization, a distinction can be made between the main storage units used in the classical manner (serial as well as random access) and so-called functional storage units such as read-only stores (ROS) and content-addressed associative stores. In an associative storage system, data is addressed and retrieved from the main store by name rather than by reference to its physical location in the memory. An associative store is characteristically prodigal in the use of logic circuitry, and serves as a good example of how hardware can replace software.

The significance of LSI to storage-unit design is immediately apparent in the small number of different chips required for memories. If they are properly designed, many replicas of two or three chip types can be fitted together to create quite large stores. Associative stores could be constructed out of standard chips to translate the names of data into physical-location addresses.

Central processors

The greatest logical complexity in most systems is found in the area of system control and arithmetic processing. Included in the CPU are temporary storage registers (for instructions and addresses as well as alphanumerical data), adders, counters, decoders, all the accompanying "traffic control" switching circuitry, sizable collections of heterogeneous combinational switching-circuit networks of varying width and depth, and sequential circuits consisting of latches, triggers, and flip-flops interconnected in various complicated ways.

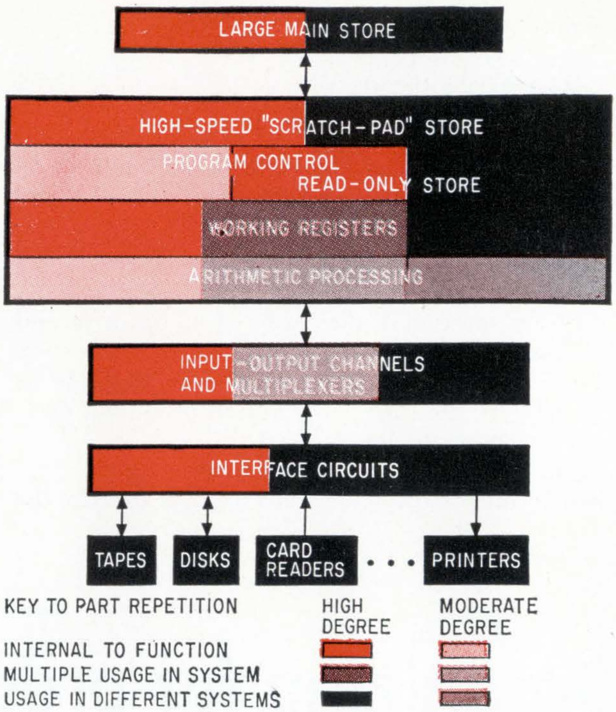
Some of these, particularly the registers, which often comprise 30% to 50% of the CPU circuits, can be designed as modules and made exactly alike except for word length. The same is true for adders, with binary counters included as special cases. Much can be done in the systematizing of so-called "control logic" by deliberately adding redundancies and superfluities to the chips for the purpose of standardization. Doubtless the ROS master slice can gain a wider role in microprogramed control devices and in the construction of combinational circuitry. For sequential circuits, the use of a general-purpose-logic master slice is attractive.

The interfaces between the main store and peripheral equipment (input-output channels) execute multiplexing, buffering, format control and synchronization functions. They bear certain resemblances to the CPU insofar as their organization is concerned, differing mainly in the reduction of arithmetic functions, and they possibly can utilize the same standard chips in their design.

Peripheral equipment

With regard to peripheral equipment, the modern trend seems to be to include as much or more digital circuitry in all the input-output units of a complete system as is built into the CPU. This trend will probably be accelerated in the future, and it's expected that LSI will have extensive applications in peripheral equipment by virtue of the degree of standardization it allows and of the specialized data-processing functions that can be incorporated.

For example, remote terminals now in use in time-shared systems could be expanded in computing power, flexibility and autonomy to any desired degree. Certainly LSI will find a place in the interfacing circuits of existing devices—magnetic tapes and disks, card readers and punches and the like—requiring code translations, code checking and buffering. The technique can also lead to the development for the mass market of highly sophisticated but compact devices for improved communications between man and ma-



Degree of part repeatability in a modern computer system. Degrees of shading indicate proportion of circuitry that can be duplicated in the various system functions.

chine. These devices include document readers, voice-recognition and vocal-response gear, graphic displays and graphic input units.

At home with the computer

Small but flexible remote terminals in the private homes of the future will be connected to computing centers by telephone lines. The programing languages used in this linkup will have to be extremely simple; experimental software systems have already been developed to enable untrained persons to use a limited-vocabulary programing language to solve simple problems.

At this stage, it seems that improvement in the man-machine interface is primarily a software problem; the main role of LSI here will doubtless be in data acquisition and display devices. More preprocessing of data by low-cost logic at the source will reduce the amount of information transmitted over communication facilities and aid in data multiplexing.

There is considerable concern today about the cost of computer software—both on the part of those who use machines to solve their problems (applications programers) and those who create the program to match the machine to the user (system programers). While the programer shortage worsens, expenditures on software today almost equal the outlay for hardware and are growing at a faster rate.

How can LSI help to alleviate this situation? Well, in the broadest sense it can lead to hardware that will simplify the programer's job. LSI can benefit applications programers, for example, by improving input-output equipment, increasing the information capacity of systems and reducing their response time.

Where hardware ousted software

System functions that have been converted from software to hardware in large machines include:

- Special instructions (multiply, divide, shift, logical, editing).
- Interrupt (branch to another instruction when specific internal or external conditions exist).
- Channel capability (for example, concurrent operation of input, output and computation).
- Look-ahead (permits parallel processing of instructions that don't depend on one another).
- Dynamic storage relocation (procedure for making a hierarchy of storage look like one large main random access storage to the programer).
- Storage protection (restricts unauthorized access to specified areas of storage).

With the advent of LSI, these functions can be included in the hardware of small systems, and greatly extended in the hardware of large machines.

The increase in reliability expected with LSI will lead to a reevaluation of error detection hardware and may result in the remodification of systems organization to include some new concepts. Intermittent failures in present computers may interrupt programs and necessitate a search for the point of failure and a rerun from that point. Despite an anticipated reduction in intermittent failures with LSI, it may be advantageous to incorporate in the system an automatic "instruction retry" feature.

Where we are headed

This has been an attempt to predict the future of an evolving LSI technology under a number of system and hardware design constraints. The forecast has generally been cost-oriented, but "ultimate" LSI costs weren't considered and it was assumed that other cost-competitive means of logic implementation were available. It was further assumed that part-number costs were very significant in small-quantity systems. In this environment, LSI would be applied first to:

- Special small storage applications where the constraints are minimal and where magnetic arrays (including peripheral circuits) aren't now economically attractive or don't meet performance requirements.
- Selected logic systems such as small computers, terminals and input-output equipment, or subsystems to be produced in large quantities.
- Selected portions of systems that can be widely used within and between systems.

Over-all, the increased logic and higher-performance storage per dollar offered by LSI will be used to ease hardware constraints and, more importantly, to expand the capability of systems to handle a growing number of computing, man-machine and software functions.

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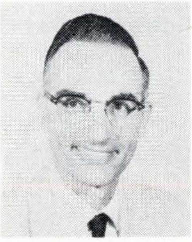

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Merlin G. Smith is currently responsible for research into the engineering aspects of an LSI program.

Large-scale integration

Active memory calls for discretion

High yield of 1600-bit memory slices is assured by a computer that converts test data into an interconnection pattern that bypasses defective cells. The approach is called discretionary wiring

By Michael Canning, Roger S. Dunn and Gerald Jeansonne

Semiconductor-Components Division, Texas Instruments Incorporated, Dallas

A high-speed general-purpose computer now being developed for the Air Force's MERA program[1] will be constructed of high-density bipolar arrays interconnected by discretionary wiring. This is an ambitious and sophisticated approach to large-scale integration.

Like the master slice, or 100%-yield approach, discretionary wiring interconnects groups of circuits or cells with multilevel metalization to form complex functions on a single silicon slice. But with discretionary wiring, each cell is tested prior to interconnection, and only the "good" circuits are used in the final array. This greatly increases the yield of usable slices, especially at high-component densities where defective cells are bound to occur.

The MERA (molecular electronics for radar applications) computer is designed around transistor-transistor logic (TTL), and the logic portions as well as the memory are being fabricated in LSI arrays. For the logic, 881 five-input NAND gates having an average propagation time of 12 nanoseconds are fabricated on a slice of silicon. The gates are tested after the first level of metalization, and good gates interconnected with two discretionary metal layers to form the desired function.

The memory for this machine is in two parts. One is a nonvolatile (it retains the stored data after power is removed) read-only memory for storing the program, various constants and "look-up" tables, and the other is a read-write memory for storing the processed data. The complete memory system is designed to be compatible with the logic portions in terms of circuitry and packaging.

Ideal for LSI

For a number of reasons, the active memory described in this article is a particularly useful vehicle for proving out the concept of large-scale integration in general, and the technique of discretionary wiring in particular. First, a basic product in the form of an array of X words containing Y bits can be applied to many functions ranging from scratchpad memories to shift register applications. As in nondiscretionary approaches, this offers the customer the advantage of availability, and offers the producer standardized testing and low development costs.

A second important feature of active memory arrays is the regularity of interconnection of the memory cells. This permits the use of a simple two-level lead pattern requiring very little silicon area for interconnection. Thus, the circuits per unit area may be maximized while the yield loss associated with more than two levels of processing is avoided.

The interconnection regularity does require the formation of a rectangular matrix of memory cells on a circular slice; a simple matrix is inefficient in the use of material. However, by including the word drivers and address decoders on the same slice, the total active area is increased, and a drastic reduction in pin connections achieved. Hence, over 1,000 cells on a chip may be controlled with about 100 pin connections.

Memory circuits

A memory cell designed for large-scale integration must meet several requirements. First, it must be small so that the slice can be used efficiently and the cost per bit minimized. Second, it must be of simple design and tolerant of large parameter variations to increase circuit yield. Third, the power dissipation of the cell should be low to reduce the cost of packaging and cooling. Fourth, its output signal must be large enough that sensing it does not limit the performance of the memory. Fifth, the cell should be fast enough to be useful in a large number of applications. Finally, the drivers and sense amplifiers must be compatible with the system logic, and the cell should allow the slice to be adaptable to a variety of organizations.

The cell designed for use in this system is a basic flip-flop storage element with provisions, by means of two emitter transistors, for writing into and reading out of the cell.

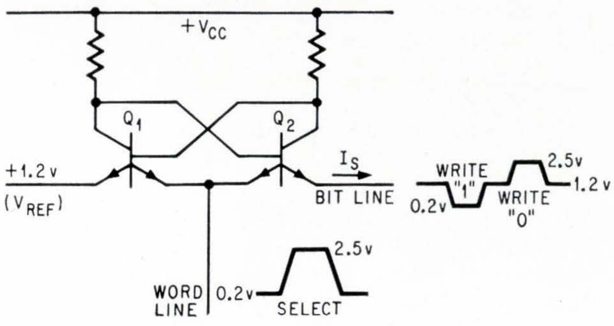
To understand the READ operation of the cell, assume that Q_1 is conducting and the cell state is defined as 0. The collector of Q_1 and the base of Q_2 is at $V_{CE(SAT)}$ volts above the unselected word line potential, or about 0.3 volt with respect to ground. The base of Q_1 and collector of Q_2 is at V_{BE} above the word line voltage or about 0.9 volt. The emitter of Q_1 connected to the word line is conducting the sum of the base and collector currents. If, while the V_{REF} line and bit line are held at 1.2 volts, the word line is raised to 2.5 volts, current flowing in the emitter connected to the word line will be switched to the V_{REF} emitter. If the cell stores a logical 1, this current is switched to the bit line where it is detected by a sense amplifier.

To write information into the cell, the word line is selected, and during selection the bit line is driven to either 0.2 volt or 2.5 volts, depending on whether a 0 or 1 is to be stored. If the bit line is driven to 0.2 volt, Q_2 is switched into conduction, and remains in that state when the word line returns to the non-select state storing a logical 1. Similarly, a 0 will be written if the bit line is driven to 2.5 volts during word select.

The circuit occupies a very small area on the slice. The present design requires an area of about 8 x 15 mils, allowing space for the bit-line contact pad and lead routing. This permits more than 3,800 cells to be fabricated on a 1¼-in. slice along with the required word drivers. Many such cells may be connected to the same word line, the number limited primarily by the word driver capacity.

Switched power

The memory requirements for low power dissipation, high signal current and short propagation delay are basically contradictory. However, a circuit has been developed which solves this problem



Basic memory cell is a flip flop with multi-emitter transistors arranged to permit writing and reading the state of the cell. More than 3,800 of these cells can be placed on a slice with required word drivers.

in a unique way. Since only one word line in the memory is selected at any time, unselected words require merely enough power to maintain noise immunity. Any excess power consumed by unselected words is inefficient. The word-driver circuit therefore, is designed to raise the power level of the cells on a word line during selection, and to reduce the power dissipation of unselected cells.

The word-driver circuit is shown at right. Before selection, Q_2 is saturated and grounds all word line current. D_3 is forward biased through R_1 and R_2. This forms a low voltage supply for cells connected between lines W_2 and W_1, where W_2 is the cell supply line and W_1 is the word line. During selection, Q_2 is turned off and Q_1 on. The voltage on lines W_2 and W_1 is raised, increasing the supply voltage to the cells and selecting the word line.

In the low power, non-select mode, the cell dissipates about 0.3 milliwatt. During selection, cell power is raised to 3.5 milliwatts where read delay time of the cell is approximately 15 nsec.

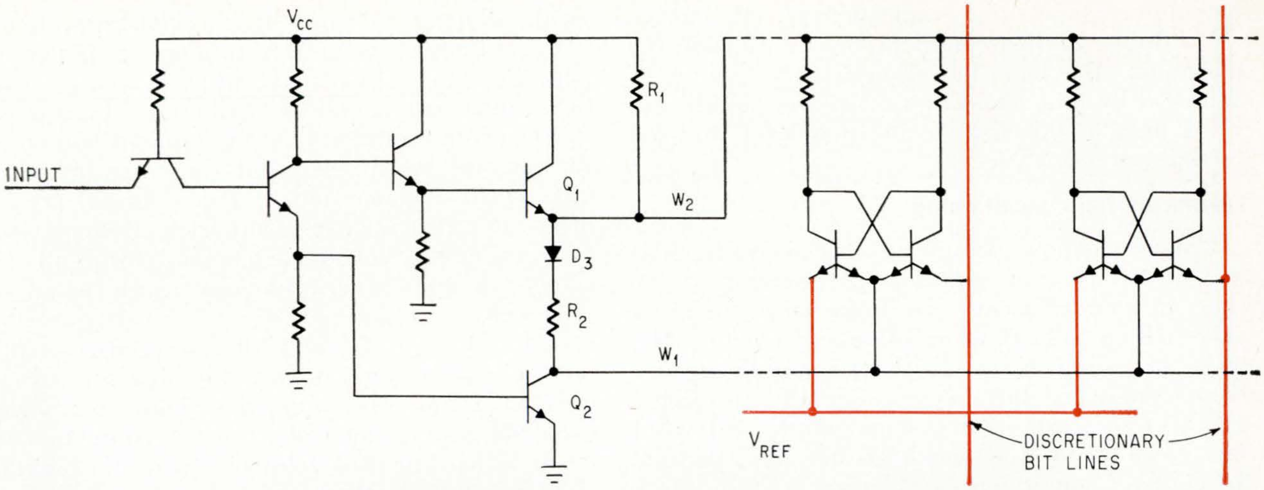
Without this provision, power dissipation in the array would be more than 6 watts for a typical slice containing 32 words. With provisions for switched power the memory cells are arranged in columns separated by an interconnection area. It should be noted that since the whole unscribed slice is packaged, no extra area need be left between circuits for scribing.

Cell parameters of particular importance are signal current, and bit-line leakage current when the cell is storing a 1 in the non-select mode. The minimum cell 1 current is specified at 500 microamperes and this parameter is tested in each cell. When the unselected cell is storing a 1, a small leakage current will flow into the emitter connected to the bit line due to the inverse current gain of the transistor. This 1 leakage current must be kept small, since it diverts signal current from the bit line when another cell on that line is selected. Switching the supply voltage to the cell reduces this leakage current by reducing the cell's operating current and its degree of saturation. Inverse current gain is minimized by doping the transistors with gold, to reduce the carrier lifetime. Also, the resistance of the base tends to reduce the saturation, and hence the leakage current.

The maximum leakage allowed on an unselected cell in the 1 state is 2 microamperes. This means that if 128 cells are connected to a bit line, up to 256 microamperes could be subtracted from the signal current of 500 microamperes, leaving only 244 microamperes of effective signal current to be detected by the sense amplifier.

Compatibility makes sense

The sense amplifier must provide an output compatible with TTL system logic. It must maintain the bit line voltage within very narrow limits during sensing and therefore must exhibit low input impedance. It must recover from very large overdrive within a relatively short time and must have a



Word-driver circuit keeps power requirements low by reducing the power to unselected words and activating only selected cells. Transistor Q_1 acts as the power switch and Q_2 grounds unselected word line current.

reasonably short propagation delay.

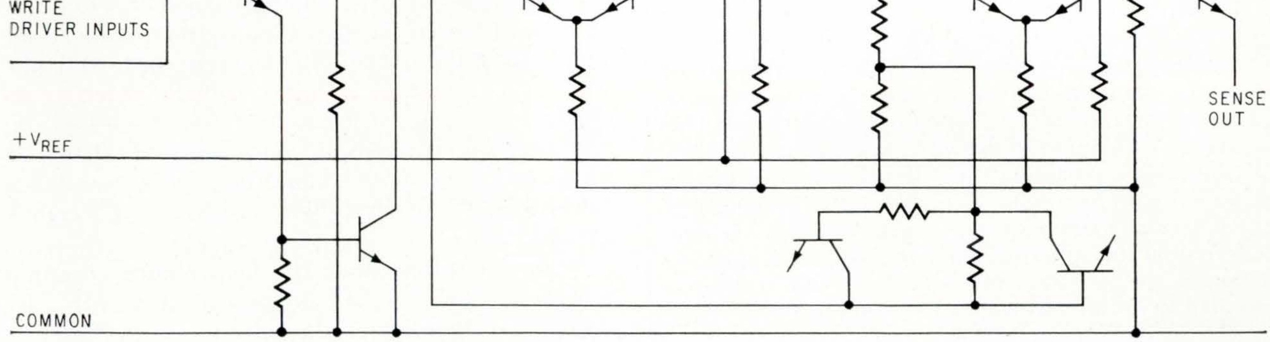
The sense amplifier circuit designed to meet these requirements is shown below. It has a propagation delay of 30 to 50 nsec and recovers from write pulses on the bit line in 50 nsec. The output stage is an emitter follower so that up to eight such circuits may be connected together into a positive wired-OR function. A SENSE INHIBIT line is provided so that sense amplifier outputs may be inhibited by a control signal. The WRITE circuit is simply a TTL gate with an added inhibit feature, so that when the WRITE INHIBIT line is lowered to a logical 0 the voltage on the bit line is determined by the sense amplifier and V_{REF}. Fifty sense amplifiers and 50 write drivers are discretionarily connected on a separate array to accommodate each 256-word by 25-bit memory module.

A memory module then, contains five circuit types: logic gates for decoding, memory cells, word drivers, sense amplifiers, and bit drivers. The word drivers are each capable of driving 50 bits, and the bit drivers and sense amplifiers will handle 128 bits.

Slice partitioning

In an LSI memory, the cells on the slice must be arranged to produce a maximum number of good circuits per slice and a minimum number of output pin connections. For this reason the circuit design was constrained to use a single bit line per cell for both reading and writing. While separate read and write lines would permit higher operational speed, more pin connections would be needed and more importantly—fewer cells would be available since the interconnection area required would be greater than the cell area.

Two word lines per cell are permitted because the word drivers on the same slice fix the number



Sense amplifier must be able to detect minimum current of 244 microamperes and maintain low output impedance. Fifty of these sense amplifier-bit drivers are required for each 256-word module.

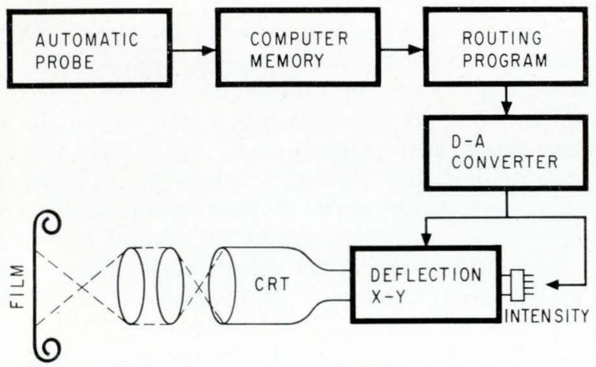
of address input pin connections to the array.

With these design considerations established, the maximum freedom for discretionary wiring is achieved by interconnecting the power supply and word lines at the first metalization level, and the bit lines at second level.

Memories help partitioning

Unique characteristics of memory arrays can also be exploited to get efficient partitioning of the slice. In memory arrays, the basic cell in the array can itself be a small array of several circuits. The yield on such a group of cells is naturally smaller than a single cell, but the area required for a single cell with its own discretionary supply and word line connections is so much greater than the cell area alone, that it is more efficient to form large arrays by discretionarily wiring groups of cells that have been preconnected by fixed wiring.

The preferred arrangement is to group the cells as parts of a single word. Each group then requires only one supply line and two word line connections for all its cells. This approach combines the benefits of fixed interconnections with the higher yields afforded by discretionary interconnections.



How discretionary wiring works

The heart of Texas Instruments' discretionary wiring facility is the multilevel interconnection generator (MIG) which produces the final interconnection pattern mask. The MIG system is shown in block diagram form above.

Good and bad cells on the slice are determined by an automatically stepped multipoint probe controlled by a computer. This test information is stored on tape for later processing by a high-speed central computer facility in direct contact with the test facility.

From the automatic probe test data, a unique discretionary interconnection pattern is determined by the computer that bypasses defective cells on the slice and achieves the desired over-all function. This becomes the input to the MIG, in which a computer-controlled cathode-ray tube beam generates the required pattern on film. The mask image is generated by incrementally exposing small spots on the film based on the data from the interconnection program. Masks generated in this way have line widths as small as 1 mil, with 1-mil spacing between lines. The procedure only takes a few seconds.

For details, see the picture story on page 148.

By positioning the cells in columns, as shown on page 147, the bit lines may run horizontally across the columns and no silicon "real estate" is required for their interconnection. At the top and bottom of the columns, word and supply lines are linked to other good columns and to the word drivers by means of a discretionary connection. With present tolerance limits, the interconnections at the end of a column of cells occupy an area nearly equal to three cells.

Redundancy in the form of extra cells incorporated in each column reduces the area needed for interconnections and improves group yield. The extra cells provide more space for the discretionary bit lines that cross the columns. They also provide some design flexibility because the internal connections may be changed while holding the external pin connections constant.

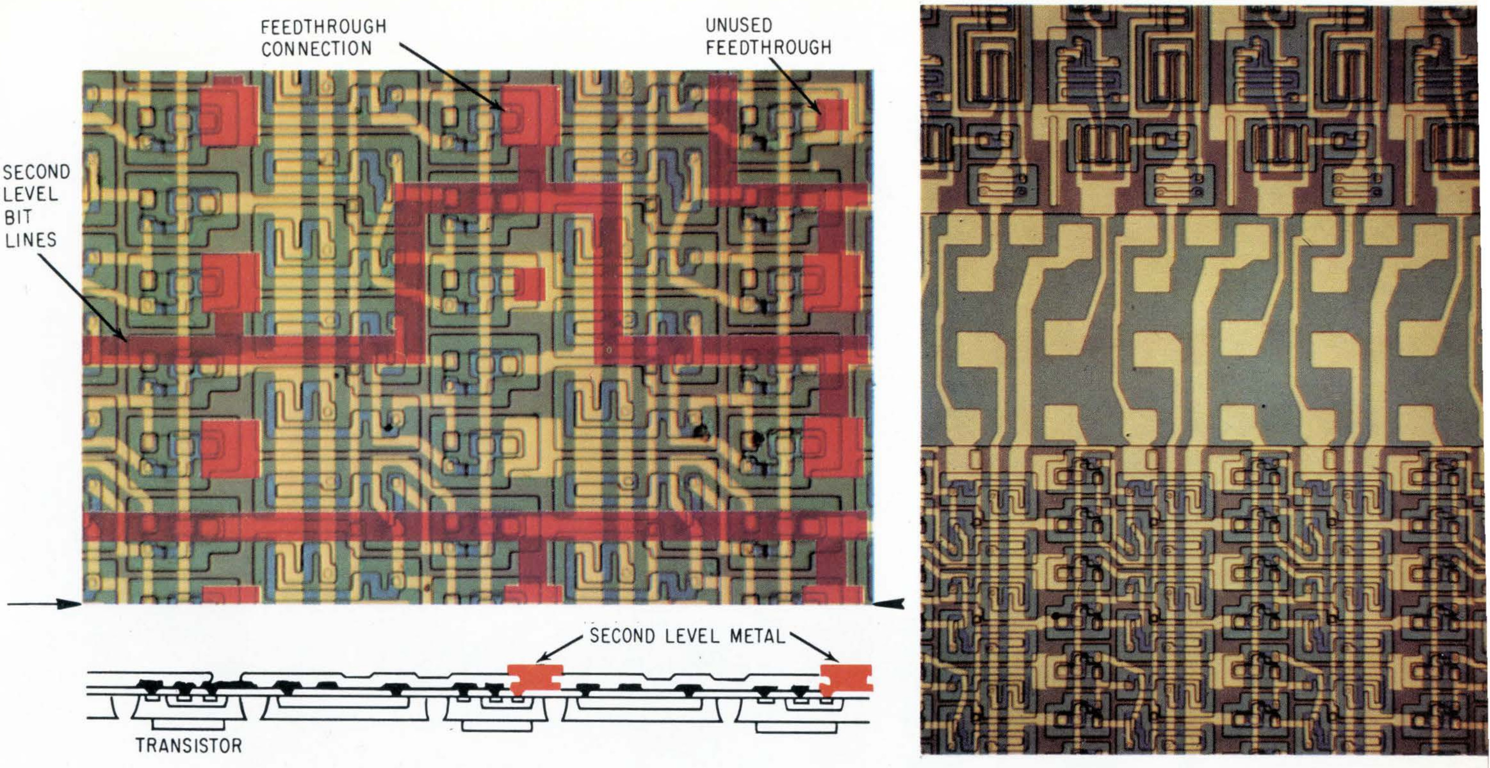
With preconnected redundant cell groups, two failure modes are possible. Such defects as transistors with high inverse leakage will affect only one cell, but a short circuit from supply line to substrate would eliminate a complete column. Data on the expected cell yield and the relative predominance of these two types of failures permits a calculation of the probability that a preconnected group of cells will be good.

If each column contains m preconnected cells of which (m —n) are redundant, the probability of obtaining at least n good cells from the m cells available must be established. For the case where m = n there is a certain probability of obtaining a good group, which increases sharply under the influence of redundancy and reaches a peak at a particular value of m. Then, as the influence of catastrophic defects becomes more pronounced, the probability of obtaining a good group falls and no advantage results from further redundancy. Therefore the best group length is that which gives the highest probability of obtaining the required number of good cells.

The considerations that combined to fix the optimum slice layout were:

- Requirements of fewest possible pin connections with highest possible packing density defined the cell design, leaving its layout flexible.
- Slice dimensions (1¼ in. diameter) and memory specifications for 25-bit words indicated that the length of the array should correspond to 25 or 50 bits. The need for discretionary interconnections that consumed little silicon area narrowed the choice to a pair of 25-bit words for each word driver.
- Available processing data showed that cell yields in excess of 80% could be expected and that fewer than 4% of the cells would have catastrophic defects.

With this information, the final choice of group length was fixed at half of one memory word. By applying redundancy, the layout could best be achieved by designing the array in preconnected groups of 16 bits each, in which at least 13 good



Second-level discretionary wiring, shown in closeup at left, interconnects columns of memory cells. In unconnected slice at right, word drivers are at top, separated from memory cells by interconnection area.

cells were needed for a good group.

The actual slice layout was defined in terms of a 60 by 64 cell matrix. Under these circumstances, the probability of obtaining a good word was estimated to be greater than 0.5. With a maximum of 60 words available on each slice, this meant that at least 32 good words should result. Consequently, only one row of word drivers across the top of the array was required.

Memory organization

The memory is organized around a basic block of 1,024 words and 25 bits per word (figure on page 151). Up to 32 such blocks may be assembled to make a memory system with a capacity of 32,768 words.

Each word block is divided into four 256-word modules, each module being handled by a set of 50 sense amplifiers. The modules are further divided into four groups of 64 words each. Each memory slice in the module, then, contains 32 word drivers (one per word pair) and 1,600 bits of memory.

Eight sense amplifier outputs are wire-OR'd together for each output data channel and a buffer gate is connected between the wired OR and the interface. Address decoding is divided into two levels. At the first level, five address bits are decoded to select one of 32 word-pair lines; and four additional bits select one of the 16 groups. At the second decoding level the word drivers are selected by a single "even-odd" address bit which gates the sense amplifiers for selection of the top or bottom half of the selected word-pair. The organization of two words per driver halves the required number of word drivers and decode circuits.

In the present design, second level decoding is performed on two slices separate from the array slices. Though inefficient, this organization was chosen to simplify the slice design and the development of the slice circuits. The second-level decoder slice holds 64 decode gates, sufficient for two array slices.

The write drivers and sense amplifiers required for a 256-word module are on another separate slice. An additional slice contains the first-level decoding circuits, on another the required fan-out generation and the write-even and write-odd gates for a 1024 word block.

Therefore, a complete 256 word module comprises four memory array slices, two second-level decode slices and one bit-channel slice. A 1,024 word block consists of four such modules plus one first level decode slice for a total of 29 arrays.

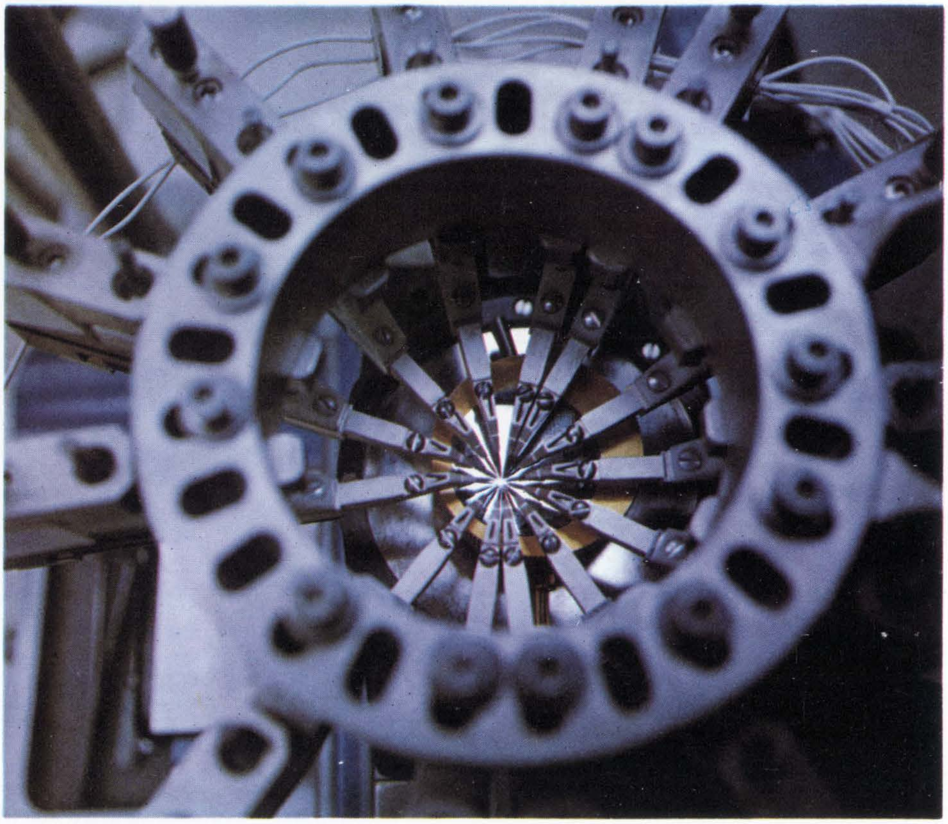
A new more efficient design is in progress where the word line driver is a three-input circuit, capable of performing second-level decoding. This will reduce the 256-word module to an assembly of five slices rather than seven, and will result in a 1,024-word block containing 21 arrays instead of 29. The new design will not only reduce the number of slices but the number of interconnections between packages as well.

First-level testing

The success of discretionary wiring stands or falls on testing of the circuits at the first level

Push a button and a mask is born

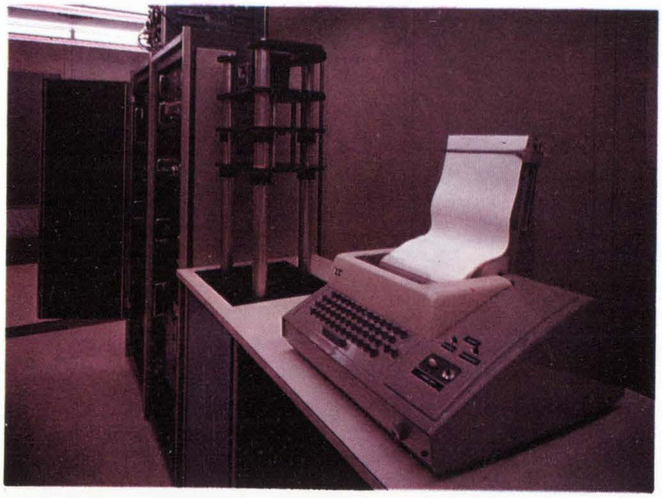
This technician is taking the first step in Texas Instruments' discretionary wiring process, initiating a test sequence on an LSI slice. After optical alignment of probes on a unit cell, the slice is automatically indexed until all cells are tested. Data from test equipment is stored on magnetic tape.



Each LSI unit cell is subjected to 32 electrical tests on this automatic multiprobe equipment.

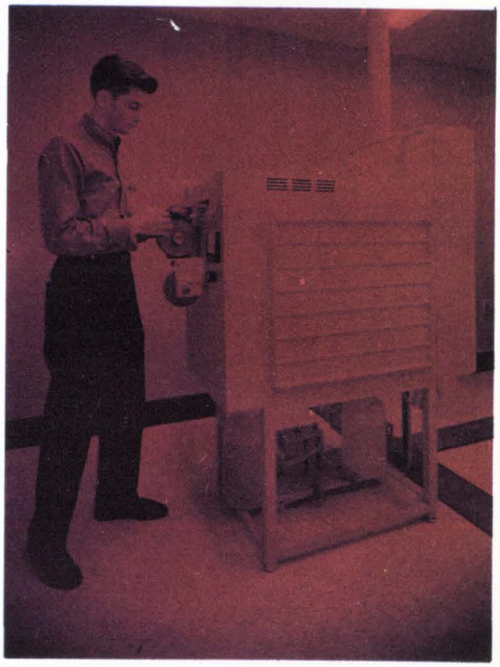
Test data is converted into a slice map showing location of good and bad gates (see p. 153). The map is transmitted in the form of magnetic tape to TI's computer center, where metalizing and insulator feedthrough routing patterns are determined for each slice.

Magnetic tape bearing the routing program from the computer center is used to control a TI 860 computer in generating an interconnection pattern. Here the program data is being checked out on a high-speed printout.

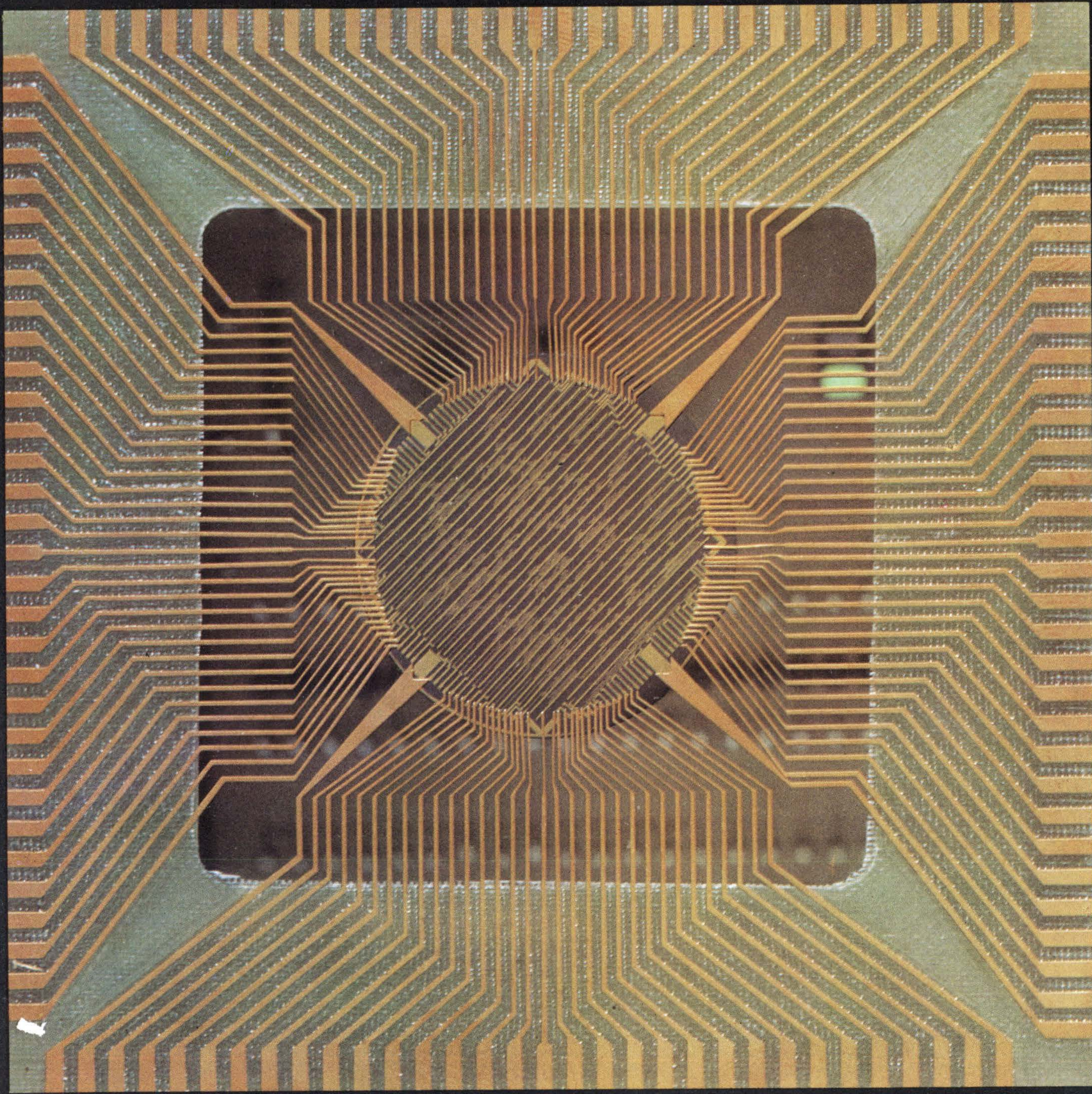


Computer-controlled pattern generator consists of a digital-to-analog converter, control electronics, a high-resolution cathode-ray tube and optical reduction film printing apparatus. Depending on the number of metal and insulating layers required, several masks are made for each slice.

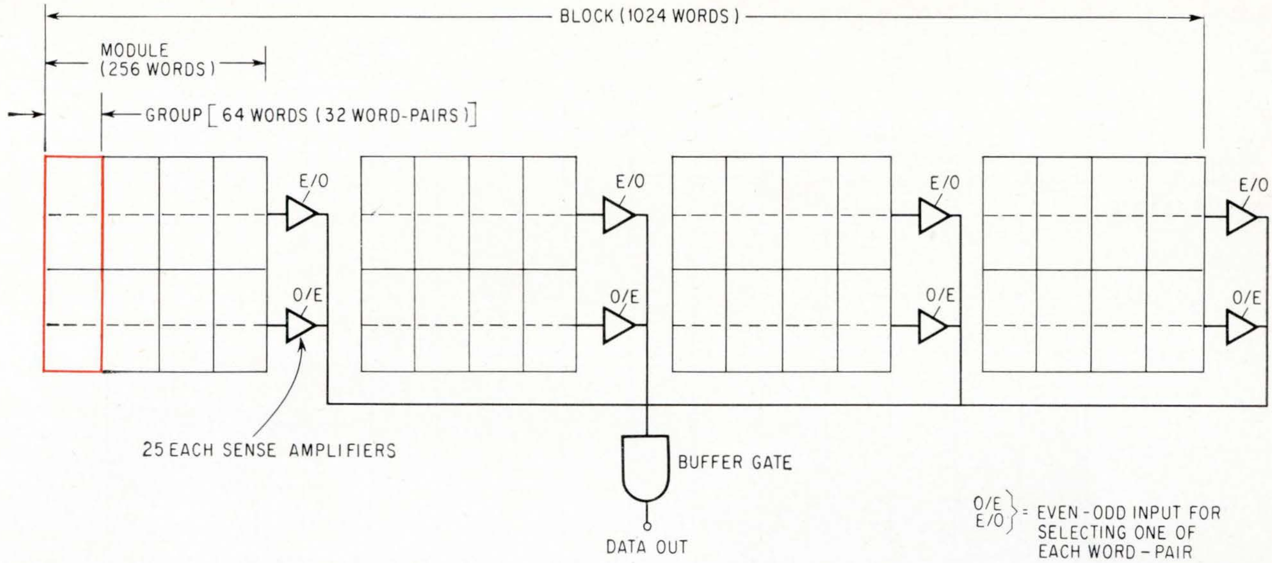
Vertical optical bench supports lens and camera system that records the patterns generated on face of crt. Photo shows roll-film camera in position to print crt image, but sheet film or glass plates may also be used.



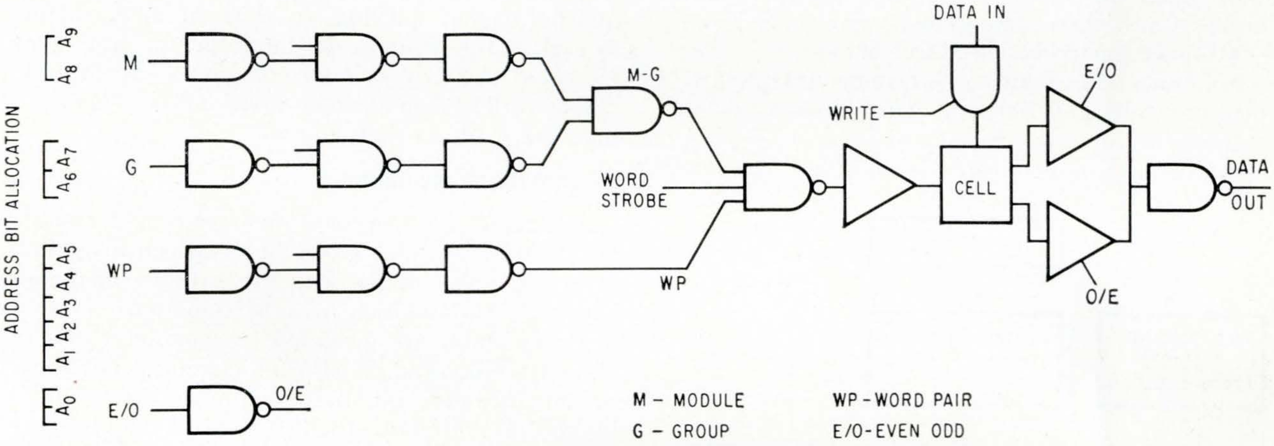
Film bearing the discretionary patterns is automatically developed in the same area. With this processor, film comes out in a few minutes completely dry and ready to be transported, with the slices, to the metal and insulation processing area.



Packaged LSI slice is 2½ inches square and has 32 leads on each side. After final metalization and insulation processes have been completed, the slice is sealed with a potting compound and mounted on a printed-circuit board frame. Leads are ultrasonically bonded to reduce package costs. TI refers to complex finished product as an integrated equipment component (IEC), as distinguished from a conventional IC.



Basic block of memory is 1,024-words by 25-bits. Each block consists of four 256-word modules and 200 sense amplifiers in groups of 50. Area outlined in color represents 64-word group which subdivides the modules.



Decoding is performed at two levels from a 10-bit address code, illustrated by logic diagram.

of metalization as indicated by the block diagram on page 152. At this stage, the location of usable cells or circuits on a slice must be determined very accurately. It doesn't matter too much if a few usable circuits are declared defective, but problems result if the test declares defective cells good.

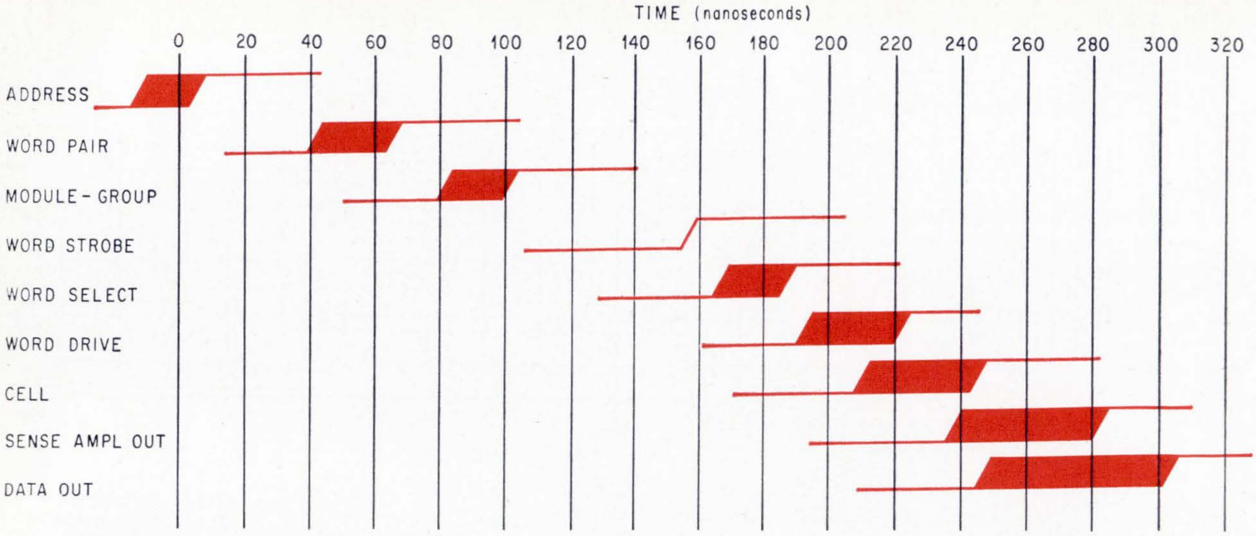
First-level testing is accomplished by using multipoint automatic probe equipment coupled to a TI-662 sequential integrated circuit tester. The results of the tests are recorded either on punched cards or on magnetic tape. Either individual parameters may be recorded, or simple go-no-go results indicated. Testing of most circuits is relatively straightforward—an input is applied and an output is measured. However, memory-cell testing poses a more difficult problem because the cell must be tested while in a known state, either storing a 0 or a 1.

Cells are tested in groups of four in the same preconnected group. There are eight probe points for the four cells—four of them (ground, cell supply, word line and V_{REF}) are common to all cells. The remaining four points are bit-line connections A, B, C and D. The test is designed so that worst-case conditions may be tested. Each cell is tested for its ability to store both a 1 and 0; other tests determine 1 current and 1 leakage current. An additional test detects the presence of a condition on the word line which would cause excessive loading on the word driver.

The test results are recorded on a slice "map" showing the location of each cell group. The test results form input data to the computer which generates the discretionary interconnection pattern for the second-level metalization photomask.

In the map on page 153, a dot represents a defective cell, and X represents catastrophic defects that eliminate the group. Note that relatively few failures are catastrophic. The over-all yield of groups containing 13 good cells is 84.4%. The word yield is limited by the minimum number of good groups in any one of the four sections. From this slice, a maximum of 41 words could be obtained, which is well in excess of the 32 words per slice specified for the memory.

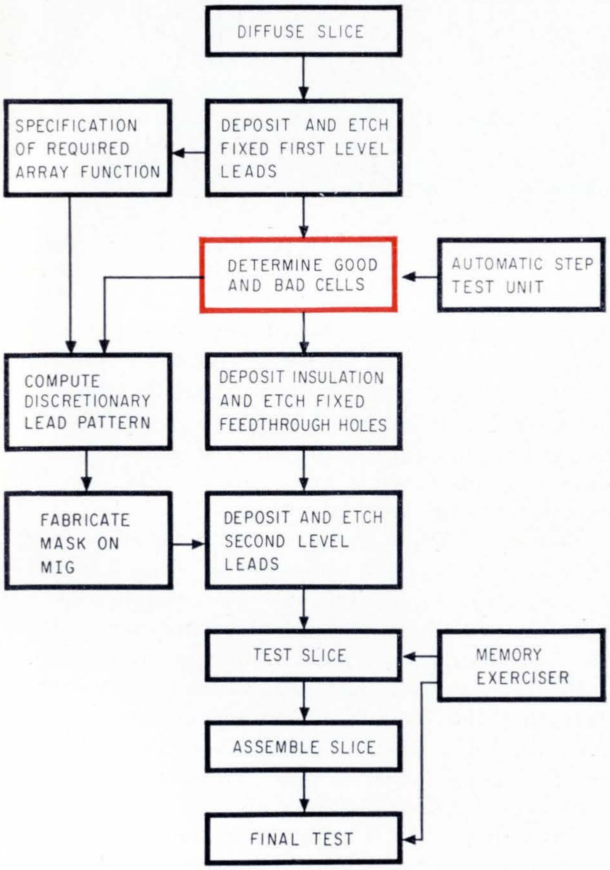
The computer-generated discretionary wiring pat-



Timing diagram of the memory-read cycle shows an over-all access time of about 300 nanoseconds.

tern illustrated on page 153 corresponds to the slice map. Interconnections on this pattern fall broadly into three categories:

- Discretionary bit line connections.
- Connections between preconnected groups of memory cells and between word drivers and cell columns.
- Connections between the array and the bonding pads along the slice periphery.



Testing is the heart of the discretionary wiring concept, as this diagram of the active memory fabrication process shows. Short turnaround time and design flexibility are provided by the multilevel interconnection generator, which can turn out the final mask in a few seconds.

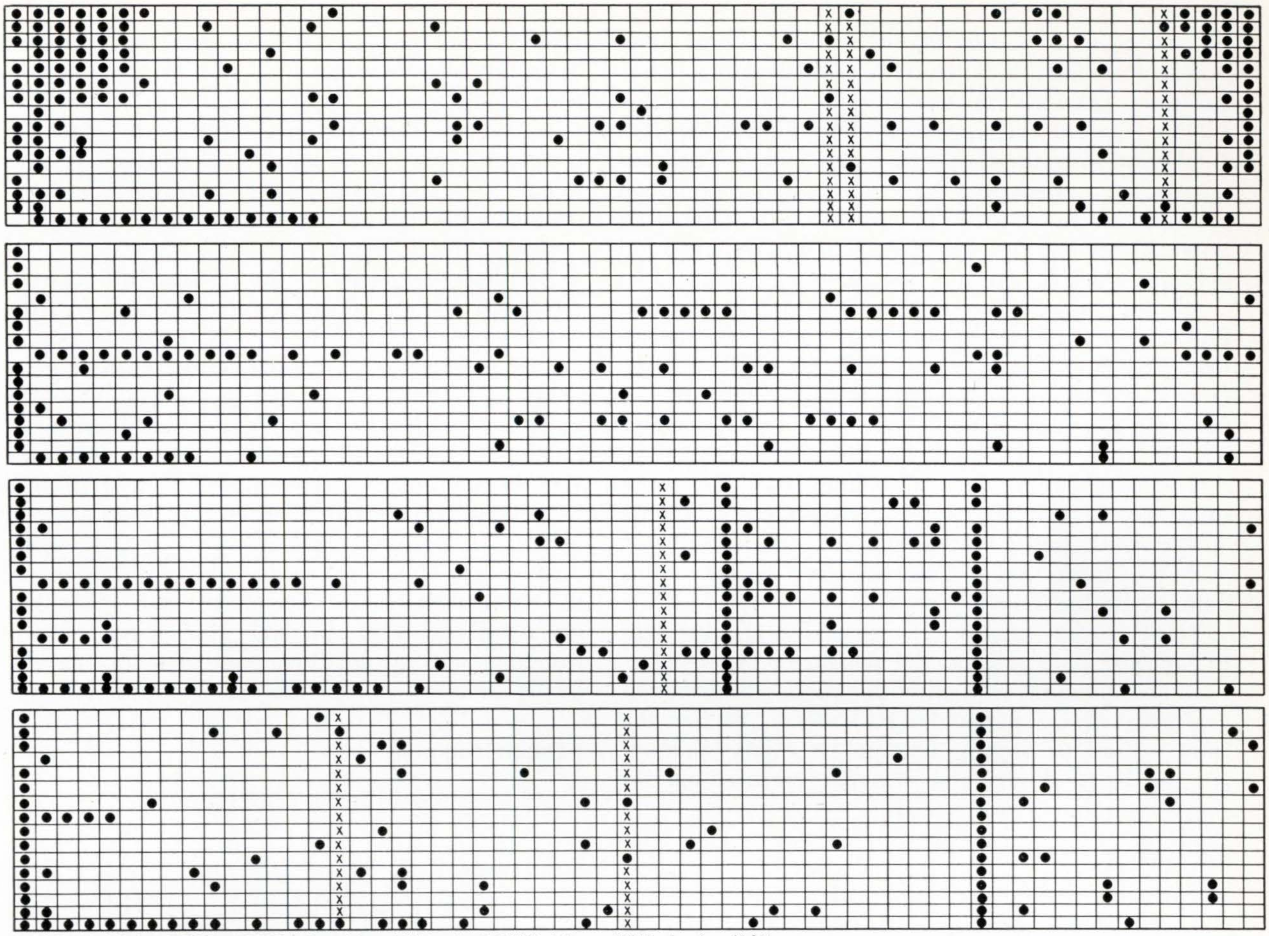
Thirteen discretionary bit lines connect to each quarter section, picking up thirteen memory bits in each usable column. If the automatic tester has indicated that any column contains a catastrophic defect or less than thirteen good cells, no connections are made to that column.

Fixed pattern insulation

The connections to good memory cells are made by small pads which cover holes in the insulation layer and make contact with the first level of metalization. The insulation is a fixed pattern, so that oxide windows are provided for contact to every memory cell on the slice. When contact is not made to any memory cell, these windows are avoided by the discretionary interconnections. Circuit layout is arranged so that there is sufficient room to run two interconnections between windows in adjacent rows and four interconnections between windows in adjacent columns. This provision of two horizontal and four vertical routing channels, and the use of a staircase interconnection pattern between columns where necessary, ensures that connections can always be made if a column contains at least thirteen good cells out of the sixteen available.

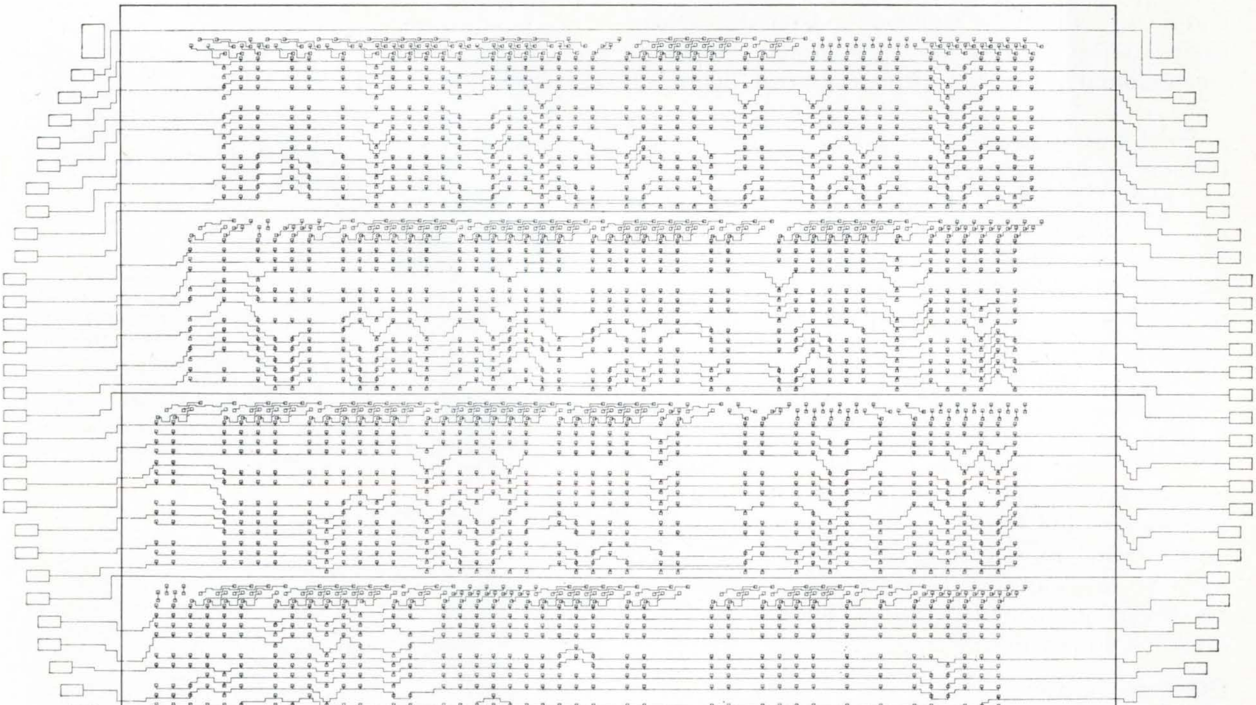
At the interconnection areas between quarter sections of the array and between the array and word drivers, three discretionary connections are made to each usable 13-cell column. One connection is made to the reference voltage line which runs across the slice at the bottom of each column and at the bottom of the row of word drivers. The other two connections, a word line and a cell supply voltage line, run through the interconnection area and link good columns in upper and lower quarter sections of the array.

Each good column in a section of the array may be connected to any one of the five columns immediately below it, provided that the column chosen is also good. This results in discretionary links, which are either vertical or move a maximum



SLICE NO. 0212, TEST LIMITS, I_0 -60μa MAX, I_1-0.6 MIN., 1.5 ma MAX., I_L-4μa MAX

Active memory slice map, produced by probe test of slice shows location of good and bad cells. Cells below specifications are shown as dots and catastrophic failures are indicated by "X." There are enough good 13-cell groups to qualify this slice for discretionary interconnection. Below is the interconnection diagram generated by the computer from the test data on the slice map.



of two column widths to either side. If this sideways movement is more than two columns, access to good columns in the upper section may be blocked, but if the upper section columns are bad the lateral movement may be more than two column widths, provided that no more than two good columns are bypassed. This flexibility in connecting good 13-bit columns ensures that nearly all good columns may be interconnected.

All the information required to define the discretionary interconnection pattern is computed from the automatic probe test data. This data becomes the input to the MIC which generates the final metalization mask. [See "How discretionary wiring works," p. 146 and picture story on p. 148].

Two depositions of radio-frequency sputtered quartz form the insulation between metal layers. The second level metalization, a molybdenum-gold system, is deposited and etched using the computer-generated discretionary mask.

Points to be connected externally are brought to bonding pads around the periphery of the slice. Fixed connections to the bonding pads are designed to ensure that a particular pad always carries the same signal or supply voltage on every memory slice. This facilitates the design of printed circuit array interconnection boards.

Packaging

The slice is packaged in a lead frame as shown on page 150. Leads are ultrasonically bonded to reduce package costs. The package is designed so that after the slice is sealed by potting, connectors may be plugged into the four edges for testing. After acceptance of the completed slice, the lead frame is sheared around the interior portion. This leaves weldable tabs protruding from the encapsulated slice package on appropriate centers for conventional multilayer printed circuit board design.

Final test equipment consists of a slice probe, memory exerciser and interface electronics. The TI memory exerciser (TIME) is capable of operating a 16,384-word by 50-bit memory, at up to a 700 nsec cycle time. It is programed by 120 rotary switches to write selected patterns into each word, to read each word and compare the output data to the proper bit pattern. Four preset bit patterns and their complements may be selected.

Interface electronics for coupling the slice probe to the exerciser include level shift circuits, address decoding, and bit-channel circuitry, all built on conventional printed circuit boards. The interface is designed for testing not only individual slices before and after packaging, but also 256-word memory modules with their sense amplifiers and bit drivers and complete blocks of 1,024 words containing address decoders.

Other applications

The 1,600-bit memory array is adaptable to a variety of applications. For example, a memory array may be addressed sequentially to function as a 1,600-bit shift register or as a digital delay line. This operation requires the addition of an input data accumulator and a sequential address counter, but with a 1,600-stage packing density the extra logic is insignificant. The feasibility of another technique which uses the discretionary wiring approach to produce up to 800 shift-register stages on one active memory slice is being evaluated.

Another possibility is to change the first-level metal pattern on the basic memory slice to form a fixed read-only array of several thousand bits.

The present day capability of 1,600 bits per array is determined primarily by cell yields and mask tolerances. As these factors are improved by techniques already demonstrated, the distribution of signal and supply current to circuits will ultimately limit cell sizes and the number of bits per array. Nevertheless 10,000 bipolar cells per array will be achieved in the foreseeable future and even more in MOS arrays. Thus it is probable that active memories will be used not only for special memory functions and applications, but also for the mainframe memory of commercial computers.

Acknowledgment

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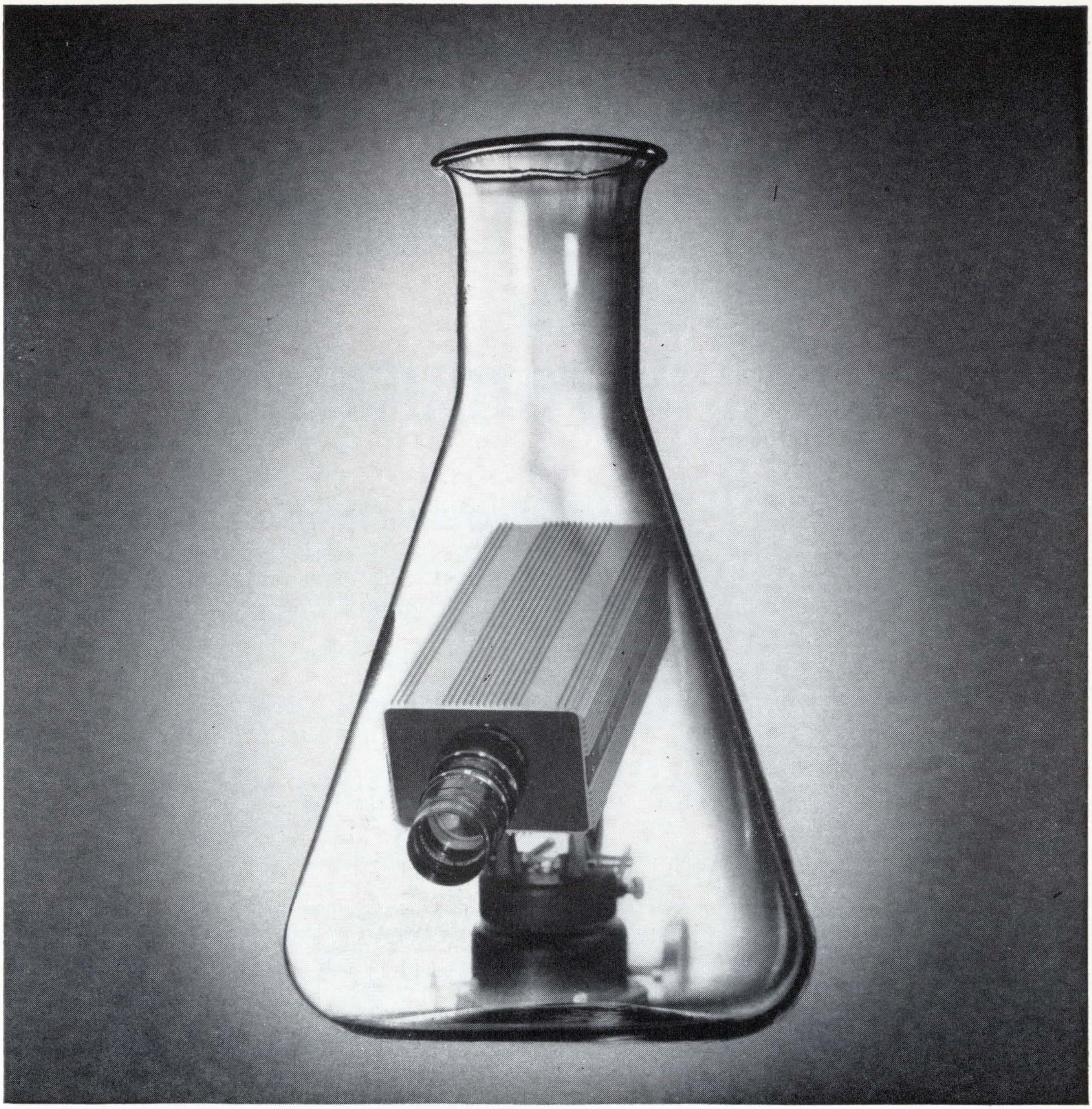
Gerald Jeansonne joined TI in 1963 and transferred to the computer components branch in 1964. He was responsible for the development of logic and driver circuitry for a thin-film memory system, and helped design a scratch-pad memory.



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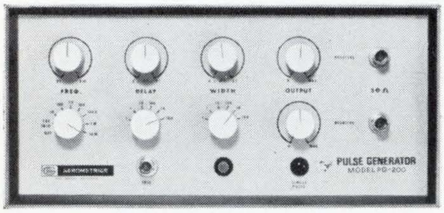

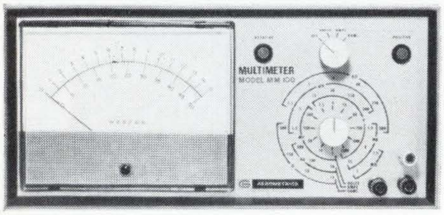

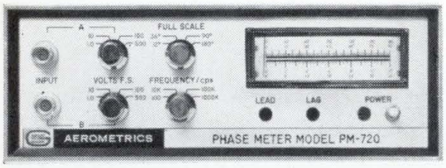

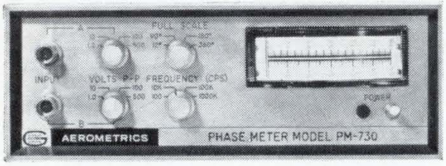

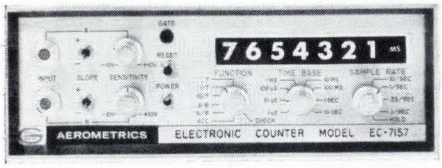

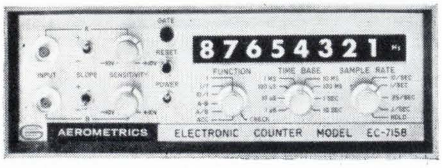

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Large-scale integration

Customizing by interconnection

One way to supply design flexibility and fast design turnaround is to start with a standard wafer and customize by metallic interconnection to produce a specific design

By Cloyd E. Marvin and Robert M. Walker

Fairchild Camera & Instrument Corp., Semiconductor Division, Mountain View, Calif.

The question of custom versus standard integrated circuits is being revived with the advent of large-scale arrays.

With LSI, the economics of custom versus standard arrays is greatly complicated by the interrelationships of yield, circuit density and the quick turnaround required to meet the customer's deadlines. There still will be a considerable demand for standard arrays composed of such repetitively used functions as shift registers, counters and simple arithmetic units like digital differential analyzers and analog and digital converters. Undoubtedly, custom arrays—subsystems equivalent to 300 to 400 gates—will also be available when large production runs justify the high design costs.

In the early days of IC's, the controversy centered around whether systems manufacturers would use off-the-shelf IC's and sacrifice a portion of contributed value to the device manufacturers in return for reduced costs.

The debate was resolved quickly when the semiconductor industry provided two alternatives for their customers. Standard circuits were made available in volume to meet the majority of needs, while facilities were also provided to produce custom devices for customers with special needs who were willing to pay the necessary development costs.

But what is needed now is an approach that satisfies the requirements of custom-built subsystems designed for moderate-volume sales, while permitting the customer a degree of design flexibility at low cost.

To meet this need, the Fairchild Camera & Instrument Corp.'s Semiconductor division has developed the Micromatrix, its version of the master-slice technique, which is described earlier in this issue [page 136].

Specialized cells

With Micromatrix, design families of cellular arrays, complete except for metalization interconnections, are provided. Each array consists of a predetermined matrix of component-pattern cells that can be interconnected to form the required custom circuit. In addition, each cell may be individually specialized by cell intraconnections to form one of a variety of fundamental building blocks, such as gates or flip-flops.

One of the fundamental rules of this concept is that customization is permitted only for the metalization connections, not for the devices. Basic wafers, completely fabricated up to metalization, will be stocked and drawn for custom arrays. This enables the wafers to be manufactured in high volume with correspondingly low costs. In addition to eliminating the costs normally involved in wafer processing and evaluation, this approach permits reduced in-process inventories of many different

The authors

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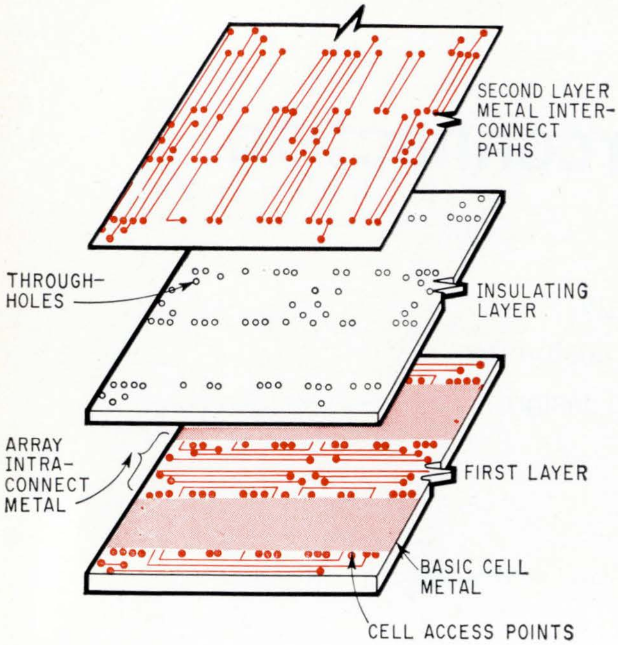


Multilayer metalization is the key to the Micromatrix approach to arrays. To provide a customized design from a standard chip, only three masks are required to complete the interconnection of the array cells.

wafer types, as well as greater process uniformity. Additionally, it provides for more thoroughly characterized devices and a large volume of data upon which reliability and failure-mode predictions can be made.

For obvious reasons, interconnection masks alone can be designed more quickly than a complete set of diffusion and interconnection masks, thus assuring a faster turnaround time than a completely custom approach.

The designer enjoys an almost infinite variety of alternatives in LSI array selection, including the number of cells, cell topology, speed, power, and MOS or bipolar. Even within a specific category, there may be requirements for special designs. For example, an array designed for general-purpose logic will not be particularly efficient for certain repetitive functions such as memory or decoding. Here again, the standardization inherent in Micromatrix allows many array types to achieve sufficient fabrication volume to be economically feasible.

Two-layer metal a must

The key to the feasibility of Micromatrix is the two-layer metal interconnection technique. Until recently, only area-consuming diffusion crossovers were available.

In the expanded view of a general-purpose cellular organized structure, the first-layer metalization pattern consists of the basic cell metal (identical for all arrays) and the first-layer array interconnections peculiar to that design. The first layer intraconnect can also contain bars of metal over the cell metal areas at predetermined points, allowing a degree of cell specialization.

An inorganic insulating layer is next applied and through-holes are etched where interconnection is required between the two metalization layers. The second-layer metalization is then applied, completing the chip. Only three masking operations, first-layer metal, insulating layer through-hole, and second-layer metal, are required to custom-connect each array.

In Micromatrix, testing is carried out after fabrication is complete; thus, if one cell is bad, the entire array is useless. This design philosophy is based on data that indicates yield is a much stronger function of chip area than of component density. Elimination of area-consuming test pads permits an array to be fabricated on a relatively small chip, while insuring reasonable yield. This approach is distinguished from the test-and-connect or discretionary wiring approach [see the article starting on page 143] in that no testing is performed at the cell level. What is often overlooked in evaluating the discretionary wiring approach is that four additional process steps are required after 100% testing of cells, followed by a complete array test. In addition, each final product will have its own unique interconnection and dynamic characteristics.

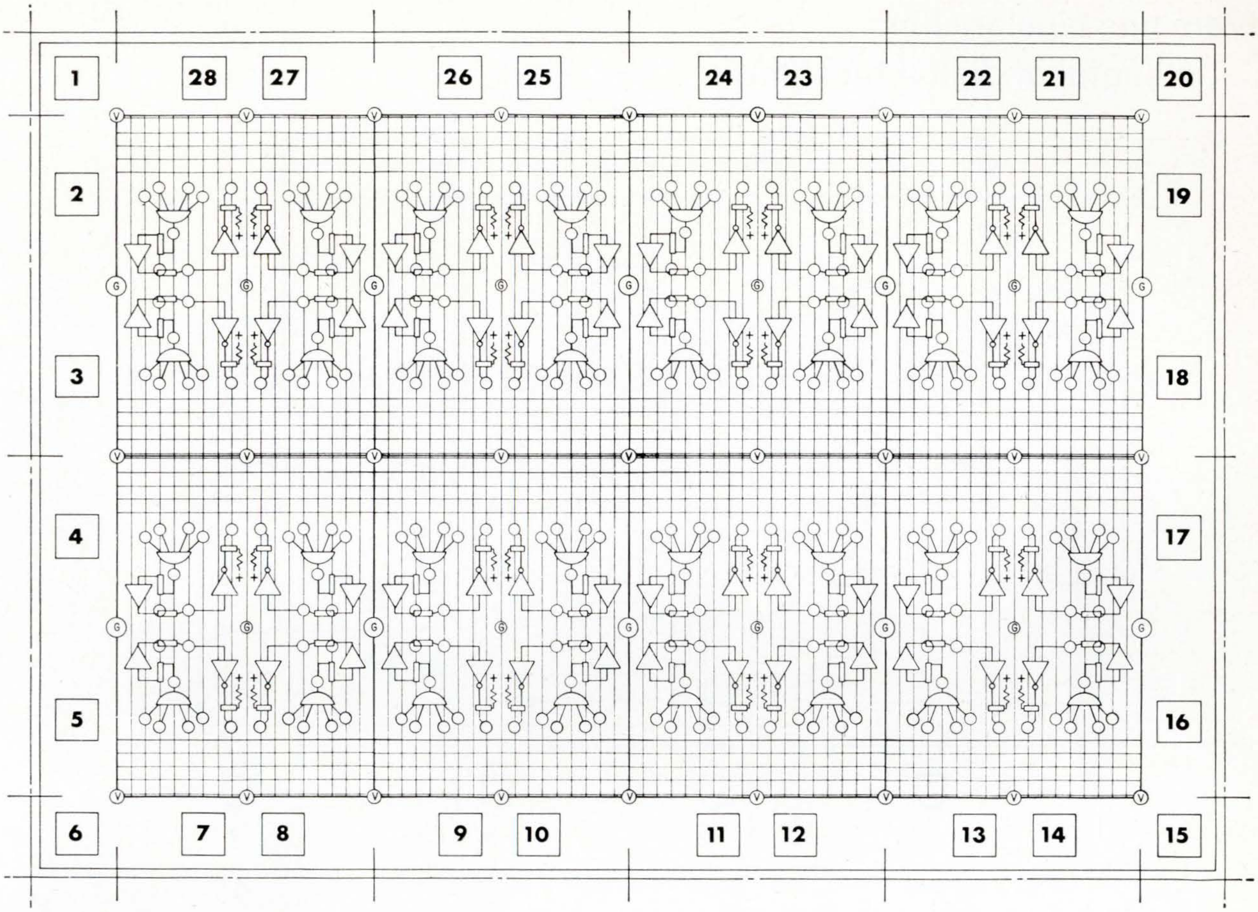
How designs proceed

The Micromatrix interconnection pattern is designed on the basis of logic specifications, provided by the customer. A step-by-step procedure is used for layout and interconnection artwork generation.

The specifications are analyzed and the appropriate array type selected. A design that will perform the desired function may already exist in a library of custom designs. Basic decisions concerning the use of MOS or bipolar technologies, and how many cells are required are made at this point. After the array is selected, cell and input-output pads are allocated. Design layout sheets are used to assign logic functions to specific devices; cell assignments are based on ease of cell interconnection, while bonding pads are chosen for ease of bonding to desired package pins.

The designer then lays out the two-layer interconnection pattern, using special layout sheets; device metal follows a precision X-Y grid. The process is similar to the layout of a conventional double-sided printed circuit board.

After layout, a set of precision artwork is taped, using the layout sheet as a guide. This corresponds to the first-layer metal, dielectric cut-pattern and second-layer metal. Using the artwork, a set of photolithographic masking plates is generated. These interconnecting patterns are then applied to the inventorized wafers containing the standard arrays of devices, and the custom design is complete. The systematic approach using the regularized grid of potential interconnection paths holds artwork to a minimum. For example, the BCD [binary coded decimal] decoder diagramed on page 163 was laid out and masks taped in eight man-hours.



Eight cells form Fairchild's 4500 bipolar array. Each cell contains four NAND gates designed with diode-transistor logic, each gate with four inputs. Extra versatility is provided by permitting each gate to be treated as a group of four independent elements.

Testing complex arrays is a formidable problem because of the inherent difficulties in testing large networks without access to intermediate cells and because the cost represents a large percentage of the price of the finished unit. The problem is so complex that fast, computer-controlled testers with rather sophisticated software will be required to test large arrays in production. While more powerful testers are being designed Fairchild is using a Fairchild model 8000A computer-controlled tester. A PDP-8 digital computer controls the functional testing of packages with up to 50 pins.

MOS versus bipolar

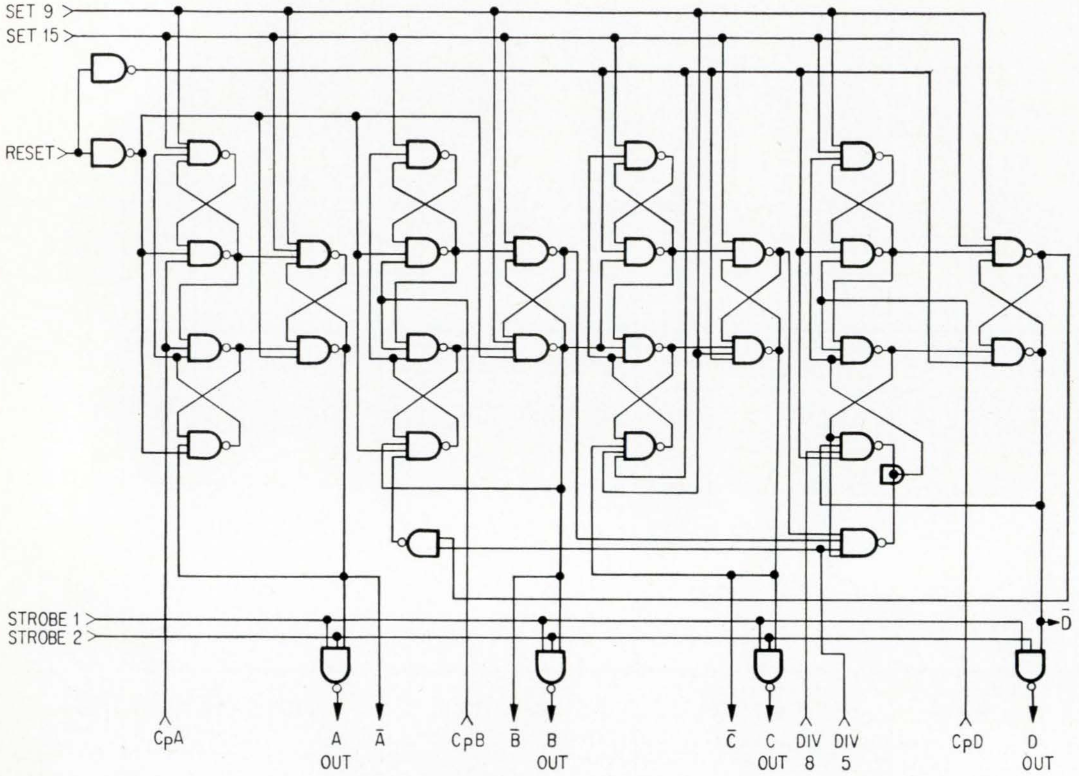
The controversy over whether MOS or bipolar technology is superior for LSI is not new. Some semiconductor firms have staked their existence on one technology to the exclusion of the other. Fairchild feels both techniques are useful, and the choice of implementation should be determined by the customer's system requirements. For example, a single-polarity MOS inverter, using an MOS load resistor exhibits at least twice the potential packing density when compared with the same circuit using bipolar transistors and a load resistor. This assumes similar process resolution capabilities. In addition, the MOS transistor's very high input resistance results in virtually unlimited d-c fan-out, and the low power requirements of MOS also enhance packing density by easing power distribution and ground requirements.

Bipolar IC's compatible

The bipolar transistor, on the other hand, shows a clear superiority on a speed-power basis. This results from the bipolar transistor's excellent transconductance per unit area, which in turn is a measure of the device's ability to charge and discharge capacitance. In addition, bipolar arrays are compatible with today's existing integrated circuit signal levels, power and logical organization. Bipolar arrays may be mixed with discrete integrated circuits and complex standard product integrated circuits for maximum cost effectiveness.

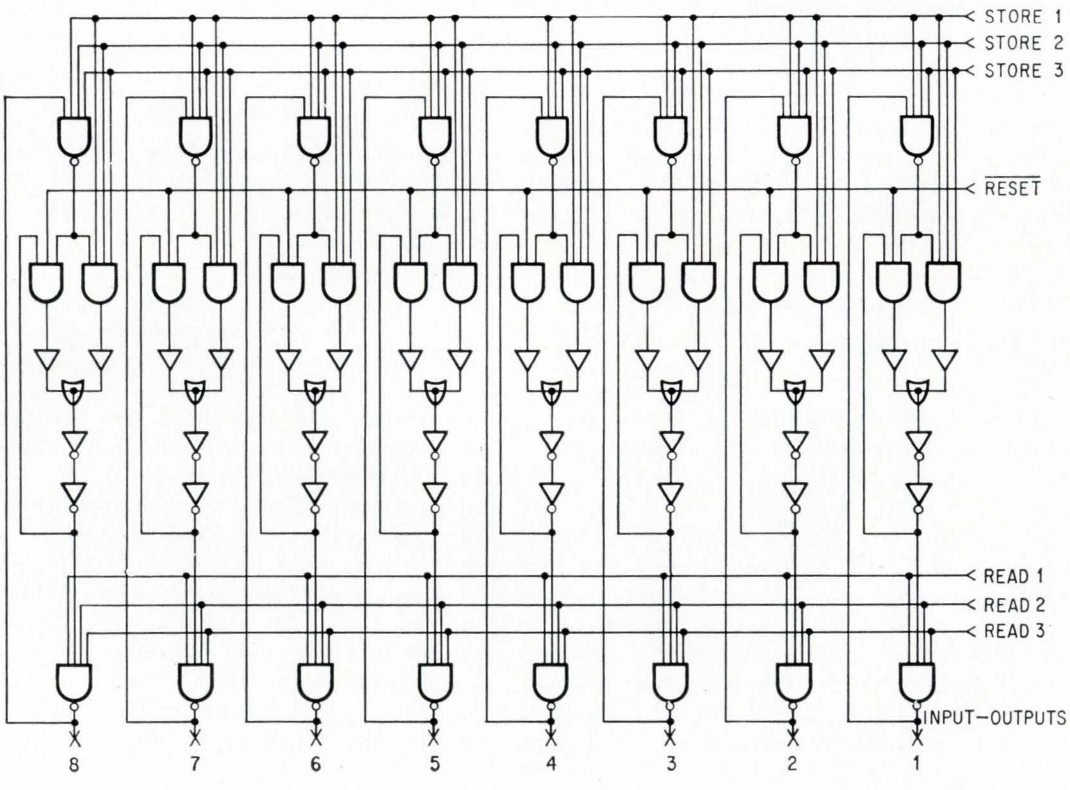
From the comparisons cited, it is clear that arrays using both technologies are required. Where the speed-power product and system compatibility permit, MOS is superior from a packing density standpoint. Where speed or power capability or both are at a premium, or compatibility with discrete integrated circuits or existing systems is required, bipolar is the choice. It should be noted that a favorite argument of the MOS advocates, namely fewer wafer processing steps, holds little

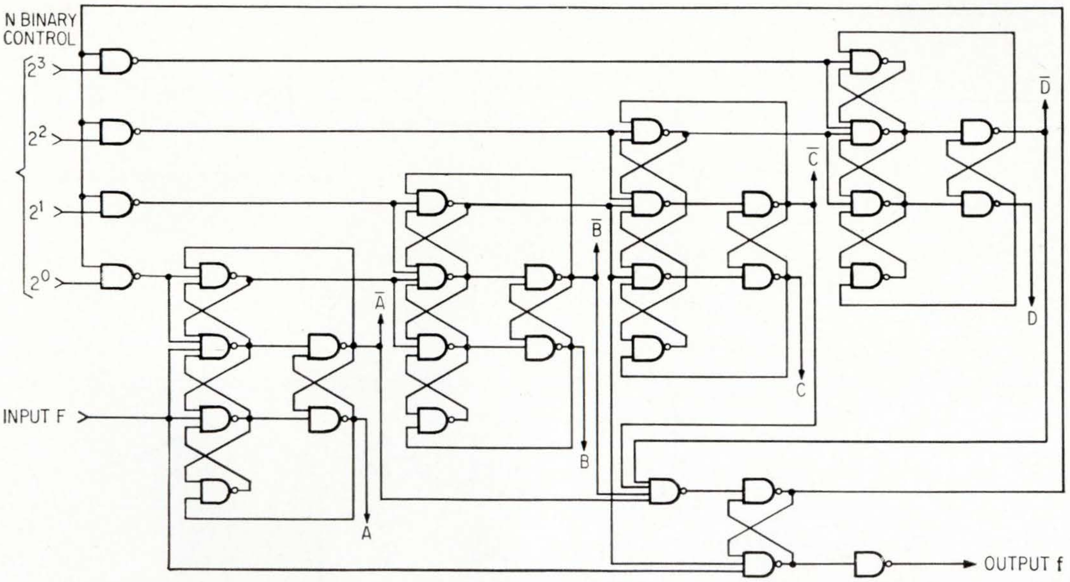
From one bipolar chip . . .
. . . a bagful of digital functions



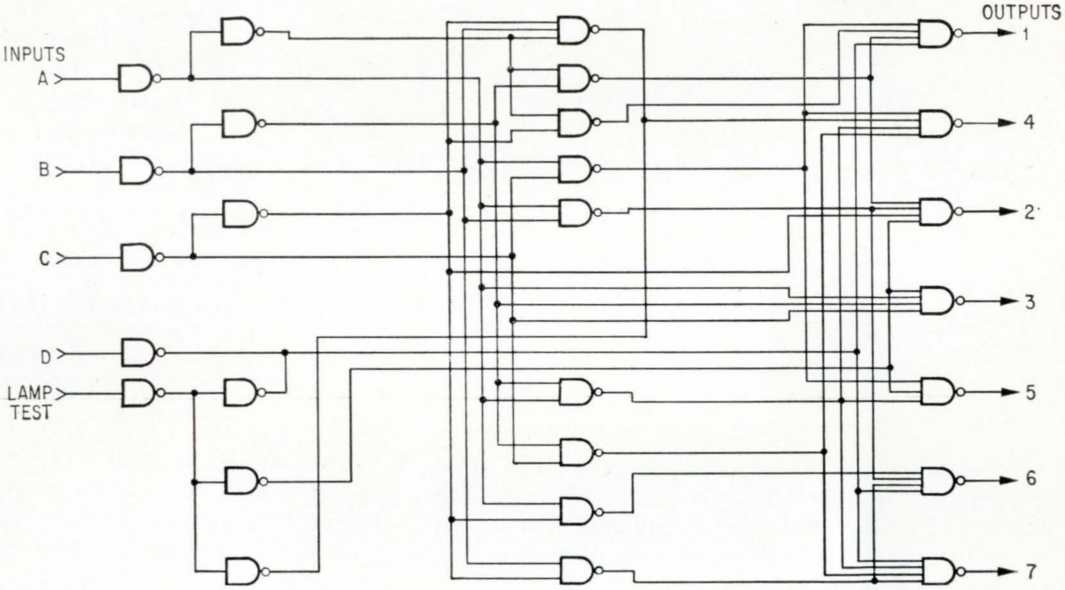
Four-bit ripple carry counter. External connections allow division by factors of 2, 4, 8, 16, 5 or 10. Strobed outputs are provided.

Word-organized eight-bit buffer storage. Data is transferred in and out of each flip-flop over a single input-output line.

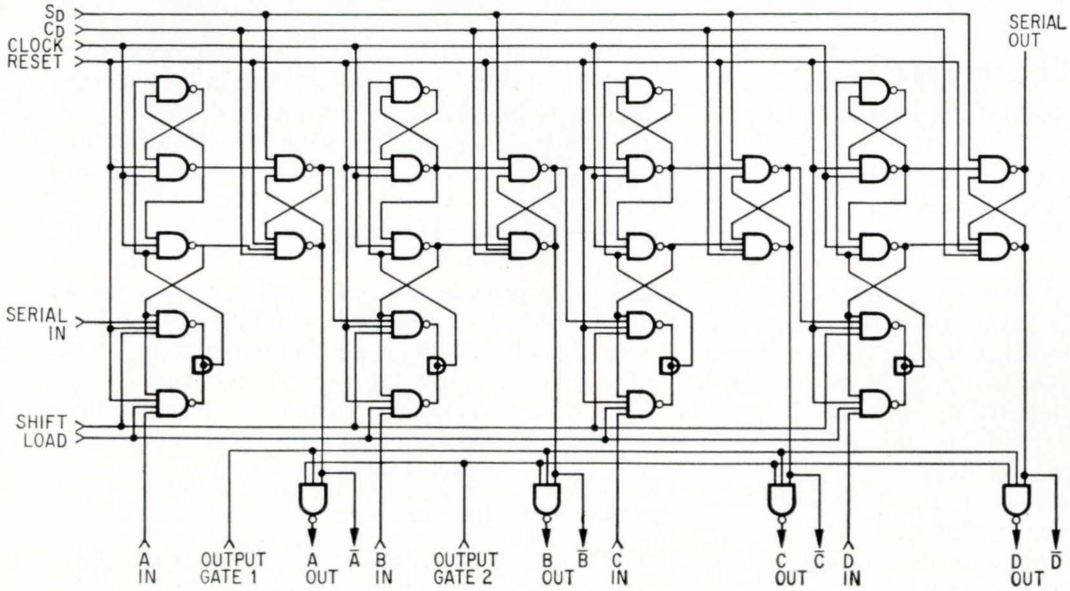




Four-bit, divide-by-N counter. Output frequency f=F/i, where F is input frequency and i any integer from 2 to 16. Output frequency is set by a four-bit binary input.

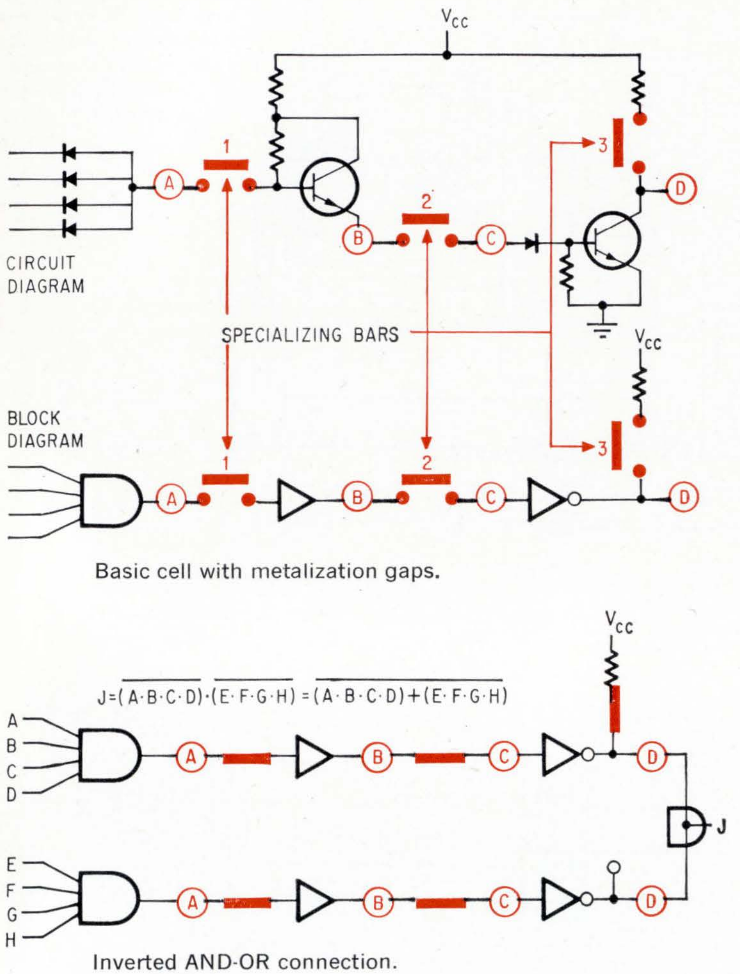


Decoder converts 1-2-4-8 binary coded decimal input to a seven-bit code suitable for driving a seven-/ segment numeric display. Discrete lamp drive-transistors may be driven directly from the logical 1 outputs of the circuit.



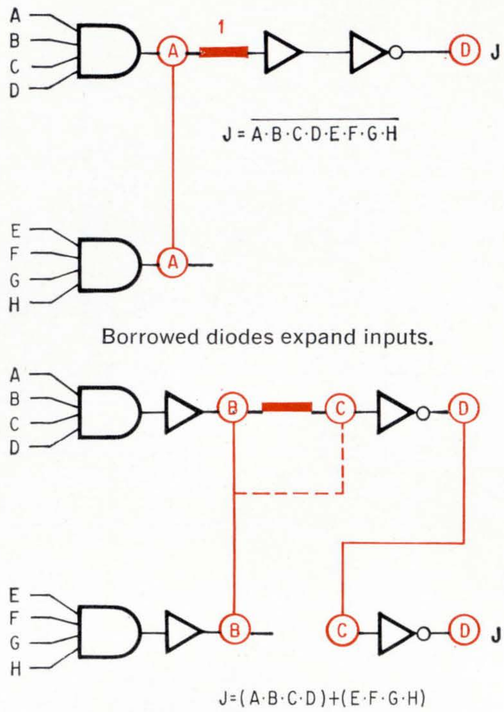
General-purpose, four-bit register adaptable for any combination of parallel or serial input or output. Control lines select either LOAD (parallel input) or SHIFT modes.

An extra measure of versatility



Basic cell with metalization gaps.

Inverted AND-OR connection.



Borrowed diodes expand inputs.

Wired-OR connection.

Gaps in the cell metalization (upper left) between elements of the basic gate can be filled in to get more logic design flexibility. Expansion of inputs is accomplished by borrowing a diode cluster from another gate (upper right). Two gates are connected to form AND-OR function (lower left) with inverted output available. Finally, OR gate connection uses only single load resistor.

applicability to Micromatrix. Unconnected array wafers will be produced in enough volume so that their processing cost will be negligible when compared to the other costs of custom interconnection, testing, and packaging.

Thus, the Micromatrix concept is independent of device implementation, and is being applied to both MOS and bipolar arrays under development.

An example of bipolar technology

One such array built using bipolar technology is Fairchild's 4500, composed of eight cells, arranged in a 4 by 2 pattern. The chip size is 80 by 110 mils with an active area of 6,000 square mils. Provision is made for up to 28 bonding pads for input-output signals and power.

The basic building block of the 4500 is the four-input, diode-transistor NAND gate; this logic configuration has well-known advantages of low power dissipation, a single power supply, high worst-case noise immunity and specified operation over a wide temperature range. In addition, the array is compatible with most forms of discrete integrated circuit logic such as DTL or TTL and Fairchild's new CCSL (compatible current sinking logic).

One unique aspect of the DTL NAND gate circuit of the 4500 array in the use of gaps in the cell metalization to allow connections not possible with discrete integrated circuits (illustrated above). The gate may be thought of as four independent elements: a diode cluster shown logically as an AND gate, a pull-up resistor and transistor shown logically as a non-inverting amplifier, a common emitter transistor shown logically as an inverting amplifier, and a load resistor. These elements may be connected by the use of "specializing" bars (first-layer metalization) to increase the logical power of the element. Expansion of the gate inputs is accomplished by using a diode cluster from another gate.

In another example, two gates are connected to form an AND-OR function. Note use of the left-over inverter to provide the additional inversion stage. The output gate "wired-OR" connection may also be used without loss of d-c fan-out margin, since only a single load resistor need be connected.

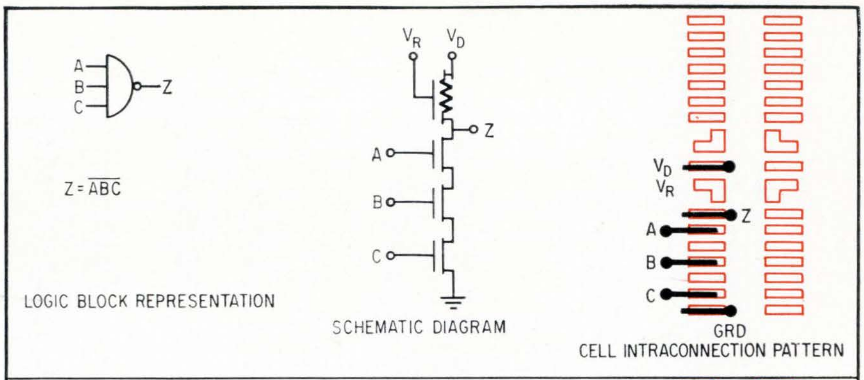
The 32-gate capability which is demonstrated on pages 160 and 161, makes the 4500 appropriate for a variety of useful designs.

MOS is versatile, too

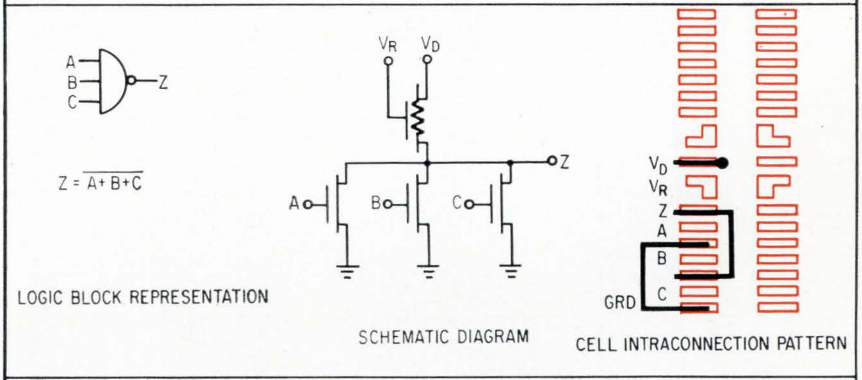
An example of MOS technology is Fairchild's

MOS cells offer quick-change logic

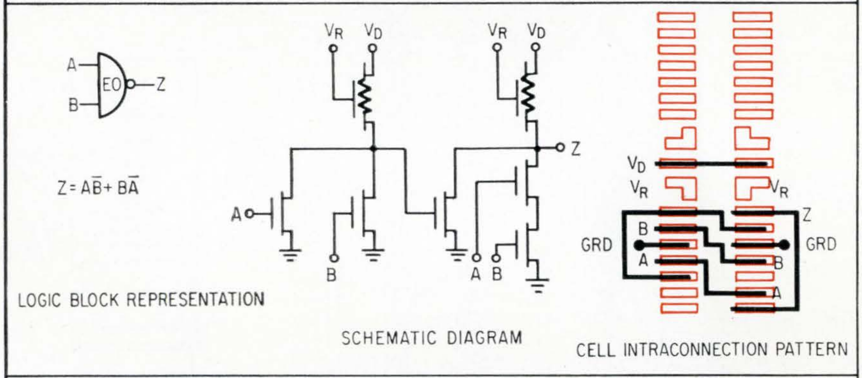
Three-input NAND gate (four per cell).



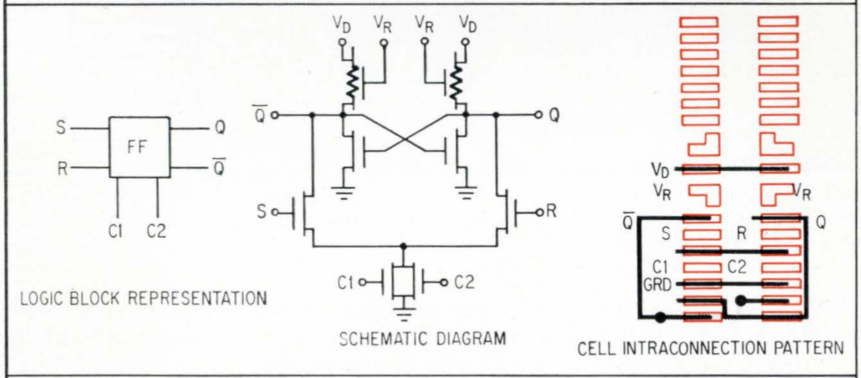
Three-input NOR gate (four per cell)



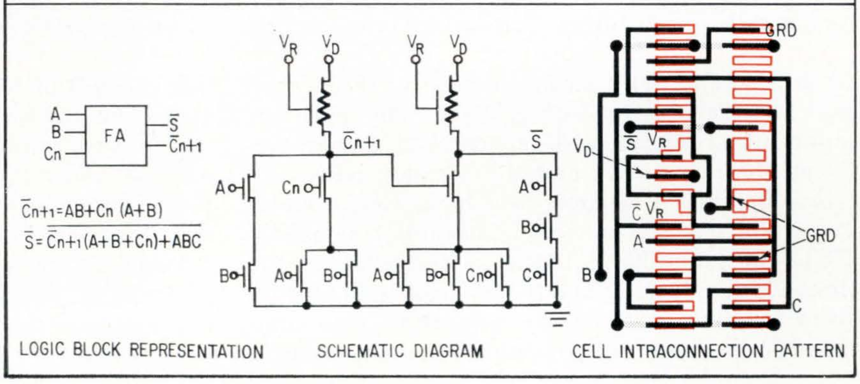
Exclusive OR gate (two per cell).



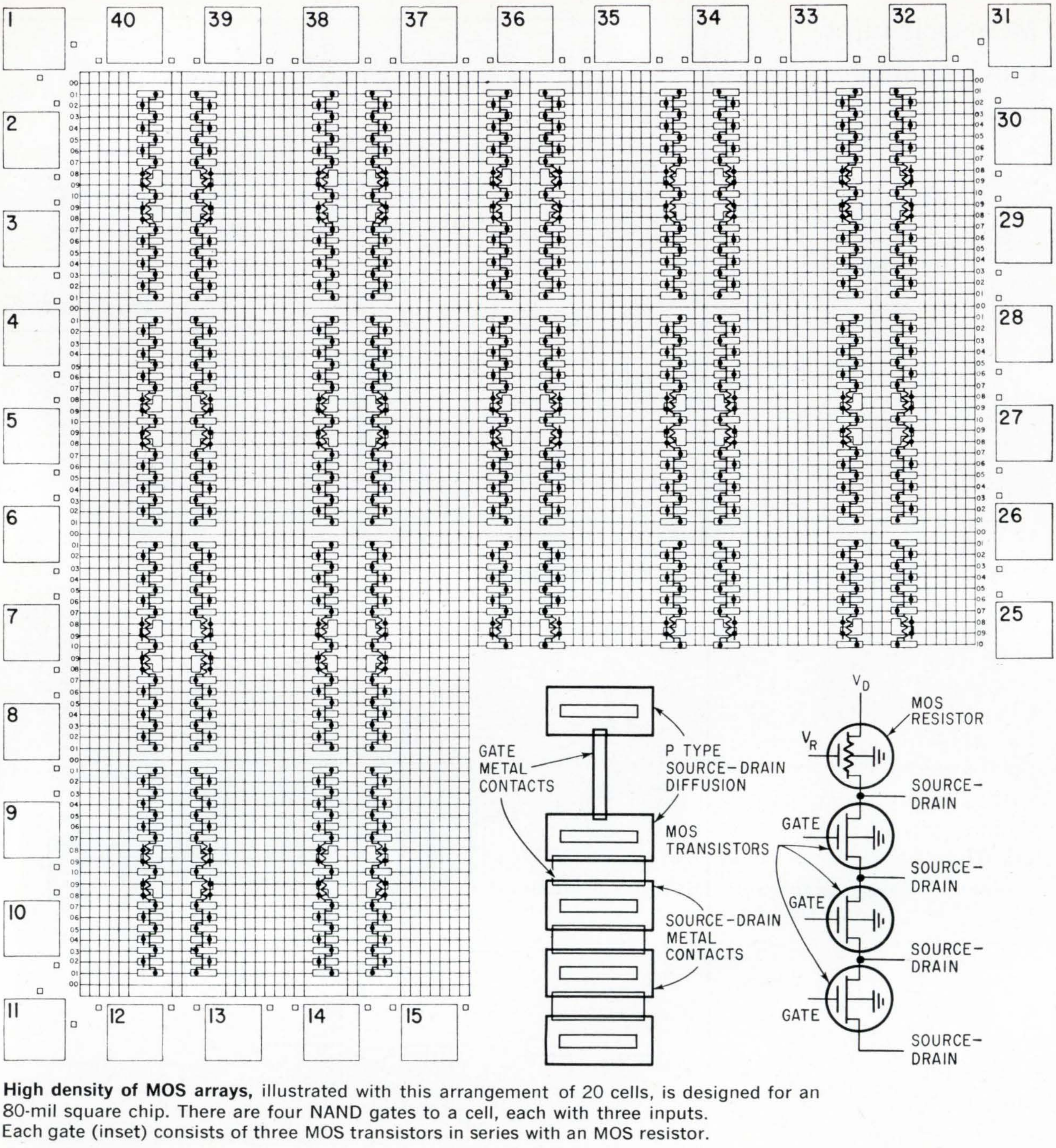
Dual clocked RS (reset-set) flip-flop.



Binary full adder requires an entire cell.



KEY:
DEVICE METAL
CELL INTRACONNECTIONS:
FIRST LAYER
DIELECTRIC CUTS
SECOND LAYER



High density of MOS arrays, illustrated with this arrangement of 20 cells, is designed for an 80-mil square chip. There are four NAND gates to a cell, each with three inputs. Each gate (inset) consists of three MOS transistors in series with an MOS resistor.

4001 array, composed of 20 cells arranged in a 5 by 4 pattern. Each cell contains four-three input NAND gates consisting of three series MOS transistors and a MOS resistor. The array provides the equivalent of 80 three-input gates. The chip size is 80 mils square, with an active area of 60 by 62.5 mils. Provision is made for 40 bonding pads for input-output signals and power. The margin between the active area and the bonding pads contains 40 diffused resistors which may be used as over-voltage protection on input-output signals.

The basic building block of the 4001 is the three-input MOS gate. The top element is an MOS resistor followed by three MOS transistors, with common source-drain regions connecting adjacent components. V_R (in the figure shown above) is the resistor control gate bias and V_D is the supply which controls the logic swing. The p-channel, enhancement mode MOS transistors exhibit an ON resistance between 2 and 4 kilohms and source-to-drain leakage currents of typically 1 nanoampere, in the OFF state. The turn-on voltage is in the -3v to -6v range.

The MOS resistors have a nominal value of 50 kilohms under normal biasing conditions. Typical propagation delay on the chip is 10 nanoseconds with V_D = -10 volts and V_R = -28 volts.

Wide design versatility with the 4001 can be achieved by proper cell intraconnection (page 163). Extensions of the concept to other applications are limited only by the designer's imagination.

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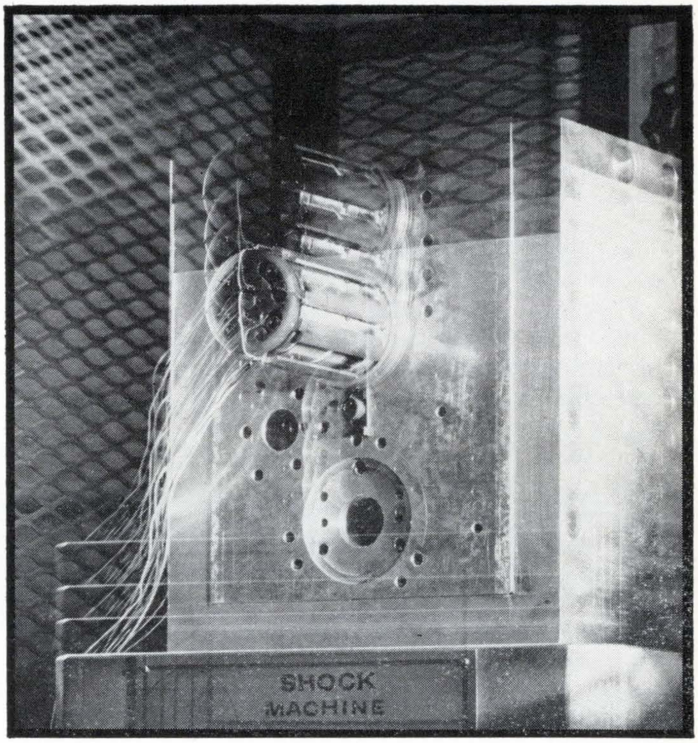

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Computer accelerates design and production of large arrays

Using logic entities called Polycells as building blocks, computers do design detailing while men do the creative work. The result: batch-fabricated integrated systems

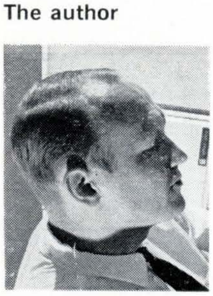
By Lester Hazlett,
Semiconductor Products Division
Motorola Inc., Phoenix, Ariz.

The complexity of arrangement and the density of components in a large-scale integration dictate that the designer have considerable help from a computer. In fact, it is doubtful if large-scale arrays of integrated electronics can be designed economically and efficiently without such help. One computer-aided design system, created especially to handle large-scale integration, uses logic entities automatically fetched from a computer memory and transformed into mask masters for circuit fabrication. Though the machine performs design detailing, the real creative work still is done by the engineer.

This technique is being developed at Motorola Inc., where it is emphasized because it promises earlier implementation and greater flexibility. Industrywide feeling that large-scale integration (LSI) should become a commercial reality within five years is shared by Motorola, based upon demonstrable results already achieved with the logic-entity idea.

The logic entity that is the basis of this approach may be a gate, a flip-flop, or a more complex function. Motorola's trademarked name for the logic entity is the Polycell. The principal advantage of the Polycell approach is that it allows cost reduction through design optimization combined with minimum response time to a new or revised design.

The author



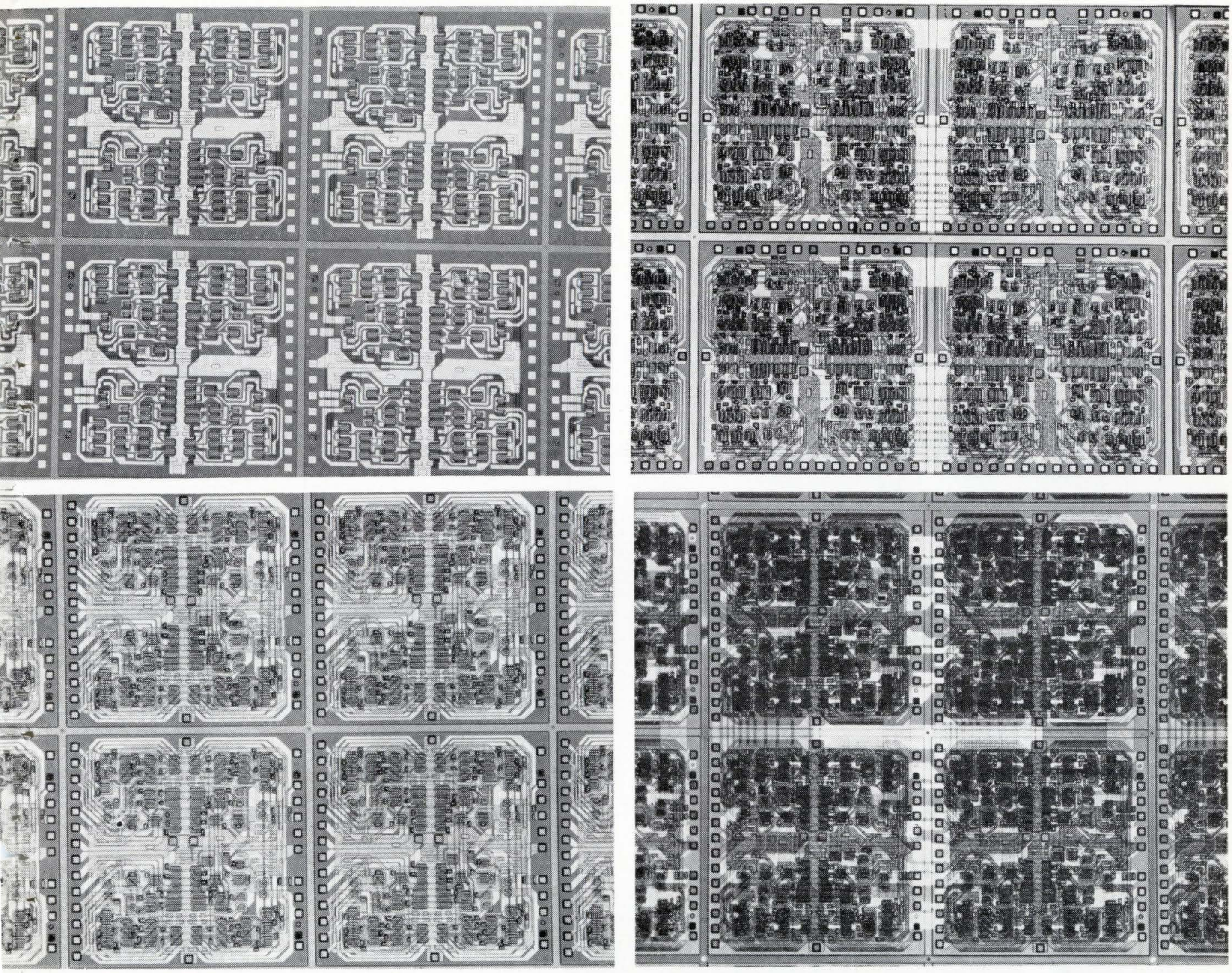
Lester Hazlett is manager of design automation at Motorola's semiconductor products division. His responsibilities include development of computer-aided design systems for IC's.

The Polycell approach

Data structures representing Polycells are stored in a computer library. For a particular array, the designer specifies to the computer the desired configuration of Polycells. The computer translates the configuration into instructions for an automatic drafting machine which prepares a complete set of mask masters for the required array.

This phase alone represents a considerable improvement over the methods in general use at this time. The machine, taking the place of the draftsmen in the tedious job of mask preparation, can perform this more rapidly and far more efficiently, with less chance for error. Moreover, the machine is able to produce more accurate artwork than the conventional coordinatograph, which can locate points to an accuracy of 0.001 inch. As a result, Polycell and array geometries can be smaller.

Final cost depends on both setup and production costs. Setup costs include product specification, design and engineering. Production costs include all the phases of material processing and testing. The Polycell approach uses simplified CAD procedures to achieve reasonably low setup costs and minimum production costs. Production cost is minimized if the design is optimized for batch fabrication. This is as essential for LSI as it has been for conventional IC's.



Steps in the fabrication of a 16-bit content-addressable memory array using Polycells. Each individual chip is a high-order Polycell made of smaller Polycells grouped together. At the upper left is part of the wafer showing four 4-bit arrays with the first layer of metalization. Below it, another layer of metal completes the highest-order Polycell. At the upper right the four arrays are connected in pairs by a third layer of metal. Finally a fourth layer of metal completes the 16-bit memory. The chip is 0.120 inch square and includes 524 diffused components.

Quick turnaround

Initial production parts and early samples of modified designs must be available quickly if LSI arrays are to be designed into large systems. The increasing complexity requires that some LSI arrays be altered when the total system is modified. What today is considered an excellent response time will be intolerable when individual chips make up complex subsystems or even entire systems.

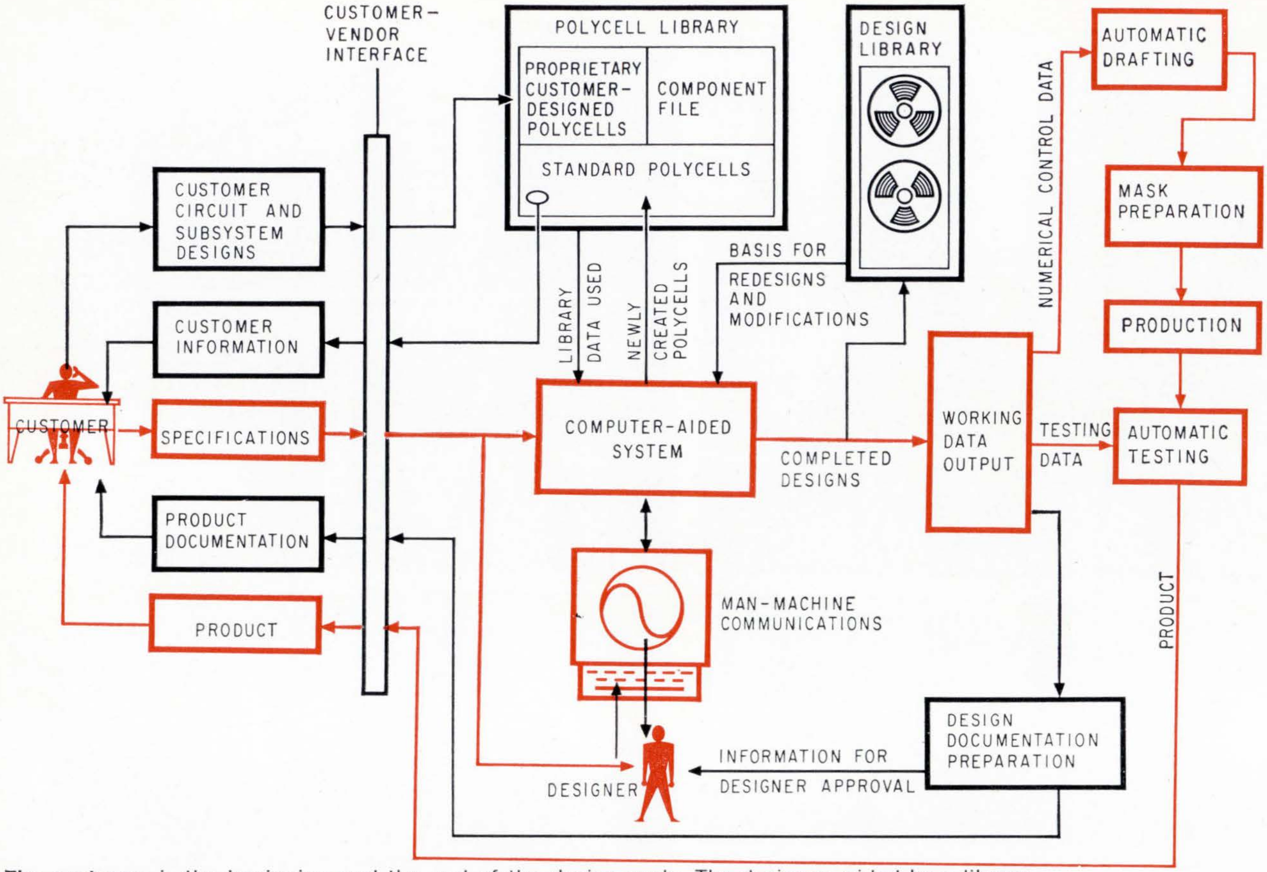
Vendor response time depends primarily on four factors:

- Communication of the product specification.
- Design, or design modification.
- Material processing.
- Product testing.

To standardize, simplify and expedite product specification requires a mutually well-defined selection of Polycells. The definitions can be in the form of standard specification sheets, like integrated circuits, or in the form of logic diagrams for more complex functions. From these definitions, any LSI array can be simply and clearly specified as a logically interconnected set of Polycells.

The CAD system on page 168 mechanizes all noncreative and repetitive design functions, while the designer controls the design procedure creatively. Such a system can be implemented in stages, allowing for early achievement of significant utility and ultimate accomplishment of full objectives.

A useful CAD system includes a computer, peripheral devices and automatic drafting equipment properly programed to allow man-machine interaction in the design of integrated semiconductor systems.



The customer is the beginning and the end of the design cycle. The designer, aided by a library of Polycells and prior designs stored in a computer memory, tries to meet the customer's specifications. The customer approves the final design before it goes into production.

The starting point of the Polycell approach to computer-aided LSI design, as in any other custom design project, is the customer. His prime inputs are the specifications for the final array. In many cases the customer will add his proprietary or preferred designs for some circuits and subsystems.

The designer works with the customer's specifications for the final system, using the CAD system. Once he analyzes the requirements and the special tools available, including the customer's proprietary Polycells, the CAD phase begins. Seated at the display console, the designer requests the desired Polycells and positions their images on the display. With a light pen and the keyboard the designer shifts or rotates Polycells. When he is satisfied with the arrangement, he switches his attention to the design of the metal interconnections between Polycells. The computer applies various algorithms to establish most of the routing. The designer can interrupt the machine if its solution becomes cumbersome and complete the routing manually.

Next the designer orders the computer to prepare design documentation and to store the design in the design library. He then carefully analyzes the documentation to guarantee that all requirements have been met and that the design is optimum.

If he is not fully satisfied, he returns to the console and calls up the complete design. He makes the required changes just as in the original design. He can insert new Polycells, remove old ones, shift the Polycells around, and revise interconnections. The computer prepares new documentation and the revised design is filed.

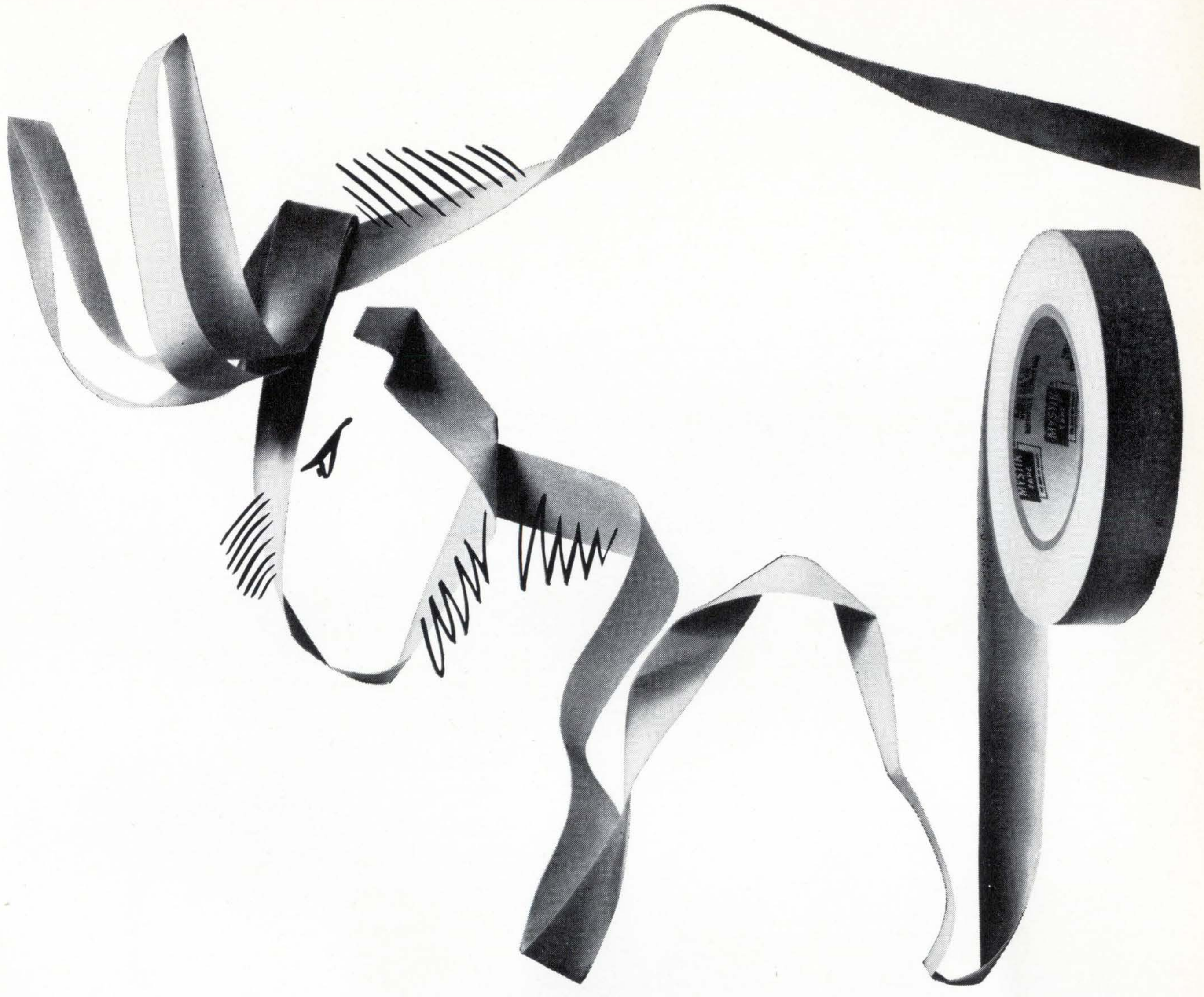
The optimization proceeds until the designer is content. Then the final documentation is submitted. The customer may then request further revisions until agreement is reached.

Now it can be built

When the design has been approved, the final version is once again called from the library. This time, the system generates numerical control data for the automatic drafting machine. These instructions specify the exact size, shape and location of each component element and for all the metalization. The drafting machine draws mask masters, from which a set of masks is prepared for the actual manufacture of the integrated system.

Though the Polycell approach to large-scale integration has not yet been proven in its entirety, it is close to implementation. Computer programs have been developed at Motorola and various phases of the operating sequences have been checked out successfully.

The progression from current technology to LSI will not be instantaneous, but a logical progression of circuits of ever-increasing complexity can be expected with correspondingly decreasing costs.



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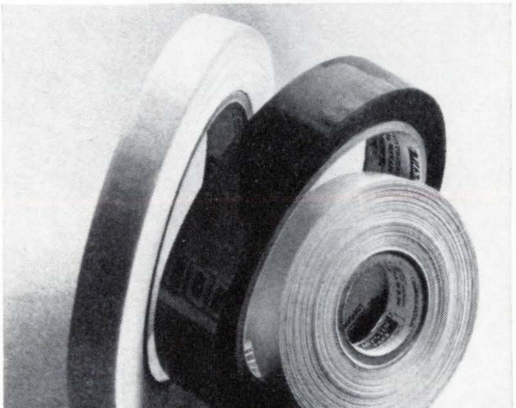

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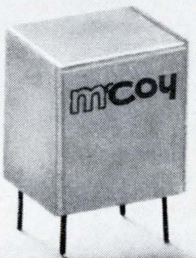

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Silicon-on-sapphire approach affords freedom and flexibility

Isolation provided by etched islands allows the mixing of different devices on a single microcircuit substrate

By Arnold Miller

Autonetics Division, North American Aviation Inc., Anaheim, Calif.

The growing complexity of conventional integrated-circuit arrays is magnifying the importance of three familiar restrictions: the parasitic capacitances of the back-biased p-n isolation junctions, the limits on mixing semiconductor devices and the difficulties of using resistive films on a silicon wafer. The silicon-on-sapphire (sos) approach, however, frees the designer from constraints and offers him the flexibility he once enjoyed with discrete-device systems.

This method, in which silicon film is deposited on the insulating sapphire substrate by heteroepitaxial techniques, affords complete isolation of semiconductor devices, allows the designer to use the devices best suited for each function, and permits the combination of precision resistive films or capacitive elements with monolithic devices on the same substrate.

After a single-crystal silicon film is grown on a single-crystal sapphire substrate, active-element locations are isolated by etching away the intervening silicon to form an array of silicon islands. The isolation thus achieved is limited only by the conductivity of the insulating substrate. The devices are then fabricated by the usual masking, oxidation and diffusion techniques and the interconnections, crossovers and precision passive components are added by vacuum deposition. The active elements formed in this way are in intimate contact with the insulating substrate and thus have thermal characteristics that allow them to operate at higher power levels than ordinarily possible with conventional integrated circuits.

Diode matrixes, metal-oxide-semiconductor complementary arrays, hybrid networks and bipolar structures all can be fabricated on a single sapphire substrate. A conservative estimate of the capabilities of present-day photolithographic methods is about 10,000 interconnected thin-film devices per square inch. It can be shown that, on a 10-mil-thick substrate, an sos 30-bit, 8,000-word memory (about 250,000 bits) with accompanying electronics would occupy less than two cubic inches of volume.

Diode structures

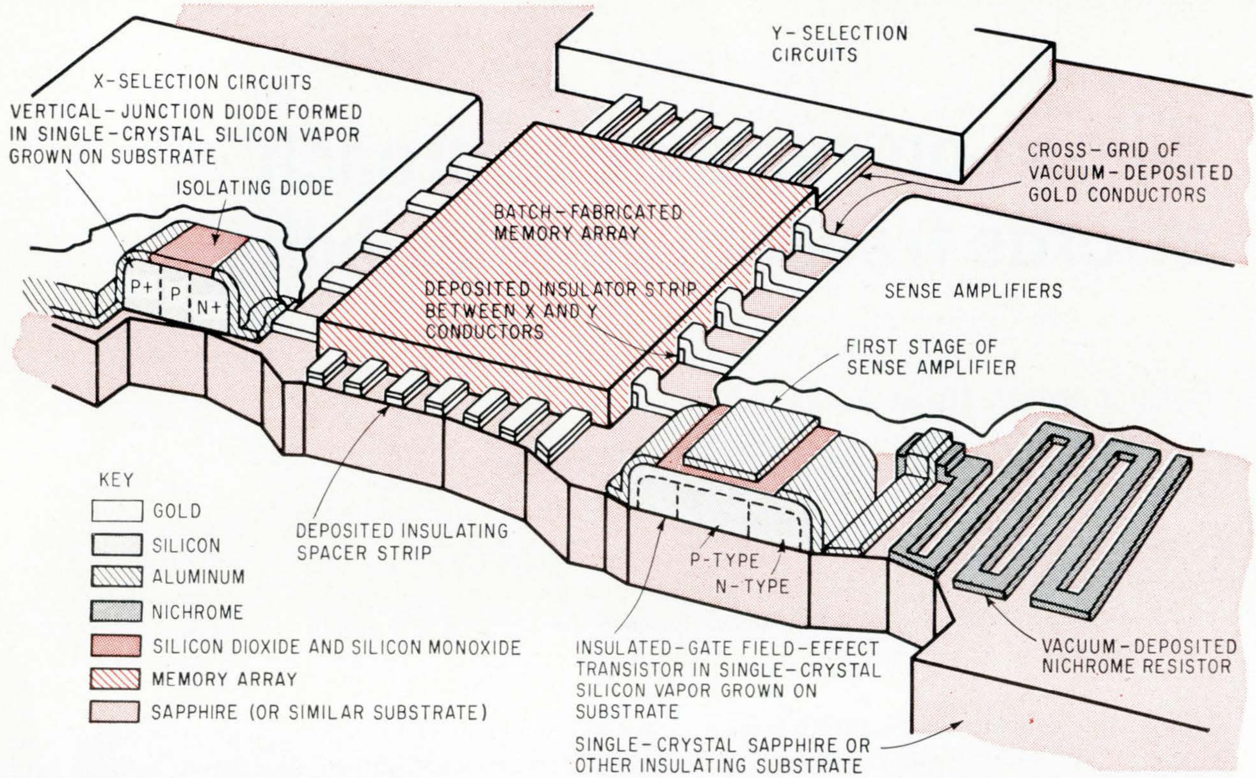
The sos film structure allows us to achieve small junction areas in the semiconductor devices. In the vertical-junction geometry produced by successive, side-by-side diffusions of p and n impurities, the junction area is simply the product of film thickness and silicon-island width. A 2-mil-wide structure in a 0.5-micron film, for example, produces a junction area of about 25 square microns that can give a junction capacitance of less than 0.005 picofarad. Without benefit of gold doping, vertical-junction diodes exhibit storage times of less than 1 nanosecond when switching from 3 milliamperes forward to 2 volts reverse, a property that suggests their use as step-recovery diodes in microwave harmonic generators.

On a single wafer, diode yield is about 99%, rectification ratios are greater than 10^5, and the variation in electrical characteristics can be held to less than $\pm 15\%$ across the wafer.

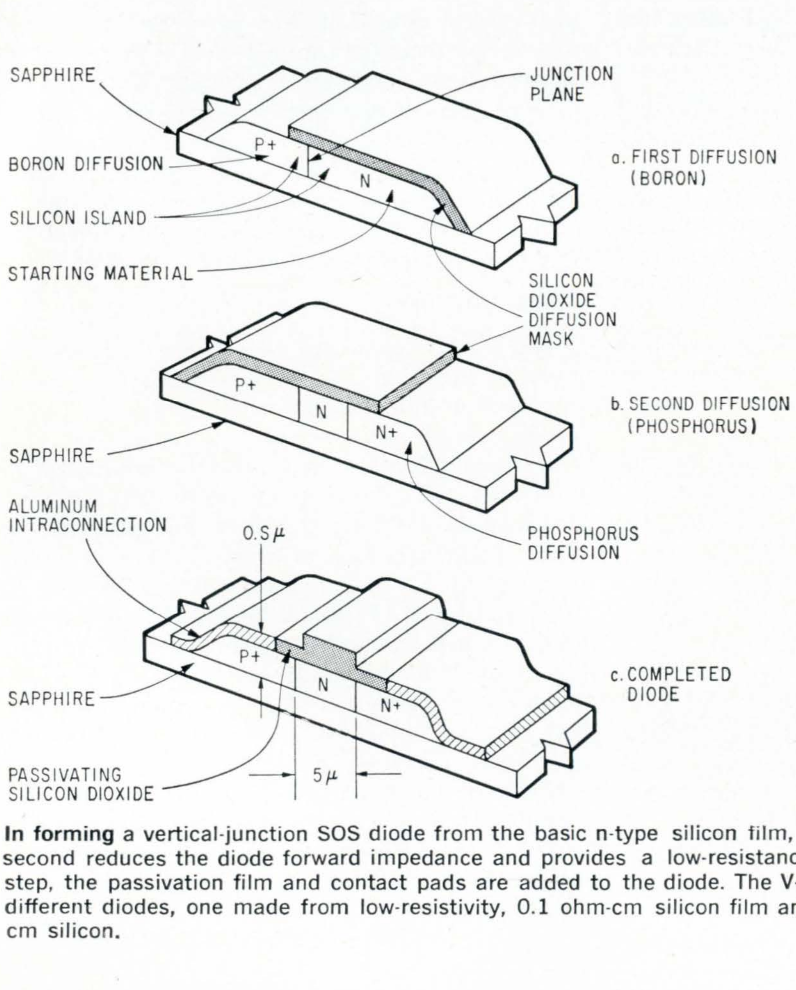
A diode read-only memory array can be used to

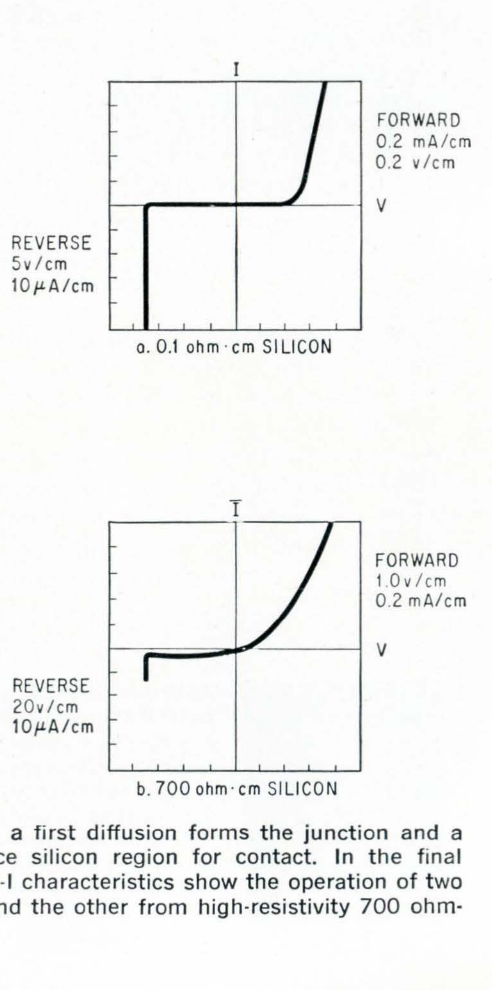
The author

Arnold Miller, director of Autonetics' central microelectronics laboratory, has spent 14 years in industrial research on surface chemistry, the physics of solids and photochemical reactions. He is a member of IEEE's Professional Committee on Integrated Circuits.



Isolation afforded by the silicon-on-sapphire approach allows the mixing of a variety of devices on the same substrate. The vertical-junction devices have small junction areas with low junction capacitances, which add to their capability at high frequencies.





In forming a vertical-junction SOS diode from the basic n-type silicon film, a first diffusion forms the junction and a second reduces the diode forward impedance and provides a low-resistance silicon region for contact. In the final step, the passivation film and contact pads are added to the diode. The V-I characteristics show the operation of two different diodes, one made from low-resistivity, 0.1 ohm-cm silicon film and the other from high-resistivity 700 ohm-cm silicon.

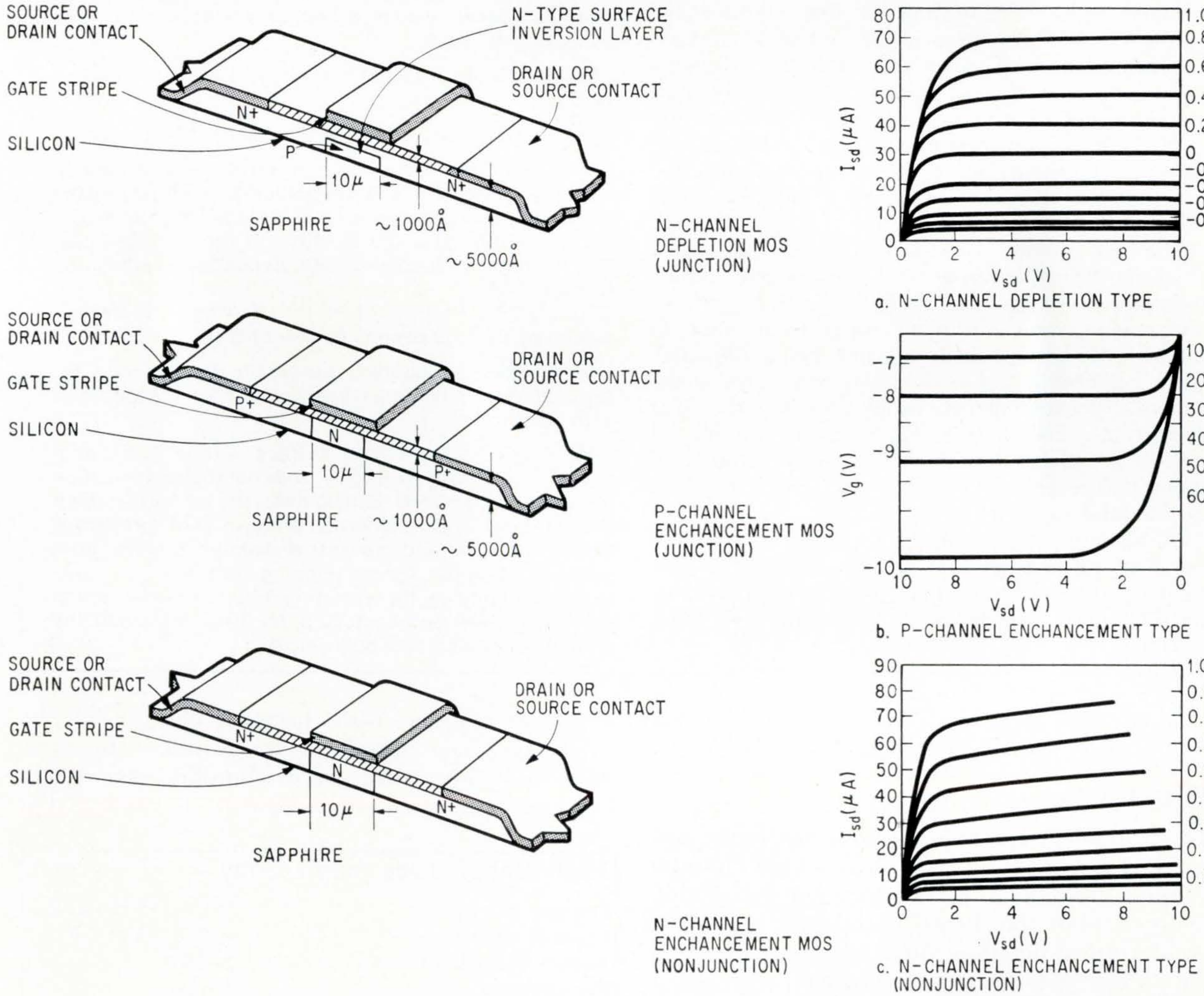
show the advantages of the sos approach. The memory not only demonstrates the capabilities of sos, but shows the two interconnection schemes that can be used.

A fixed-memory diode array uses prewired diodes to store information and provide address selection. Though hardly new, such diode stores haven't been used often because of the cost of discrete diodes, the limitations imposed by leakage paths, capacitance restrictions and the advances made in other types of memories. The availability of sos, however, refocuses attention on diode stores.

A 26-by-26 diode matrix structure on a 0.75-inch sapphire wafer was made as a prototype.[1] The 676 thin-film silicon islands located in the center ¼- x ¼-in.-square of the substrate were fabricated into the appropriate 2-mil by 5-mil diodes, arranged on 10-mil centers. Gold lines, 2 mils wide, were deposited in a parallel array; contacting the end of each diode, they formed the column lines of the matrix. Wide silicon monoxide layers overlaid the column lines for insulation and orthogonal sets of gold conductors were deposited to form the row lines. The final step was the appropriate connection of individual diodes to the column lines with a gold link.

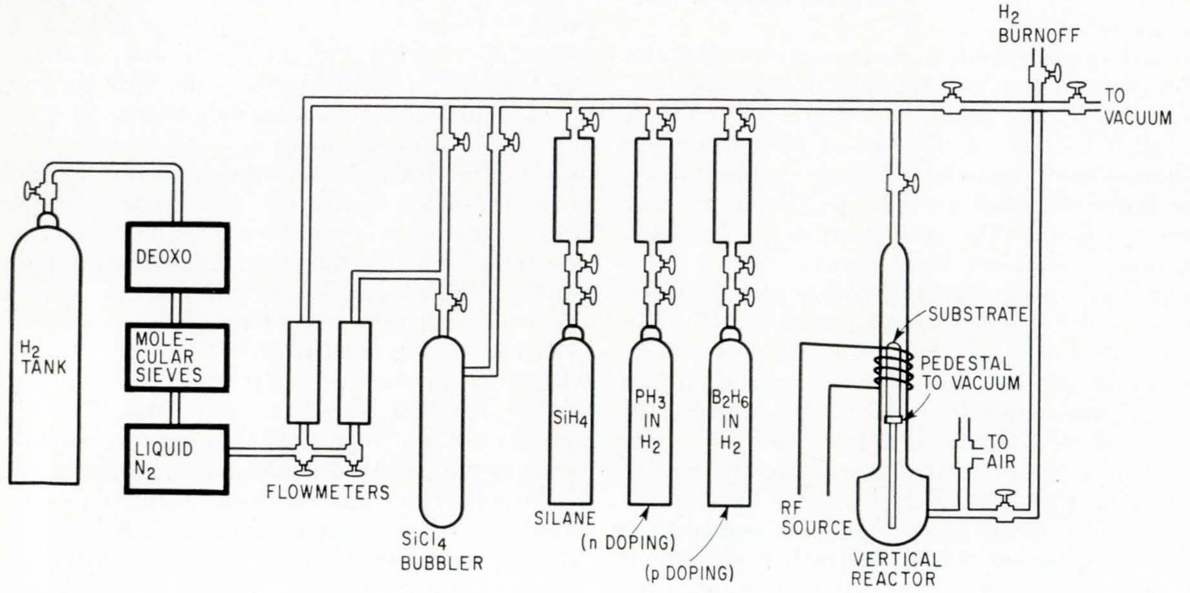
Early prototype structures exhibited rectification ratios in excess of 3 x 10^5 and read-in and read-out capacitances from the interconnection matrix of less than 1.5 pf. Yields were in the 99% range for an appropriately interconnected system[2] at a density of 10^4 bits per square in.

After the initial demonstration of the feasibility of the 676-diode matrix unit, a more complex high-density matrix was considered.[2] The second unit was built on a 1-in.-diameter, 20-mil-thick sapphire wafer, and consisted of a 96-column by 70-row array with a double redundant diode pair at each intersection. The matrix itself occupies 0.25 in.[2], with final interconnection to the drive and sense circuits handled by a fan-out pattern. The components are interconnected through low-resistance, n-degenerate silicon islands at the crossover point. In building this unit, a thick silicon dioxide insulating layer was formed over the exposed silicon islands, and contact points were exposed by etching. An orthogonal array of conductors was then deposited so that the column lines contacted the



Three types of MOS field effect transistors have been made in the SOS structure. The amplification factors for the devices are typically in the 50-to-300 range. The fourth possible device, the p-channel depletion model FET, hasn't been successfully made because of instabilities related to charges in the oxide layer, a problem common to conventional MOS structures.

Heteroepitaxy



The successful growth of a single-crystal film of one substance upon another largely depends on the crystallographic relationships at the interface and on the physical condition of the substrate surface. The substrate itself must first of all be a single-crystal material free of surface grain boundaries, scratches and impurities. Its surface must be prepared carefully by multiple lapping, polishing and ultrasonic cleaning before the substrate is inserted into the reactor, and it must get a final gas-phase polishing inside the reactor.

The film quality is also related to the source of silicon. Films deposited with silicon tetrachloride are usually of medium- to high-resistivity p-type. With silane, some variations occur from batch to batch, with both p and n types being obtained. Silane has been found to yield films with fewer dislocations, dislocation density usually being on the order of $10^8/cm^2$. The dislocations probably are related both to the dislocation density of the substrate and to the differences in expansion coefficients between the film and the substrate.

During processing, the film quality is affected by the substrate temperature, the gas composition and the flow rate, although satisfactory silicon films have been obtained over a fairly wide range of these variables.

Steps in growing a silicon film on a sapphire substrate

1. Place the sapphire wafer in the reactor on an alumina spacer resting on either a silicon or carbon rf-heating susceptor.

2. Polish the sapphire surface at 1,450° C with HCl or SF_6.

3. Pretreat the surface with H_2 at 1,250° C.

4. Lower the temperature to 1,150° C and deposit silicon with either silicon tetrachloride ($SiCl_4$) or silane (SiH_4) at a concentration of 0.3 mole percent in H_2:

Using $SiCl_4$: pass the H_2 through the $SiCl_4$ bubbler. The hydrogen reduction of $SiCl_4$ deposits the silicon on the sapphire.

Using SiH_4: feed the silane into flowing H_2 to deposit silicon by thermal decomposition of SiH_4.

5. Bypass the bubbler, purge the reactor with H_2, turn off the r-f heating supply and cool the pedestal with flowing H_2.

6. Passivate the silicon surface with a 1,000-angstrom oxide layer and give thermal homogenization treatment in an inert atmosphere (H_2 or He) at high temperature. This maintains uniform film properties across the wafer and prevents aluminum transfer from sapphire to silicon (an autodoping process).

The mobility in the resulting film, because of imperfections, will be about 20% to 30% less than the mobility of comparable bulk silicon.

beveled edges of the islands under the oxide, while the row lines crossed over the insulated regions.

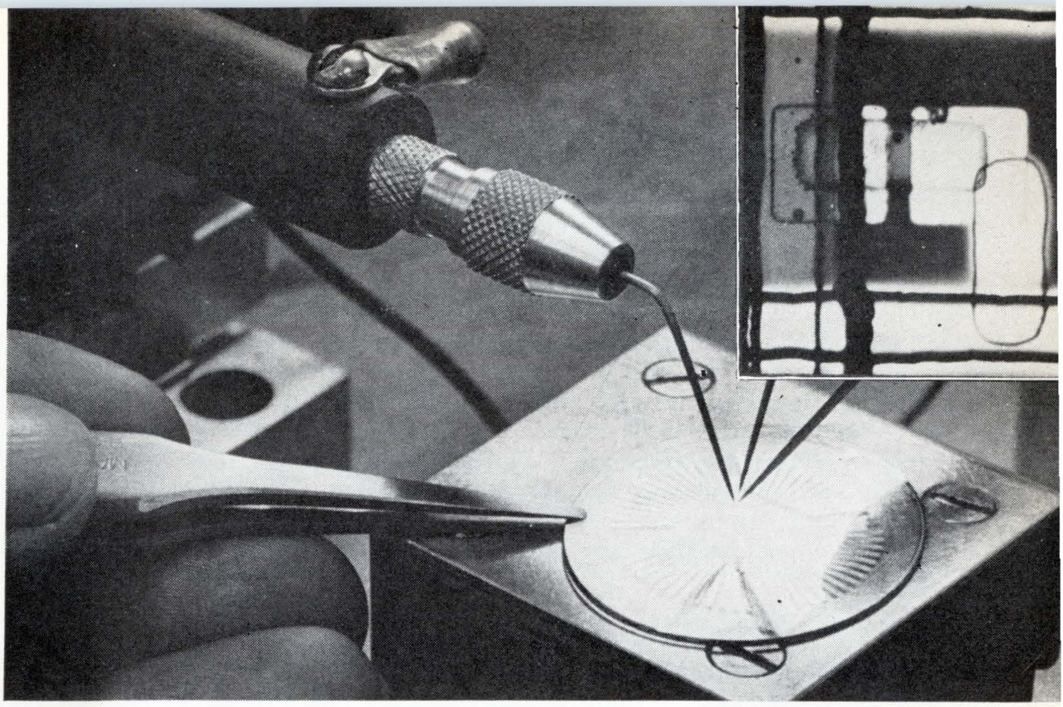
MOS structures

Mos field-effect transistors of various types and geometries can be fabricated in sos form through techniques developed for vertical-junction diode structures.[3] After the device islands are formed, a series of vertical-junction diffusions are made. The silicon-dioxide gate insulation is formed by masked vacuum evaporation, and the structure is completed by vacuum-deposited aluminum source, drain, gate and interconnection stripes.

Useful p-channel depletion devices haven't yet been successfully made because charges in the oxide layer have introduced instabilities. However, with the unique structure of thin-film sos we can build a nonjunction enhancement-type device that

High-density diode matrix array

Forward current	0.1 to 0.5 ma at 2 v
Leakage current	$<$ 100 na at 5 v
Voltage breakdown	$>$ 15 v
Storage time	1 nsec
Junction capacitance	0.005 pf/diode
Row-line capacitance	3.4 pf
Reverse-to-forward resistance ratio	$10^7 - 10^8$
Wafer electrical variation	± 15%



A 676-diode memory array is spot checked for forward current, voltage and leakage current before the attachment of leads and encapsulation. The inset shows one method of connecting devices to the gold interconnection stripes. A gold link is added from the conductor to the device pad. A silicon monoxide film insulates the row lines from the column lines.

can't be made in bulk silicon. This structure is comparable to the polycrystalline, vacuum-deposited MOS field effect transistor, but with its single-crystal nature, it has enhanced characteristics and better stability.

The channel width of the device affects its transconductance and drain-resistance values. In the structures illustrated, the gate length is held at 2 mils. The amplification factor, which is relatively insensitive to the gate length, is typically in the 50-to-300 range.

Leakage measurements show values in the 10-to-100-picoampere range, depending on the device geometry. At 10 microamps, the threshold voltage is usually 1.5 to 2 v when oxide thicknesses are maintained at 1,000 angstroms. For a 10-mil channel width, gate capacitance is approximately 1.5 pf, with source-to-drain breakdown voltages of about 25 v. For a 20-mil channel width, switching-time measurements indicate typical rise and fall times of 10 nsec.

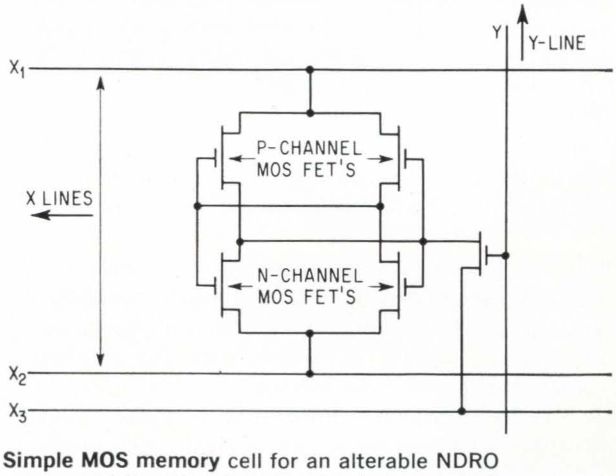
The thin-film rendering of MOS field-effect transistors in an SOS system provides a number of additional advantages in complex circuit designs requiring large numbers of devices. For maximum speed, stray capacitance must be reduced to a minimum, and this is a severe problem where large numbers of devices must be interconnected. With sapphire as an insulating substrate, however, the only capacitance contributions are at the crossover points and in the devices themselves; there is no capacitance to the substrate. Thus, MOS drain-to-source capacitance can be neglected, although the gate-to-source and gate-to-drain capacitance contributions are still significant.

The SOS approach permits the ready fabrication of both p- and n-channel MOS field effect devices on the same substrate. This ability to design with MOS devices of both types results in circuit simplification and a reduced power requirement.

Resistors and capacitors also may be added on the same sapphire substrate. The silicon films themselves may be used as resistors; at film thicknesses of 0.5 micron, with 10 ohm-cm resistivity silicon, sheet resistors of 200 kilohms per square are attainable. Precision nichrome thin-film resistors can be deposited with conventional masked evaporation techniques. The MOS structures may be used as capacitors where required.

Low-power flip-flops using complementary p- and n-channel, enhancement-mode, junction-type MOS field effect transistors have been fabricated in SOS form in an experimental memory-array configuration. A circuit structure of this type would yield significantly reduced power consumption and improved frequency characteristics without requiring the use of multiphase clocking.

A simple memory cell, for example, consists of two inverter circuits connected back-to-back to form a flip-flop, plus a fifth MOS field effect transistor for cell readout. The basic flip-flop occupies an area of 225 sq. mils. Low-level leakage measurements give values in the nanoampere range on the complementary array. The p-channel devices exhibit thresholds of 4 v at 10 μa, while the n-channel



Simple MOS memory cell for an alterable NDRO array consists of two inverter circuits connected back-to-back to form a flip-flop, with a fifth MOS transistor added for cell readout. The basic flip-flop occupies 225 square mils.

devices have thresholds of less than 2 v.

Another example of sos design is provided by a nondestructive readout (NDRO) scratch-pad memory plane consisting of 24 columns and 22 rows, plus peripheral circuits. Each individual cell in the array is a circuit composed of six p-channel and six n-channel MOS transistors and five diodes; the heart of each circuit is a four-transistor, complementary bistable flip-flop. At the top of each column, a column-selection circuit is integrated into the array; at the bottom of each column, a complementary inverter permits the "folding" of columns without an increase in capacitance loading. Along the sides of the array, an extensive crossover matrix and read/write contact pads are integrated into the storage plane.

Bipolar structures

To date, sos bipolar structures showing current gain have been successfully built in conventional planar npn form, as well as in vertical-junction npn and pnp forms, but much more work is necessary.[4,5]

Using sos films of thicknesses on the order of 5 microns, a series of conventional planar npn devices has been fabricated. Since the silicon films currently under investigation have dislocation densities of approximately $1 \times 10^8/cm^2$, the work centered on structures of small device areas. No device structure of a larger size showed transistor action, and the failure in all cases was traced to collector-emitter shorting.

In a planar npn transistor fabricated from 2 ohm-cm material, an h_{FE} of only 2 was observed, but current gain was achieved. Going from a 2 ohm-cm film to a 0.1 ohm-cm film (on Czochralski sapphire) leads to a deeper base penetration with a correspondingly wider base region and results in h_{FE} values of 20.

Interesting results of perhaps greater ultimate promise have been achieved with small-area, vertical-junction bipolar transistors. In an experimental homogeneous-base pnp bipolar device made in silicon films on the order of 0.5 microns in thickness, the emitter-base area is 92 square microns and collector-base area is 135 square microns. The h_{FE} is low, with a sharp decrease occurring when only a few microamps collector current is attained. At 40 na, the h_{FE} observed is 19.

The homogeneous-base transistor has a limited frequency response due to the absence of drift fields in the base region. However, the low device capacitance, in combination with thin-film, high-value silicon resistors, could well result in integrated amplifiers capable of operating at frequencies of at least 10 megahertz. The diffusion process control would be considerably less critical for the homogeneous-base bipolar transistor than for the corresponding diffused-base device.

A vertical-junction, diffused-base npn bipolar transistor that was built differs from the corresponding homogeneous-base structure in processing sequence and geometry. The collector-base junction area of this device is 30 square microns and the emitter-base junction area is 6 square microns. This structure is similar to the homogeneous-base device in that it shows an h_{FE} peak at low current. A current gain of about 2 is obtained at the 10-na collector current level.

This device has the low capacitance of the vertical-junction, graded-base bipolar transistor, and can be integrated into microstrip or stripline circuits with sapphire as the dielectric material and a ground plane on the back side. This kind of device could thus be used to advantage in microwave IC's operating in X band. Its possible application in low-power subnanosecond digital IC's and integrated-circuit arrays is also apparent.

The small-area vertical-junction devices with collector-base and emitter-base junction areas of 10 and 5 square microns respectively give rise to associated capacitances in the 0.001-pf regions, an order of magnitude smaller than can currently be achieved in bulk with conventional techniques.

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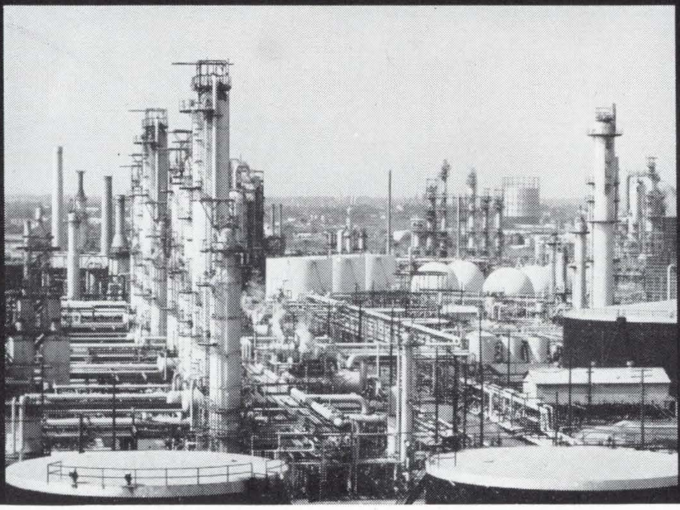

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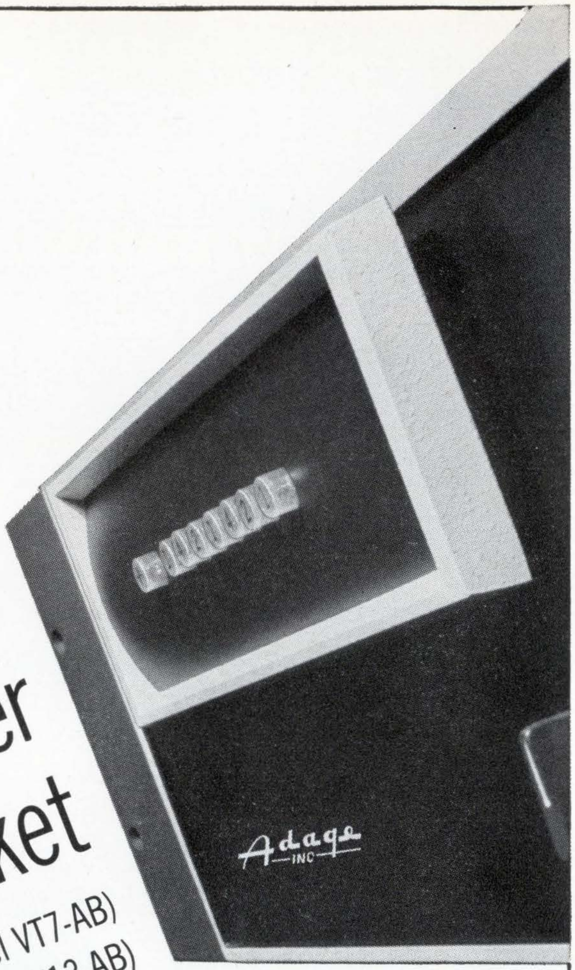

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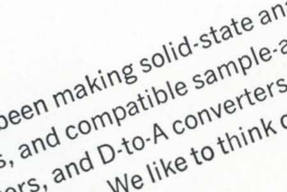

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Large-scale integration

Slow, but small, may win the race

MOS integrated circuits, with hundreds of transistors on a chip, got a head start in the LSI sweepstakes, but lag behind bipolar IC's in speed; better processes and faster designs help close the gap

By Earl Thomas and J. David Callan

General Instrument Corp., Newark, N.J.

Large-scale integration and metal-oxide-semiconductors circuits are old friends. Mos integrated circuits with nearly 1,000 devices were being produced before bipolar LSI arrays had emerged from the laboratory.[1] Their potential of providing complete digital subsystems on a single chip was recognized even before the term LSI was coined.

In view of MOS's head start and clear superiority in small size, why is there a controversy between MOS and bipolar LSI approaches? The main drawback of MOS circuits hasn't been cost, because they cost less to make than bipolar IC's. The problems have been the relatively slow speed of MOS circuits, compared with bipolar circuits, and the need to design systems that could quickly process data despite low internal clock speeds.

A year ago, the maximum clock frequency was normally about 2 megahertz. That has just recently been more than doubled and there is no doubt that it will be doubled again soon. Clock rates can be expected to continue to climb, to about 15 Mhz in the future.

This progress in MOS design and processing is typified by a 64-bit shift register that the Microelectronics division of General Instrument Corp. is now producing and delivering as a custom-made IC. It has an operating frequency of 5 megahertz. The shift register is a dynamic one, with all the logic circuitry needed for loading and recirculating data on the chip. Each internal bit occupies only 11 square mils of chip area and the whole circuit, including bonding pads has an area of 3,364 mils.

The increase in speed and the smaller size of the elements of the IC is largely due to an improved MOS process, which General Instrument calls MTOS, for metal-thick oxide-semiconductor. The oxide at metalization crossover points is made thick to reduce shorting through pinholes, while the oxide in gate areas is made thin to enable the device to work properly [Electronics, Jan. 23, 1966, p. 38]. This process has also significantly improved the yield of good IC's from each starting wafer of silicon.

The shift register is also a good example of how far MOS design has progressed in terms of controlling power dissipation and heat generation. At a frequency of 5 Mhz, the register dissipates 100 microwatts at each internal node. The data outputs are both true and inverted. Each output stage dissipates 14 milliwatts into a 7-picofarad load. Total dissipation of the register is about 80 milliwatts when each output has a load of 7 pf. Each register can drive another directly without the addition of external components. If the operating frequency is reduced, the power dissipation drops proportionately since power is dissipated only during the switching transient.

The major advantages of MOS over bipolar IC's

The authors

J. Earl Thomas joined the General Instrument Corp. in 1964 as a corporate new products manager and technical adviser to the president. Before that, he was director of research and engineering for Sylvania Electric Products Inc.

Since 1966, as manager of the digital computation section of General Instrument's Microelectronic division at Tarzana, Calif., J. David Callan has been responsible for the development of LSI circuit chips. He has a master's degree in engineering from the University of Southern California.

have been cited before, but are worth discussing again since the numbers continually change. In general, the advantages of MOS are:

- Higher yield because the process is simpler.
- Inherently high device impedances.
- More circuits can be put into a chip.
- Arrays are in production while bipolar large-scale IC's are still experimental.

In comparison with bipolar devices, MOS devices also have a number of circuit advantages. The bias voltage levels are simpler to supply and MOS devices can be used in place of high-value load resistances. The "tree building" and stacking of devices that made old-fashioned relay logic systems so easy to design can be accomplished in MOS. Four-phase MOS circuits allow stacks of 32 switches at frequencies of 5 Mhz. Two examples of tree-type MOS circuits are shift registers and differential digital amplifiers, which will be described later. To duplicate these functions with bipolar IC's would require more circuit elements and twice as many processing steps for each element.

Two sets of building blocks

On the system level, the trade offs between the two types of IC's are more complicated, because the advantages of each are intertwined.

For example, LSI requires that a computer be divided, or partitioned, into blocks of circuits that can be made together as a single chip. Designers of large general-purpose computers almost invariably turn to tailor-made IC's to optimize manufacturing cost and to allow the computer to perform a variety of computational problems in the shortest possible time. These designers strive to take advantage of the maximum speed capabilities of bipolar logic, when they use such IC's. This design fact has several consequences:

First, it will obviously be impossible to use standard LSI building blocks—at least until an entirely new philosophy of system design evolves that is based upon the use of functional blocks instead of unit logic circuits. In any case, simple partitioning of large computers inevitably leads to a greater number of input-output leads on each IC than the IC designer can easily provide.

Second, when LSI chips are tailored to a specific computer, the processing plant is locked into a short-run manufacturing situation. This makes design and setup costs difficult to amortize and militates against the yield advantages of long-run, repetitive processing.

The number of leads per unit length of chip edge, which governs the maximum number of leads per chip, can be reduced if the chip contains so many unit circuits that it represents a significant fraction of the computer. With planning, the bigger the function, the fewer the number of input and output signals needed. That kind of super-LSI is not yet practical and even if it were, the short-run cost and yield problems would be even more acute. An orderly transition from medium-scale integration to large-scale integration is needed.

On the other hand, if special-purpose computers can be made less costly, the economic advantage of the general-purpose machine will be reduced. When the computer designer thinks about using several special-purpose systems instead of one all-purpose system, he finds that he can make repetitive use of such building blocks as digital differential amplifiers and shift registers. Such classes of functional blocks are ideal for LSI applications because they are complete functions requiring only power input, information input and information output.

Now that he has solved his pin problem, the designer can consider the long-run production advantages. Shift registers, digital differential analyzers (DDA), analog to digital converters and similar functional blocks are useful in many types of data-processing systems, from airborne navigation receivers to process control computers. This makes possible wide use of the blocks by many customers, providing each customer's engineer is willing to change his design concepts to achieve low system costs.

Digital differential analyzer

An example of a building block is the General Instrument MEM 5021 DDA integrator. It consists of two chips. One is a 32- or 50-bit serial memory and the other contains all the logic that operates the memory. On the logic chip, which measures 86 by 72 mils, are 230 MOS transistors interconnected as about 65 gate functions.

A DDA integrator employs the following algorithm

$$Y_{n+1} = Y_n + \Delta Y$$

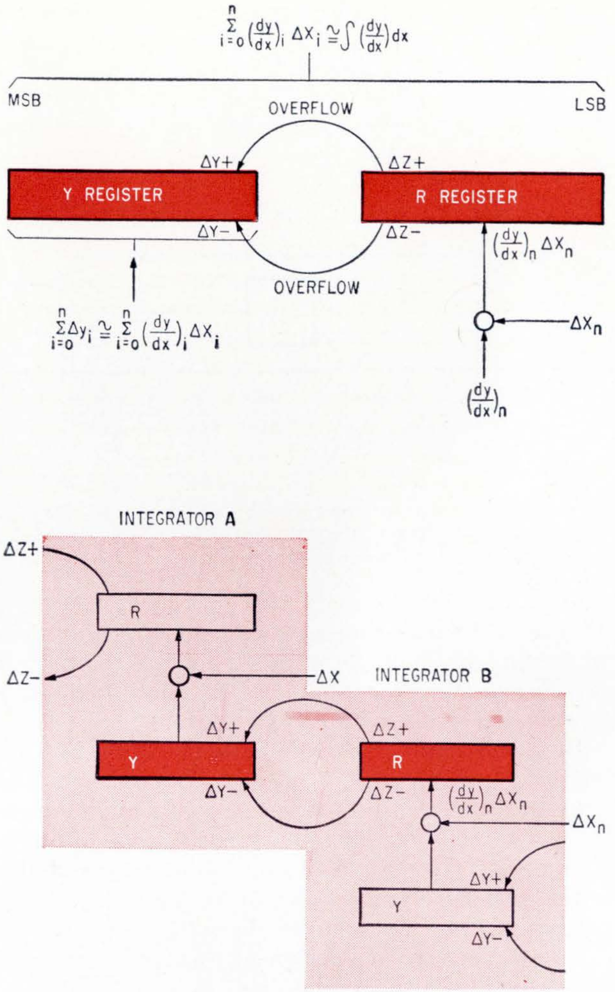
$$\text{where} \quad \Delta Y = \left(\frac{dy}{dx}\right)\Delta X$$

The ΔY and ΔX functions are discrete increments that take on values of $+2^{-n}$, zero and -2^{-n}. Therefore, the integration is a finite summation process

$$\int\left(\frac{dy}{dx}\right)dx \cong \sum\left(\frac{dy}{dx}\right)\Delta X$$

The integration requires two registers, one for the remainder (R) and one for the integral (Y), as in the upper part of the diagram on page 181. As the R register overflows or underflows into the Y register, the integral is rounded off and only the most significant part in the Y register is used. To conveniently use more than one integrator, the MOS registers and logic circuits can be paired as shown in the lower part of the diagram. Aside from improving the functional organization, this keeps the number of inputs and outputs to each block at a minimum.

Seven such integrators, arranged as on page 182 solve the differential equation for Bessel's functions. The over-all clock speed of such a computer would be rather low, about 500 khz; for a 10-bit number this represents a 50-khz integration rate so the equation is solved every 20 microseconds when the data flow is continuous. This is a very high over-all computing speed, probably 10 times faster than



Two registers perform the integration operation in a digital differential analyzer by the summation process given in the formula of the upper diagram. Rearrangement of the registers (lower diagram) in the MOS circuits allows stacking of the integrators to perform more complex functions. The registers in color are the same in both diagrams.

a general-purpose machine. A general-purpose computer would have to do many simpler operations to complete one integration.

Other integrator arrangements will solve trigonometric equations, control feedback, compute aircraft positions, or perform any function that can be expressed as a differential equation or a set of them.

High impedance

The inherently high impedance of MOS devices means that signal voltages in MOS circuits will be four to five times as high as in bipolar IC's. Therefore, the MOS circuit has greater immunity to noise and other unplanned transients in the voltage supply. The reduced likelihood of false operation is a boon to the engineer who might otherwise spend months debugging a computer designed with IC's sensitive to noise.

A second advantage of high impedance is that multilayer wiring can be avoided through the use of cross-under conduction paths diffused into the silicon substrate. The technique is used in bipolar circuits, too, but sparingly because the diffused connection introduces considerably higher series resistance than the metalized wiring. The resistive unbalances are difficult to compensate for in bipolar designs, but are of little consequence in MOS design, since the resistances are extremely high.

Speed versus clock rate

As the price paid for high impedance, the speed of MOS devices is lower than that of bipolar IC's. But systems can be built with MOS circuits that have a higher data processing rate than systems built with bipolar IC's, which is the important point.

Since a one-sided answer to the speed question can be misleading, a few statistics are in order first. General Instrument is marketing a 50-bit MOS shift register with a specified clock frequency of 1 Mhz. Some customers are running it at 2 Mhz. In contrast, an 8-bit bipolar shift register is available elsewhere (Texas Instruments Incorporated) that operates at 15 Mhz.

The GI chip size is 40 by 60 mils and the TI chip size is 130 by 60 mils. In development at General Instrument is a 256-bit shift register that would have a chip size of 70 by 80 mils and operate at a clock frequency of 8 Mhz. On a bits-per-second-per-unit-area of silicon basis, this indicates MOS is eight times as fast as bipolar. This is, of course, a numbers game that is strongly influenced by the fact that bipolar IC yield is presently to low to permit the commercial sale of shift registers longer than 8 bits.

There is no denying that bipolar clock rates are much higher. The clock rates appear to be converging, but the ultimate clock rate available with the two technologies is hard to forecast. One reason is that LSI is probably going to make it attractive to use more circuits to process a given amount of data, rather than push the data through a lesser number of circuits operating at the ultimate clock rate of the type of LSI used.

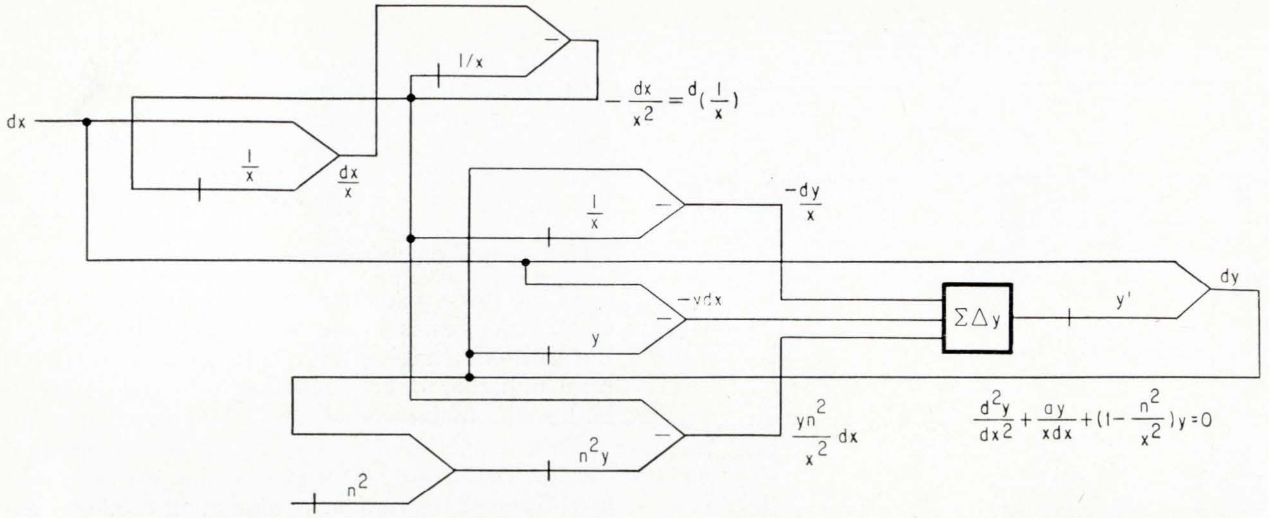
The clock rates of MOS circuits may never surpass those of bipolar IC's, but who cares? As soon as the designer familiarizes himself with special-purpose "wired-logic" systems like the integrator, he finds MOS logic is not limited by clock speed. A machine designed to solve a specific class of problem can solve it an order of magnitude faster than a general-purpose machine. Simply put, its operation isn't cluttered up by hardware it can't use on a particular task.

For example, it is believed that missile guidance calculations can be done with digital differential analyzers 100 times as rapidly as with the best existing general-purpose computers.

Another way of boosting speed is to provide each memory circuit with an arithmetic circuit—an associative computer—so arithmetic operations can be performed concurrently.

High yield, low cost

In production costs, bipolar cannot compete with



Bessel's equation, often used in circuit design, is solved by a combination of seven integrators. Other combinations of integrators solve navigation and control problems that can be expressed as differential equations.

MOS. The basic MOS process requires only one diffusion and four masking steps, while the bipolar process can require up to four diffusions and as many as 10 masking steps if multilayer wiring is used. Most bipolar LSI approaches involve multilayer wiring.

In addition, an MOS circuit's silicon substrate is homogeneous. Bipolar requires the growth of an epitaxial layer, probably preceded by a diffusion step. Because it is more complicated, the yield of the bipolar process is less.

An example of a specific processing disadvantage is that the epitaxial layer always has small defects. This further limits yield and makes it impossible to use chrome masks for oxide photoetching. These masks are economical because they last a long time, if not damaged, and they improve yield by improving consistency from one batch of circuits to another. The defects in the epitaxial layer puncture the thin film of chrome, allowing light to expose a spot of resist the next time the mask is used.

A pinhole in the oxide at that spot can cause a short from the metalization layer to the silicon substrate. The loss of a circuit is not too serious when the IC's are to be used individually, but several such shorts can play havoc with LSI approaches that depend upon fairly high yield of complex cells of circuits.

Even a fraction of a percent better yield is an important advantage in LSI production. The final yield of an LSI circuit consists of the product of many numbers—the number of processing steps and the number of devices. Since no process is perfect, each number is less than 1. For example, if device yield is improved from 0.99 to 0.995 (99% to 99.5%), the yield of LSI circuits with 500 devices will go from 0.7% to 8%, an improvement factor of 12.

Packing density

The number of circuits a user can afford is dependent on how many circuits can be put on a chip. This, too, is hard to forecast, since it depends upon processing and factors that have nothing to do with processing—for example, how much of the chip must be reserved for input and output leads?

In round numbers, the functional equivalent of 10 to 20 conventional bipolar transistors and diffused resistors can be made in MOS form today on 20 square mils of silicon substrate. The ultimate packing density depends upon how cleverly the wiring can be arranged and how small the wiring pattern can be.

Considering system design again, the true packing density of MOS can be even more dramatic. A transistor DDA, for example, is customarily used with an acoustic delay line, rather than a shift register, for the memory function. An MOS DDA requires only two chips.

Much of the apparent competition between bipolar and MOS approaches to LSI doesn't exist. Mos is in production and is winning a place in system design. When both are available, the system designer who weighs their pros and cons will find that they compete like beef and carrots. Each will win different fractions of the market as their relative prices change.

The system designer will have to make his choice at the outset because bipolar and MOS arrays are not interchangeable and will never be completely interchangeable. He'll have to choose one system design concept or another and follow it through. If bipolar arrays were sucessfully being produced now, the average engineer might give MOS short shrift. Actually, the shoe seems to be on the other foot for the present.

Reference

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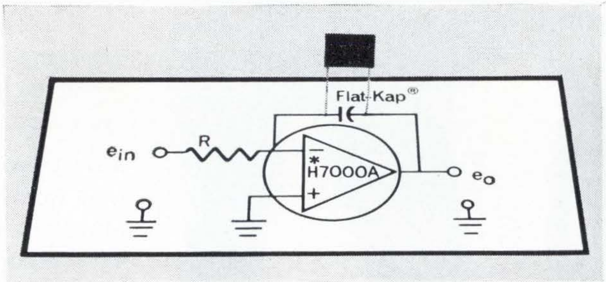

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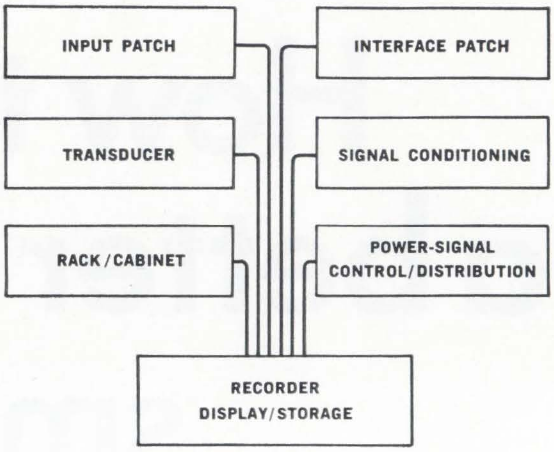

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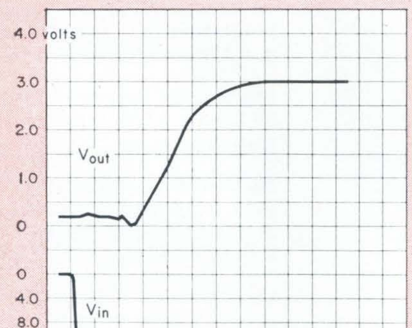

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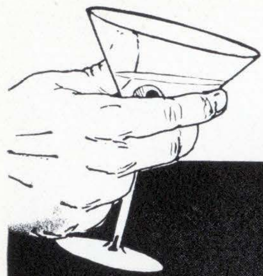

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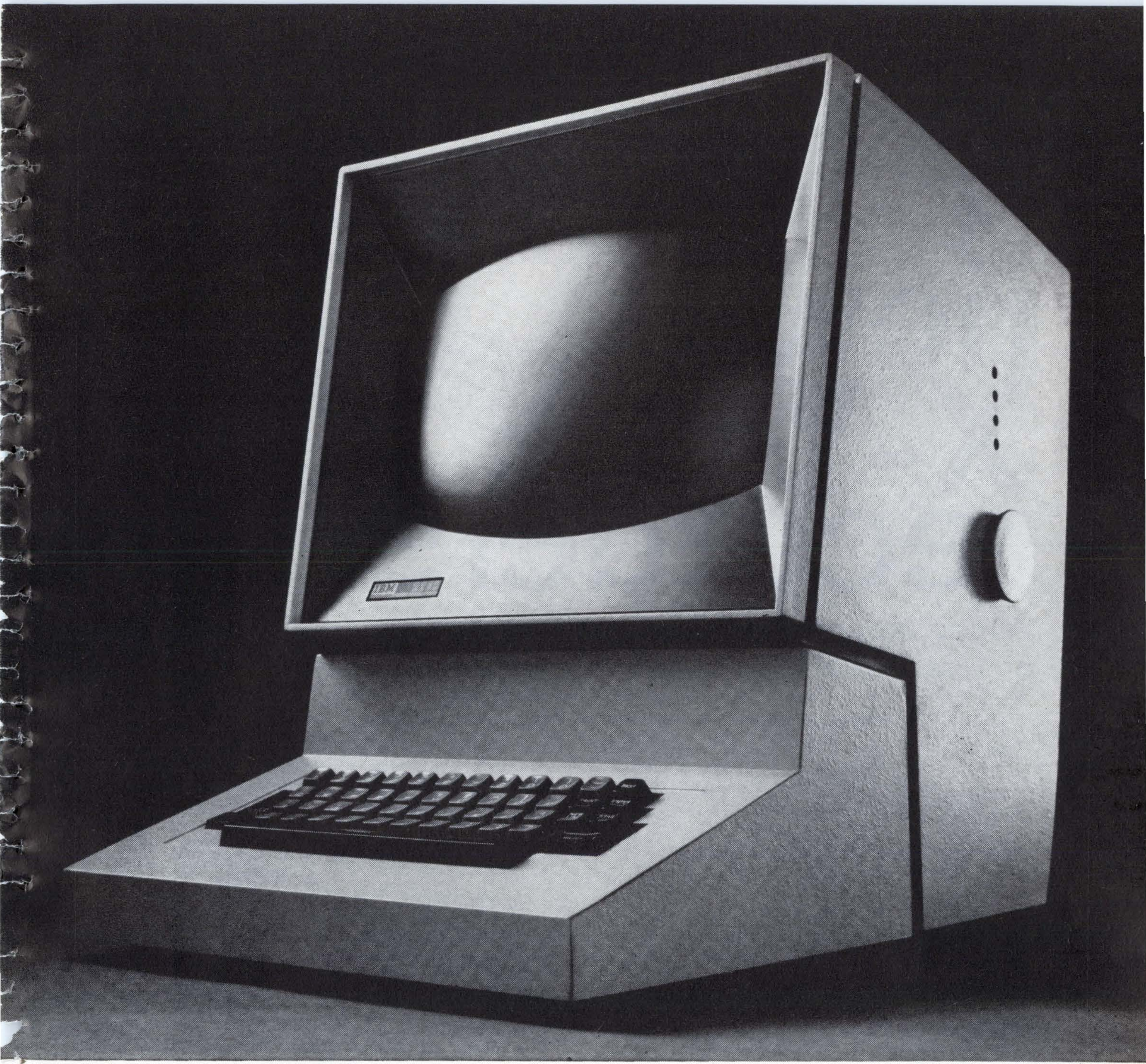

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A big case for G-E NORYL®
THERMOPLASTIC RESIN

Once you learn about Noryl resin, it's easy to build a big case for using this new General Electric engineering thermoplastic. IBM did with its computer display station. The finished unit measures 17" x 17" x 13" and uses 12 pounds of molded Noryl.

Take high heat resistance. The unit operates at temperatures up to 200°F. No problem for Noryl with its heat deflection temperature of 265°F at 264 psi. In fact, Noryl was one of the few materials that could withstand bake cycles up to 250°F after the case is painted.

This unit required the best self-extinguishing material. Noryl came through again. New grade SE-I is self-extinguishing, non-dripping UL Group I, even in 1/16" thin sections.

Moldability and appearance were also important considerations. Flow requirements of 25 inches into .060" walls, 12 right angle changes of direction and 128 ventilation slots measuring 4½" x 3/32".

And economy? Noryl met these specifications more economically than other materials tested. One reason is its low specific gravity which means more-parts-per-pound than most materials.

Noryl is also tough, dimensionally stable, has low, predictable mold shrinkage and offers outstanding hydrolytic stability.

Looking for a material that offers good properties, economy and easy processing? IBM found a good case for Noryl. So can you. For more information contact your Chemical Materials Sales Representative. Or write Section **6B6,** Polymer Products Operation, General Electric Company, One Plastics Avenue, Pittsfield, Massachusetts 01201. In Europe contact, N. V. Polychemie AKU-GE, 76 Velperweg—Arnhem (The Netherlands).

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Circle 189 on reader service card

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3 new X-Y recorders

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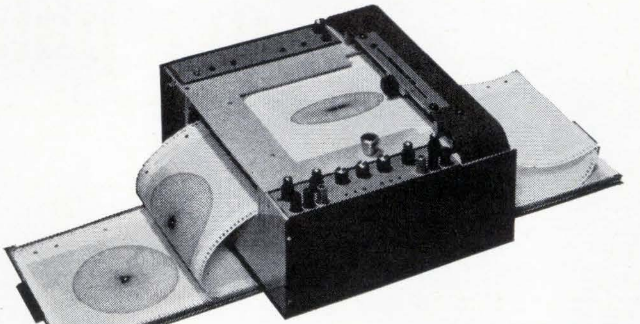

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8½" x 11" Recording Surface

Chart Paper Z-fold. Perforated for ease in tearing out to notebook size. Automatic chart advance eliminates the need to manually load and unload each chart.

Recording Mechanism Two independent servo drives for X and Y.
Automatic index or reversal of chart on command—local or remote.

Slewing Speed 15 in/sec., of course.

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Input Impedance 1 megohm all ranges—fixed or variable.

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Standardization Dual regulated temperature compensated zener reference.

Pen Control Local or remote.

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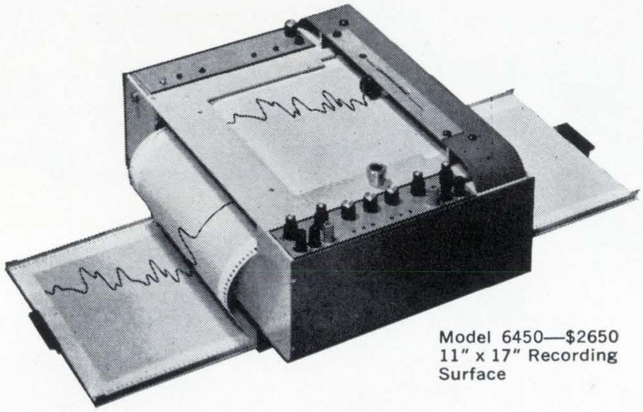

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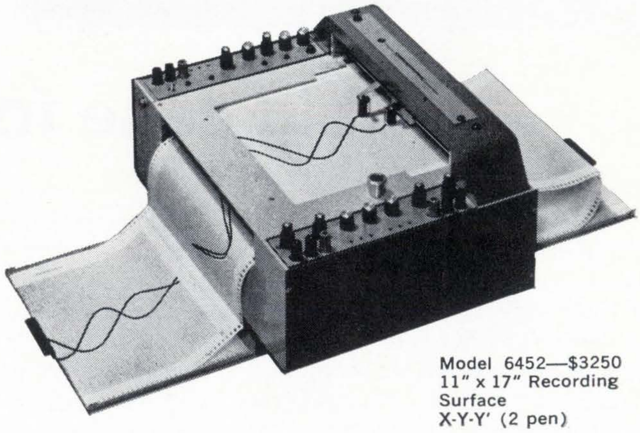
11" x 17" Recording Surface



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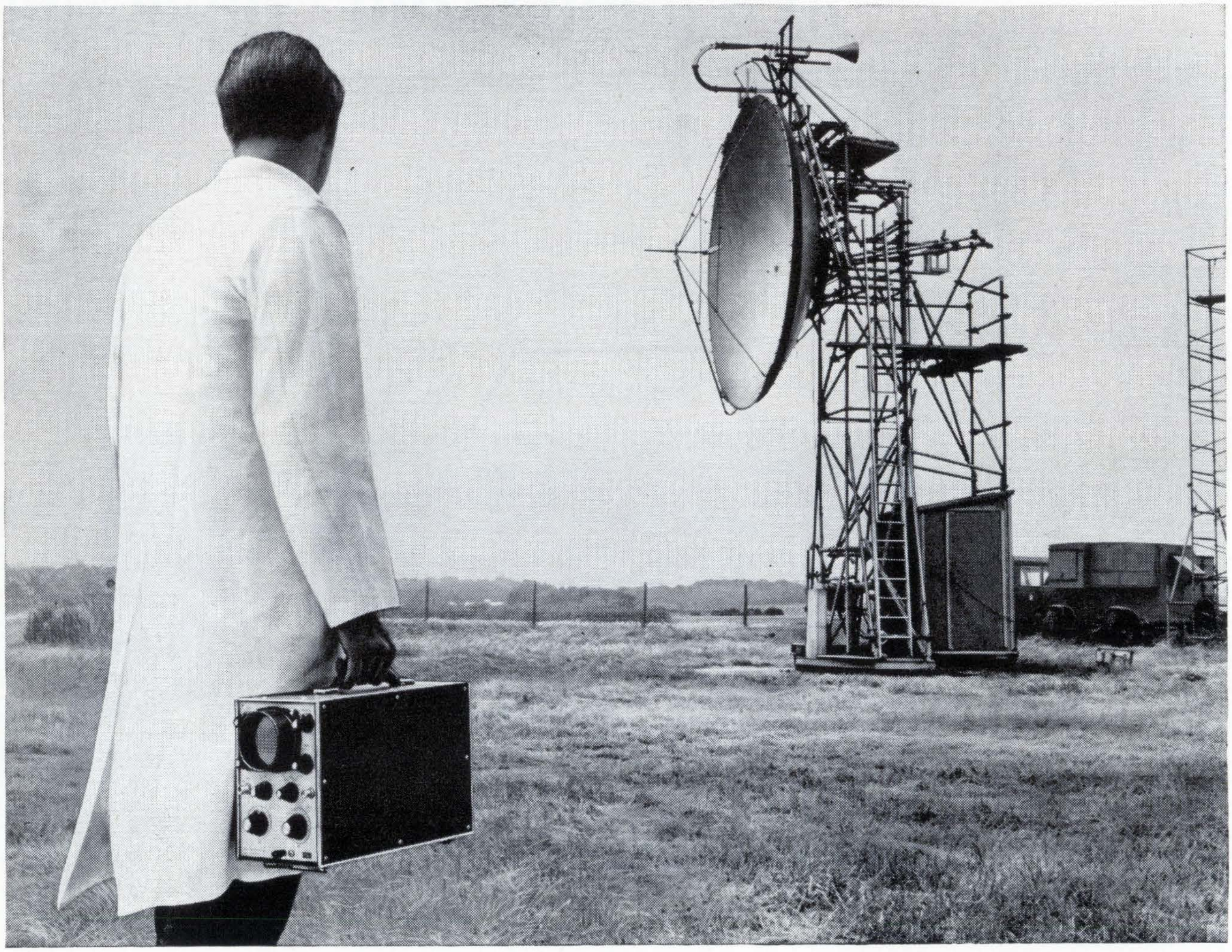

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Its batteries give 4 hours operation per charge, and it has its own integral charging unit. Yet it weighs only 22 lbs. complete.

Y sensitivity is 5 mV per division and the sweep ranges cover 40 nanoseconds to 0.5 second per division. Other features are a 3″ high intensity P.D.A. tube and an internal square wave calibrator.

This high performance general purpose oscilloscope is the Bradley Type 150.

We shall be pleased to send you full details on request. See your Electronic Engineering Index Library for full technical data.

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Circle 193 on reader service card→

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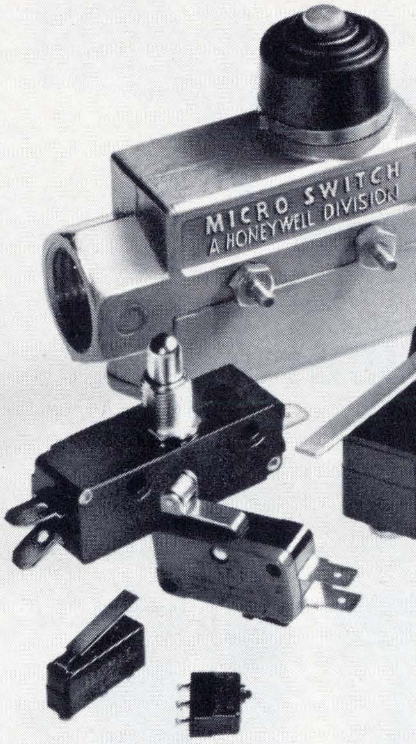
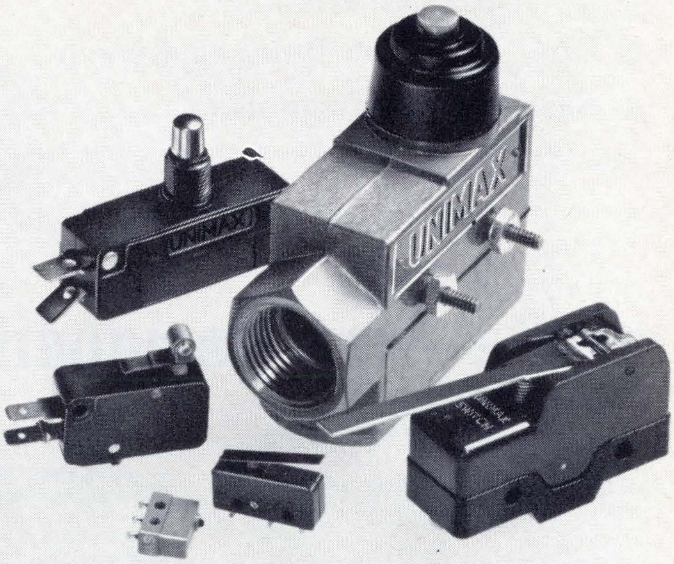


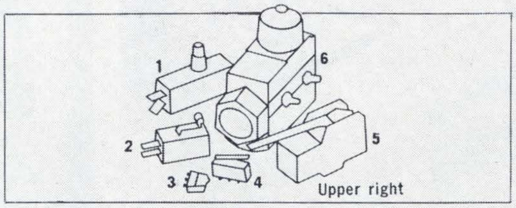


Think Unimax.

Break the Brand M habit—think twice about your switch supplier. The Unimax line is complete from miniature sub-miniature to big, rugged, explosion-proof metal-cased switches. And we bow to no one in the quality, price or delivery of our products.

If your switch requirement decisions have become automatic Brand M selections, you may not have considered Unimax's 20 years of experience in snap-acting switch design and manufacture. Or the thousands of specials we have developed for individual applications.

Why not—this time—think twice before you act? The coupon at right offers you, free, your personal "Think Twice" button and any or all of our detailed, full specification catalogues.



Typical switches from each category of the complete Unimax line.

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3. Miniature Subminiature. Differential motion as low as .0005″ max. Leaf and leaf-roller integral actuators available.

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6. Metal-Cased. Compact, Heavy-duty, Splash-proof and Explosion-proof models, with all types of actuators.

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Unimax Switch

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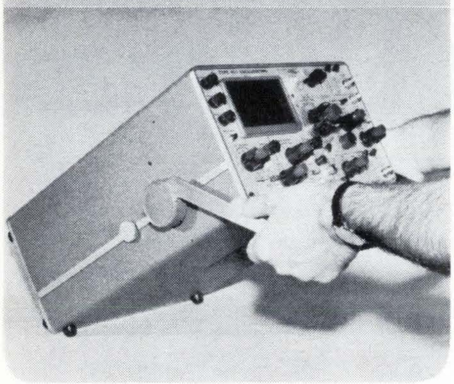
Tektronix Type 453 oscilloscope has

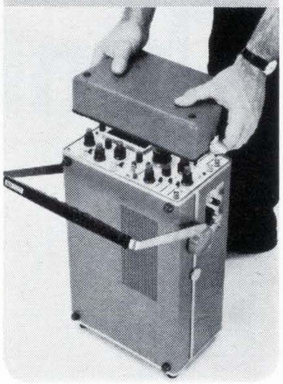
- 50 MHz Performance
- Dual Trace ● Delayed Sweep
- Easy-to-Use Triggering

and-----it's designed to be carried!

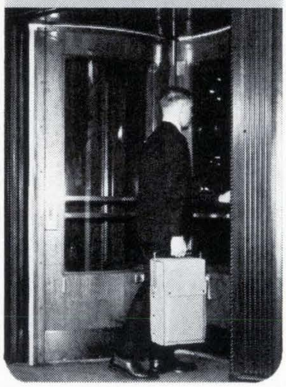
Pick it up and be convinced. The Type 453 weighs 28¾ pounds and is built to go when and where you go.



Don't worry about damaging the front panel and knobs—they're protected by a cover that also carries the accessories.



Take the Type 453 through tight places easily . . . the vertical carrying position increases portability.



Take it anywhere. The rain/dust cover is a standard accessory and carries the complete manual and optional viewing hood.

The Type 453 is a portable instrument with rugged environmental capabilities plus the built-in high performance normally found only in multiple plug-in instruments.

The vertical amplifier provides dual trace, DC to 50 MHz bandwidth with 7 ns risetime from 20 mV/div to 10 V/div. (DC to 40 MHz, 8.75 ns T_r at 5 mV/div.) The two included Type P6010 miniature 10X probes maintain system bandwidth and risetime performance at the probe tip—DC-50 MHz, 7 ns—with an increase in deflection factors of 10X. You can also make 5 mV/div X-Y and 1 mV/div single trace measurements.

The Type 453 trigger system takes the guesswork out of triggering. Pushing all the lever switches up provides a sweep and the most often used trigger logic. The sweep triggered light gives the operator a positive indication of a triggered sweep and the automatic triggering provides greater usability.

You can operate the delayed sweep with ease. Lever control to the right and HORIZ DISPLAY switch to A INTEN DURING B gives delayed sweep operation. Setting the B TIME/DIV and the DELAY-TIME MULTIPLIER to meet your requirements and switching to DELAYED SWEEP allows $\pm 1.5\%$ delay measurements to be made.

The Type 453 is a continuation of the Tektronix commitment to quality workmanship. Its design and layout make it easy to maintain and calibrate. Transistors plug in and are easily removed for out-of-circuit testing. An accurate time ($\pm 0.5\%$) and amplitude ($\pm 1\%$) calibrator permits quick field calibration.

The front panel protection cover carries all the accessories with the complete manual carried in the rain and dust cover. The Type C-30 Camera and a viewing hood that fits in the rain cover also are available.

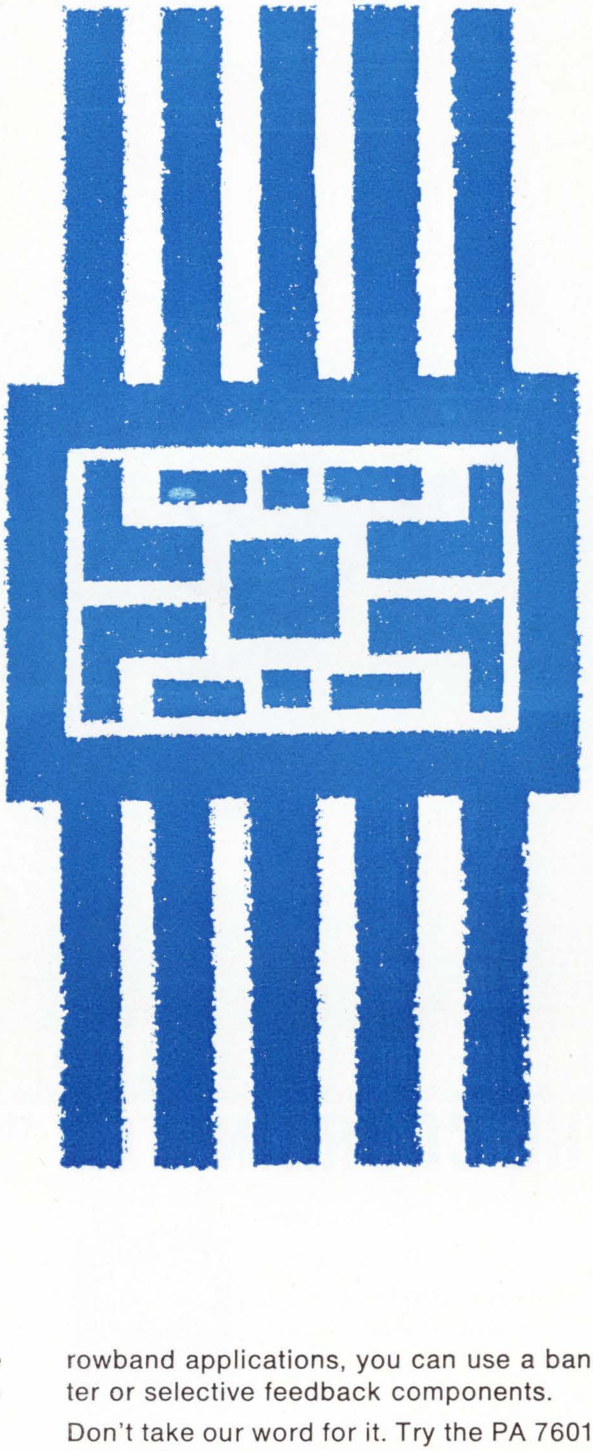
Type 453 (complete with probes and accessories) . . .	$1950.00
Type C-30 Camera	$ 390.00
Collapsible Viewing Hood	$ 7.50

U.S. Sales Prices, FOB Beaverton, Oregon

Tektronix, Inc.

For complete information, contact your nearby Tektronix field engineer or write:
Tektronix, Inc., P.O. Box 500, Beaverton, Oregon 97005

Almost every engineer who uses our IC bandpass amplifier says it's better than a discrete amplifier.



(Charlie Wisgard says it's just as good.)

But, at the price, we know that you won't be able to get a discrete or IC bandpass amplifier that can out-perform the PA 7601.

Look at the performance. It has a gain control circuit which provides 12 db of gain reduction with typically less than 10% variation in output terminal impedance. In broadband applications, gain control from 0 to 12 db produces negligible effect on bandwidth over a frequency range of 30 to 150 MHz.

Our PA 7601 is your best solution to high-frequency phase and amplitude distortion problems. For narrowband applications, you can use a bandpass filter or selective feedback components.

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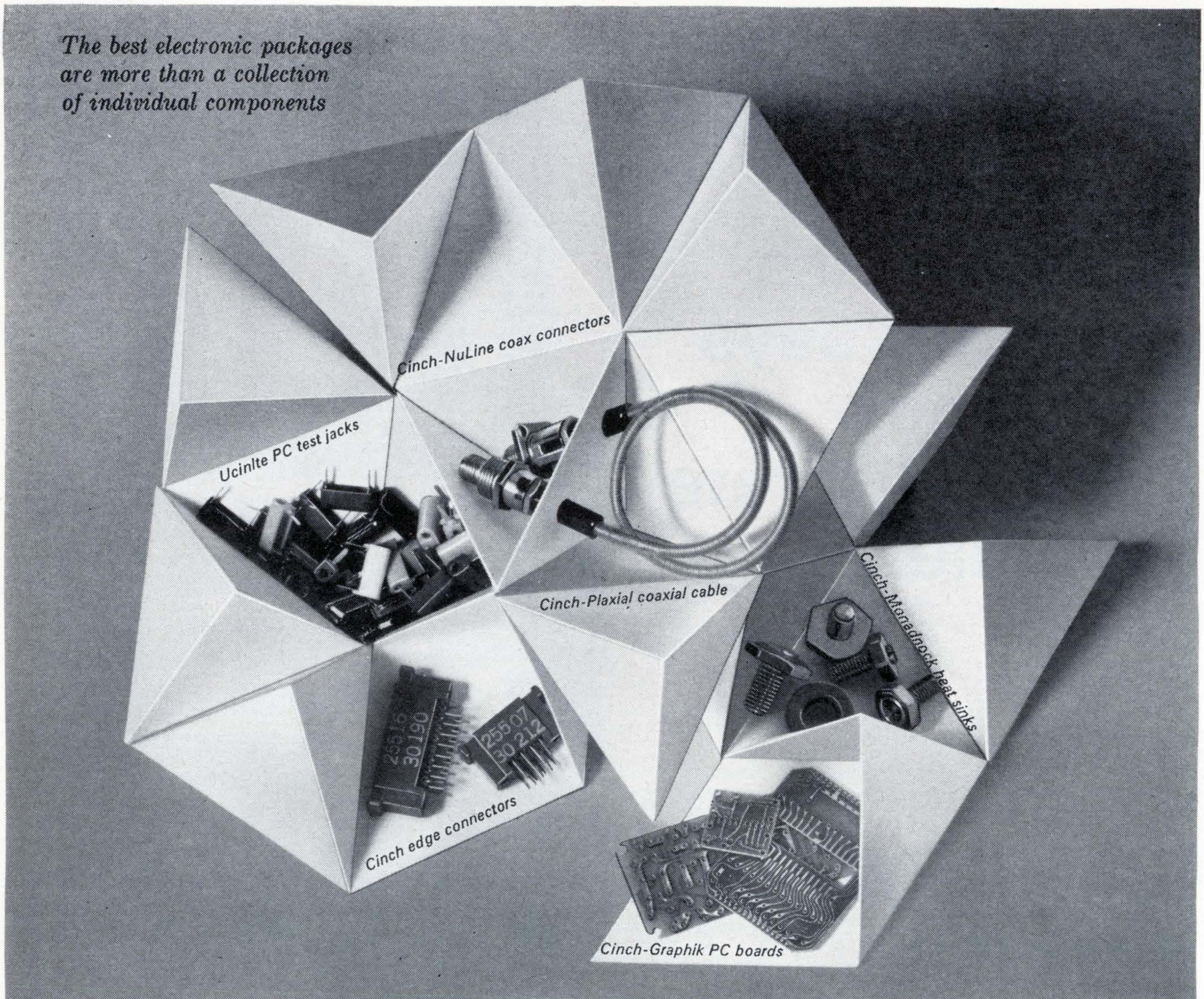

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CINCH-NULINE
coaxial connectors and cable termination

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A new approach to component packaging? We think so. The Cinch Electronics Group coordinates design, application engineering and production for six related divisions of United-Carr Incorporated and provides one central ordering point for all parts. (We call the result the "Package-Package"—you'll call it an efficient way to achieve a superior product!)

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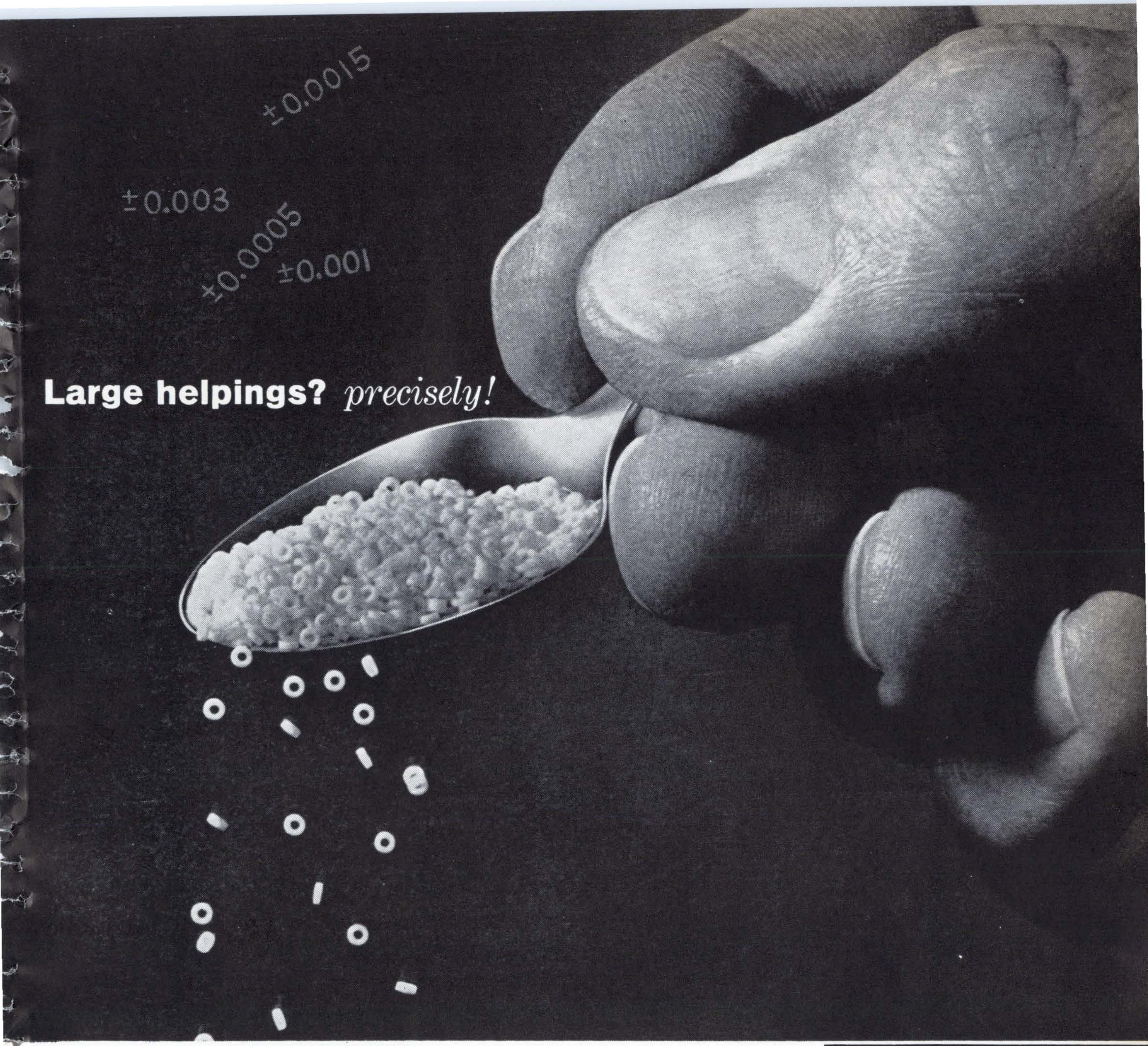

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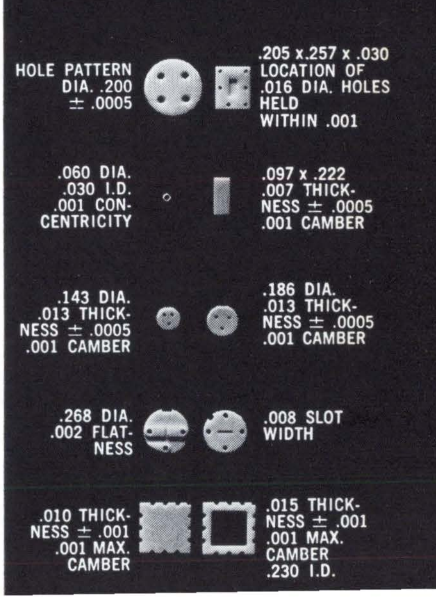

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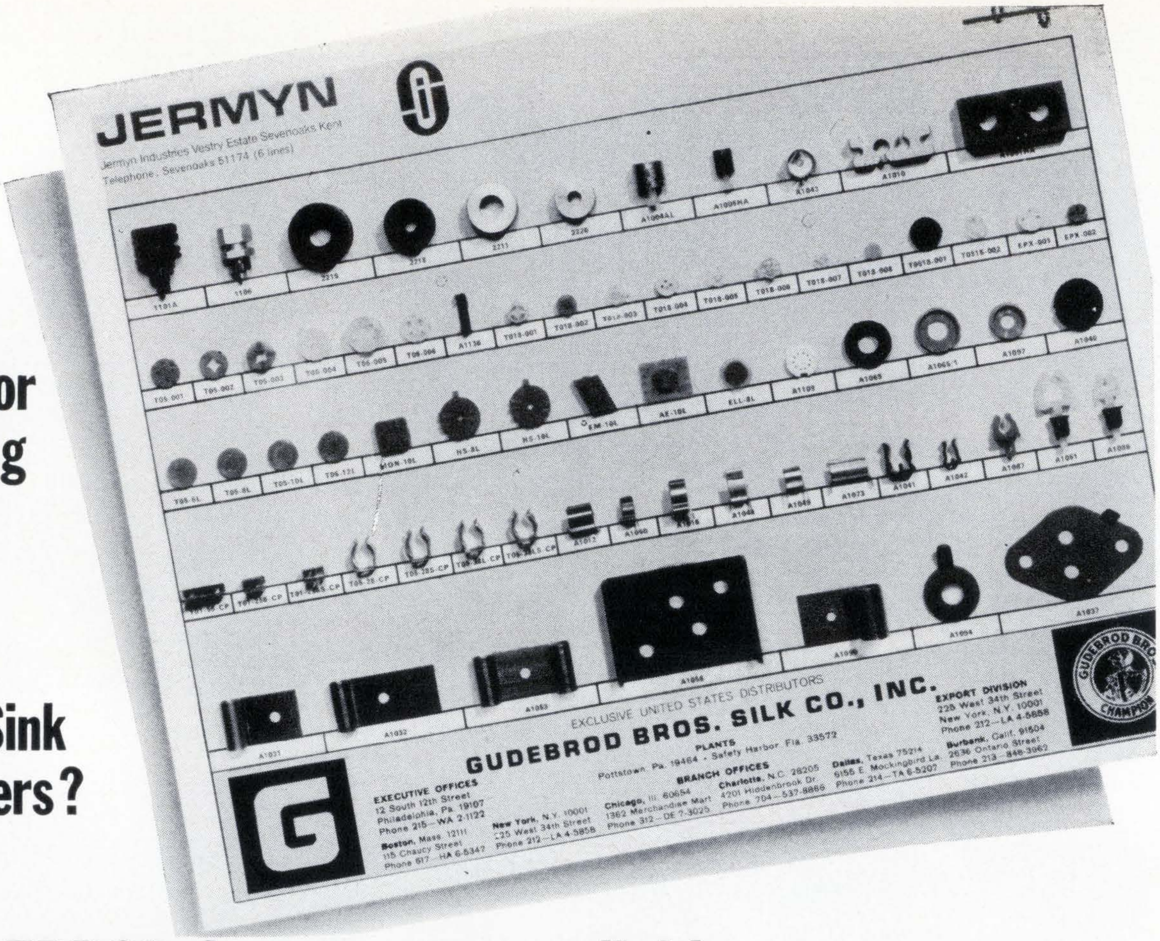

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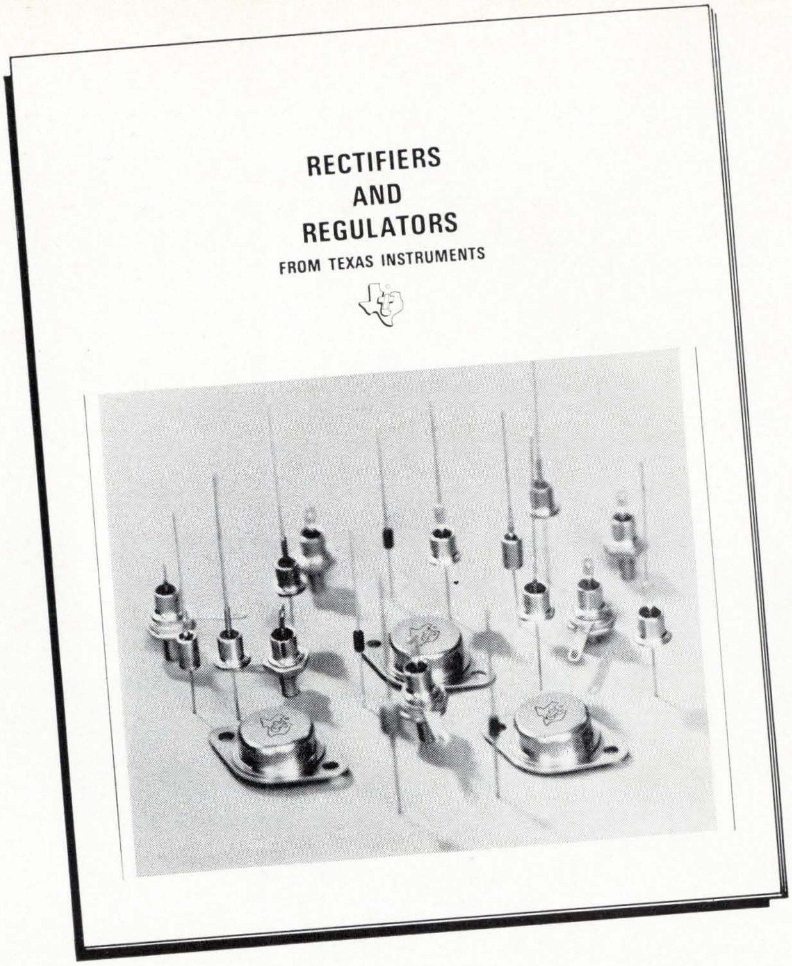

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Because K&E has more experience with more different varieties of reproduction materials than anybody else. And because K&E aims to keep it that way. (For a look at one of our most popular papers, please turn the page.)

K+E 1867 INTO CENTURY II 1967
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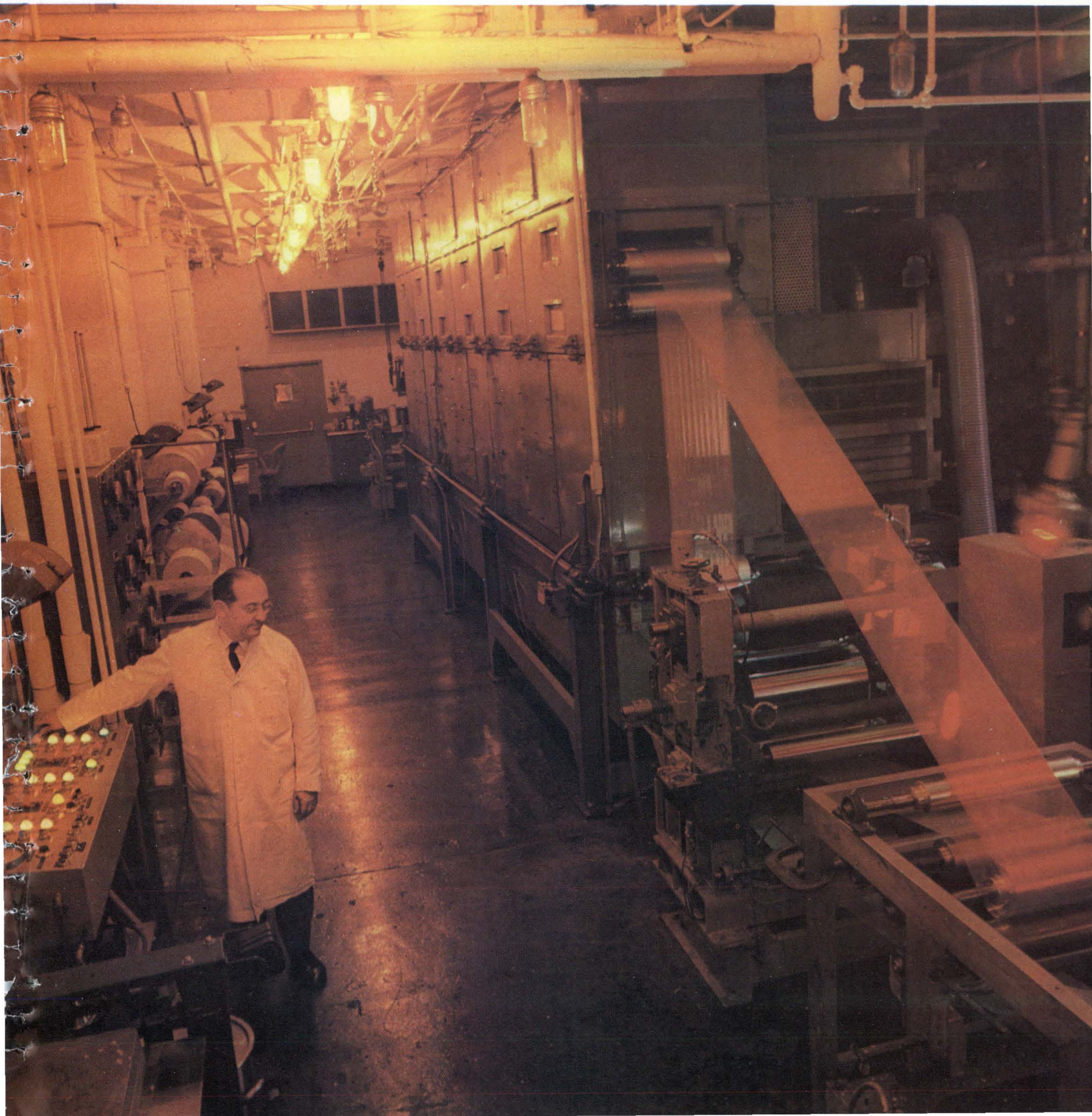

R&D: PLEASE DON'T IMPROVE THIS ONE.

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21 2145 is hardy, durable paper. Takes a lot of wear and tear. Because it's made of 100 per cent rag bond.

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Probing the News

While military and civilian markets for compact digital computers promise to be vast, they pose difficult questions for manufacturers.

1. **Should systems be custom designed or off the shelf?**
2. **How big a threat is European competition in domestic markets?**
3. **Will demand be greater for multiprocessors or special-purpose units?**

Computers

Airborne computers set to take off

Bandwagon demand for small digital machines spurs an industrywide scramble to climb aboard

By Paul Dickson
Staff writer

The sky's not the limit for the compact digital computer. In addition to a certain future in military and commercial avionics systems, lightweight, speedy little machines, in both multifunction and special-purpose versions, are set for a variety of shipboard and land-based jobs. So good are the prospects—the total market is being measured in billions of dollars—that a score of companies are scrambling for a piece of the action.

A recent Government survey illustrates what the scramble is all about; it estimated that during the next five to seven years the Department of Defense will purchase between 10,000 and 20,000 airborne digital computers. Included are units to be employed in such areas as the Tacfire artillery management system, the SAM-D missile, the 407L tactical air-control system and aboard Navy vessels. With many general-purpose computers selling for better than $100,000 apiece, the Pentagon's prospective demand alone represents a tidy sum. When the requirements of the National Aeronautics and Space Administration, other Government agencies and commercial aviation are added, the dollar market is staggering.

I. High hurdles

The compact computer field is now the preserve of a dozen or so companies. None enjoys an overwhelming technical edge and most share common problems.

Interservice commonality is but one of many difficulties that must be faced by manufacturers anticipating the needs of the future. John W. Koltz, assistant director for Tactical Control and Surveillance Systems at the Director of Defense Research and Engineering Office, says: "We tell the services that they had better be able to live with the decisions they make. The Navy would look pretty foolish if one whole deck of an aircraft carrier had to be used for maintaining different types of computers."

One aspect of the commonality problem is being studied at Holloman Air Force Base, Alamogordo, N.M. A low-cost inertial navigation system with a digital computer to provide continuously updated flight coordinates is being developed there. Called the AN/ASN-66, the system would be made initially for the Air Force. But officials are hopeful that it can eventually be used to navigate all aircraft. They intend to make their findings avail-

. . . the problem is to get the computer to interface with the real world . . .

able to the other services as well as to commercial airlines. The contract for the computer is expected to go to either the Northrup Co.'s Nortronics division or Lear Siegler Inc.'s Instrument division when the system goes into production.

But even if the commonality problem could be overcome, another still exists: multipurpose versus special-purpose units. In the AN/ASN-66 the computer does one job, leaving fault-finding, fire-control and related tasks to other systems. On the other hand, the Air Force's Research and Technology division at Wright-Patterson Air Force Base recently awarded a contract to the Teledyne Systems Co. of Hawthorne, Calif., to study the possibility of a doppler-inertial-loran system using a single multipurpose computer.

II. Schools of thought

Entrants in the compact digital computer field are at odds over what kind of production is best. On one side are firms like the Kearfott division of General Precision Inc. which favor the customer-oriented approach, producing a specific system for a specific application. An opposite tack has been adopted by the International Business Machines Corp. which prefers to have a family of versatile off-the-shelf computers that can be adapted to the needs of many customers.

Availability of three digital computers, called the 4 Pi series [Electronics, Oct. 31, 1966, p. 42], has something to do with IBM's marketing stance. J.B. Jackson, vice president and general manager of the company's Electronics Systems Center says, "There has been an excellent acceptance of 4 Pi and we now have firm contracts for a number of applications." Jackson points to the machines' "read-only-store" capability as having been critical to the acceptance of the series but also points to reliability, maintainability and cost advantages.

Marketing. The outlook for the 4 Pi computers is bright, according to Jackson. "Anyplace there is a hardened military environment, I see an application for 4 Pi," he says. Thus far, IBM has four contracts. The most significant is the order for the Mark II avionics system for the Air Force's F-111 fighter-bomber. About 1,000 computers will be produced for this system: two units for each aircraft, one for weapons delivery and a second for navigation. Other 4 Pi contracts include applications in the Manned Orbiting Laboratory, the EA6B Navy attack aircraft; and the target identification acquisition system for the antiradiation missile. Moreover, IBM and Litton Industries Inc. are currently the only two manufacturers still in the running for the computer contract in the E2A early warning aircraft.

The 4 Pi may become a factor in commercial aviation as well. Eastern Air Lines is flying IBM equipment to determine whether failure patterns can be recognized

Some entries in the airborne digital computer race

Companies	Computers
AC Electronics	Magic series
Autonetics	D26 line
General Precision	Dydan, L-90-1 and Micro Minac
Honeywell	Alert, SIGN-3
IBM	4 Pi series
Lear-Siegler	Divic
Litton	300 and 3000 series
Nortronics	1051 and 1051A
Raytheon	R-11, R-25 and R-31
RCA	VIC
Sagem (French)	AE51c
Sperry Gyroscope	Mark 12 and Mark 14
Teledyne	DIL
Univac	1830A and 1824

before a breakdown occurs. Joseph E. Jenette, marketing manager at IBM's Electronic Systems Center, sees commercial aviation "as a definite marketplace for 4 Pi."

GPI's customer approach has also been successful with one digital computer system alone generating $20 million worth of annual volume. Its AN/ASN-24(V) is in production for the central navigation system in the Air Force's C-141 transport and a system designated GPK-10 is being readied as a solid-state follow-on for the same program. In addition, the company's GPK-33 is being turned out for the Centaur B space launch vehicle while the GPK-20 is in production for the Navy's P3C patrol aircraft. Awaiting applications are Dydan, an incremental computer for low-cost navigation systems; the L-90-1, a high-capacity general-purpose unit for navigation and central processing tasks; and Micro Minac, a special-purpose solid-state digital computer for low-cost airborne navigation applications.

"Any three graduates of a good engineering school with a course in digital design can produce a compact digital computer," says Alfred F. Schmitt, director of the aerospace digital computer department at Kearfott. According to Schmitt, the problem is to fit the computer into the system, or as he puts it, "interface with the real world." High-speed aircraft pose difficulties not present in a ground-based system, he says, citing power sources, progressive error, scaling (the placement of decimal point to record a real value) and achievement of real time in milliseconds.

Bundles from Britain. Still another problem for American firms trying to establish a position in the airborne digital computer field is British competition. A Pentagon agreement to buy $300 million worth of British hardware to offset the cost of the 50 F-111's to be ordered by Britain puts a very large foot in the door. Elliott Automation Ltd., Ferranti Ltd., the Marconi Co., the Decca Navigator Co. and G.E.C. Computers and Automation Ltd. all have bantam airborne digital computers for sale. Elliott has been awarded a contract to supply analog units for the giant C-5A transport and is developing the digital computer interface and

Raytheon's multipurpose R-11 computer is designed for weapons systems use.

power supply for the Navy's integrated light attack avionics system.

III. Economy sizes

With the complex and crowded conditions prevailing in the airborne digital computer field, many manufacturers are concentrating on specialized segments of the market in their efforts to establish a niche.

Nortronics is betting on low cost with its 1051 computer which is price tagged in the $25,000 to $30,000 bracket each in production quantities of 100 or more. E.A. Klein, chief of Nortronics' computer development group, says, "Our ratio between labor charges and material costs used to be 70:30, but we have nearly reversed that."

In addition to the 1051 system, Nortronics has a 1050A being tested at Holloman for the low-cost inertial navigation program. This computer is installed in the doppler-inertial navigation system and the malfunction-and-analysis detection and recording system to be used in the C-5A. Nortronics considers Loran-D, weapons delivery and navigation systems, airborne data processing and space missions as outlets.

Throwaways. Low cost has undeniable appeal and the Raytheon Co. is currently investing large amounts of its own money in an effort to produce a low-cost digital computer using large-scale integration (LSI) techniques. Wendell Smith, marketing manager at the company's Bedford Laboratories, explains, "By low-cost computers, I mean those in the $5,000-to-$10,000 range. This will put them in the throwaway category. Military managers are encouraging electronics systems that will not need maintenance but which will simply be used up to failure and then discarded."

New offerings. For the immediate future, Raytheon's computer roster includes three new airborne machines that resulted in part from systems work on the Army's Hawk and the Navy's Sparrow missiles. The first in the new series of Raytheon computers is the R-11, a high-speed, large-memory multipurpose computer. Designed for installation in complex weapons systems, it has a cycle time of 1-microsecond. Raytheon shortly will introduce a cut-down version designated R-25, which will give up speed in return for advantages in size, weight and power consumption. The R-11 weighs 100 pounds and the R-25 only 38. Raytheon would like to find R-25 applications in airborne fire control, airborne guidance and navigation, simulation and training, and shipboard navigation. A third member of the family to be ready this month is the R-31, which has been designed specifically for the Hawk, for which Raytheon is prime contractor.

Donald R. Kirsch, the company's military marketing manager emphasizes that the R-31 is a multipurpose machine. The company plans to market the R-31 for a wide variety of airborne and military applications. A salient feature of the R-31 is that input-output has direct access to memory. "This allows very high speed data transfer," Kirsch says. "Any competent electronics house can build a central processor and buy or build a memory. But the important distinction among machines is in input-output, including the ability of the computer to handle peripherals at high data rates."

One of the earliest applications of the Raytheon computer will be in tactical phased-array radar systems for airborne, ground and shipboard use [Electronics, Jan. 9, p. 172].

Lear Siegler is also aiming at the economy computer market with its 25-pound Divic (digital variable increment computer) [Electronics, Sept. 5, 1966, p. 105]. Divic features a core-rope memory which has an extremely low cost per bit—about two cents. The read-write memory is a conventional ferrite core. The company is getting sales price down to $20,000 per unit in large production quantities.

The mating game. Compatibility is the word being used at the Radio Corp. of America's Aerospace Systems division. "With our approach in VIC (variable instruction computer) we've found a way to be compatible with a wide range of ground computers," says Edward H. Miller, manager of aerospace computer applications. Next month, the VIC system—demonstrated last December for the Air Force—will undergo an airborne test of its compatibility with an IBM 7090 in a command and control environment [Electronics, Dec. 12, 1966, p. 45].

Preliminary design work is under way on variations of the VIC and RCA is looking to the data processing needs of the Awacs (airborne warning and control system) and airborne antisubmarine defense programs for additional outlets. Miller sees commonality of the airborne system with ground-based computers as a major trend in command and control. An advocate of customer-oriented policies, Miller says program managers are finding that attempts to use a universal off-the-shelf computer impose penalties in weight and price.

IV. Commercial inertial

Inertial navigation systems have the greatest sales potential for digital computers in commercial aviation. E. Leslie Keates, senior marketing representative at the Sperry Gyroscope Co., a division of the Sperry Rand Corp., believes "every new aircraft built for overseas transport from here on out will contain two systems and possibly more. The supersonic transport (SST) may contain as many as four redundant inertial systems." Sales estimates of inertial systems in the commercial sector during the next five years have run as high as 3,000 units. System price tags are in the $100,000 class.

Two companies with an edge in this field are Sperry Gyroscope and the AC Electronics division of the General Motors Corp.

Sperry is already producing an inertial navigation system, the SGN-

10, which it is delivering to Pan American World Airways for use on the Boeing 707's. There are now 28 systems on 14 Pan Am aircraft. According to Keates, the system's Mark 12 digital computer "is performing well within specification and improving with quantity production." Sperry expects the Federal Aviation Agency to certify the SGN-10 sometime this spring and anticipates additional orders to result from it. The Mark 12 is also being used as part of the radar system on the Canadian weather ship, Vancouver, and in the control system aboard the Navy's deep submergence vessel Trieste II.

Another Sperry computer in production is the Mark 14, being delivered to the Army for the Loran-D tactical navigation system.

Company-supported research and development at AC Electronics has paid off in the award of production and development contracts for the company's Magic series of airborne computers. One order covers the inertial navigation system for the Boeing 747 Jumbo Transport [Electronics, Feb. 6, p. 38]. Another machine in AC's Magic line of computers is in pilot production for the inertial guidance on the SRAM (short range attack missile). The company also has a contract for development work on the computer for the Navy's ship's self-contained navigation system.

Foreign commercial. The influence of the French-British Concorde SST on commercial aviation extends into the digital computer field and success in the area could prove a strong selling point. A pair of computers aboard the Concorde will perform self-checking and fault diagnosis, provide steering signals, navigate inertially and provide such housekeeping data as fuel consumption. A unique feature of the system will be computation in concert with a pictorial-situation display which will project a map of the area over which the plane is flying on a cockpit console. The combination will enable Concorde pilots to carry all navigation information in a film casette. Supplied by the French Societe d'Applications Generales d'Electricite et de Mecanique, the computer is designated the AE51c; the display portion will be made by Ferranti.

Upkeep. In some computer markets, maintainability is a powerful sales weapon. Teledyne and the Univac Defense Systems divisions of Sperry Rand each has recently received contracts for airborne digital computers which feature simplified maintenance.

Teledyne's latest was a $24 million production contract for avionics systems in the CH-53A and CH-46A helicopters. The company is also a subcontractor of the Lockheed Aircraft Corp. for a triply redundant computer complex for the Army's advanced aerial fire-support system.

Univac offers two small digital computers: the 1830A, a general purpose command-and-control unit which will go into production for the Navy's A-New antisubmarine warfare system [Electronics, Dec. 12, 1966, p. 184], and the 1824, for the inertial navigation system in the Titan III booster.

V. Off the shelf

"We looked ahead to what our potential users will need and then went ahead and developed the series to meet these requirements," says Leon Bloom, special assistant to the vice president for special programs at Litton's Data Systems division. "Litton thinks like IBM in this area," says Bloom.

Litton is working on two lines which each have three small stored-program machines with different computation speeds. The 304 from the company's 300 series is in production and being evaluated for the E2A aircraft. A prototype 3050 for the 3000 line is also being built.

Litton's Guidance and Control division has turned out more than 5,000 analog and digital computers for navigation systems in military aircraft. It is now working on a design contract for a "wafer" computer which will have extreme accuracy, reliability and a sufficiently low price to permit convenient replacement.

Alert, a computer being produced by the aeronautical division of the Military Products Group at Honeywell Inc., is, according to M.J. Leonard, divisional marketing manager, "the most powerful off-the-shelf computer in production today." Honeywell, an off-the-shelf advocate, also has a prototype general-purpose airborne digital computer which is designated SIGN-3 for inertial navigation applications.

Contract awards. Alert figures in a number of development contracts including two automatic reconnaissance projects. The system is also being considered for the X-15 rocket plane's energy management system and the AN/USQ-28 photo mapping system. Leonard says Alert has been selected for additional programs by several prime contractors.

North American Aviation Inc.'s Autonetics division supplied the systems in the Minuteman I and II missiles, and an improved version is being developed for the Minuteman III. Autonetics' D-26 line is designed for avionics use. The latest model, D-26J, a small single-purpose unit underwritten by the company, will be the inertial navigation computer in the F-111. Autonetics is also developing a D-26J-type machine for the control system in the RF-111.

Debuts. Newcomers also are flocking into the compact field. Last month the Control Data Corp. formed a new aero systems department to vend special-purpose airborne computer systems. Also among the more recent entrants is the guidance and control division of the Aerospace Group at the Hughes Aircraft Co. It has a fire-control computer, the HCM-205, and a full-scale data handling system, the HCM-206, which can be adapted for command-and-control applications. The 206 uses multiple arithmetic units and multiple memory modules to make it suitable for rugged military environment. Hughes officials say the firm is negotiating its first contract for the 206 in a classified program. Charles F. Saunders, marketing manager for the division, says, "The 206 will be in full-scale production by the end of the year."

Saunders, who believes this family of computers has a lifetime of five years, echoes the sentiments of his counterparts around the industry. "The next level of technology —breakthroughs in cost and productivity—will probably occur within five years and will make extensive use of LSI techniques," he says. Saunders may be off in his estimate. Texas Instruments Incorporated is scheduled to deliver a prototype digital computer featuring LSI to the Air Force in 1968.

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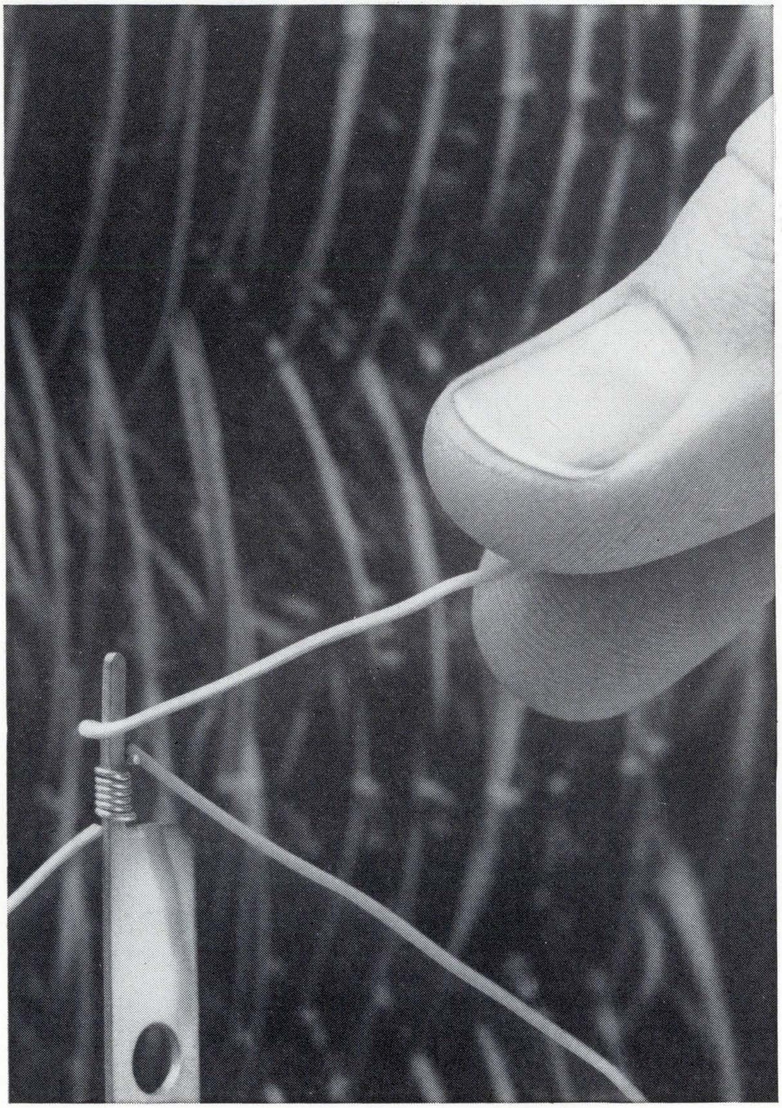

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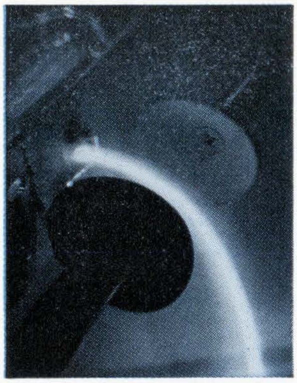

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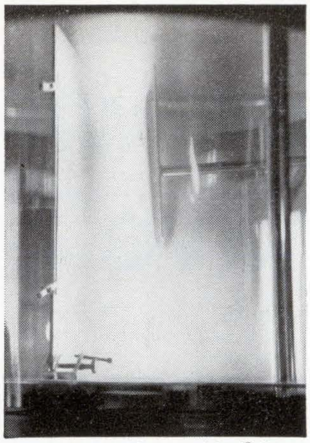

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Sea dogs' seeing eye

The Naval Tactical Data System coordinates fleet's battle operations and provides commanders with instant intelligence

By Gerald Parkinson
Los Angeles Bureau

Though battle-proven and efficient, the Naval Tactical Data System is set for a facelifting. Provision for sonar inputs, a navigation capacity, incorporation of integrated circuits and standardization of display consoles are among the refinements planned for the system, now in its third generation.

The NTDS, which has been operational in Vietnam waters, provides battle commanders aboard warships with a comprehensive, real-time picture of friendly and hostile ships and aircraft from conventional electronic sensors. It is installed on 30 to 40 vessels, including aircraft carriers, destroyer leaders and cruisers.

The Hughes Aircraft Co. has a three-year, $18.9-million contract to supply 343 display consoles and related equipment for 15 more ships.

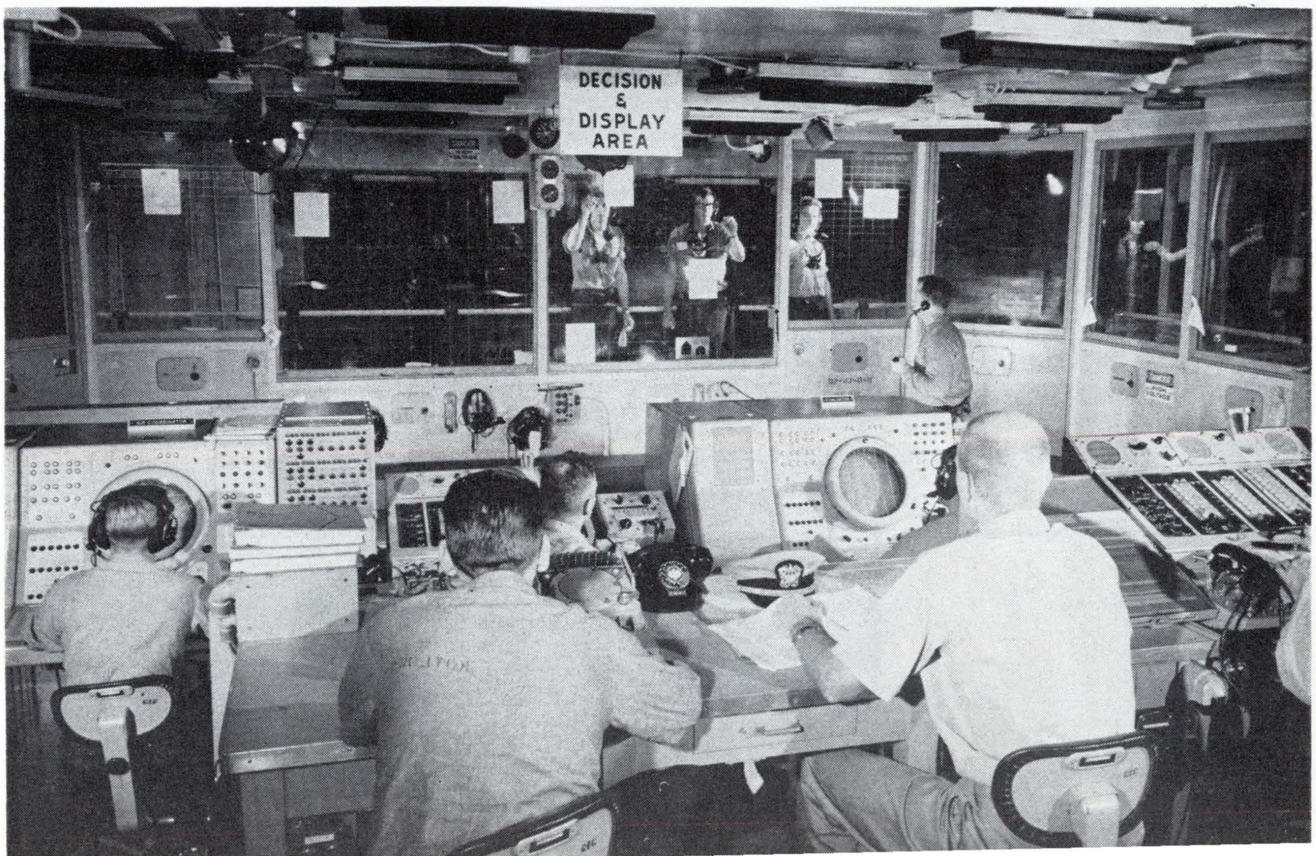
At the heart of the NTDS are computers supplied by the Univac division of the Sperry Rand Corp. Configurations depend on the class of ship that is involved, but there can be as many as four computers in a system. The AN/USQ-20 is a general-purpose, stored-program digital computer processor with a 4-microsecond cycle time and 32,000-word memory. It occupies about 54 cubic feet of space, weighs 2,100 pounds and operates in real time. Among other things, the computer stores information on the fleet's aircraft and weapons status. It also serves as a way station for data supplied from surveillance gear.

Track information from such sources as long-range, height-finding and navigation radars and sonar is presented on the 12-inch radarscopes of data input (DI) consoles. An aircraft carrier's NTDS might have as many as 10 DI consoles.

I. Seascape

To track, the console operator simply places a marker over the target on his scope. He pushes a button to feed the target's coordinates into the computer. Operators can also send iff (identification, friend or foe) and ecm (electronic counter measures) data and information as to whether a track is

Data utilization consoles, important elements of the NTDS, installed aboard the carrier Enterprise, enable battle commanders to evaluate threats and decide on effective countermeasures.



surface or air. Meanwhile, the computer automatically plots the course and speed of the target in real time.

When a DI console operator is following more than one target, he pushes a sequence button to record coordinates. This enables the computer to indicate which track the operator should update next. If a target moves out of range, the computer actuates a warning light. The repeating accuracy of the Hughes scopes is 0.1%, regardless of the symbol's position.

Although all DI console operators have access to the same data, they are responsible only for discrete geographical sectors or situations. A supervisor, who can switch consoles to an area where the load is heavy, monitors the input operation. An NTDS generally includes several consoles in the DI area to display data from height-finding radar or enlargements of other sensor information. According to David Heebner, division manager for Navy programs at Hughes, the system can handle hundreds of tracks simultaneously. He declines, however, to give specific figures.

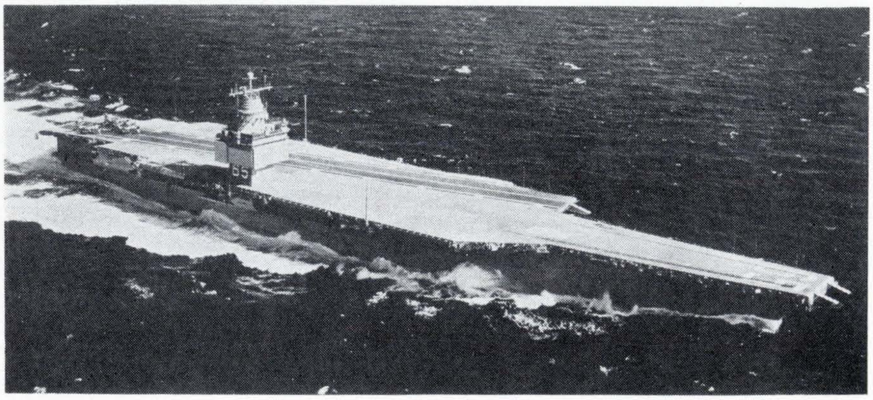
Display details. An NTDS installation has another display section which may include as many as 15 data utilization (DU) consoles. These units reproduce for battle commanders information supplied by the DI equipment through the computers and symbol generators. There are several dozen symbols, including alphanumerics, to provide detail on tracked objects. Operators can determine whether a target is surface, subsurface or air and whether it is friendly or unfriendly. If the craft in question is not hostile, symbols indicate whether it is engaged or ready for engagement. When an operator requests information for display, logic circuits within the console extract it from the computer's data flow by closing all but the appropriate gate.

Air controllers and the weapons officer have their own consoles to follow aircraft during battle. A plane in combat can be continuously monitored by DI consoles. Since the computer has been programed with data on each aircraft's fuel and ordnance supply before the engagement, it can furnish immediate information on reserves. The controllers can thus calculate quickly how much longer any given plane can stay in the air as well as its remaining ammunition by identifying the aircraft from its coordinates or by dialing its code number into a computer.

The display capability of the NTDS enables the weapons officer to analyze threats rapidly and decide on the best way to meet them. When the pertinent data has been presented, he can select shipboard missiles, aircraft or both.

II. All at sea

In an NTDS-equipped task force, an aircraft carrier flagship and perhaps four destroyer leaders coordinate operations. Each system ship transmits digital track data in a net-controlled, roll-call sequence to other vessels. The receiving warships correlate force track data with their own ship's data to make tactical decisions. The system automatically controls track reporting so that no two ships report on the same target. In the event that two systems are tracking the same target, computers screen the available inputs to assign a priority. The ves-



Enterprise is equipped with an NTDS that presents a comprehensive picture of ships, aircraft and submarines within range of the fleet's electronic sensors.

sel closest to the target receives top billing and its inputs are displayed on the DI consoles throughout the NTDS.

Consolidating gains. In the third-generation NTDS, the DI and DU consoles have been standardized into a single general-purpose unit which can handle both input and utilization functions. The new assembly will also incorporate an auxiliary display for amplifying alphanumeric data that cannot conveniently be presented by symbol encoding.

In the standardized version of the consoles, IC flatpacks will replace discrete solid state components. These modifications will not only simplify the system's configuration but also save the Navy money and space. The use of IC's will cut labor outlays, and since only one kind of production line is now required for the key display units, manufacturing economies have been obtained. The Navy has also reduced its cost by purchasing the system in volume over a three-year period. It had previously bought the NTDS on an annual basis. Hughes will not comment on the aggregate amount of dollar savings.

Another improvement in the upcoming NTDS is the provision for sonar inputs. Previous systems are presumed to have had an anti-submarine warfare capability but they could not plug directly into sonar sensors. The new configuration remedies the deficiency.

A summary console, with a 22-inch, flat-face, multiple-viewing display, which provides battle commanders with better-quality navigation data, is a completely new feature in the third-generation NTDS. It presents immediate information which is far more accurate than that obtainable from a manual, dead-reckoning tracer.

Finally, two standard cabinets will house the symbol generators, pulse amplifiers and sensor data converters that were installed separately in earlier versions of the NTDS. The sensor switchboards that enable console operators to change from one sensor to another are still discrete.

III. Behind the scenes

The most significant technical feature of the new NTDS, in Heebner's opinion, is its capacity to present sensor data interlaced with computer-generated data without degrading the accuracy of either.

Another major feature, according to John Molloy, Navy marketing manager at Hughes' Data Processing Products division, is that the system is entirely digital. "We make the digital conversion at the sensor end, and by switching all data into a common digital format, get a general-purpose display. This makes for greater accuracy and cuts out noise," Molloy reports.

While analog sweep signals may vary from one sensor to another, they are all converted so the displays will have only to handle a variety of digital pulse trains. If the conversions were not made at the sensors, each console in the system would have to incorporate electromechanical assemblies. This would tend to aggravate maintenance problems. The same techniques that have been successfully applied to radar and television inputs are now being used on integrating sonar.

IC's for logic. "The consoles have as much digital equipment in them as the average small-scale computer," Heebner says. The display, a one-gun cathode-ray tube, is actually digital because the beam's analog deflection amplifiers are driven by a series of digital pulses. In addition, digital data services both the computer and the display. Digital logic in each console converts operator actions into 30-bit words for processing by the computers. In the third-generation system, IC's are being used in the logic assemblies. The new NTDS is reportedly twice as reliable as its predecessors.

The NTDS represents something of an embarrassment of riches for the Navy. Basic hardware modifications would throw a huge investment in software overboard, so a gradual policy has been adopted on design changes. The Navy is now doing its own programing, and one reason for this, a Hughes man surmises, is that the service believes it is easier to teach a crewman programing than it is to teach a civilian programer military doctrine.

Multimission. Although originally a mobile air-defense system, the NTDS has been assigned a role in a flock of additional missions, including amphibious, electronic and anti-submarine warfare.

It's a fact! ITT Jennings has more experience in using the vacuum dielectric than anyone else in the world . . . and when it comes to high-voltage switching and control — any kind, any description — nothing else comes close to the compact size, speed and reliability of vacuum components.

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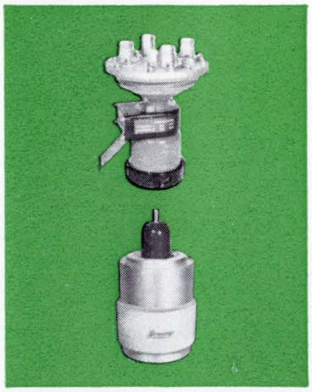
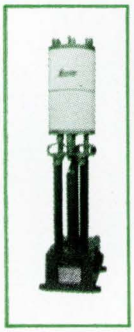
ITT Jennings probably already has a vacuum device to meet your reliability and size requirements; if not, no one is more experienced or qualified to find one. For information on any of the above vacuum components, or our complete catalog, write to ITT Jennings, a division of International Telephone and Telegraph Corporation, 970 McLaughlin Avenue, San Jose, California 95108.





WE'VE GOT PLENTY OF NOTHING

JENNINGS ITT

Numbers game comes to naught

Industry apathy has stymied the lengthy efforts of the Electronic Industries Association to register IC's

Robert Henkel
Washington regional editor

Attempts by the Electronic Industries Association to register integrated circuits have so far failed to get results. Although EIA officials talked of issuing type numbers for "several hundred" IC's when the registration program was announced in December 1965, not one circuit number with the 6N prefix for IC's has ever been put out. In fact, there is still no IC with a data sheet written to the EIA format. The latest word is that the first numbers "may" be issued sometime this year.

Registration is supposed to be the first step toward greater standardization of IC's. Nonstandardization, the reasoning goes, generally results in higher unit costs and a fragmented market, factors that make it difficult for IC customers to develop more than one supply source.

There has been some debate—but no real outcry—about the delay in the registration program. One reason for this is the absence of the kind of pressure exerted by the Pentagon to obtain registration of discrete semiconductor devices during the 1950's.

Edmund E. Farrell, marketing manager for Stewart-Warner Microcircuits Inc., a subsidiary of the Stewart-Warner Corp., thinks that the new policies of the Defense Department, together with the advent of large-scale integration, will work against the adoption of standardized circuits. One big argument for standardization, Farrell notes, is that with it, spare parts could be plugged into existing systems. But the Pentagon is no longer stockpiling components; it is banking on redundancy within systems and on throwaway modules. "The drive for standardization is a hangover from transistor days," says Farrell, adding that he hasn't been aware of any real pressure for it except from relatively unsophisticated buyers of IC's.

I. Industry: pro and con

The Lockheed Missiles & Space division of the Lockheed Aircraft Corp. buys large quantities of IC's but sees no real need for registration. The unit feels that technology is advancing so rapidly and new devices are being introduced so quickly that the EIA and suppliers are hard put to process data before it is outdated. Lockheed gets current specifications by going directly to the vendor. A staff engineer at the division suggests that the EIA shorten the registration period because better devices might become available in the interim.

"You certainly can't be opposed to standards," says Robert C. Baron, director of modular products at Honeywell Inc. But he sees problems in the question of which IC's and which specifications should be accepted. Obviously, he points out, there would be complaints from manufacturers who had to change their IC's to conform to standards that perhaps competitors had already met.

"If they try to specify the same level as for transistors," Baron says, "they'll have to overspecify or underspecify and hope that IC makers will fill in the gaps." Baron feels that the Government is the only agency able to force something like registration. He does, however, give the EIA full credit for motivation: "If by instituting standards, we're trying to guarantee that only a few types of IC's are in use, we'll fail. But if we're trying to guarantee that when a manufacturer and user sit down to talk, they talk on the same terms, then I believe that's a very good idea."

A funny thing. "A system—standardized in families by name or number—would be ideal because we could buy the entire slice to offer greater savings to our customers," says Edward Martin, product manager at the Microelectronics division of the Bunker-Ramo Corp., a custom packager of IC's. On the whole, however, the company hasn't found the lack of standardization a serious obstacle, he says, since its customers have usually chosen the type of chip best suited to their needs before coming to Bunker-Ramo. Nevertheless, Martin would still like to see metalization patterns and bonding diagrams of the chips in all IC literature. "It's a funny thing that manufacturers don't provide it," he says. "We need to know the size of the chip, what it looks like and how big the lands are before we try to use it."

On behalf of the manufacturers, Murray Siegel, industrial applications manager at the Fairchild Semiconductor division of the Fairchild Camera & Instrument Corp., puts matters this way: "Devices are moving forward at such a dynamic pace that by the time you have the information you would like to register, the device itself is a part of the passing parade. We come up with a new family about every six months and we just don't like to register obsolete data." Siegel says to those who urge standardization: "Baby, we can't even stand still; we're moving like a frog."

Fairchild takes the position that the knowledgeable user treats data sheets as a guide, and, after deciding on his requirements, goes to the vendor to negotiate individual specifications.

Seeing the situation in a some-

... it may be too late to implement registration of integrated circuits ...

what different light, R. Edward Shaut, product sales manager at the Transitron Electronic Corp., another manufacturer, comments: "We're all for standardization, but it may be too late to implement registration of IC's." He notes that some users have raised the question but that there has been no determined pressure for standardization.

"Obviously we are in favor of registration if it can be practically implemented," asserts Steve Levy, Motorola Inc.'s integrated-circuit department manager. "In fact we are pushing toward it, as evidenced by the number of our people serving on the EIA committees." However, Levy says the company's representatives can't recommend registration because so far there isn't a practical format of detailed recommendations.

II. Miscalculation

The fact is that the EIA and the industry—both circuit users and suppliers—greatly underestimated the complexity of the problems involved in registering IC's. New packages and higher-speed devices have arrived at a far faster rate than was anticipated by the association and its various committees.

After many months of debate, the first IC format was released in September 1965 by a committee of the Joint Electron Device Council. The EIA assumed control of this committee in January 1966 and the problem of IC registration was assigned to an engineering committee of the association's microelectronics subdivision.

Covering semiconductor integrated logic gating circuits, the first format provided an 11-page registration outline plus two standard test methods for measuring direct current and dynamic characteristics. "We attempted to provide a really clean format, a standardized method of presenting data, tests and parameters," says C. Everett Coon, the engineer running the registration program for the EIA. Expectations of rapid progress were at least partially based on the erroneous premise that IC's could be treated like discrete semiconductor devices, which required only a two-page format.

Aside from being lengthy, the format is also proving troublesome because it covers characteristics or descriptions for which IC suppliers often don't have information. Moreover, each firm presents its data differently.

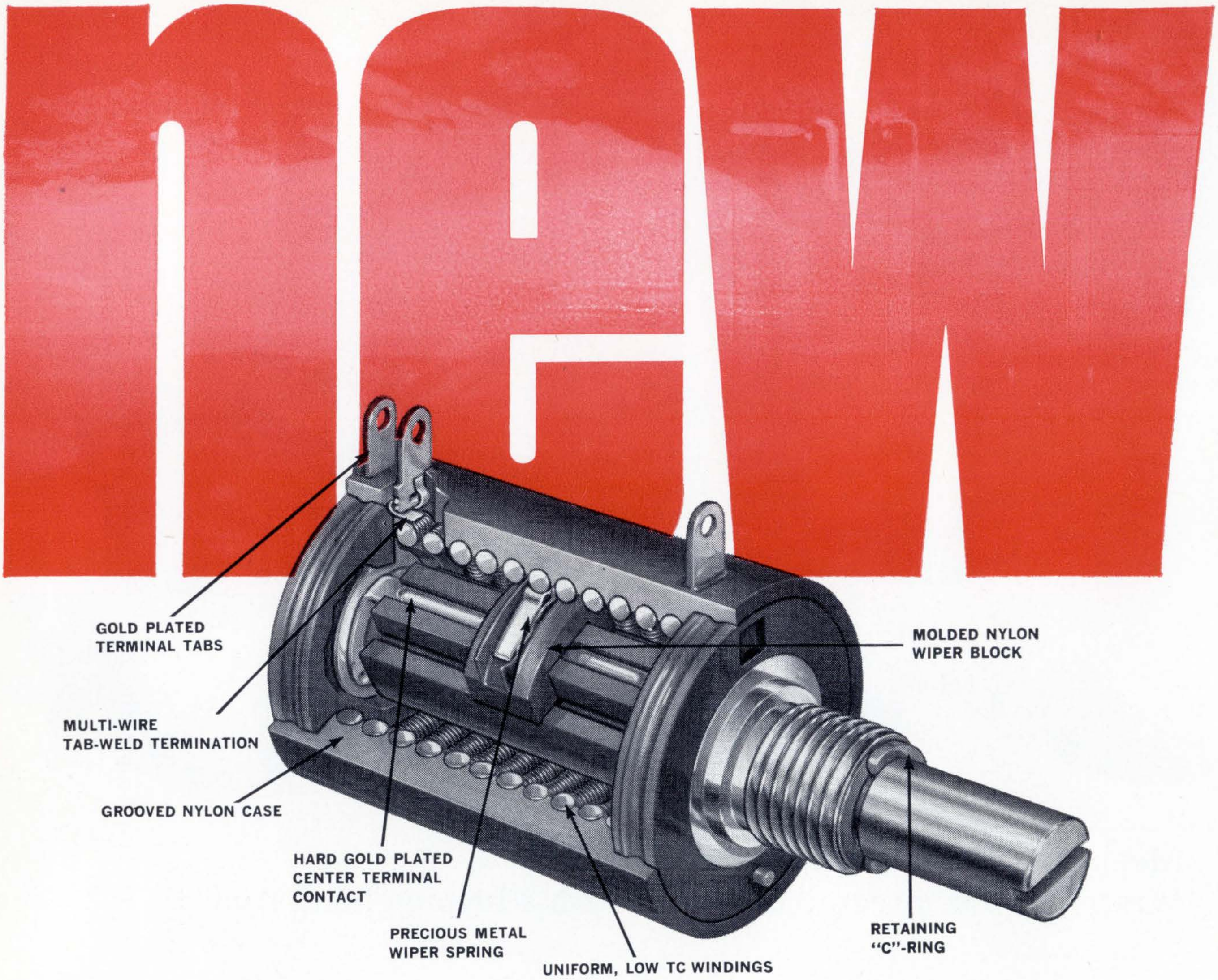
The upshot is that additional material, which some manufacturers feel is irrelevant, must be collected for registration. The EIA's procedure, developed by IC engineers with the cooperation of customers, is divided into two parts: the reservation of numbers, a four-month process; and registration, requiring one more month. Several manufacturers have reached the point where they need only complete the registration statement, Coon says. But no one has yet taken the final step. The two dozen or so letters received by the EIA asking for type-number reservations for IC's are, in Coon's opinion, trial balloons.

Second format. Another difficulty has been that the format for gating circuits covers only about 70% of all digital IC's. However, the association will soon issue a format covering bistable devices, which account for another 15% or so of the total number of digital IC's.

Also delaying progress is that fact that the registration system doesn't take into account company families of logic circuits. For the past nine months, the EIA has been studying a designation system that would be more appropriate for such groupings. But because many IC's are on the borderline between digital and nondigital categories, the association has shelved a tentative plan to use the 7N prefix for nondigital units.

Last October, the EIA released its first format for nondigital IC's—direct-coupled, open-loop amplifiers and operational amplifier circuits. Two more nondigital formats are close to being issued, Coon says, but "a multitude of them will be needed to cover the entire area."

Despite the delays, Coon is still willing to bet that type registrations for IC's will be released sometime during 1967.



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CAPSULE SPECIFICATIONS
IRC TYPE 8400

SIZE	⅞″ diameter
TURNS	10
POWER	2 watts @ 25° C
INDEPENDENT LINEARITY	±0.25%
TOLERANCE	±5%
RESISTANCE	100 to 100K Ω
END RESISTANCE	0.1% or 2 Ω (whichever is greater)

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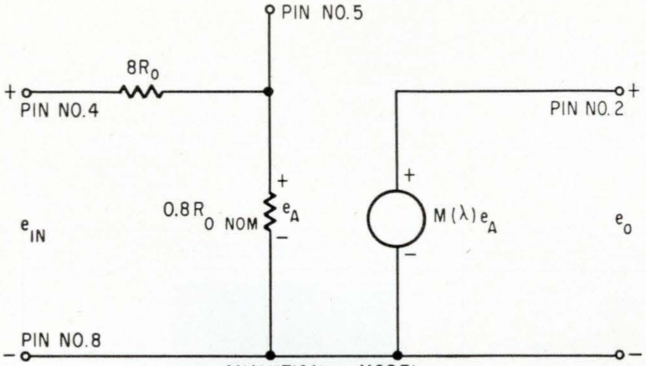
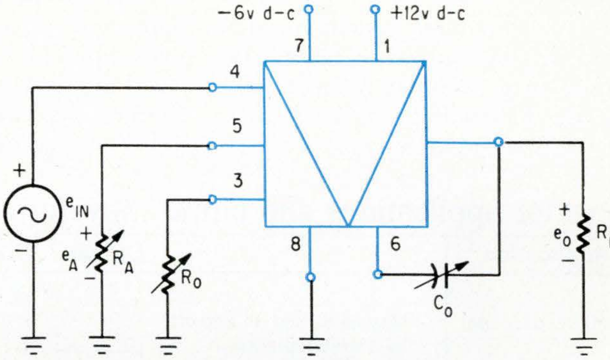
Synthesize your own active filter

External resistor and capacitor connected to miniature active resonator produce a wide variety of active filters



ANALYTICAL MODEL



MINACTOR CONNECTION DIAGRAM FOR COMPLEX POLE GENERATION

Design from scratch was once the rule for active filters. This was not only costly, but it was always a tedious time-consuming job that often produced unsatisfactory results. Now all an engineer has to do is decide on a filter configuration, reach for a new miniature eight-pin component, the Minactor, add a few external resistors and capacitors and he has a completely tunable low-pass, bandpass or high-pass active filter. Seventy-five percent of the synthesis, supplied in the form of a characteristic curve shipped with each unit, is already performed by the manufacturer, EG&G Inc., Boston.

The Minactor (for miniature active resonator) is a completely encapsulated unit that contains a thick-film resistor substrate, discrete capacitors for fixed frequency operation, and an integrated-circuit amplifier with eight transistors. Each device provides an independent pair of complex conjugate poles and a tunable Q in its voltage transfer function. The resonant frequency can be tuned externally with optimum results from 0.7 to 1.4 of the nominal resonant frequency. The Q of the device can be tuned from less than one to infinity (the condition for oscillation) at each frequency over the range of 0.25 to 4.0 times the nominal frequency of the unit. [Electronics, Jan. 23, 1967, p. 40.]

Each Minactor measures 0.8 by 0.6 by 0.2 inch and has a 0.1-inch spacing between pins. With 10 nominal units spanning the range of 100 hertz to 18 kilohertz, temperature-stabilized filters can be designed for operation at any frequency in the 70-hz to 25-hz interval.

The combination of resonator and passive components can provide low-pass, bandpass and

New products in this issue

New Products

high-pass filters; notch filters; low-frequency f-m modulators, low-frequency sine-wave oscillators, low-frequency automatic gain control for specific frequencies, low-frequency f-m demodulators or discriminators and complex pole-zero generators for elliptic filter synthesis.

In the equivalent circuit for the Minactor the output is equal to a function of frequency and a voltage e_A. The voltage e_A is a fraction of the input voltage and is not frequency dependent. When a frequency dependent voltage is desired it can be applied to pin 5. In one typical application, complex pole generation, an external resistor R_A is connected to pin 5 to attenuate voltage e_A. Resistor R_o, connected to pin 3, shifts the pair of poles from left to right in the s-plane and capacitor C_o shifts the poles up and down along the ωj axis. Pin 8 is a common ground.

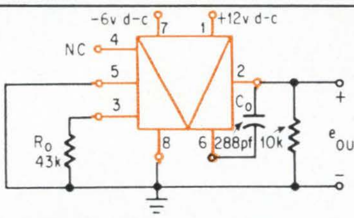
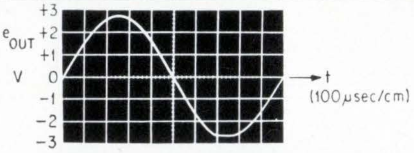
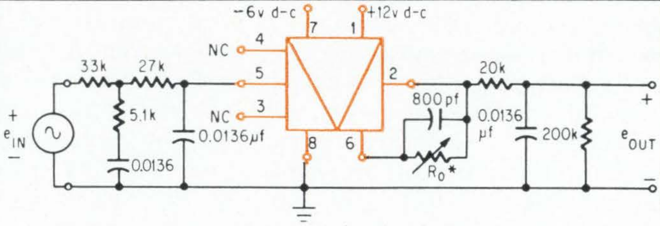
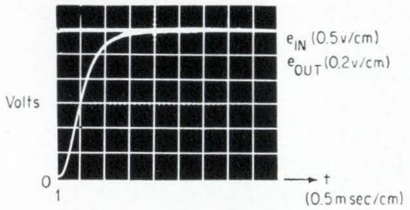
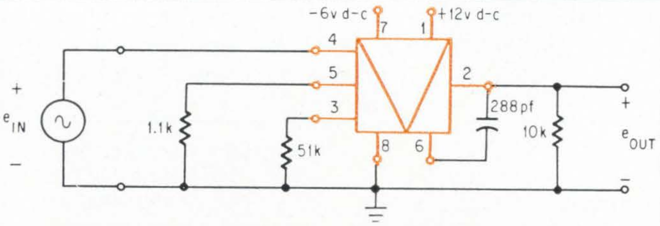
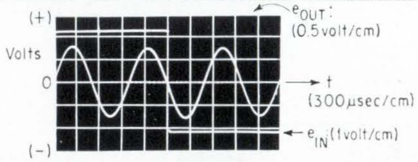
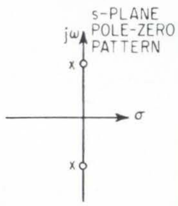
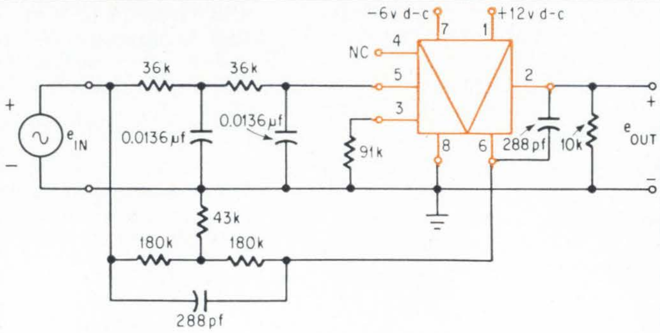
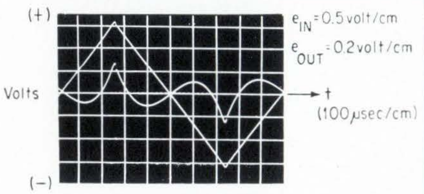
Other typical applications, together with appropriate component values and corresponding waveshapes, are tabulated.

Specifications

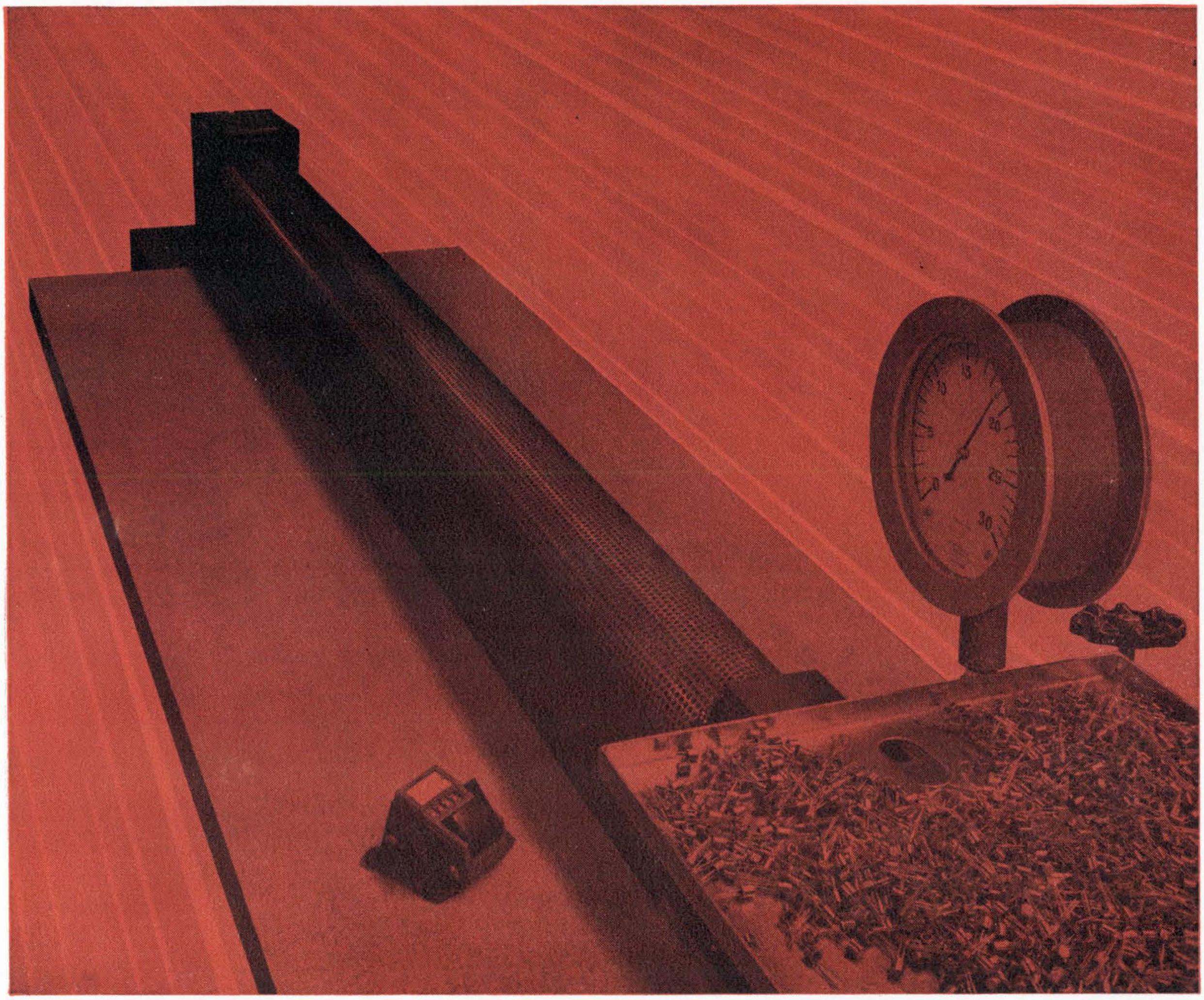
Bias supply	+12 volts d-c at 5 milliamperes −6 volts d-c at 5 milliamperes
Output maximum	2.5 volts rms to a 10 kilohm load
Short-circuit output noise	1 millivolt rms
Short-circuit d-c offset	±100 milivolts
Minimum peak gain	60 decibels
Price	$95 in quantities from 1 to 24
Availability	Off the shelf

EG & G Inc., Boston, Mass.
Circle **350** on reader service card.

Minactor applications and output waveforms

Application	Circuit	Waveshapes
1000-hz oscillator	May be turned on and off by a switch placed in series with R_0. 	 Waveshape is controlled by R_0 and the frequency by C_0.
Bessel, 3-pole low-pass filter	 Provides minimum delay and rise time in its step response function while maintaining zero overshoot for a given cutoff frequency. Cutoff was chosen at 500 hz. R_0 = 120 k, Bessel t_0 = 550 μsec or 200 k for t_0 = 500 μsec (shown)	 Optimum transient response is achieved by adjusting the Q of the unit.
Bandpass filter	 Circuit could be used in telemetry, spectrum analysis or whenever tone filtering is required. Cascading of circuits provides sharper selectivity. Q = 50 at 1000 hz.	 The bandpass behavior is demonstrated in the time-domain by passing only the 3rd-harmonic component of a squarewave input signal.
1000-hz notch filter (complex pole generator) 	 Circuit may be used to design elliptic filters (low-pass or bandpass), notch filters or unbalanced all-pass networks. Both the pole and zero are identically adjustable.	 The notch filtering is shown in the time-domain by the rejection of the fundamental signal in a triangular waveform, leaving the total harmonic content of the input signal.

The Predictables.



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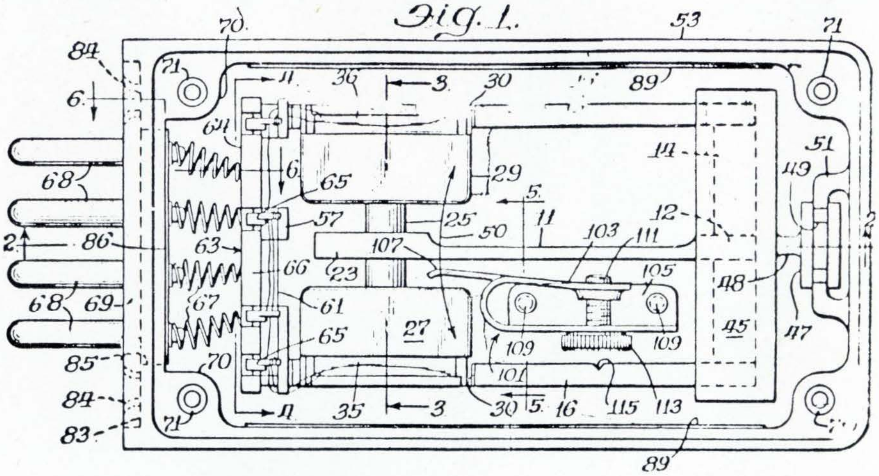
Contacts dropped from resonant-reed relay

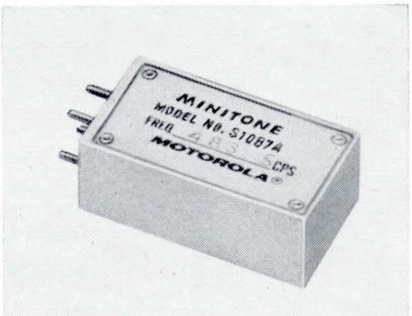


In a contactless resonant-reed relay, reed 11 has a magnet 25 mounted on its end which vibrates at the resonant frequency through the two coils 35 and 36 (input and output). The Q of the device may be adjusted by inserting conducting sleeves of varying thicknesses inside coil bobbins.

The resonant-reed relay is the backbone of selective tone-signaling systems used in telemetry, industrial controls and remote alarms. But the chore of continually replacing corroded contacts on most resonant reeds has been a constant irritation to users. Although at least one other company has already announced a contactless reed relay, this new unit from Motorola Inc. appears to have a major edge. The unit is covered by Motorola's patent No. 3,221,120, granted on Nov. 30, 1965.

Motorola Communications division, the manufacturer, has been using the unit in its own systems since 1965. The company has now decided to go commercial with the "Minitone," model 51087A, available from stock at a price of $20.

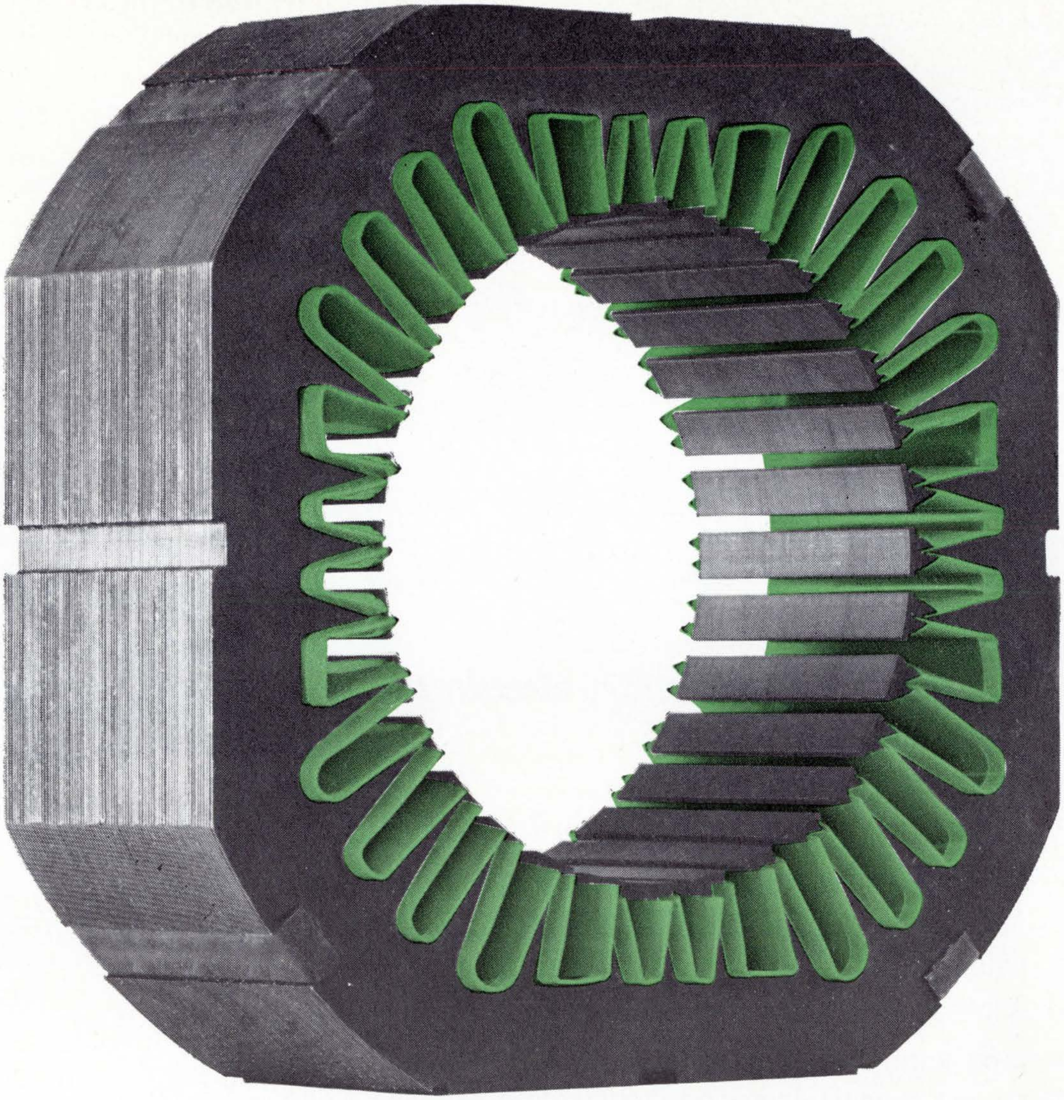
The Minitone, with 207 different units, covers the frequency range of 67 to 3,150 hertz. The all-important frequency tolerance is ±0.1%, for units between 67 and 230 hz and is ±0.05% for units between 230 and 3,150 hz, which is somewhat better than the ±0.15% tolerance announced for the competing unit.



Specifications

Frequency range	67—3,150 hz
Frequency tolerance	±0.1% (67-230 hz) ±0.05% (230-3,150 hz)
Temperature stability —30°C to 100°C (25°C ref.)	±0.05% (230-3,150 3,150 hz) ±0.00075%/°C (230-3,150 hz)
3-db bandwidth	1 hz at 67 hz 3 hz at 3,000 hz
Coil resistance	400 ohms
Nominal input	0.4 v rms below 230 hz 0.75 v rms above 230 hz
Nominal input power	0.2 mw below 230 hz 0.7 mw above 230 hz
Size	1.114 x 0.619 x 0.343 in.

The relay operates on a simple principle: a permanent magnet attached to the end of the resonant reed vibrates through the center of two coils, input and output. When the input coil is energized at the proper frequency, the coil drives the reed and magnet, which in turn sets up a voltage in the output coil at the resonant frequency of the reed. A well-shaped sinusoid is thus delivered to the output circuit for any control purpose. The unit



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Two-Speed, General-Purpose ⅓ HP	($1.40)	($1.20)	but	$0.08	$0.13

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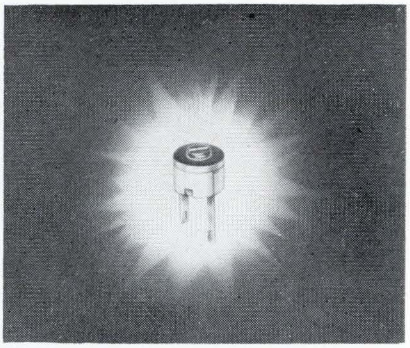
New Components

may also be used as a tone generator.

Motorola Inc., Communications Division, 4900 W. Flournoy St., Chicago, Ill. 60644 **[351]**

Trimmer capacitor occupies small space



A precision trimmer capacitor, the 518, features 5 to 25 pf capacitance range and occupies less than 0.007 cu in. Diameter is 0.218 in. The unit is rated at 100 w v d-c 85° C and 50 w v d-c to 125° C. It operates efficiently in the temperature range of −55° to +125° C and has a dielectric strength of 200 v d-c to 1 to 5 seconds.

The high capacitance-to-volume capability of the 518 is made possible by the Monobloc process, whereby ceramic film dielectrics are fired into solid structures of one or more layers, yielding high-performance, monolithic dielectrics.

Erie Technological Products Inc., 644 West 12th St., Erie, Pa. **[352]**

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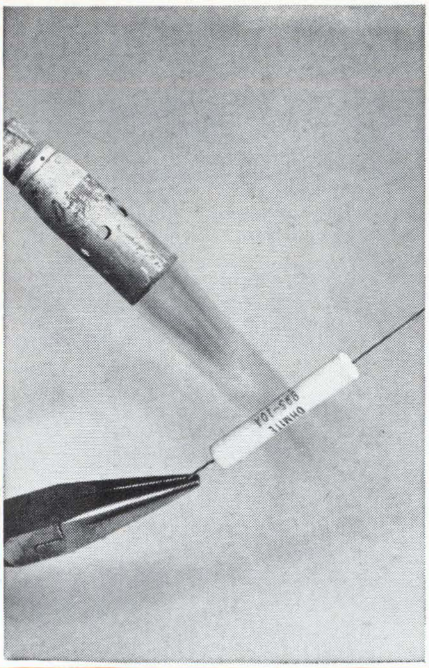
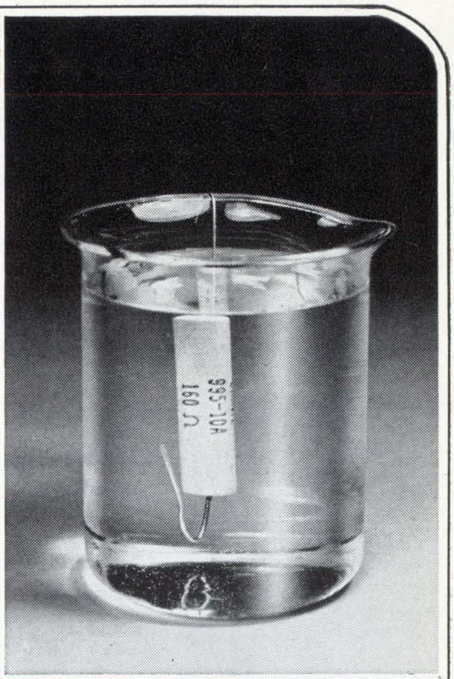
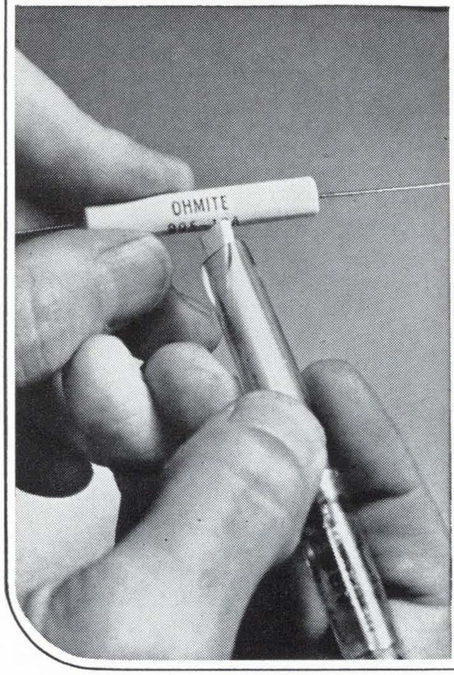
Over-all dimensions are as small

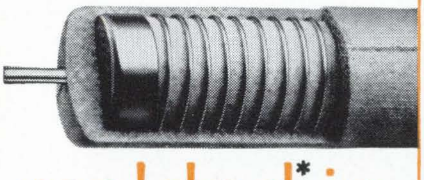
any other resistor would holler UNCLE...





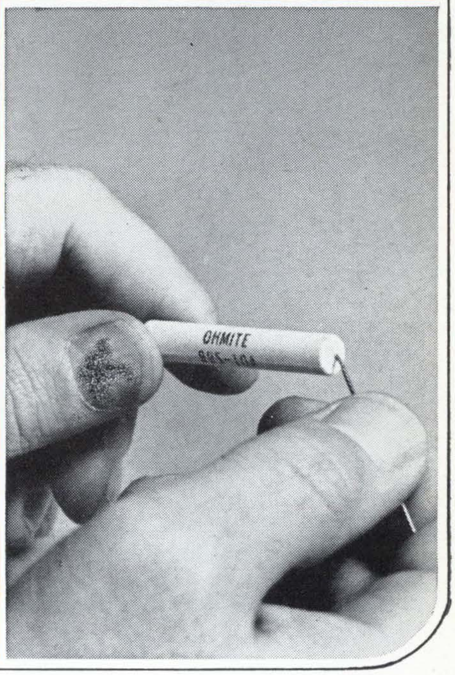


but not the "99"



molded* in vitreous enamel

*Patent No. 3,229,237



The Series 99 is the resistor that won't soften or deform at a cherry-red 1500°F . . . that clings to its markings like a leopard to its spots against the onslaught of solvents, abrasion, and extreme overloads. This is the resistor that laughs at abuse because of its tough, exclusive "molded" coating of vitreous enamel. This is the resistor of such uniform shape and size that metal clips can hold it securely and also provide a big increase in heat dissipation.

No wonder design engineers throughout industry are hollerin' for the resistor of incomparable performance—the Series 99, molded in vitreous enamel.

Series 99 is supplied in commercial, MIL-R-26, and close tolerance types. *Commercial units are stocked in 5 sizes and 146 resistance values.*

WATTAGES (COMMERCIAL): 1.5, 2.25, 3.25, 5, 6.5, 9, 11 watts at 25°C.

RESISTANCE RANGE: 0.1 to 187K ohms.

TOLERANCES: 0.25% to 5%

TEMPERATURE COEFFICIENT: 0±30 ppm/°C at 25°C to +350°C for 10 ohms and above.

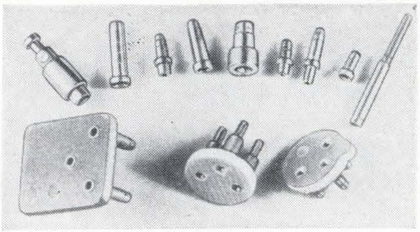
Write for Bulletin 103

RHEOSTATS • POWER RESISTORS • PRECISION RESISTORS • VARIABLE TRANSFORMERS • RELAYS TAP SWITCHES • TANTALUM CAPACITORS • SEMICONDUCTOR CONTROLS • R.F. CHOKES

OHMITE

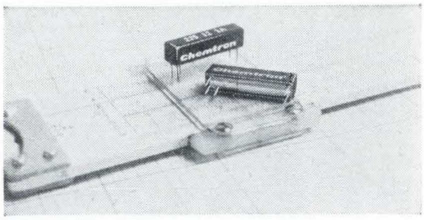
MANUFACTURING COMPANY
3610 Howard Street • Skokie, Illinois 60076
Phone: (312) ORchard 5-2600

New Components



as ¼-in. high and ⅜-in. diameter. All contacts are machined beryllium copper, hard gold plated. Sockets are available with straight terminals for dip-soldering with turret terminals for soldering in a pot, or with terminals to be riveted. Body material is normally G-10 glass epoxy. Leads may be any length from 0.125 in. upwards.
Robinson Nugent Inc., 802 E. Eighth St., New Albany, Ind., 47150. [353]

P-c reed relays offer speed, small size



Printed circuit reed relays with a switching time of less than 0.5 msec (including bounce) are suited for aerospace and computer applications. The relay measures 0.8x0.2 in., has 0.1-in. pin spacing and simplifies p-c board layout. Direct p-c mounting eliminates the changes in reed characteristics resulting from cutting and bending axial-type leads.

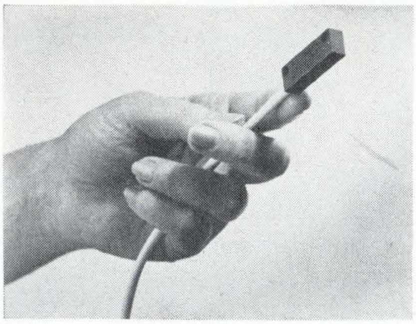
To form an integrated assembly, the mounting pins are welded to the reeds and the relay is vacuum-encapsulated in epoxy resin. Voids in the encapsulant and stresses on reeds and mounting pins are eliminated during manufacturing. Automatic soldering does not change reed characteristics.

The reed's electrostatic shield minimizes coil-to-reed capacitance for low-loss switching of r-f or low-level a-c signals. A magnetic shield prevents erratic operation when the

relay is near another relay or in a magnetic field, and also serves as a protective housing. The spst contact rating when normally open is 250 ma at 250 v max into a noninductive load. A 12-v coil is standard. The Chemtron 225 relay is designed to withstand rugged environmental conditions.

Self-Organizing Systems Inc., Box 9918, Dallas, Texas, 75214. **[354]**

Switch can sense without touching



An inexpensive a-c/d-c magnetic proximity switch checks, counts and positions moving devices with high reliability. When operated within specified tolerances the permanent-magnet device has a life of many millions of operations.

Designated model 01041, the $1\frac{15}{32}$ x ½ x $\frac{5}{16}$ in. switch is easily installed in any position behind any nonferrous shield. It accurately detects the presence of a specific magnetic body at a predetermined distance from a reference point. Repeatability is ±0.002 in. Unaffected by shock and vibrations up to 50 g's, the encapsulated switch will operate while immersed in any fluid or under pressure and is not affected by dirt, grease, oil, paint sprays, or other contaminating substances.

Available off the shelf in both the normally-open and normally-closed positions, the switch can be used on liquid level devices, measurement control equipment, machine tools, counters, material handling equipment, electrical interlocks, positioning controls, or industrial processing equipment.

The switches are normally sup-

For those who think big—about availability, that is. Babcock's 1/6-size Model BR10 with unique universal contacts gives you "nonstop" load performance dry circuit to 1 amp. in the same unit. Now, you can order *one* relay to meet all your high-density circuit-board requirements—at no cost premium. And you'll find that this subminiature unit has everything... MIL-R-5757 conformance, unitized construction, solder-sealed or welded versions, standard circuit-board grid pattern, and a wide choice of terminal and mounting styles. Get more information about the BR10, and the complete Babcock line of relays, all with universal contacts. Write Babcock Relays, Division of Babcock Electronics Corp., 3501 Harbor Blvd., Costa Mesa, Calif.; (714) 540-1234.

SPECIFICATIONS

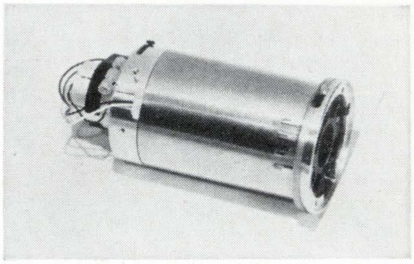
SIZE: .405″ h. x .500″ l. x .230″ w.	PULL-IN POWER: Low as 80 mw.
WEIGHT: Approx. 0.15 oz.	LIFE: To 150,000 operations
CONTACT ARRANGEMENT: DPDT	TEMP. RANGE: —65° C + 125° C

Babcock model BR10 1/6-size relays

dry circuit to 1 amp universal contacts

plied with 18 inches of insulated flexible cable. Price is $4.20 each.
Electro-Tec Corp., Box 667, Ormond Beach, Fla., 32074. **[355]**

Deflection assembly handles many vidicons



All vidicon tubes that have 40-gauss fields will work well with a new 1-inch deflection assembly.

The assembly includes a yoke, focus coil and an alignment device and offers full adjustment of individual components included within the assembly. The adjustments are: locking rotation of the yoke within the focus coil, forward and reverse positioning of the yoke, centering bushing and tube within the focus coil and adjusting and removing vidicon face mask.

Other features include four insulated feed-throughs for passage of the remote control leads of the lens from the face of the camera and deflection assembly for ease of installation. The yoke is felt-padded.

Lake Electronics Inc., 3311 Perkins Ave., Cleveland, Ohio, 44114. **[356]**

Plastic cable ties secure wire bundles

One plastic cable tie replaces three older types. Two versions, TY-55 and TY-55M, are for securing wire bundles to places where breakouts from the main bundle are made. The ties are preformed and can easily be positioned and secured around the branching wires, producing a figure eight. Previously, three separate ties were required to fasten the bundle at this point.

Both ties are fabricated of nylon

Westinghouse 0.5 to 820 amp rectifiers keep everything from TV sets to locomotives competitive into the 1970's

TV sets and locomotives have one thing in common—both need top quality silicon rectifiers with competitive price and performance.

TV rectifiers must withstand repetitive surges, be highly reliable, yet low in cost. The new Westinghouse 1N4816 series, rated at 1.5 A. half-wave average at voltages to 1000 V., meets the need. It offers plastic economy with metal case performance for TV, Hi-Fi, and other consumer applications. Exclusive manufacturing techniques insure hermeticity. Replaces 1N536, 1N1217, similar rectifiers. Price of 400 V. (1N4820) unit in 1000 quantity: only 30¢.

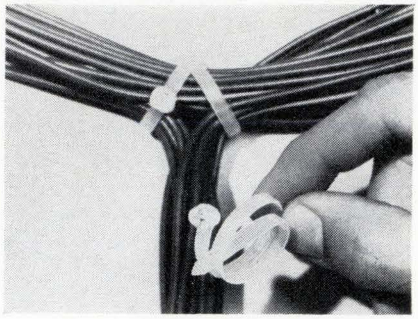
The new Westinghouse Type 790 rectifier, rated 240 A. at 2400 V. allows upgrading of diesel-electric locomotive performance. Alternator rectifiers must provide 3500 KW under conditions of heat, cold, dirt, and overloads. The 790 rectifier meets this requirement. Exclusive Westinghouse Compression Bonded Encapsulation makes it immune to thermal fatique and rugged enough for railroad service.

Anywhere between these extremes, Westinghouse has advanced-performance rectifiers for your application—low, medium, or high power; standard and high speed. High voltage stacks and potted assemblies are also available in most ratings. And most have the unique Westinghouse Lifetime Guarantee identified by this symbol ✤ on the case.

Get data now. Call your Westinghouse distributor for a copy of our Semiconductor Condensed Catalog. Or write to Westinghouse Semiconductor Division, Youngwood, Pa., 15697.

✤ Westinghouse warrants to the original purchaser that it will correct any defect or defects in workmanship, by repair or replacement f.o.b. factory, for any silicon power semiconductor bearing this symbol ✤ during the life of the equipment in which it is originally installed, provided said device is used within manufacturer's published ratings and applied in accordance with good engineering practice. This warranty shall constitute a fulfillment of all Westinghouse liabilities in respect to said products. This warranty is in lieu of all other warranties expressed or implied. Westinghouse shall not be liable for any consequential damages.

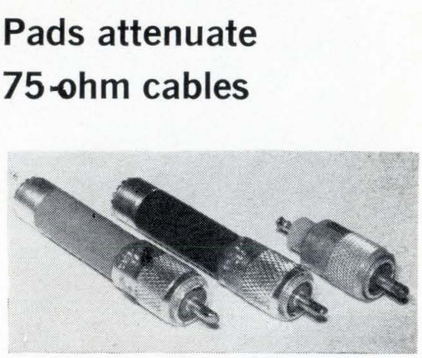
You can be sure if it's Westinghouse



with maximum wire bundle diameter of ¾ in. The TY-55 is twist-locking. Installation is with a Ty-Rap tool, as follows: position the tie around the bundle, thread the tip through the eye, twist and cut off. The TY-55M is self-locking and features a stainless steel tooth, mounted in the eye, that is designed to lock the tie at any given diameter.

The Thomas & Betts Co., 36 Butler St., Elizabeth, N.J. 07207. **[357]**

Pads attenuate 75-ohm cables



Coaxial attenuator pads have been designed for tv and radio broadcasting. The barrel of the attenuator pad is color coded according to the attenuation of the particular pad.

Type AN connectors are normally supplied and the standard impedance is 75 ohms, for attenuating 75-ohm cables.

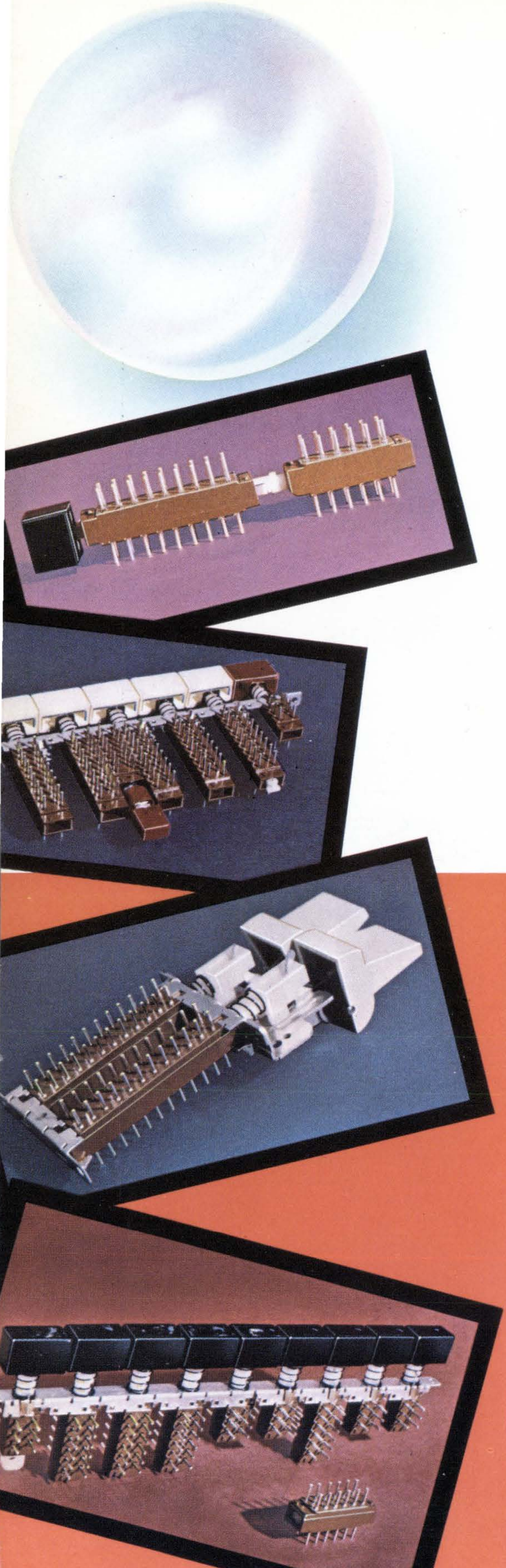
The units are 3⅝-in. long including connector and ⅝ in. in diameter. Pads are available with either 3-db or 6-db attenuation.

A 75-ohm termination is also available with a test point.

Price of the 3-db and 6-db pads is $10 with three weeks delivery. The terminations are $5 each with two-week delivery.

Fairlane Electronics Inc., Box 335, Long Valley, N.J., 07853. **[358]**

Centralab push button switches* will revolutionize your switching designs



New from Centralab! A low-cost push button switch that's small, easy to wire, easy to mount and twice as versatile as any you now use!

PRICES are competitive with multiple position rotary types for many applications, much lower than other push button switches. And our new modular design facilitates same day price quotations.

SIZE of these new switches is so small that there's room to spare in printed circuit or conventionally wired chassis. Centerline spacings are 25/64″ (Model 10), 19/32″ (Model 15) and 29/32″ (Model 20).

VERSATILITY is exceptional. Switch action may be momentary, independent, push-push, row latching or even a combination of these anywhere in the same row! A zero block which releases the other blocks from the latching assembly is also available. Each switch can have two, four, six or eight double throw functions and a ganging arrangement permits up to 14 pole double throw action when required. Up to 19 switches may be ganged side-by-side on the same mounting bracket! A rear coupling is available for any switch. A line switch can be included in the assembly.

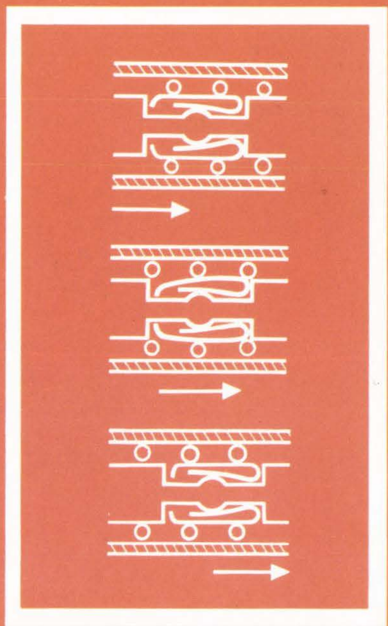
WIRING is particularly easy. Use standard dip or wave soldering methods with printed circuits. You can also make connections to the OTHER side of the switch with a pc board! In wired chassis, the design permits easy hand wiring and is ideal for automatic wire wrapping.

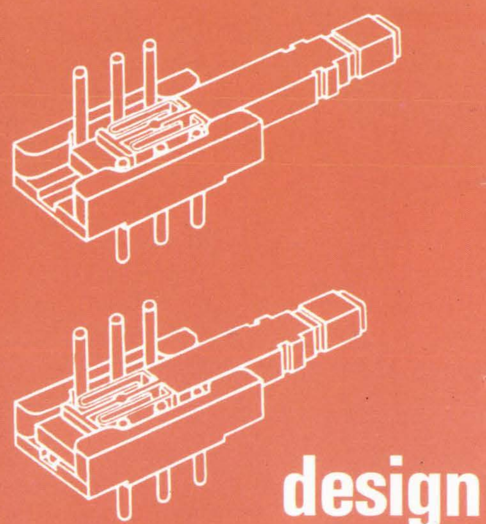
MOUNTING is simplified because Centralab provides a complete family of integrated hardware. Typical is a low-labor-content tab lock front mounting bracket.

Find out how you can revolutionize your designs with push button switches by writing to Centralab, The Electronics Division of Globe-Union Inc. at 5757 North Green Bay Avenue, Milwaukee, Wisconsin 53201.

CENTRALAB

ELECTRONICS DIVISION
GLOBE-UNION INC.





design principles

Centralab's new push button switches are completely machine-made of injection molded plastic. Even the contacts are inserted automatically for machine-sure quality control.

The unusual contacts provide excellent wiping action for electrically reliable performance. Their mechanical configuration assures even pressure on both fixed contacts, eliminates local high stress points in the contact for long failure-free life. The sketches show the simplicity and self-aligning characteristics.

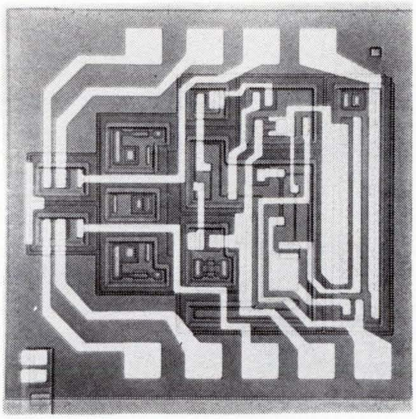
Smooth switch action is assured by the low friction plastic slider which holds the moving contacts. The switch body completely encloses the switch contacts for protection from solder and dust.

P-6615

*Isostat licensed.

For additional information circle number 125

Built-in sensors stabilize IC



A pair of temperature-sensing transistors built into the chip help stabilize Fairchild Semiconductor's μA726 monolithic preamplifier. The result is a device that tracks extremely well. The temperature coefficients for offset voltage and offset current are 1 μv/°C and 30 pa/°C, respectively. The 45-mil-square silicon device contains a matched differential transistor pair and a substrate "heater."

The heating function is achieved by adding the emitter-base voltages of the two sensing transistors, then applying the resulting voltage across a resistor. The current through the resistor, which is inversely proportional to the chip temperature, is amplified through the two transistors, one of which is a high-power device. Power to heat the substrate is dissipated at the collector-emitter junction of the second transistor. A maximum of 1.5 watts can be sunk into the chip, which reaches a stable temperature in under 1 second as a result of its good thermal characteristics and small size. Average heating power runs about 250 milliwatts.

Engineers at Fairchild, a division of the Fairchild Camera & Instrument Corp., say the temperature sensing elements are centrally located in a unique circuit design and layout. The heating transistor is on one side of the die and the differential pair on the other; both are produced by the planar process.

The new device comes in two versions: μA726 is guaranteed over the full military temperature range and μA726C is guaranteed over a 0°C to 85°C range.

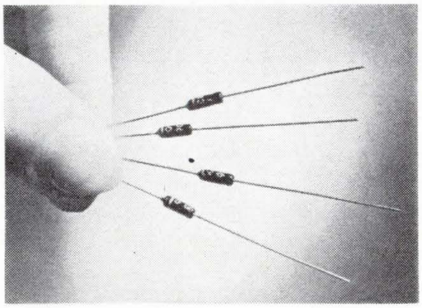
Selected units can provide an offset voltage as low as 0.1 μv per °C. Frequency response is about 70 Mhz. The unit, aimed at operational amplifiers and instrumentation, provides stable gain for signal levels under 100 μv. The devices are available from stock in prices ranging from $12.50 to $37.50, depending on temperature range and quantity.

Specifications

Temperature coefficient	
Offset voltage	1 μv/°C
Offset current	30 pa/°C
Power dissipation	250 mw (min)
Frequency	70 Mhz
Noise	4 μv peak-to-peak
Long-term stability	5 μv/week
Temperature range	−55°C to 125°C (μA726) 0°C to 85°C (μA726C)

Fairchild Semiconductor division, 313 Fairchild Drive, Mountain View, Calif., 94040. **[361]**

Silicon diodes rated from 1 to 5 kv



Avalanche silicon glass diodes having ratings from 1,000 to 5,000 v are available in a DO-7 package.

The MD100 series can deliver up to 50 ma from 1 kv to 5 kv and up to 100 ma from 1 kv to 4 kv. Units are designed to operate in ambient temperatures of −65° C to +150° C with reverse current ratings of 1 μa maximum at 25° C, and 10 μa maximum at 100° C provided they are operating within their rated peak inverse voltage. The avalanche voltage at 50 μa d-c is a minimum of 20% above the rated peak inverse voltage for all types.

Atlantic Semiconductor Inc., 905 Mattison Ave., Asbury Park, N.J. **[362]**

Half-ampere, h-v npn transistors

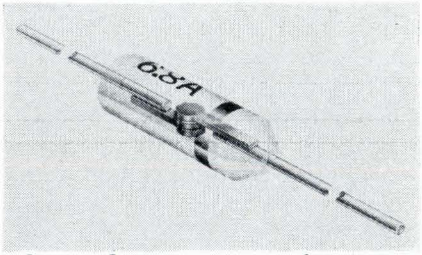
Claimed to be the only ½ amp npn silicon transistor having a rating above 500 v, a new transistor is listed as capable of withstanding 800 v. The device has a beta of 15 (minimum) at a collector current of 500 ma and a collector-emitter voltage of 10 v. It has a beta of 30 (minimum) at a collector current of 250 ma and a collector-emitter voltage of 10 v. The collector-emitter saturation voltage is 2 v maximum at a collector current of 250 ma and a base current of 25 ma.

The gain bandwidth product is 25. Power rating is 15 watts.

The unit is available in both the TO-5 and MD-14 packages.

Industro Transistor Corp., Long Island City, N.Y. **[363]**

Small zener diode power-rated at 1 watt



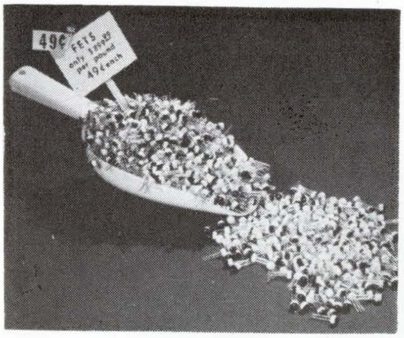
Advanced construction of a 1-watt zener diode provides a smaller package than was previously offered as a ½-w power-rated diode. The silicon wafer is aligned between two parallel, offset tantalum heat sink tabs instead of in a typical nailhead design, which places the fracture plane of the junction in the direction of lead tension.

Many such nailhead designs employ soft silver leads to reduce the strain, but this in turn destroys the moisture barrier when the soft leads extrude under tension. T new design incorporates gold-plated nickel leads welded to the tantalum tabs. These leads do not extrude, and the long, bidirectional leakage path assures positive moisture protection. The body is high-pressure molded and has a banded and tapered cathode. The diode is 0.160 in. in diameter x $\frac{7}{16}$ in long. Lead lengths are 1⅛ in.

The 1-watt zener is available in 1%, 2%, 5%, 10% and 20% tolerance units, and in 21 voltages from 2.4 to 16.

Price is 32 cents each for 10% tolerance diodes, in lots of 1,000.
Schauer Manufacturing Corp., Cincinnati, Ohio, 45242. [364]

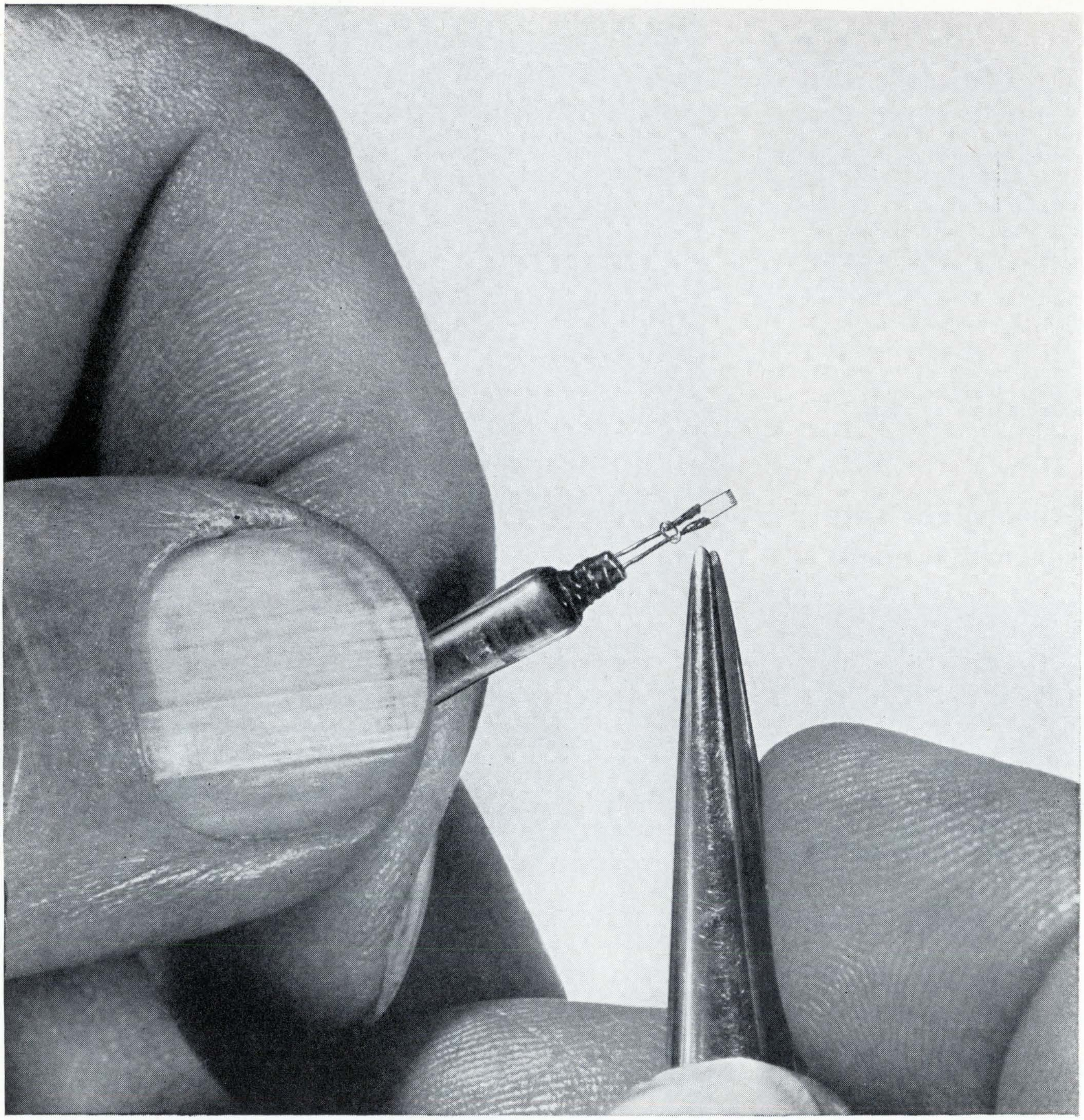
N-channel FET's are economically priced



Epoxy-encapsulated n-channel junction FET's are designed for industrial and consumer applications including amplifiers, choppers and variable resistors. The E100 series offers low leakage (10 picoamps at 20 v) and low noise figure (1.8 db typical at 1 megohm, 10 hz).

Other characteristics include 50 v typical gate-source breakdown voltage, and a 5:1 drain current (I_{DSS}) and pinch-off voltage spread for types E101, 102 and 103. The E100 is a more loosely specified lower cost version. Maximum reverse transfer capacitance is 3 pf. The TO-18 lead configuration makes this series mechanically interchangeable with many other FET's without need for new sockets.

The E100, 101, 102 and 103 are priced at 49, 92, 74 and 60 cents each, respectively, in quantities of 1,000.
Siliconix Inc., 1140 W. Evelyn Ave., Sunnyvale, Calif., 94086. [365]



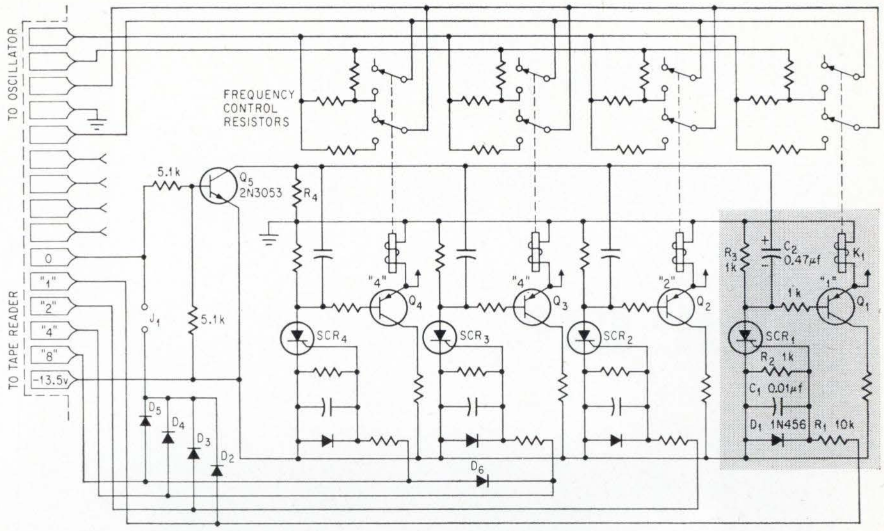
ENGELHARD platinum wire is best for H. Boehm & Co. miniature lamps.

H. Boehm & Company makes miniature lamps as small as 1/16 of an inch in diameter and 1/4 of an inch long for delicate surgical instruments. The electrical connections in these lamps are made of Engelhard platinum wire only .005" to .007" in diameter. The reasons for selecting this material are: platinum has a high melting point and excellent electrical conductivity.

Making reliable lamps from hair thin platinum wire is precise business. The platinum wire is pounded flat on one end and drawn through a die that fastens the flat end into a small tube. Then the wire is cut to an average length of 5/16 of an inch. Two wires are fastened together with a small glass and a tungsten filament is inserted into their tubes. Finally the wires are sealed in hot glass. Since platinum and glass have the same heat expansion rate, the seal remains perfect. This is absolutely necessary for maintaining the high vacuum in the lamp.

Engelhard, a leader in precious metals, is always searching for new and better applications to improve almost any product or process. For help with your metallurgical problems, write Engelhard: *the company that is working wonders with the wonder-working metals!*

Programer with simple touch



In the scr-operated transistor relay driver for one decade in Krohn-Hite's programable oscillator, a signal from an input terminal, for instance terminal 1, is coupled to the scr's gate, in this case through R_1 to SCR_1. This forces Q_1 to conduct and energize K_1. Resistor R_2 in the scr's gate circuit prevents charge accumulation that would lead to the false firing of SCR_1. Diode D_1 protects the associated scr from an improperly polarized pulse. Q_5 inhibits all conducting scr's to cause automatic reset. An input from terminal 8 is coupled simultaneously to SCR_3 and SCR_4 to produce the desired 8. The diode D_6 prevents a 4 input from energizing SCR_4.

A programer originally designed as an integral part of an oscillator may prove to be more marketable than the oscillator itself. The Krohn-Hite Corp. reports its programer has several advantages that ideally suit it for applications that require converting binary-coded decimal inputs to relay closures.

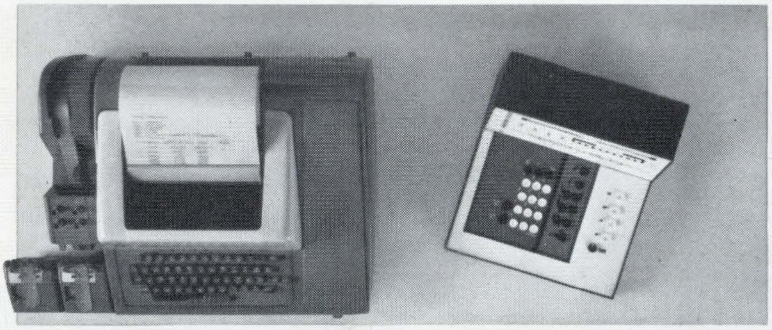
Krohn-Hite's device consists of sets of transistor relay-driver circuits operated by silicon controlled rectifiers. Momentary low-current relay closures in a bcd format, such as those derived from a punched-tape reader, are all that is needed to activate the circuit. The output can be either relay contact closures or the transistor driving current itself.

Among the advantages that accrue from replacing conventional relays with the scr-operated circuits are the three-in-one function of circuit isolation, latching and automatic reset. Since the only input information necessary is in the form of short-duration switch closures, a tape programer may contain much more information in a given space. And since no reset command is necessary, programing is less complex.

In their normal state, the scr's are off. An input, such as the momentary closure of a tape-reader contact, triggers the associated scr on. When the scr conducts, the transistor also is turned on and the relay is energized. When used in the company's oscillator, the relays switch resistances in and out of the oscillator's frequency-controlling RC networks. Since the scr's are d-c powered, they remain on once triggered, providing inherent circuit latching.

To reset the circuit—in selecting a new frequency, for example—the scr's gate control must be reestablished. This is accomplished by an automatic reset circuit in the programer that responds only to the start of the next frequency digit block on the tape. If the next frequency requires a different complement of relay closures, the unused scr's will be turned off but those needed for the new frequency will be left on since the on-command overrides the reset function.

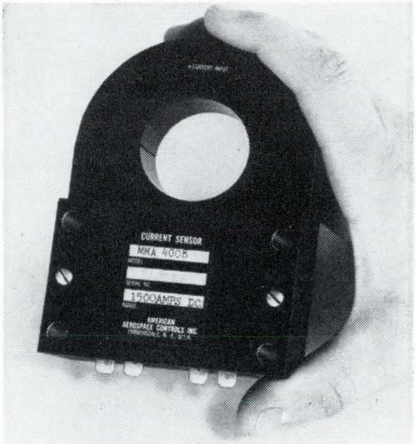
Krohn-Hite's programer is avail-



able with or without relays. When it was used in the oscillator, for example, the relays isolated the sensitive RC circuits from the inconsistent impedance levels among the semiconductor circuits in the driver in addition to performing the switching function. The programer can be supplied with a straight binary code or variations of the bcd scheme. It will sell for about $500, depending on whether or not the relays are included and the code scheme used.

Krohn-Hite Corp., 580 Massachusetts Ave., Cambridge, Mass. 02139 **[366]**

Current sensors clamp around cables



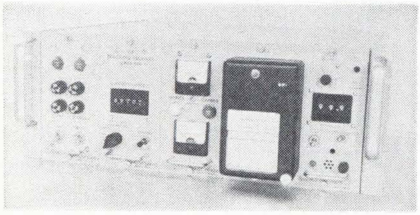
Solid state transducers use magnetoresistors to detect d-c current in ranges from 0 to 100 amps to 0 to 10,000 amps. Designated type 4008, these current sensors have applications in industrial and military applications requiring the measurement and control of large d-c currents without breaking into the current carrying cable. The sensor features a removable yoke that can be clamped around cables up to 1½ in. in diameter.

There is complete electrical isolation between the current in the cable and the sensor output, allowing the sensor to be used safely with high potential lines. The device will accurately respond to current spikes as fast as 200 μsec.

Output from the sensor is a d-c voltage suitable for remote transmission or meter indication. The sensor requires a nominal excitation voltage of 24- or 28-v d-c but will operate accurately over an 18- to 36-v supply since voltage regulation is incorporated within the device.

Price is $225 each in lots of one to nine and delivery is four weeks. American Aerospace Controls Inc., 129 Verdi St., Farmingdale, N.Y. **[367]**

Phase tracking receiver operates on vlf band



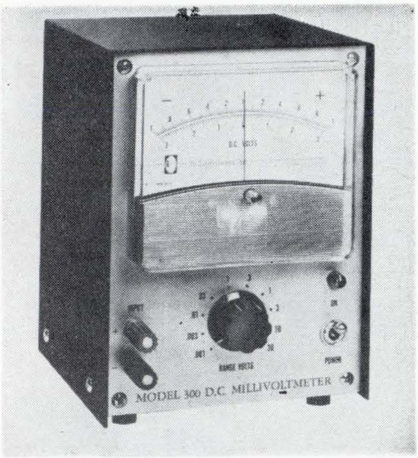
Continuous tuning from 3 kilohertz to 99.95 khz, in 50 hz increments, is provided by the model 599J very-low-frequency phase tracking receiver. The instrument is of particular interest to those responsible for frequency measurement, calibration and standardization, who wish to take advantage of the full range of carrier stabilized transmissions on the vlf/l-f band.

The receiver uses a single-sideband technique in the r-f section which has eliminated the need for r-f filters. The cancelling properties of this technique reject images by at least 60 db below 30 khz and 50 db above 30 khz.

Receiver sensitivity of 10 nanovolts allows normal phase tracking anywhere in the world. Tracking is maintained at an input signal-to-noise ratio of —50 db. Short and long-term stability is better than ±0.25 μsec relative to the received carrier. Calibration accuracy is better than ±1 x 10[11] when averaging for 24 hours. Tracor, Inc., Industrial Instruments division, 6500 Tracor Lane, Austin, Texas, 78721. **[368]**

Millivoltmeter serves both lab and test line

Fully transistorized and chopper stabilized, the model 300 d-c millivoltmeter features a basic range sensitivity of 0.001 v. It offers 10



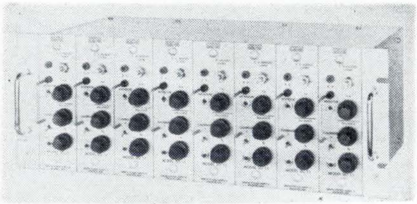
ranges, up to 30 v, floating input and an input resistance of 10 megohms.

Because of the feedback application, the stability of the instrument is such that no zero adjustment is provided. The instrument employs a zero-center meter and can be used as a null detector in bridge and potentiometer circuits. Available as an option is a zero-left modification and output terminals for graphic recorders. Accuracy of the unit is ±2% of full scale.

Line operated, the instrument is available in either 115- or 230-v, 50 to 60 hertz, style.

The standard model 300 sells for $185. Delivery is two to four weeks. IB Instruments, Inc., 7016 Euclid Ave., Cleveland, Ohio, 44103. **[369]**

Transducer bridge signal conditioners



Ultrastable, transducer bridge signal conditioners, known as the SG-11 series, are constructed as plug-in modules which may be installed eight-abreast in a rack-mounting enclosure, or used individually in a portable carrying case.

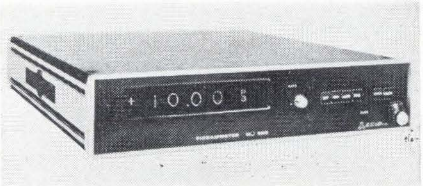
Each unit consists of an all-silicon power supply and a bridge conditioning circuit for four, six, or eight wire systems. The power supply is adjustable from 1 to 16 v d-c with line changes from 95 to 135 v and/or load changes from zero to full load. An automatic current limit makes the output short-circuit proof.

These units feature extremely high isolation from the power line—less than 0.03 picofarad—so that they can effectively serve as an adjustable battery. This permits the operation of a bridge with a floating power supply and a single-ended output.

Price of the basic plug-in unit is $187.50.

PPM, 7016 Euclid Ave., Cleveland, Ohio, 44103. **[370]**

Digital picoammeter is fast and accurate



New performance records in the automatic measurement of extremely low currents are claimed for the series 930 picoammeter. This digital device measures currents ranging from 10 picoamps to 10 milliamps, producing accurate readings as fast as 100 milliseconds. It functions automatically when measurements of extremely low currents are critical, particularly in production lines, in quality assurance programs, in engineering laboratories and in nuclear reactor monitoring and control systems.

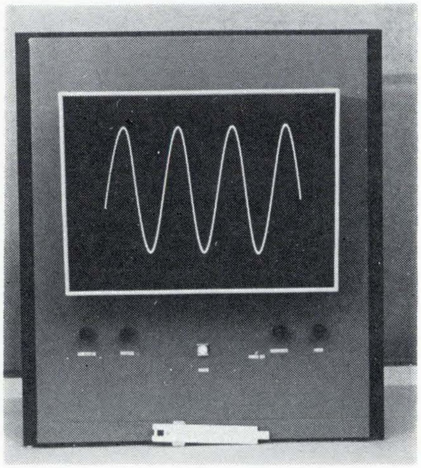
The series 930 features all-silicon solid state components, automatic polarity, digital readout, and optional drive for printers. The instruments feature easily interpreted readings and rapid recovery time from overload transients. They can be used either as a precision laboratory instrument or as a component in a control or monitoring system.

Accuracy is from ±5% to ±0.5%, bandwidth to 10 khz.

Dimensions of the picoammeter are 17x17x3½ in. Price is $2,435.

EG&G Inc., 680 East Sunset Road, Las Vegas, Nev., 89101. **[371]**

Circuit for brighter crt display



Fast sweep time afforded by a new solid-state deflection circuit results in very bright cathode-ray-tube computer displays, according to the circuit's developers, the Atlantic Technology Corp. The company says its model 8000 series of 10-, 12-, and 16-inch crt computer display systems has a deflection system that permits time-shared or chopped presentations with no loss of data.

The display dead time—the time used for slewing and settling the beam—is less than half that of earlier systems, Atlantic says, so there is greater beam dwell time and thus greater average light output; the older large-screen electrostatic computer displays use vacuum-tube circuits to position the spot. Also, solid-state circuitry cuts the new display's volume and weight by more than a third and increases reliability.

An example of how the brightness provided by this display can be exploited is found in the point plotting of random input data at a rate of 10 microseconds per point. If 5 μsec are consumed in beam slewing and settling time, then only 5 μsec are available for spot intensification. But if the slewing and settling time is only 2 μsec, as is typical with the new display, then 8 μsec are available for intensification and the average light output, or brightness, is increased by 60%. The surface brightness of the Atlantic display is about 50 foot-lamberts; other computer displays have surface brightnesses of less than 30 foot-lamberts.

One of the biggest problems encountered by engineers working on this display was that commercially available transistors have voltage ratings of no more than 500 volts. Their solution was to connect the transistors in parallel series to develop enough voltage to drive the screen's deflection plates and enough current to charge the circuit's stray capacitance. The display's dynamic focusing techniques assure that the beam is in focus anywhere on the face of the screen.

The display uses a d-c to d-c converter operating at 7 kilohertz and regulated by feedback. High-voltage components are potted in silicone rubber in a replaceable module. All other circuits, including the power-supply regulators, are on 4½ x 6½-inch etched circuit boards that plug into a larger 7 x 17-inch motherboard; the motherboard has all interconnecting wires printed on it. Front panel controls are mounted to the motherboard, and all wiring except the cathode-ray tube socket and anode cap wires are thus eliminated.

Model 8000 displays sell for $2,600 each in quantities of 100 and are available 60 days after receipt of order.

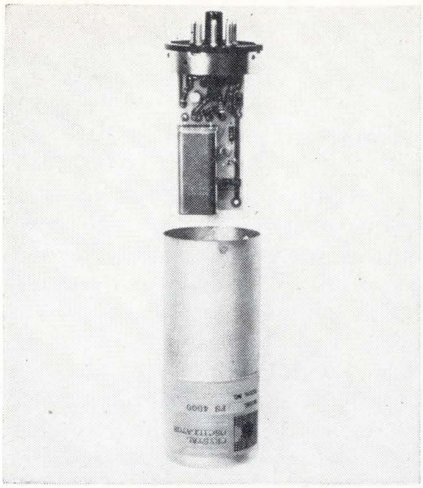
Specifications

Speed	Slew time 1 microsecond
Phase shift	0.5° to 100 khz
Bandwidth	
X and Y	d-c to 500 khz
video	d-c to 5 Mhz
Resolution	80 lines per inch
Mean time between failure	10,000 hours minimum

Atlantic Technology Corp., Somers Point, N.J. 08244 [372]

Frequency standard has many purposes

A new plug-in crystal frequency standard fits a variety of industrial, commercial and laboratory applications. The devices can serve as a precision clock or frequency ref-



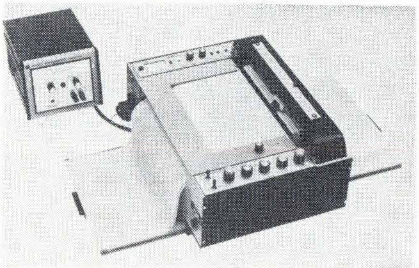
erence for commercial or industrial control equipment, precision production testing, and instrument calibration. They feature all-silicon semiconductors, internal voltage regulation, low input power and a standard octal plug-in base.

The series is available in frequencies from 100 kilohertz to 10 Mhz with stabilities of ±0.0005% as standard units. Under relatively constant temperature conditions, stabilities of better than 2×10^{-7} are realized. The input voltage may be 12, 15 or 24 v d-c with an output of 1 v rms sine wave, or 7 v peak-to-peak square wave into 5,000 ohms.

Dimensions of the units are $1\frac{11}{16}$-in. diameter by 3 in. high. Cost of a typical device is $95.

Robinson-Halpern Corp., 5 Union Hill Road, West Conshohocken, Pa., 19428. [373]

Plotting system uses digital interface



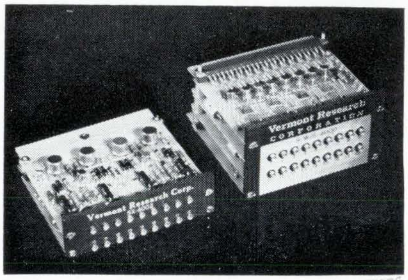
A combination of the model 6810 digital interface with model 6550 Omnigraphic plotter provides a versatile plotting system that can operate from either analog or digital data, either binary or binary-coded-decimal. Analog sensitivity is variable from 1 mv to 10 v per inch with a constant 100,000-ohm input impedance. Digital input is 10 bit binary or 3 digit BCD. System accuracy is 0.2% at slewing speeds up to 40 inches per second.

The plotter records up to 10 inches wide on fan-fold paper 11 inches wide and up to 144 feet long. The paper is perforated every 8½ inches at fold points, so that the recording can be separated into notebook-size 8½-by-11 or 11-by-17 inch sheets. The record can be read like a book and loaded into or removed from the recorder at any point on the record.

Price is $3,725; availability, 45 days after receipt of order.

Houston Omnigraphic Corp., 4950 Terminal Ave., Bellaire, Texas, 77401. [374]

IC modules improve drum memory systems



Up to 256 read-write heads in a magnetic drum memory can be selected using a pair of integrated circuit modules.

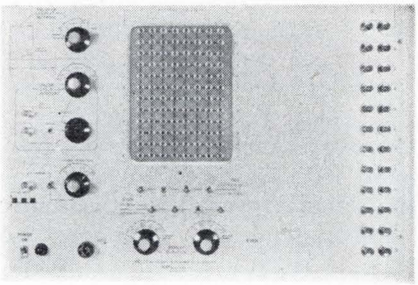
The RWS-4000 at the right in photo, contains a linear preamplifier for reading, a power amplifier for writing, and a matrix decoder that selects one of 16 pairs of lines with a 4-binary-digit input. Each of the 16 pairs connects to the two ends of the windings in 16 read-write heads arranged in a single vertical column.

The SX-4002 at the left contains only a matrix decoder for selecting another set of 16 single lines. Each of these lines connects to the center tap of 16 read-write heads in a horizontal row. When a selection has been made with both the RWS-4000 and the SX-4002 the two lines will intersect at one specific read-write head in a 16-by-16 array.

Both modules are made primarily of micrologic elements, but a few discrete components are required. The circuits can handle recording currents of up to 150 milliamperes and frequencies of up to 5 megahertz. Turn-on and turn-off times are less than 1 microsecond.

Vermont Research Corp., Precision Park, North Springfield, Vt., 05150. [375]

Pulse generator acts as clock, controller



Solid state, integrated circuit logic is featured in a pulse generator that has a 16 by 12 program matrix board. Programing is accomplished by inserting diode pins. The 16 time steps make a single pass through the program, operating at stepping rates from 1 khz to 10 Mhz. Any step may be repeated, either singly or in pairs, with the number of repeats controlled by an analog timer. Trigger pulses constitute the 12 parallel channel outputs. The repeat duration control also allows very long repeat periods under the operator's manual control.

The SQ-200 programable pulse generator can serve as the clock and controller for any sequencing system, such as a memory tester. It also can detect hazards in logic networks and investigate the effects of regular duty cycles.

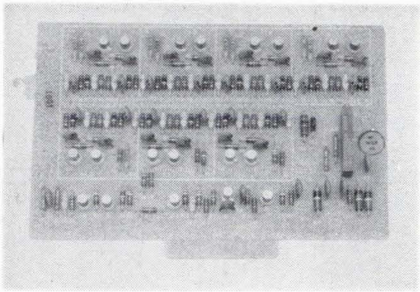
Price is $4,000.

Adar Associates Inc., 73 Union Square, Somerville, Mass., 02143. [376]

Voltage memory card monitors transients

A voltage memory card provides an economical approach to the monitoring of single or repetitive voltage transients in pulse widths

New Subassemblies



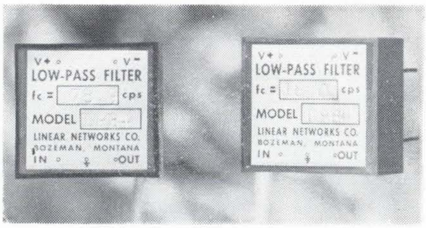
from 100 microseconds to infinity. The card is used with an external meter and power supplies, and mounts in the user's equipment.

The card converts the peak amplitude of any input voltage signal of 100 microseconds or longer duration into an unvarying output and holds it indefinitely in an electronic memory until reset or until a higher amplitude input pulse is received. Input impedance is 10,000 ohms minimum. Output of the memory card is 0 to 100 microamperes d-c, full scale, and is internally adjustable to full scale for meters of 500 to 1,000 ohms internal resistance. Accuracy is $\pm 2\%$ of full scale.

Model 5221 is a printed circuit card 6⅜ in. long x 4⅝ in. wide, including connector fingers. Price is $150 each in quantities of one to nine. Discounts are available on larger quantities.

Micro Instrument Co., 12901 Crenshaw Blvd., Hawthorne, Calif., 90250. **[377]**

Low-pass filters fill variety of needs



A series of epoxy-encapsulated active low-pass filter networks has been developed with a low cutoff frequency for applications that include seismology, medical electronics, sonar, oceanography and speech analysis. The networks may be used wherever small temperature-dependent d-c offset voltage is not objectionable.

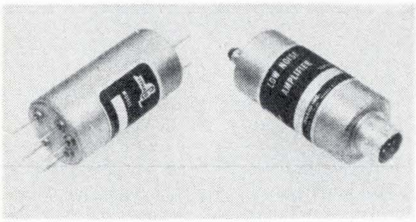
The LPB4 filters have the four-pole Butterworth (maximally-flat) frequency response characteristic in gain and phase. The operating temperature range is −40° to +70°C, over which the attenuation is 3 ±0.5 db at cutoff frequency; the attenuation rolloff is 24 db per octave. The filters will not be damaged if stored at temperatures between −55° and +125°C.

The filters have small physical size (0.8 cu in.), and low insertion loss (0.1 db); they can accommodate a wide range of source and load impedances and are insensitive to power supply variations. Standard cutoff frequencies from 1 to 1,000 hertz are available; other cutoff frequencies are available on special order.

The devices are priced from $45 in small quantities, and are available from stock to 30 days.

Linear Networks Co., 1309 S. Black Ave., Bozeman, Mont., 59715. [378]

Preamplifier features remote gain switching



Premium noise performance and 1,000-megohm input impedance are provided in a preamplifier with remotely-switchable gain. The preamplifiers can be used in hydrophones, low-noise vibration work, radiometry, and in any application where widely varying signal amplitude is encountered.

Model 155 preamplifiers may be operated with remote gain switching at distances limited only by the output stage—typically 10,000 feet or more.

The preamplifier's construction is all solid state; it contains no mechanical contacts. Each unit is encapsulated and hermetically sealed in a cylindrical module 1⅛-in. diameter and 2¼ in. long. Versions are available with either connector or solder pin terminations.

The two switchable gain states are 20 db and 40 db, with long-

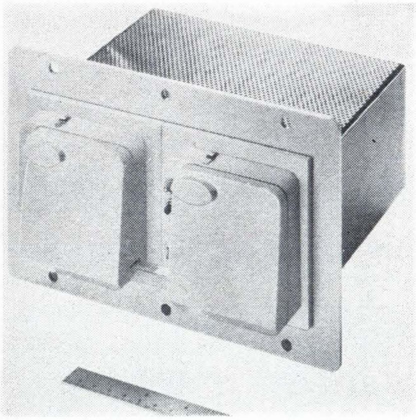
New Subassemblies

term gain stability of 1%. The passband is 0.5 hertz to 200 khz. Broadband noise, referred to the input, is 3 μv maximum. Dynamic output impedance is 50 ohms. An internal divider network permits injection of a calibration signal.

Any two gain states in the range 10 to 50 db are available on special order. Variations in frequency response are also available.

Ithaco Inc., 413 Taughannock Blvd., Ithaca, N.Y., 14850. **[379]**

Strip printer with take-up spooler



Representative of the company's military line of digital printers is the AN-16 strip printer with take-up spooler. Utilizing the on-the-fly printing technique as used in large on-line computer output printers for several years, the mechanisms have been reduced to five functional subassemblies, an indication of the simplicity and inherent reliability. The complete unit with electronics has been miniaturized for easy installation in instrument panels of large systems where hard copy data recording is required.

The AN-16 is a mil-spec alphanumeric strip printer, weighing less than 5½ lbs and occupying only 200 cu. in. It was designed to meet applicable sections of Mil-E-5400 and Mil-I-26600 and will operate under severe environment.

The printed information is presented serially to the operator at up to 25 characters per second with a selection of 64 characters, and the printer can be adapted to accept

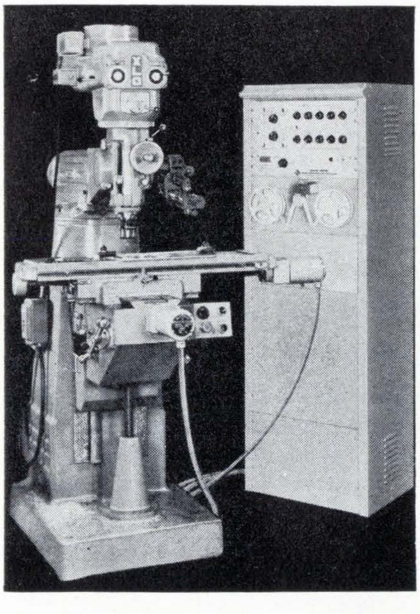
New Subassemblies

any parallel 6-line BCD code at several interface logic voltage options requiring low driving currents limited by the 5-kilohm input impedance. Integrated circuits mounted on replaceable p-c cards are used in the electronic section. The use of $\frac{5}{16}$-in.-wide pressure-sensitive tape eliminates the need for ribbons or inker mechanisms. Calculated mean-time-between-failure of printer and spooler is in excess of 3,000 hours.

The AN-16 with take-up spooler sells for $4,375, with substantial quantity discounts.

Clary Corp., Military Products division, 320 W. Clary Ave., San Gabriel, Calif., 91776. **[380]**

Numerical control offers many functions



Tape-controlled initiation of two additional external functions, plus tape actuation of rapid traverse during slow feed drilling and milling machine operations, are standard features of the Slo-Syn tape-controlled indexer.

For pocket milling applications, tool feed and retract can be actuated from tape command. When used in drilling and similar applications, the tool can be actuated automatically after positioning. The tape-controlled functions are used for multiple spindle selection, coolant flow or other needs. These fea-

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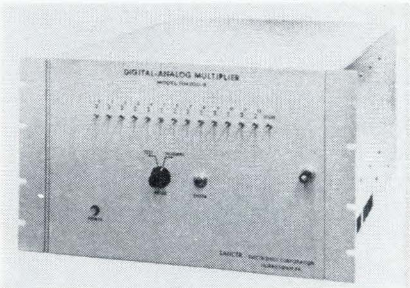
tures permit the milling of elongated holes, keyway slots or pockets while drilling the same workpieces. Positioning increments and tool actuation can be directed manually when required.

Designed for point-to-point positioning or straight-line milling applications, the indexer, model TCI-100B, can be fitted to a wide variety of equipment including drilling, milling and boring machines, automated assembly fixtures, welders, cutters, automatic drafting and wiring machines and many others.

Superior Electric Co., Bristol, Conn., 06010. **[381]**

Hybrid multiplier operates at high speed



Up to eight digital-analog multiplier channels in a single rack-mountable housing are provided by a hybrid multiplier system.

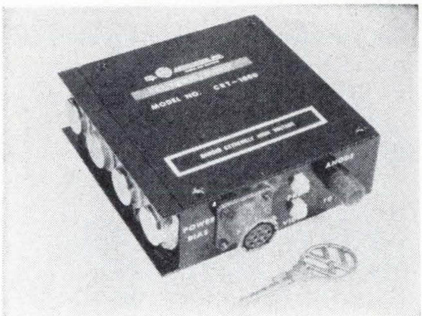
It performs high speed multiplication or division between ±100 volt analog and 14 bit digital variables. The system performs with an operational error of less than 0.01% of full scale and operates directly upon an analog input up to ±150 v without preliminary scaling.

Digital representation of negative signed data is accepted in either one's complement or two's complement format. Digital input buffer registers are available in single rank or double rank models. Second rank storage allows for random acquisition of data, which is to be held until required for simultaneous transfer to first rank storage for next computation.

The system, model HM200, fea-

tures solid state construction with integrated circuit storage registers and FET chopper-stabilized amplifiers. System output capability per channel is ±100 v at ±35 ma with full power bandwidth beyond 50 khz.
Lancer Electronics Corp., Box 142, Norristown, Pa., 19404. **[382]**

Solid state supply for crt displays



Compact packaging of a high-voltage power supply permits its easy design into a variety of cathode-ray-tube displays. The integrated, solid state unit occupies only 4¼x4½x1½ in. and weighs less than 1½ pounds.

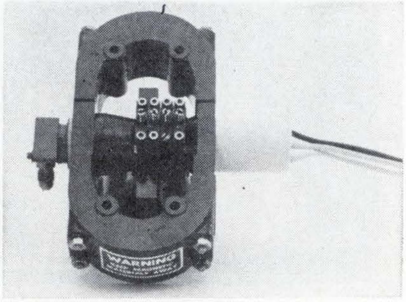
Anode voltages up to 18 kv are available at 0.5 ma. The filament voltage is 6.3 v d-c at 1 amp. Both the focus and the grid bias outputs are adjustable and readily accessible on a single face of the package. The supply provides high voltage outputs with a stability of better than 1% from 0 to full load.

Several circuit protection features are built into the package. All outputs have full short-circuit protection. There is a built-in, 30-second high voltage delay to prevent damage from high voltage reaching the circuit before the filaments obtain operating temperature. An automatic sweep failure protection circuit is also included. If the sweep signal fails, a digital input from the sweep circuitry automatically biases the tube to cut-off in less than 10 μsec. This prevents burnout of the tube from concentration of a single spot at the tube face.

Basic price of the crt power supplies is less than $300 when purchased in quantity.
Mil Associates, Inc., Dracut Road, Hudson, N.H., 03051. **[383]**

New Microwave

Radar klystron delivers 300 w c-w



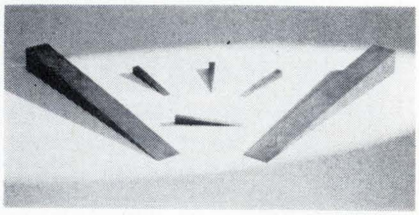
Rugged klystron amplifiers, which deliver at least 300 w at a center frequency located between 9.2 and 10.6 Ghz, are claimed to be ideal for airborne doppler radar. The tube has a very low inherent noise with random a-m noise at least 100 db below the carrier in a 1 khz band. The liquid-cooled amplifier weighs less than 6 lbs and measures 6.6x5.6x4.3 inches.

Models in the VA-896 series operating at any center frequency between 9.2 and 9.6 Ghz are tunable ±50 Mhz; others within 9.6 to 10 Ghz are tunable ±100 Mhz; and those in the 10 to 10.6 Ghz range are tunable ±125 Mhz.

Gain is high—at least 45 db—minimizing drive power requirements. Focusing is by an integral permanent magnet, a feature that eliminates focusing adjustments and the need for extra power supplies.

Varian, Palo Alto Tube division, 611 Hansen Way, Palo Alto, Calif., 94303. **[391]**

Waveguide terminations for S to Ku band



Low-power waveguide terminating elements are available for frequencies from S band to Ku band. The terminations, shaped like wedges, are made from lossy dielectric absorbing material.

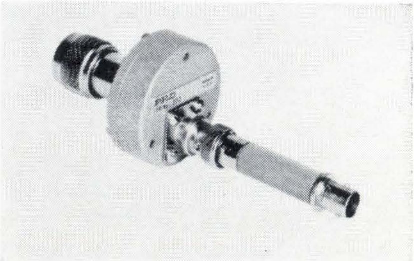
In use, one side of the wedge is mounted in contact with the bottom (broad) wall of the waveguide to provide a rugged structure that will withstand far more abuse than the pyramidal-type termination. This construction also permits greatly improved heat dissipation because of the contact of the wedge with the waveguide. Also, the wedge can be adhered to the waveguide wall with an adhesive with the same properties as the wedge material.

The wedge fineness ratio of approximately 10:1 insures very low vswr of the element over the entire waveguide band—maximum vswr is 1.01. Length of the element varies from 2¾ in. for Ku band to 12¼ in. for S band.

The terminations are priced from $15 to $75.

Emerson & Cuming Inc., Microwave Products division, Canton, Mass., 02021. **[392]**

Bolometer unit covers wide band

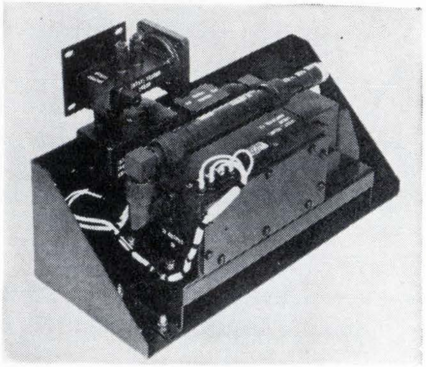


A fixed-tuned bolometer unit operates from 50 Mhz to 10 Ghz. Consisting of a length of ⅜-in. coaxial line and a filter network, it is particularly useful for low power measurements. The bolometer's element, a thermistor, is a flat disk structure which is clamped between round flanges. Matching is provided by inductive undercuts in the mount's coaxial line and by the proper shaping of the bolometer's electrode. Maximum power rating for the type G27-AM1 is 10 milliwatts.

Connectors are type N or BNC,

and variation of fixed and tuned coaxial mounts are available on special order.
PRD Electronics, Inc., 1200 Prospect Ave., Westbury, N.Y., 11590. **[393]**

Frequency translator offers high stability



High stability under severe environments is featured in a field-transportable microwave frequency translator for communications systems. The solid state unit consists of a tunnel diode amplifier, isolator, image rejection filter, mixer/i-f amplifier and a bandpass filter.

The device converts signal inputs of 7.25 to 7.75 Ghz to outputs at 400 Mhz with an r-f to i-f gain of 50 db and a noise figure of less than 8 db. Intermodulations and spurious responses are at least 60 db below the desired output level.

The signal translator provides linear amplification to signal levels as high as +9 dbm with a 1-db bandwidth of 60 Mhz minimum. Local oscillator rejection is at least 20 db below the l-o input level.
The Micro State Electronics Corp., a subsidiary of Raytheon Co., Murray Hill, N.J. **[394]**

Air-strip package operates at X band

A strip transmission line mixer is available that minimizes the response to the image frequency and requires no tuning through the entire band from 8.2 through 10 Ghz. Image rejection is greater than 25 db from 9.2 to 9.55 Ghz, and all

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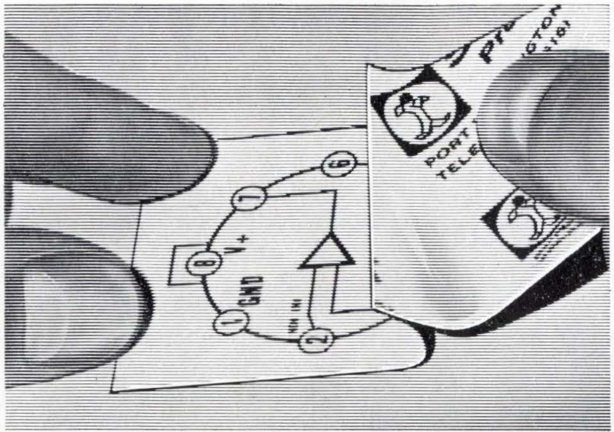

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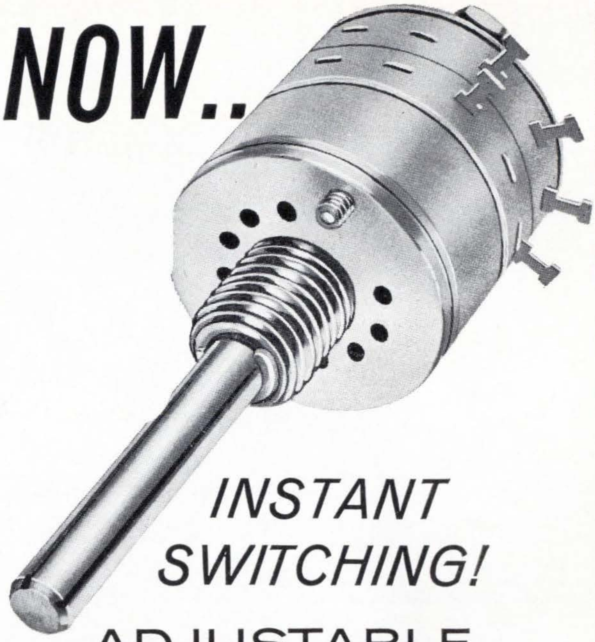

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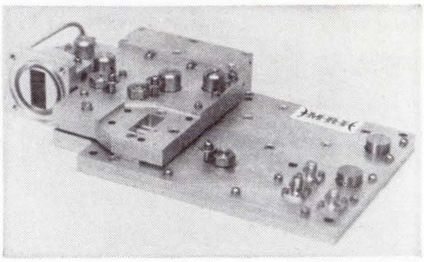
New Microwave



spurious signals are down more than 40 db.

The lightweight package includes a waveguide-to-coaxial transition for local oscillator input to the lower section. This section includes three isolators, a differential phase shifter and three variable attenuators for use with the mixer and other functions.

The manufacturer says the rugged package uses the latest techniques in low-loss printed strip transmission circuitry. It meets all the requirements of MIL-E-5400 including long life and ultrahigh reliability. All diodes are easily replaced because they are mounted in accessible holders.

The package is 9.1x5.3x1.6 in. and weighs less than 37 oz.

Micro-Radionics Inc., Van Nuys, Calif. **[395]**

Pulsed twt drives wideband radar

Designed for use as a driver or output stage in advanced wideband radar systems, a pulsed traveling-wave amplifier tube covers the 2.8- to 3.5-Ghz band. It produces a peak output greater than 7 kw with less than 5 w of drive power without mechanical or electrical adjustment at pulse lengths up to 200 μsec.

The tube, VA-642C, is liquid cooled, electromagnetically focused, and of all metal-ceramic construction. It weighs 10 pounds; its electromagnet weighs 65 lbs. Diameter of the tube is 2.615 in. and length is 26.5 in. Coolant fittings accommodate ¼-in. outside-diameter tubing.

Varian, Palo Alto Tube division, 611 Hansen Way, Palo Alto, Calif. 94303. **[396]**

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π type　　NA type

Now, adding new efficiency to ultrasonic propagation, Tohoku Metal introduces VIBROX—unique *ferrite* magnetostrictive vibrators. Developed by Dr. Yoshimitsu Kikuchi of Tohoku University, VIBROX has minimum eddy current loss and a far greater electro-mechanical transduction efficiency than conventional vibrators. A wide range of application embraces ultrasonic cleaning and degreasing; metal, textile, and chemical processing; and echo-sounding and navigation devices such as depth-sounder, fish-finders, etc.

Tohoku VIBROX is supplied in two shape-types with nominal frequencies ranging from 15 to 100Kc. Termed NA and π respectively, both make use of associated permanent magnets to totally eliminate the need for DC bias — despite the fact that VIBROX is magnetostrictive.

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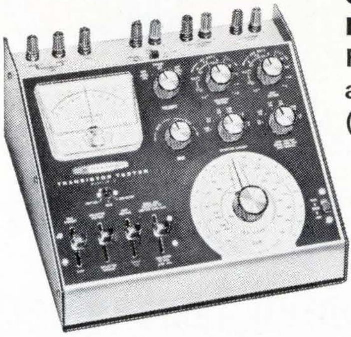

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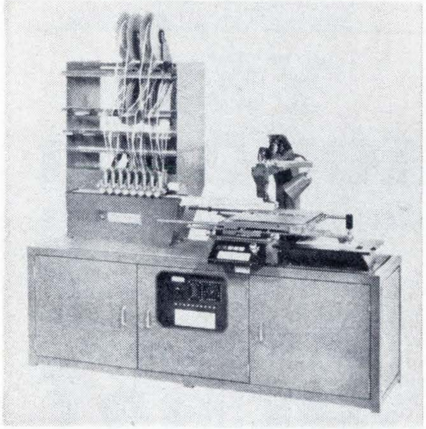
 Circle 264 on reader service card

Circle 327 on reader service card

New Production Equipment

High-speed component insertion

Insertion of components by hand into printed circuit boards, while cumbersome and time-consuming, is frequently necessary when several types of axial-leaded components have to be put in a relatively small number of boards. To cover just such small production runs, the Universal Instruments Corp. has developed a machine it says will allow one operator to do the work of 15 hand-assemblers.



The company's model 6710 achieves this efficiency by combining the sequencing and insertion processes. Its three racks hold as many as 10 component reels, each as large as 16 inches in diameter. Individual components drop through dispensing stations below the racks and are carried on a chain conveyor operated by a two-way air cylinder. A sensing device poised above the belt determines the component's presence.

The actual insertion assembly is an adaptation of the company's Pantograph, an earlier machine working from only one reel. The insertion head in the center of the machine is guided by a stylus at the extreme right. The operator moves and depresses the stylus in the proper sequence into holes on a template. A cut-and-clinch unit coming up from below the head insures uniform lead length and tightness even with components of varying diameters.

Although there is provision for only 10 reels, the model 6710 isn't restricted to production runs where the total number of components on the p-c board is 10 or less. As long as only 10 or fewer different types of components are needed, the machine can prove economical where the annual number of components to be inserted is roughly 1 million or 2 million.

The machine will make insertions on one axis only; if the leads are positioned on two axes, the board must be repositioned and a second pass-through made.

The sequencer can also be fed from magazines, but magazines hold fewer components than reels, and Universal warns that the gravity feed introduces more possibilities for error.

The model 6710 is priced at $19,000, plus the cost of the template. Universal estimates that if the operator is paid $2.50 an hour and can hand-insert 400 components an hour, the machine can pay for itself in 63½ 7-hour working days.

Specifications

Insertion rate	3,000/hr
Size	73 x 83 x 42 inches
Weight	1,500 lb.
Area	70 sq. ft.
Power requirements	115 v, 60 hz
Air requirements	80 psi, 1 cfm

Universal Instruments Corp., East Frederick St., Binghamton, N.Y. 13902 [401]

Ultrasonic degreasers in a compact package

Light-duty vapor degreasers provide ultrasonic washing, spray and vapor rinsing in a compact package from which parts emerge clean and dry. The units come in three standard sizes with working volumes of 9x12x10 in., 12x18x12 in., and 24x18x12 in. They can handle between 300 and 1,200 lbs of steel parts per hour, or the equivalent in other materials.

Typical applications for the ultrasonic degreasers—which use Freon TR degreasing solvent—include the cleaning of p-c boards, switches, relays, bearings, micromodules, precision instruments and electronic components.

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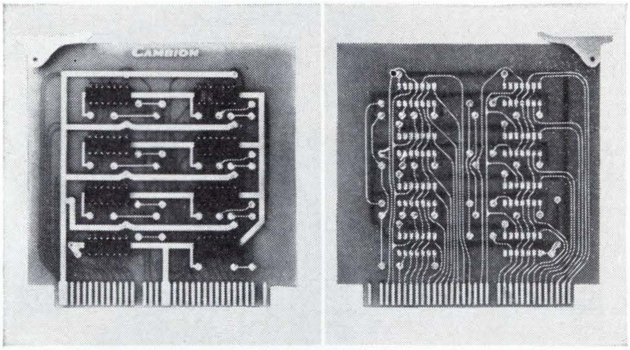

Typical Logic Assembly (4½" x 4½") Shown Front and Back

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Circle 267 on reader service card

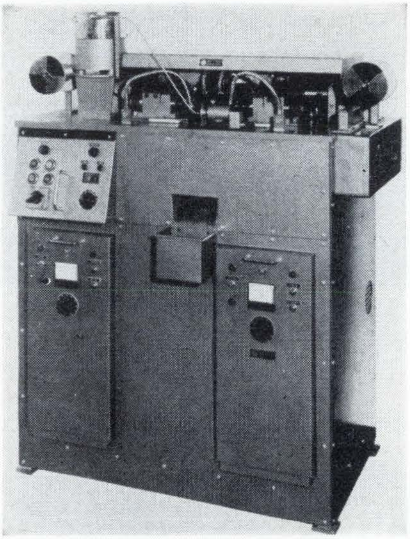
ously purifies the ultrasonic sump by concentrating solubles, such as fluxes and oils, in the boiling area and delivering pure distillate. A recirculating filter removes particulate matter. Tanks, condensing coils and water separator are of stainless steel.

The units are equipped with the manufacturer's Sonogen A-series solid state, automatically tuned ultrasonic generators and Sonogen Z transducer elements.

Depending on options, the price of the UF series ranges from $1,250 to $4,450.

Branson Instruments Inc., Equipment Division, 51 Terminal Ave., Clark, N.J., 07066. **[402]**

Automatic machine welds component leads



An automatic lead welding machine that can make 8,400 welds per hour is being offered by the West Germany manufacturer Witte & Sutor. The machine can handle a wide variety of components and wire sizes. Wire is fed continuously and automatically cut to any length between 0.70 and 2.5 in.

The welder accepts components ranging in body length from 0.19 in. to 0.78 in. and diameters from 0.070 in. to 0.236 in. Wire diameter sizes range from 0.019 in. up to 0.034 in. Up to 4,200 double welds can be made in an hour.

The machine's feed system and

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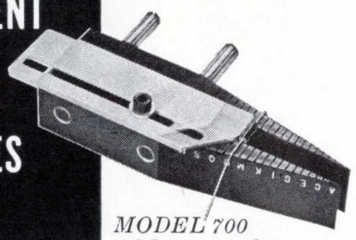

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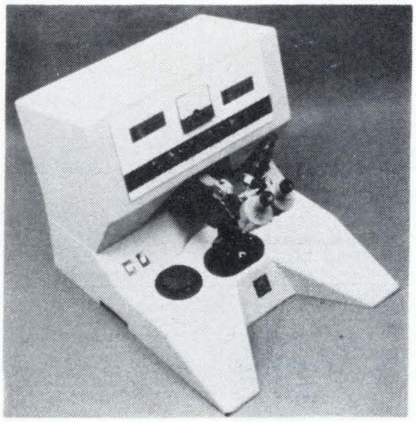
Circle 269 on reader service card

Production Equipment

component clamps are easily interchanged and specially designed electrodes eliminate the need to prepare wires before welding. The machine comes with two power packs and tooling for one component body size.

A vibratory bowl feed for components plus the necessary tooling for additional component sizes are optional.
B. Freudenberg Inc., 50 Rockefeller Plaza, New York, N.Y., 10020 **[403]**

Ultrasonic lead bonder for semiconductors



Leads on semiconductor devices can be bonded quickly with an ultrasonic lead bonder that has handled as many as 600 flatpacks with 14 leads of two bonds each in a day. The model 1200 has an automatic bonding cycle and two separate channels for post and chip bonding. Its operation has been made as simple as possible so that personnel training time is short and margin of error is minimized.

A key to the success of the device is a 20-watt ultrasonic generator and transducer, with a temperature compensated feedback network for operational stability. The bonder incorporates a cam locking device for superior reproduceability of bonds and elimination of costly maintenance.

The model 1200 can also handle TO-5 and TO-18 packages, with various flatpack chucks available.
Hugle Industries, 587 North Mathilda Ave., Sunnyvale, Calif., 94086. **[404]**

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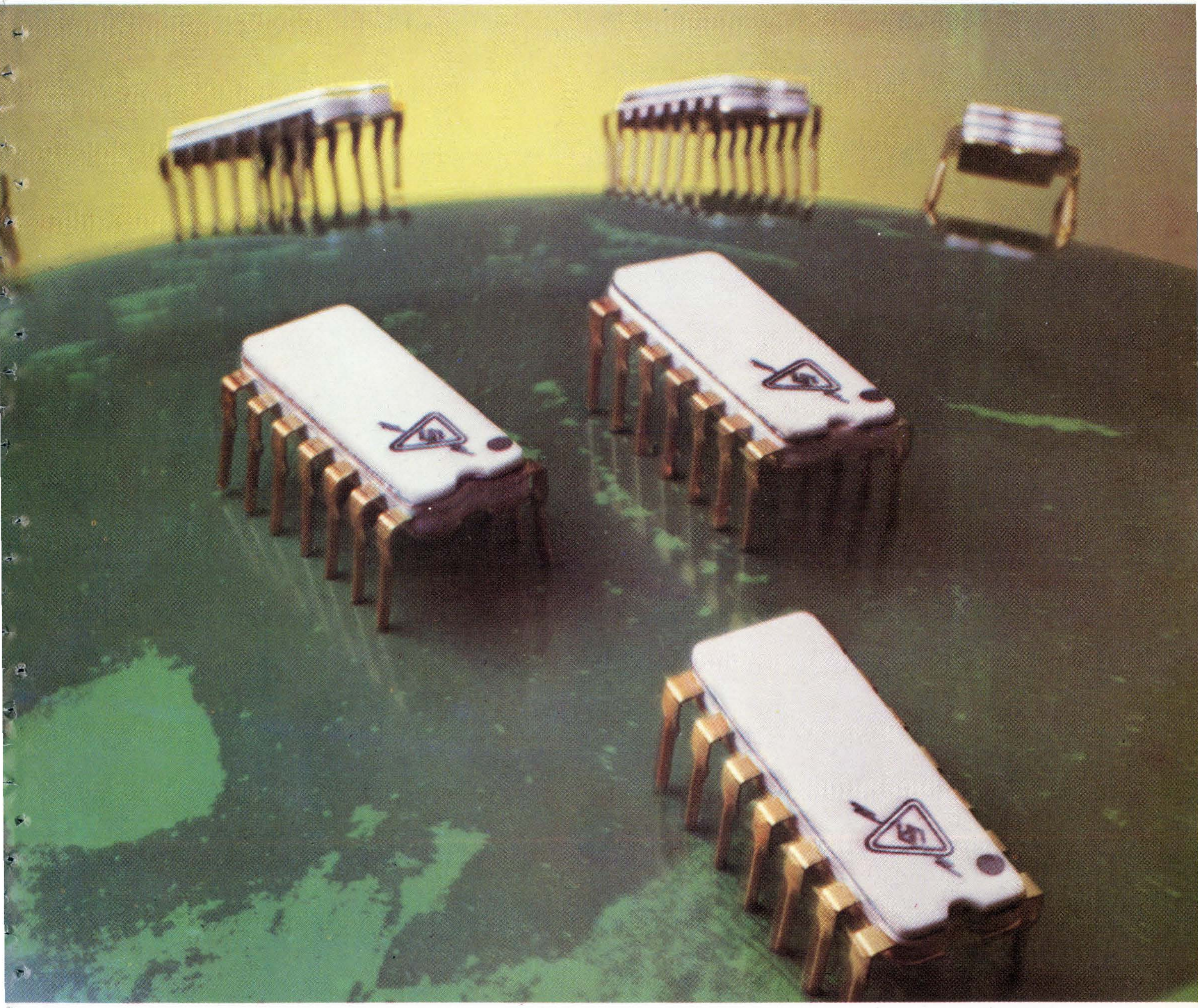

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Circle 271 on reader service card

New Materials

Long glass pipes light the way

Flexible glass optical fibers spooled in 10,000-foot lengths are now available from the Corning Glass Works.

The light guides, strengthened with a lubricant, are encased in a polyvinylchloride (PVC) jacket. An all-plastic counterpart has already been made available in long lengths [Electronics, June 27, 1966, p. 184]. Corning, claiming glass gives better light transmission than plastic, says that light transmitted with a 10-foot length of glass fiber is 40% of the input, against approximately 20% for plastic.

The glass-plus-PVC combination is also said to operate without degradation at a sustained temperature of 212°F, about 35° higher than all-plastic pipes.

The fibers are already being tested in a fluid level monitoring system for automobiles by the Packard Electric division of the General Motors Co. Packard hopes to use the pipes to transmit light from the brake-fluid container's reflective sides to a dashboard indicator whenever the fluid falls below the safety level. Other applications include transmitting remote light or optical data in data processors, medical instruments, inspection systems and high-speed printing systems.

Individual glass fibers are 0.0025 inch in diameter and the entire bundle, without jacket, is about 0.045 inch in diameter. Multiples of the standard bundle are also available.

Five spools cost about $5,000.

Specifications

Standard bundle	
Numerical aperture	0.55 minimum
Minimum acceptance angle	65°
Spectrum (3 db points)	0.37 to 1.9 microns

Corning Glass Works, Corning, N.Y. **[406]**

Epoxy molding powders for delicate devices

The soft flow characteristics of the MG6 series of epoxy Hyflo molding powders suit them for encapsulation of delicate and complex components such as solenoid coils, modules, glass diodes, relays and a variety of semiconductor devices. The material is characterized by extreme toughness, low shrinkage, excellent moisture and thermal shock resistance, high dielectric strength and chemical resistance.

It is available in mineral filled, fiber reinforced and special nonburning versions.

Hysol Corp., Olean, N.Y. **[407]**

Water-soluble fluxes for batch soldering

Three water-soluble fluxes have been formulated for batch soldering processes. They may be applied to printed boards by roller, spray, brush or foam.

One of the fluxes, called Microflux, can be applied and allowed to dry before soldering to eliminate spattering. No precleaning is required. Flux residue is noncorrosive. After soldering, boards may be cleaned using ordinary tap water.

Superior flux action could virtually eliminate rejects. Ease of cleaning lowers production costs associated with the soldering and cleaning operation by greater than 50% compared to similar operations using rosin fluxes, according to the company that developed the flux. Ultrasonic cleaning techniques aren't needed—preventing the possibility of component injury.

The second material, known as K-Flux, has all of the attributes of Microflux, plus a fluorescent dye. When exposed to ultraviolet light it glows a bright red, thus incorporating an inspection device to insure proper cleaning.

Microflux-A incorporates all of the features of Microflux with the additional advantages of very rapid drying—thus assuring no spattering and allowing the soldering operation to proceed on a continuous basis.

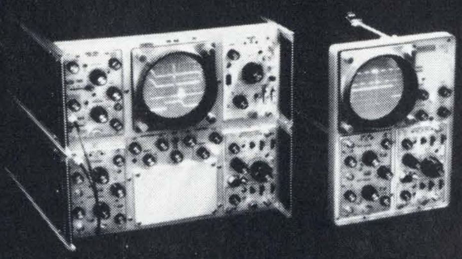
Krohn, Inc., 73 No. 2nd St., Easton, Pa. **[408]**

Inexpensive ruby rod aids laser research

Maximum laser efficiency with the least amount of pumping is provided by a new ruby laser rod, according to the company. The rod is grown by the Czochralski process and is available in sizes of 0.150-in. diameter by 1.5 in. long.

Each rod costs $99.50.

Semi-Elements, Inc., Saxonburg, Pa. **[409]**



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Single beam, solid-state scope with 6 x 10 cm scan, 13kV accelerating potential and algebraic add. The 766 H/F accepts any of the plug-ins listed to the right, but the 79-02A amplifier and 74-17 beam switching and delaying sweep time base are recommended. With these plug-ins the scope has 100MHz bandwidth, 100mV/div sensitivity, 3.5nsec. risetime, and a 5nsec. sweep.

777 Main Frame:
The 777 is a true dual-beam scope, with a dual gun CRT. It has a 13kV accelerating potential and a 6 x 10 cm display area for each beam, with a 4 cm overlap. Each gun can be independently blanked or intensified. The 777 accepts any four of the plug-ins listed to the right.

For detailed information, call us, or write.

The Plug-ins:

Time Base Modules:

74-03A	General purpose, 5nsec.
74-13A	Delaying sweep with calibrated delay
74-14	General Purpose time base
74-17A	Automatic beam switching delaying sweep with calibrated delay

Vertical Amplifier Modules:

74-12	1mV/cm differential amplifier, 850kHz
74-15	20mV, 1MHz amplifier
74-19A	Single trace, DC to 5MHz, 50mV/cm
76-01A	Single trace, 5mV/cm, 25MHz
76-02A	Dual trace, 5mV/cm, 25MHz
76-05	Single trace, 100MHz, 50 ohms input
76-06	Four trace, 20mV/cm, 20MHz
76-08	Dual trace, 5mV/cm, 50MHz
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New Books

Putting Fourier to work

Fourier Transforms and the Theory of Distributions
J. Arsac
Translated by Allen Nussbaum and Gretchen Heim
Prentice-Hall, Inc., 318 pp., $14

Engineers who have taken one or two graduate courses in Fourier transforms should find this translation from the French a useful supplement, both for its mathematical exposition and for its applications section. In reviewing the transforms, much space is devoted to a simplified discussion of the theory of distributions that was developed in the 1950's. This theory establishes a firm mathematical basis for finding transforms of the common trigonometric functions — transforms involving the delta (impulse) function.

The applications section concentrates on topics pertaining to optics (Arsac works at France's Meudon Observatory). The material is general enough, however, so that engineers working in antenna theory, propagation studies, lasers and holography will find much useful information. The author's discussion of linear filters covers both resolving power theory and probability functions. Other topics are diffraction at infinity, solution of wave equations and methods of approximating Fourier functions to obtain numerical solutions.

Designing the i-f stage

Transistor Bandpass Amplifiers
W.Th.H. Hetterscheid
Philips Technical Library, Springer-Verlag New York Inc., 314 pp., $12

By concentrating on transistorized selective amplifiers that are a part of the intermediate-frequency stage in every radio, television and radar receiver, the author has produced a thorough, practical design guide that should be a welcome addition to the communications or radar designer's library.

Hetterscheid gives detailed analyses of single-stage amplifiers with single-tuned and double-tuned circuits, then shows how these analyses can be modified when designing multistage amplifiers with other types of interstage coupling. He also explains how deviations in the parameters of transistors and passive components affect the designs. In addition to discussing stability, loop gain and neutralization, the author gives a detailed comparison of tuning procedures used for aligning amplifiers.

The book is not new; it was first published in the Netherlands in 1964 but distributed in this country only recently. The information, nevertheless, is still timely.

A pinch of impurity

The Electronic Theory of Heavily Doped Semiconductors
V.L. Bonch-Bruyevich
Translated by Robert S. Knox
American Elsevier Publishing Co., 131 pp., $7.50

Retrieving information about the electronics industry is a continuing challenge; sifting through the many articles about solid state physics is an overwhelming task. But help has arrived from the Soviet Union with this excellent presentation of recent findings in the field of heavily doped semiconductors.

Theoretical treatments of high-level subjects can be dull. This book is not. Physical principles and mathematical steps (all clearly explained) are interwoven, yielding an interesting and smooth-flowing text that demonstrates the depth of the author's knowledge. Numerous references—many to work by the author and his students—make this a valuable guide for solid state physicists, physical chemists and scientists and engineers involved with device theory. The author assumes the reader has knowledge of the two prerequisites, quantum theory and solid state physics.

Bonch-Bruyevich, a professor at Moscow State University, begins by comparing the energy bands of both moderately and heavily doped semiconductors. Using a physical model of a lightly doped semiconductor under high injection conditions which make it similar to a heavily doped material, the author discusses screening efforts.

Physical properties, such as density of states and complex electrical conductivity, are determined

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At the same time, the Audio Equipment Exhibition will take place in an adjacent area, where engineers & technicians from all countries will be welcomed.

International Seminar on Space Electronics

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Reservations should be made.

The aim of the seminar is to study how the electronics industry has adapted and up-dated itself in relation to the development in aerospace activities.

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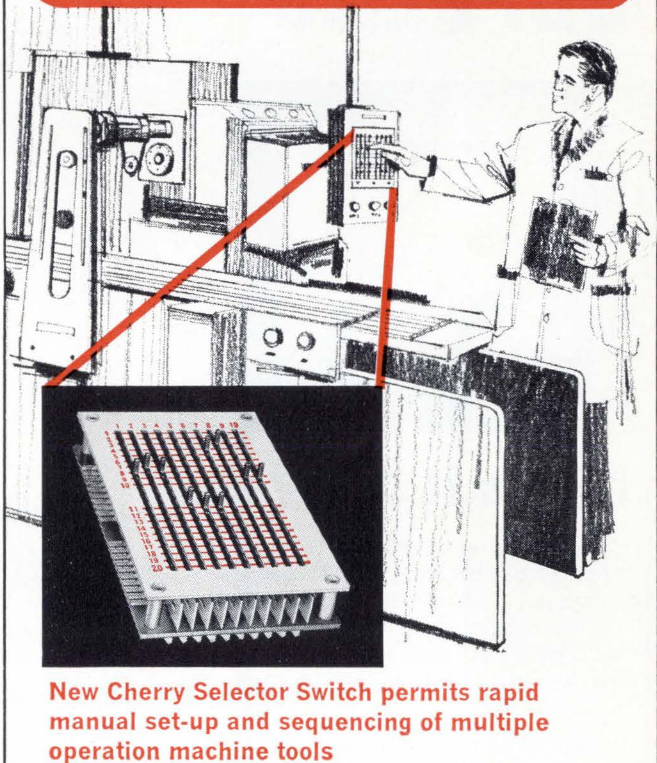

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using Green's function. The author establishes this function using approximation techniques, then determines the properties in detail. In heavily doped semiconductors the energy bands are not sharply defined, and no well-defined forbidden region [an energy band in which there can be no electrons] separates the conduction and valence bands. The author shows that each band has a tail that extends —or "smears out"—into the forbidden band. In studying the location of Fermi-level electrons, both the change in the density-of-state function and the presence of the band tails are taken into account.

Other topics include static electrical conductivity, absorption of electromagnetic waves and the interaction of charge-polarized oscillations of a heavily-doped semiconductor's lattice.

The author concludes with a theoretical discussion on making contact between two heavily doped semiconductors with different properties.

Ronald B. Schilling
Radio Corp. of America
Sommerville, N.J.

Technical snapshots

Photographic System for Engineers
Edited by F.M. Brown, H.J. Hall and J. Kosar
Society of Photographic Scientists and Engineers, Washington, 215 pp., $5

The reader who assimilates this relatively short book will be well on his way to becoming an expert in the field of photography as practiced by engineers—mechanical, optical and chemical as well as electronic. The one-volume course contains papers the Society of Photographic Scientists and Engineers presented on the subject in a two-day seminar in New York in 1959 and then repeated with some updating on the West Coast in 1966.

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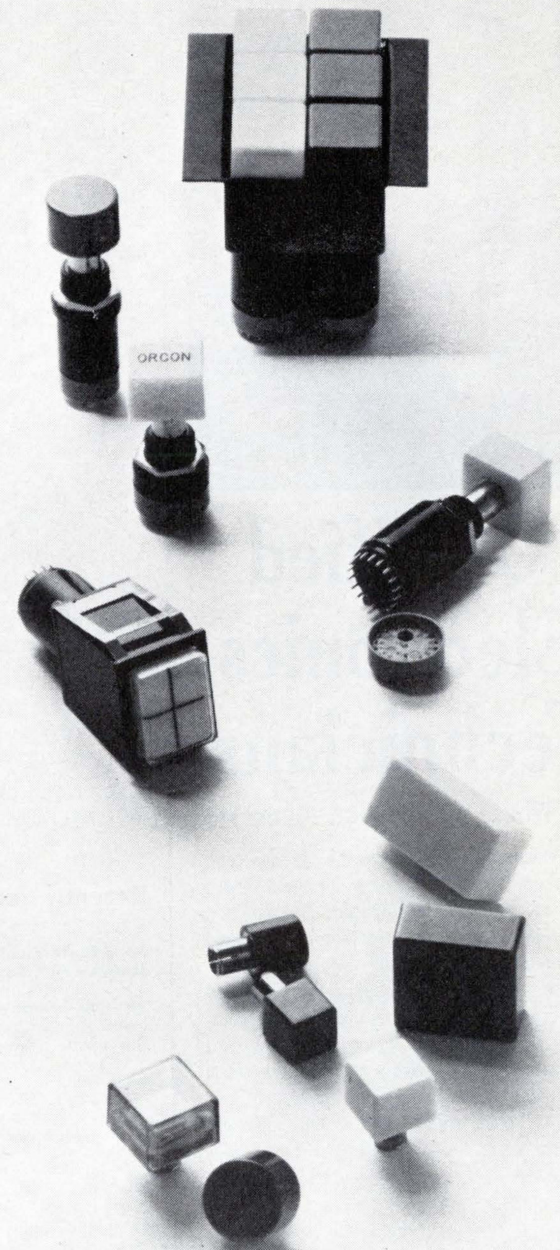

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kinds of photography are described along with the equipment and materials used for each. Detailed explanations for processing the film are provided.

Review of technology

Advances in Computers, Vol. 7
Edited by Franz L. Alt and Morris Rubinoff
Academic Press, 303 pp., $14

The latest annual purporting to review what's new in computer technology is rather a mixed bag. Of interest to this reviewer were Wayne A. Danielson's explanation of how men and machines work together in copy editing, William R. Bozman's paper on computer-aided typesetting and Andries Van Dam's discussion of visual displays.

John C. Murtha's article on parallel information processing, however, is hard to follow. The two articles on programing languages presume extensive knowledge of the subject, but, for the neophyte, Arnold C. Satterthwait does provide a lucid explanation of just what computational linguistics is.

Recently published

Solid-State Electronics, Shyh Wang, McGraw-Hill Book Co., 778 pp., $15.50

To help bridge the gap between physics and electronic engineering, the author presents the properties of solid state materials from a device standpoint. Detailed quantitative analysis is given for several physical models.

Radio Telescopes, edited by D.V. Skobel'tsyn, Plenum Publishing Corp., 171 pp., $22.50

The English version of the Proceedings of the P.N. Lebedev Physics Institute in Moscow arrives several years late in an inexpensive format (thin paper and soft covers). It may, however, interest those who are following the Soviets' progress in building radio telescopes such as a cross-type antenna system covering 80,000 square meters.

Analysis and Synthesis of Tunnel Diode Circuits, J.O. Scanlan, John Wiley & Sons, 274 pp., $9.75

A discussion of the sinusoidal aspects of tunnel diodes, covering both design theory and applications for narrow- and broad-band amplifiers.

Laplace Transforms for Electronic Engineers, James G. Holbrook, Pergamon Press, 344 pp., $10

Second, revised edition of 1959 book concentrates on practical applications of Laplace transforms in electronic engineering. Specific examples include Pascal's triangle for finding the transfer functions of iterated networks, the treatment of single-band, wide-range oscillators and charge amplifiers.

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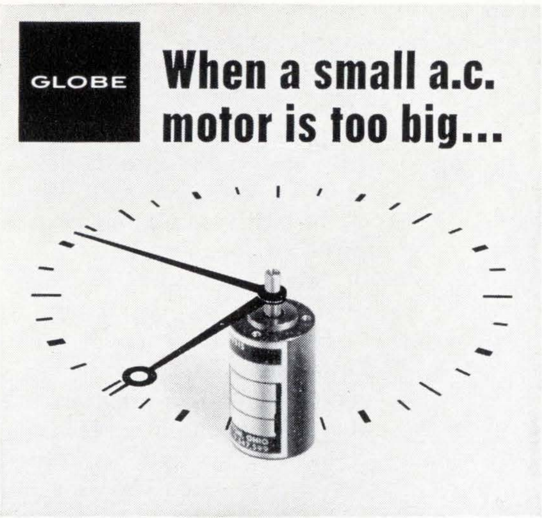

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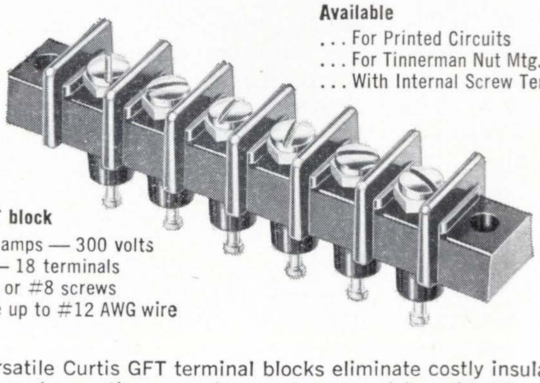

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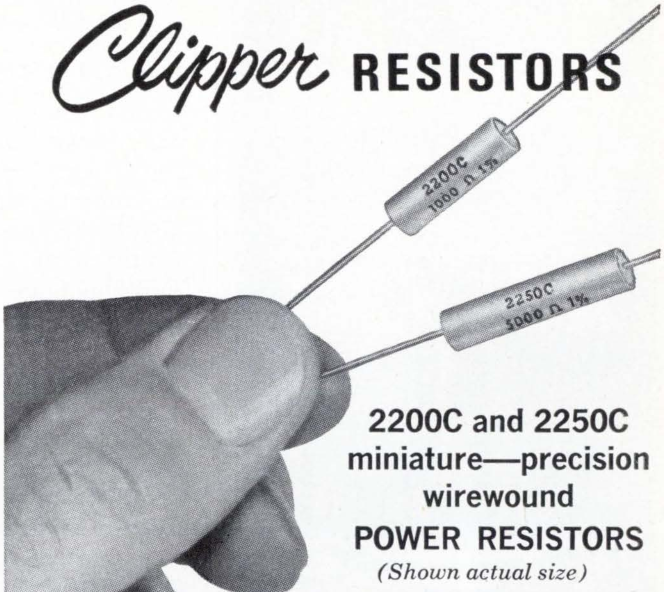

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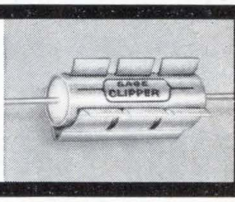

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Technical Abstracts

Building LSI

Partitioning for large-scale integration
H.R. Beelitz and H.S. Miller,
RCA Laboratories, Princeton, N.J.
R.J. Linhardt and R.D. Sidman
Electronic Data Processing Division,
Radio Corp. of America, Camden, N.J.

Large-scale integration will never be achieved if systems engineers continue to depend on current design technology. Irregularity in the control logic structure is the main limiting factor. Effective use of large-scale integration will require a new system architecture.

Many present-day computers use a memory-oriented design, where a multiplicity of registers store program instructions, addresses, machine status words, results and so forth, in one high-speed memory.

Associated with the memory is a logic loop by which data is repeatedly called forth from the memory, processed in a matrix inserted in the loop, and regenerated for storage in the memory again. A large portion of the machine's logic is circuitry that controls this data loop but is not directly associated with the data path.

The authors describe a systematic two-step partitioning procedure which overcomes this difficulty. The first step partitions the data path into registers and an associated processing matrix. In the second step, control logic is subdivided into two control functions, that is, information transfer control (instruction retrieval, data transfer) is separated from data process control. This allows functionally independent partitions to be distributed among the data path arrays.

As an example of LSI system architecture, the authors discuss Limac (large integrated monolithic array computer) a general-purpose machine being built by RCA for the Air Force and capable of solving complex navigational problems. Limac's main memory is a 4,096-word, 14-bit, 2-microsecond core array. A 100-nanosecond scratch-pad memory of 256 16-bit words is being made from arrays of complementary total oxide semiconductor transistors.

By functionally dividing the control and data path logic, Limac ends up with arrays of 30 gates or more with minimum gate-to-pin ratios of 1.4 to 1. This is an order of magnitude greater than that available in computers now in use.

Three current-mode logic circuits chosen for low power dissipation and small area, are used in the Limac computer. They include a basic array gate, an interface-buffer gate and a set-reset flip-flop.

Presented at the International Solid State Circuit Conference, Philadelphia, Pa. Feb. 16.

Assuring IC reliability

Modern approaches to microcircuit reliability assessment
R.C. Hilow, E.P. O'Connell, A.L. Tamburrino
Rome Air Development Center,
Rome, N.Y.

In selecting integrated circuits for high-reliability systems, a customer should avail himself of as much test data as he can. The problem here is that large-scale reliability testing of IC's is most economically performed by the manufacturer, and the results of these measurements are often extremely sensitive. Such data, for example, may describe proprietary processes or reveal yield figures that could affect pricing.

In this situation, the user can either press the manufacturer for this information or perform nondestructive screening tests himself.

If he takes the latter course, the customer should begin with a circuit analysis that includes pulse or a-c and d-c operations under various input and load conditions, and assesses the sensitivity of output characteristics to variations in component tolerance, drift, noise and supply voltage. The user should also evaluate the materials in the device and the packaging, including the method used to connect the die to the header. One advantage he has over the maker in conducting this study is that he can concentrate on the factors that relate directly to his application.

High stress tests can supplement this general device study. In such testing, stress is usually applied to

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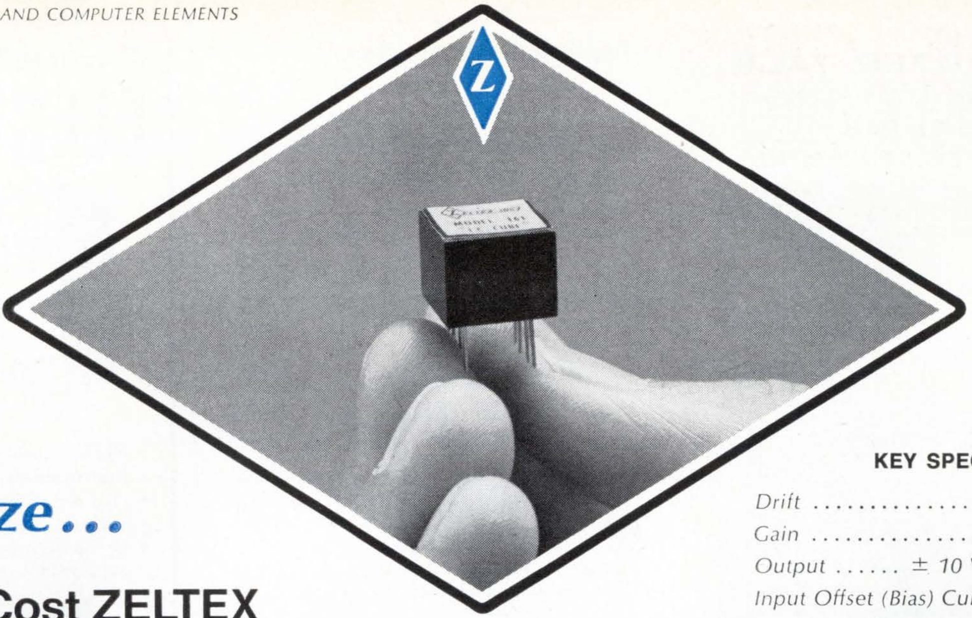

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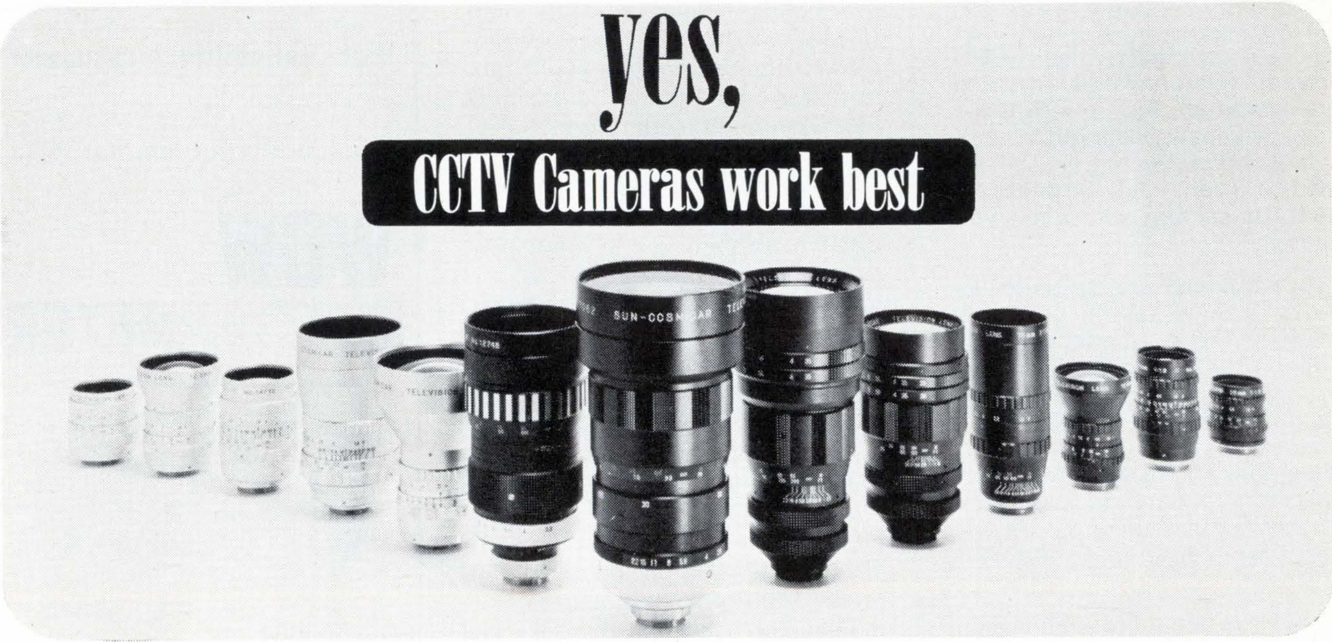

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Technical Abstracts

vital regions of the device at a normal or rated level and then increased until failure.

Accelerated life testing can also be performed, but the customer should be warned that some circuit degradation mechanisms do not age under high stress as they would under normal conditions.

All test data the customer comes up with, however, will prove a useful complement to the manufacturer's quality-control work and failure analyses.

Presented at the 1967 Symposium on Reliability, Washington, D.C., Jan. 10-12.

IC's and Biomedicine

Microelectronic bio-instrumentation and implants
Wen H. Ko
Case Institute of Technology, Cleveland

Applications in biomedicine currently fall into two areas—monitoring devices and stimulation systems. As a monitor, a microelectronic system could provide readings of a patient's brain waves, heart rate, blood pressure and respiration during surgery. A pattern-recognition system could rapidly scan parameters and signal any abnormalities during the operation.

Besides volume and weight considerations, the advantages of IC instruments here, as in other projected biomedical applications, are higher-speed performance, better reliability and lower cost than gear with conventional circuits.

One of the challenges facing microelectronics engineers is the development of transducers in which amplifiers and signal processors are integral parts, and in which, possibly, the sensor and associated electronics can be operated by power from biological sources.

In research work at the Case Institute, five types of single-channel telemetry transmitters have been built—three with discrete components, one with thin films and one with a multichip silicon IC. The latter device shows better frequency and temperature stability and much higher input impedance than the others, while consuming less power.

The IC transmitters have been

Technical Abstracts

implanted in rabbits, rats and mice to telemeter electrocardiograph signals. Metal input sensors were mounted on both sides of the transmitters and the assemblies were sealed with plastic, paraffin and silastic. With some electrode placements, respiration as well as EKG readings were obtained, with the respiration rate showing up as periodic variations in the EKG's line.

Presented at the Symposium on the Engineering Significance of Biological Sciences, Pittsburgh, Jan. 26-28.

'Listening' for IC defects

Screening silicon integrated circuits
B.C. Peralta
Battele Memorial Institute,
Columbus, Ohio

Failure-sensitive parameters are needed to detect the most common causes of integrated-circuit failure —surface phenomena or defects in bonding or metalization.

When IC chip surfaces have been purposely damaged in experiments, nonlinearities in the common-emitter families of curves have resulted. High-temperature storage aggravates the defects, and circuit analysis has shown that the nonlinearities result from negative-resistance regions. The defects are also found to be accompanied by an increase in low-frequency noise.

Devices studied were dual, two-input integrated circuits. Besides noise, the following parameters were considered for empirical screening of such devices: input, output, forward transfer and inverse transfer static characteristics; dynamic and d-c fan-out and fan-in; noise immunity, total element current, switching times and propagation delay. The surface phenomena defects appear to be related primarily to the low-frequency noise.

Areas that ought to be studied further include failures in multi-storage digital circuits, methods of stressing to enhance a failure-sensitive parameter without damaging a normal device, and improved instrumentation for measuring failure-sensitive parameters.

Presented at the 1967 Annual Symposium on Reliability, Washington, D.C., Jan. 10-12.

New Literature

Precision potentiometers. New England Instrument Co., Kendall Lane, Natick, Mass. A six-page brochure summarizes the company's capabilities in custom designed, conductive plastic and wire-wound pots and elements, and provides data on standardized Waferpot and Econopot lines.
Circle **420** on reader service card.

Analog telemetering system. Quindar Electronics Inc., 60 Fadem Road, Springfield, N.J., 07081, has available a four-page bulletin covering the QATS-10 analog telemetering system. **[421]**

F-m discriminator. Sonex Inc., 20 East Herman St., Philadelphia, Pa., 19144. A solid state f-m discriminator, capable of providing phase-locked-loop or pulse-averaging detection, is described in a two-color bulletin. **[422]**

Transistors and IC's. National Semiconductor Corp., Danbury, Conn., 06810, has released an 18-page catalog describing more than 500 types of silicon transistors and integrated circuits. **[423]**

Ceramic capacitors. King Electronics Inc., 150 Waverly Drive, Pasadena, Calif., 91105, offers a short-form catalog covering a complete line of microminiature ceramic capacitors. **[424]**

A/D interfacing system. Datametrics Corp., 8217 Lankershim Blvd., North Hollywood, Calif., 91605, has prepared a two-page data sheet on the model IS1108 analog-to-digital interfacing conversion system. **[425]**

Antenna systems. Andrew Corp., P.O. Box 807, Chicago, Ill., 60642, has released a catalog containing product information and engineering data on microwave, uhf, vhf, telemetry antennas, flexible coaxial cables and elliptical waveguides, switching and pressurization equipment and system accessories such as radomes, positioners and telescoping masts. **[426]**

Spacer/bushings. Sealectro Corp., 225 Hoyt St., Mamaroneck, N.Y., 10543. Press-Fit Teflon spacer/bushings for mounting p-c boards to metal panels are described in an illustrated catalog sheet. **[427]**

Environmental testing. Blue M Engineering Co., a division of Blue M Electric Co., 138th & Chatham St., Blue Island, Ill., 60406. A 16-page illustrated brochure describes the company's capabilities in the environmental testing field. **[428]**

Chemical specialty products. Transene Co., 121 Conant St., Danvers, Mass., 01923, has available a technical brochure entitled "Chemical Specialty Products for Solid State, Electronics, and Aerospace Industries." **[429]**

Mercury switches. MicroSwitch, a division of Honeywell Inc., 11 W. Spring St., Freeport, Ill., 61032, has released a booklet that describes applications of mercury switches in industry. **[430]**

Solid-state chopper. Airpax Electronics Inc., Cambridge, Md., 21613. Bulletin C-121R describes a prepackaged transistorized chopper that provides total isolation between drive and signal circuits. **[431]**

Digital displays. Tung-Sol division of Wagner Electric Corp., One Summer Ave., Newark, N.J., 01704, has published a booklet describing its line of optimum contrast, illuminated digital readouts. **[432]**

Miniature connectors. Elpac Microwave, a division of Elpac Inc., 3800 Campus Drive, Newport Beach, Calif., 92660. A two-page data sheet covers the OM-105 series of miniature connectors for flange, panel, bulkhead, and stripline mounting. **[433]**

Insertion-loss test set. Weinschel Engineering, Gaithersburg, Md. Application note No. 4 illustrates and describes a dual-channel insertion-loss test set. **[434]**

Data display system. Laboratory for Electronics Inc., 1075 Commonwealth Ave., Boston, Mass., 02215. Model SM-2A data display system is fully described in an eight-page, technically oriented brochure. **[435]**

Molded ceramic capacitor. Scionics Corp., 8900 Winnetka Ave., Northridge, Calif., has available a technical data sheet covering the S-Cap 500 series microminiature, axial-lead, molded ceramic capacitor. **[436]**

Heated-glass bonding tips. Specialty Glass Products Inc., 2561 Wyandotte Road, Willow Grove, Pa., 19090. Bulletin 2556 gives complete technical data on recently developed heated glass capillaries that fit standard magnetic holders and cost less than one-half as much as tungsten carbide tips. **[437]**

Voltage-sensing devices. Bourns Inc., 1200 Columbia Ave., Riverside, Calif., 92507, offers two technical bulletins, one on the model 3910 dpdt voltage-sensing relay, and the other on the model 3917 spst normally-open (solid state output) voltage-sensing module. **[438]**

Monolithic diode matrixes. Radiation Inc., Microelectronics division, P.O. Box 37, Melbourne, Fla. Applications of monolithic diode matrixes to electronic data processing systems are described in a 60-page manual. **[439]**

Prestressed mica. Perfection Mica Co.,

New Literature

1322 No. Elston Ave., Chicago, Ill., 60622. Data sheet K-8 tells how prestressed mica reduces handling and fabrication costs when used as electrical insulation and spacers in devices incorporating resistive heating elements. [440]

Tv connectors. ITT Cannon Electric, 3208 Humboldt St., Los Angeles, Calif., 90031, offers technical bulletin T-497 on the series LKTMA connectors for color and monochrome tv. [441]

Modular interconnection system. AMP Inc., Harrisburg, Pa., 17105. An eight-page bulletin describes a modular interconnection concept for perpendicular, or parallel stacking of p-c boards. [442]

Frequency scaler. Fischer & Porter Co., 143 Jacksonville Road, Warminster, Pa., 18974, has available a specification sheet on its frequency scaler, a divider and shaper network which converts the actual pulse rate from a transmitter or transducer to a more conveniently handled and decimally related pulse rate/engineering unit ratio. [443]

Parametric amplifier. American Electronic Laboratories Inc., P.O. Box 552, Lansdale, Pa., 19446, has available a technical bulletin on an avalanche diode-pumped parametric amplifier. [444]

Translatory potentiometers. Gamewell division of The E.W. Bliss Co., 1238 Chestnut St., Newton, Mass. A two-page bulletin describes precision potentiometers that are used to translate linear motion into resistive values. [445]

Tunnel mixers. Aertech, 250 Polaris Ave., Mountain View, Calif. Standard models including mixer mounts, stripline mixers, balanced mixers and waveguide units are covered in a technical data sheet. [446]

Memory systems. Honeywell Inc., Computer Control division, Old Connecticut Path, Framingham, Mass., 01701. A summary brochure describes features, system organization, interface and options for the ICM-40 and ICM-47 memory systems. [447]

Transducer amplifier systems. Natel Engineering Co., 7129 Gerald Ave., Van Nuys, Calif., 91406, offers a four-page catalog on its a-c/d-c transducer amplifier systems. [448]

Integrated circuits. Transitron Electronics Corp., 168 Albion St., Wakefield, Mass. An integrated-circuit data handbook, priced at $15, will be provided free to all qualified recipients. [449]

Permeability-tuned oscillator. TRW Electronic Components division, Davis and Copewood Streets, Camden, N.J., 08103, offers a specification sheet for its low-cost, transistorized, permeability-tuned oscillator. **[450]**

Core memory stack. Electronic Memories, 12621 Chadron Ave., Hawthorne, Calif., 90250. A four-page brochure describes the Nanostak, a 2½-dimensional core memory stack, with cycle times of 650 or 900 nsec, for use in the highest speed commercial computers. **[451]**

Printed-circuit laminates. The Mica Corp., 4031 Elenda St., Culver City, Calif., has available an eight-page catalog on high-reliability Micaply glass/epoxy laminates for printed circuits. **[452]**

Circular connectors. ITT Cannon Electric, 3208 Humboldt St., Los Angeles, Calif., 90031, offers catalog K-9, which includes complete product information, specifications, and ordering instructions for its line of K circular connectors and its LKTMA tv connector. **[453]**

Multiconductor wiring systems. Methode Electronics Inc., 7447 West Wilson Ave., Chicago, Ill., 60656, has published a catalog on its Plycon multiconductor card extenders and wiring systems. **[454]**

Shaft encoder. Theta Instrument Corp., Saddle Brook, N.J., 07662. Bulletin 66-14 describes a three-digit, binary-coded decimal shaft encoder for rugged industrial and scientific applications. **[455]**

Operational amplifiers. Melcor Electronics Corp., 1750 New Highway, Farmingdale, N.Y., 11735. A six-page condensed catalog (C1003), describes a complete line of solid-state operational amplifiers. **[456]**

R-f connectors. Sealectro Corp., 225 Hoyt St., Mamaroneck, N.Y., 10543, has released catalog 468-51C covering 65 microminiature r-f connectors in a 12-page display. **[457]**

Tachometer transducer. Airpax Electronics Inc., Box 8488, Fort Lauderdale, Fla., 33310, offers bulletin F-111-1 on the type TDS9 self-generating transducer designed for mounting on a rotating shaft for rpm measurement. **[458]**

Beacon magnetrons. Microwave Associates Inc., Northwest Industrial Park, Burlington, Mass., has published a four-page illustrated booklet (SF-1503) describing its complete line of fixed-frequency and tunable beacon magnetrons. **[459]**

Wideband data amplifiers. Dana Laboratories Inc., Campus Drive at Von Karman Ave., Irvine, Calif., has issued two data sheets with detailed descriptions of the series 3840 wideband data amplifiers and the series 3850 dual-output amplifiers. **[460]**

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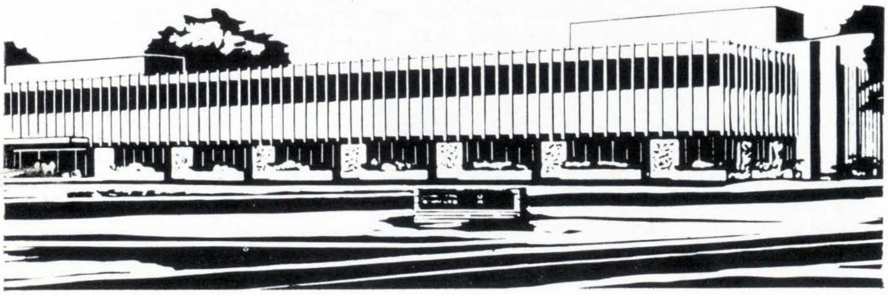

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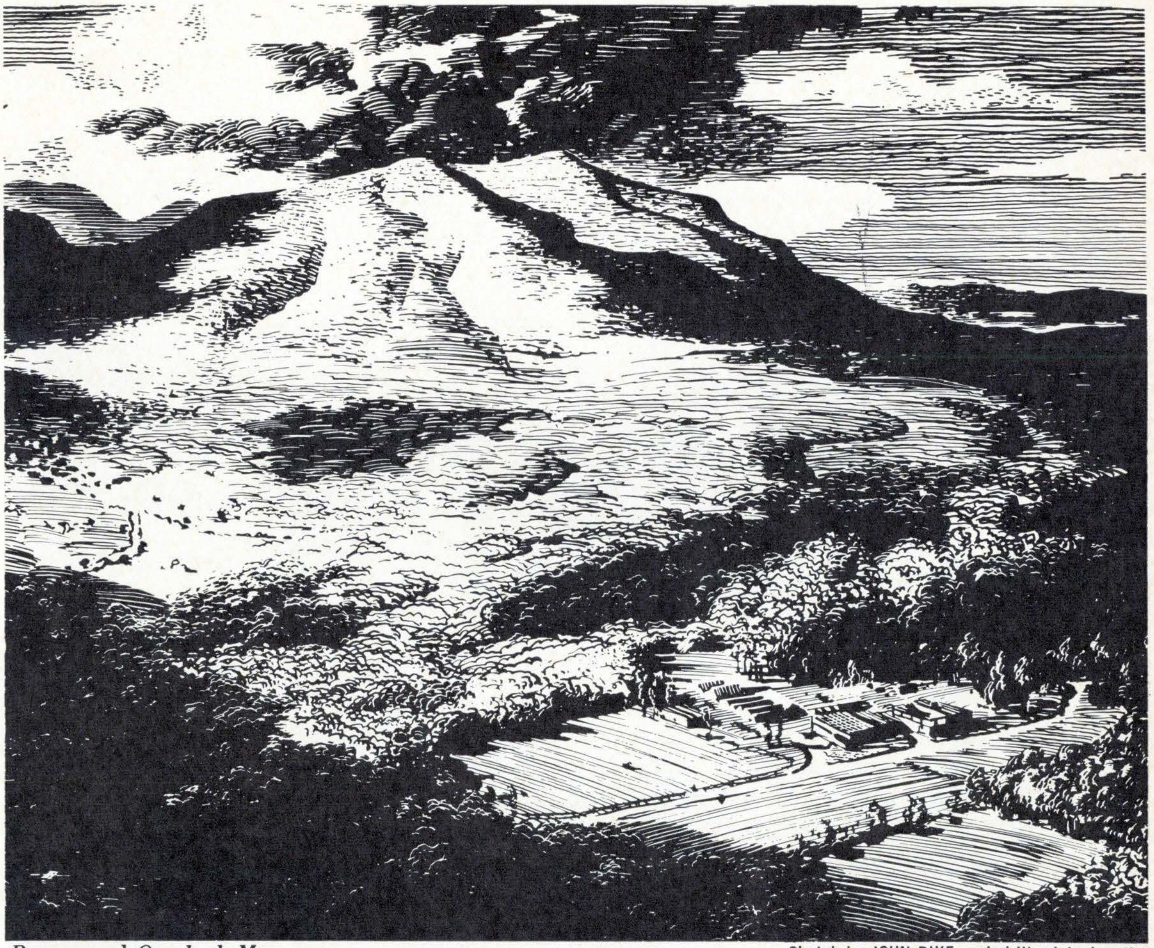

Rotron and Overlook Mt. Sketch by JOHN PIKE, noted Woodstock artist

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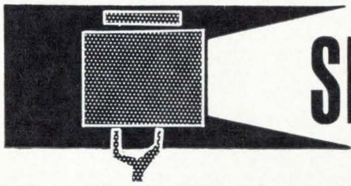

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12-66

Newsletter from Abroad

February 20, 1967

Matsushita aglow over new color tube

The Matsushita Electronics Corp. has pulled ahead of the pack in the scramble to get on the market with brighter color television tubes. **The firm has switched to a europium-activated yttrium oxide for the red-phosphor in all its tubes. The switch, it claims, makes the new tubes anywhere from 20% to 30% brighter than tubes using europium-activated yttrium vanadate, the prevailing "bright" red phosphor.** Matsushita is a joint venture of Philips Gloeilampenfabrieken NV of the Netherlands and the Matsushita Electric Industrial Co.

Matsushita's lead, though, most likely won't last long. **All the major U.S. color-tube producers are pushing phosphor technology hard and a spate of even brighter American tubes seems certain this year.** In Japan, Hitachi Ltd. also has an yttrium oxide phosphor in the works. Tokyo Shibaura Electric Co. (Toshiba), the country's largest producer of color tubes, however, is standing pat for the moment with its europium-activated vanadate tubes.

Pakistanis see satellites as way to skip over India

Pakistani telecommunications officials may turn to satellites to link their country's two regions without running cables through nearly 1,000 miles of Indian territory.

The satellites are being considered for a 20-year telecommunications expansion project now being mapped by Pakistan with support from the United Nations. The total outlay involved could run as high as $395 million, with most of the money coming from the World Bank and the Pakistani government. The Soviet Union and Italy, reportedly, also will extend credit for equipment purchases.

Hayakawa calculator has IC memory . . .

The Hayakawa Electric Co. jumped the gun on itself this month when it offered Japanese buyers a 14-digit desk calculator with an integrated-circuit memory. **The calculator—first production model in Japan with IC's—is about a half-year ahead of the all-IC calculator Hayakawa plans to start selling late this summer or early fall.**

For the IC memory, Hayakawa uses 28 identical circuit packages. On the chip: a low-speed quadruple two-input NAND circuit. The 28 packages replace a total of 112 transistors, 112 diodes and 326 resistors. **Because of the IC economies, Hayakawa sells the IC version for $972, some $200 cheaper than the predecessor model** with a discrete-component memory.

The circuit packages were developed jointly by Hayakawa and Mitsubishi Electric Corp. They are similar to the ones Hayakawa will use in its all-IC calculators.

. . . Nippon Electric shifts to IC's for small computer

The Nippon Electric Co. has indirectly doomed the parametron, a Japanese-developed majority logic device, with a new integrated-circuit ultrasmall business computer. Although NEC still hasn't dropped—officially—the ultrasmall parametron computer from its line, the new IC model is a heads-on competitor. Both models are aimed at the small-business market.

Desk calculators excepted, NEC is the sole computer maker with parametron models. **The company apparently plans to phase out its**

parametron model quietly in order to ward off a flurry of returns from users renting them.

The shift to IC's makes the new computer's logic circuits 300 times as fast as the parametron. For business computations, the faster speed of the IC logic can't be fully exploited because of limitations of the input and output circuits. All the same, the new ultrasmall computer is about **three times as fast as its parametron predecessor. When running scientific problems, its speed is about 30 times better.**

Core memory of the IC model has an 800-word capacity that can be doubled. The memory cycle time is 5.3 microseconds and the addition time averages 400 microseconds.

Small U.K. firm set to produce 'pocket' radar

Telta Ltd., a small London company that specializes in burglar alarms, apparently has beat Britain's electronics giants in the scramble to get into production of the matchbox-size radar developed by the Royal Radar Establishment. **The Telta tiny radar probably will be on the U.K. market within a month, priced at about $250.**

Like the Royal Radar prototype, Telta's pocket radar uses a gallium arsenide Gunn-effect diode oscillator as the microwave source. Although Mullard Ltd., a subsidiary of Philips Gloeilampenfabrieken, developed the diode used in the prototype, **Telta says another supplier—whom it won't name—quoted a better price than Mullard.**

Saab wings upward in computer sales

After two lean years, sales have suddenly spurted at home and abroad for Datasaab, the computer division of the Swedish aircraft and auto maker Saab AB. A half-dozen early-year orders pushed to 30 the number of Saab computers that will be in service by this summer.

The small flurry brought Datasaab **its first important export business: a pair of computers each for Czechoslovakia and Finland. Datasaab officials see more export business in the offing.** Gunnar Lindstrom, the division's managing director, says negotiations are under way with companies in several countries.

For the Czech orders, **Datasaab bested British and American competitors at last year's Prague computer show.** One of the Swedish computers will go to the University of Brno; the other will be used by a Prague construction organization.

The Finnish order for two computers came from Wartsila, a privately owned industrial group with a heavy emphasis on shipbuilding. Wartsila will swap computer programs and know-how with Kockums Mekaniska Verkstads AB, a Malmo shipbuilding outfit that together with Saab has developed a computer program to generate hull shapes.

Computer system to aid Bobbies

Britain's Home Office—the country's law and order agency—intends to back up its policemen with a real-time computer system. **The agency this month completed a feasibility study and, when details are worked out, will follow through on the project.**

The system will store data on wanted men, stolen property and the like. When they run into suspicious situations, Bobbies on the beat will query the computer system by means of walkie-talkies. The Home Office already has begun to equip police with small two-way radios and all constables will have them by the spring of 1968.

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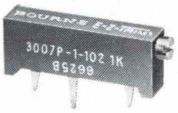

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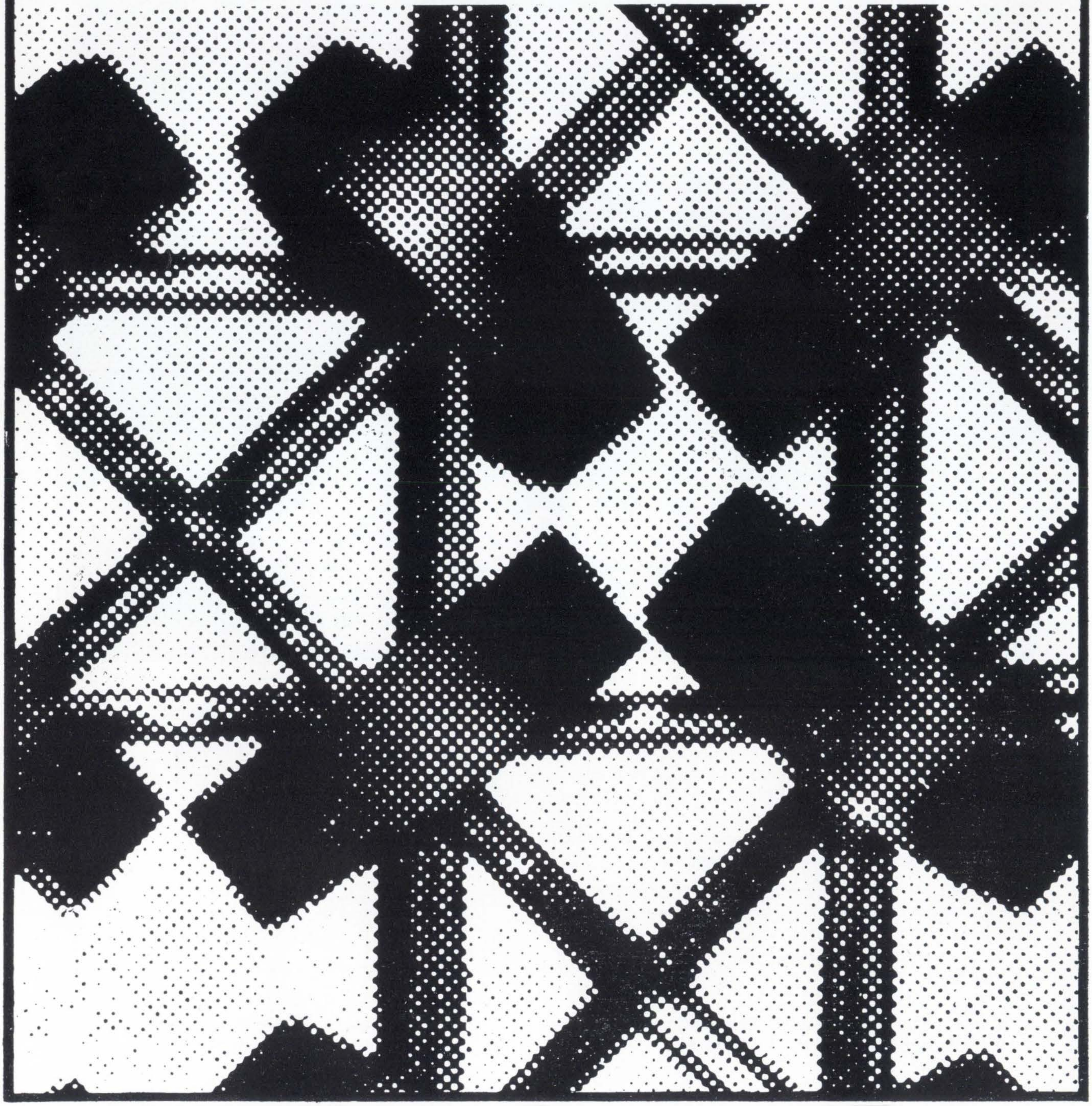

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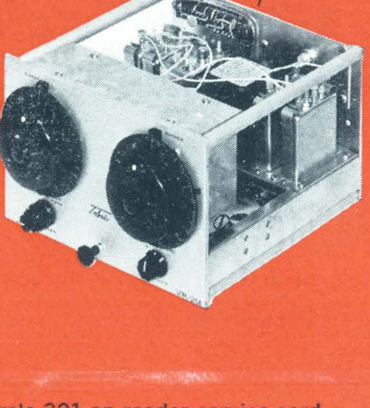


Circle 321 on reader service card

Electronics Abroad

Volume 40
Number 4

France

Countdown

The day of the conventional $1,000 digital voltmeter is fast approaching an end. For producers of the instrument the question is not whether but when to switch to integrated circuits to cut its cost and package size.

France's Schneider Radio Television contends it will be another two years or so before IC's will be competitive with discrete components for digital voltmeters. And Schneider has readied for market an instrument that backs up the contention. At this April's Mesucora control and instrumentation show in Paris, Schneider will start selling a discrete-component digital volt-ohm-ammeter with a retail price tag of about $300, equivalent to a manufacturer's price of less than $200.

Competitive. To be sure, Schneider's $300 digital multimeter doesn't come anywhere near the "less than $100" predicted as an eventual going price for digital multimeters built around IC's—much to the annoyance of some instrument makers [Electronics, Jan. 9, p. 7]. However, Schneider's discrete-component instrument apparently will compare favorably to the first IC digital multimeters. It's a safe bet that some American instrument maker will introduce an IC digital multimeter that handles only direct-current measurements for under $300 at next month's Institute of Electrical and Electronics Engineers exhibition. In that case, the Schneider instrument will have the edge; it handles alternating-current as well.

The Digitest, as Schneider calls its digital multimeter, is built up of discrete components arranged in cordwood modules. The circuitry is based on the double-ramp technique, which converts the analog input into a pulse whose width is proportional to the input amplitude. Digital circuitry, with a clock-rate of 400 megahertz, converts the pulse width into a three-digit readout.

Ranges. The instrument measures 10 by 6 by 6 inches and is powered by five 1.5-volt dry cells. All in all, the multimeter has 23 measurement ranges. For d-c, five cover voltages from 100 microvolts to 1,000 volts and four currents from 100 nanoamperes to 1 amp. For a-c, the span is from 1 millivolt to 300 volts in five ranges and 1 microamp to 300 milliamps in four ranges. The ohmmeter's five ranges extend from 0.1 ohm to 1 megohm. Input impedance is 5 megohms for most voltage ranges and the accuracy runs from 0.5% ±1 digit for d-c voltages to 2% ±1 digit for a-c currents.

Schneider plans to turn out 2,000 or more of the discrete-component digital multimeters before it goes into production on an IC version already under development. Before the IC version comes, though, Schneider will upgrade the current model with rechargeable-battery and line-operated options. Also on the way are accessories like a very-high-frequency probe, a high-voltage probe and a capacitance probe.

Changing the guard

There's a new man in the top slot at the French electronics industry's trade association and a new direction for the industry may be in the offing.

Named last month as president of the Fédération Nationale des Industries Electroniques was Jacques Dontot, the 51-year-old managing director of Compagnie Française Thomson Houston-Hotchkiss Brandt, one of the heavyweights in the industry. Dontot is convinced that many of the industry's woes could be cured by more aggressive selling in export markets. And Dontot feels the in-

By the numbers. Schneider Radio Television has set a $300 retail price for the digital multimeter it will introduce in April.

dustry should widen its contacts in the de Gaulle government even though the administration has already solidly backed electronics companies in their export efforts.

Active. As FNIE's new president, Dontot has tread softly thus far. But people in the industry expect he'll soon pump new life into the trade association. Says an executive of La Radiotechnique SA, a subsidiary of Philips Gloeilampenfabrieken NV and a major French producer of consumer electronics and components: "Dontot will vastly strengthen FNIE's stature abroad." And one of his business associates says that under Dontot the industry association will become "much less passive and more active."

A less-passive FNIE, though, means some run-ins with the government's Ministry of Finance, which over the past two years has let a half-dozen American semiconductor producers build plants in France. The de Gaulle government justified its action on the grounds that American companies would bring in advanced technology needed for defense and space projects.

Dontot thinks the government has overdone it. He says, "When companies from one big country install plants in one smaller country and all in the same sector of a single industry, that is economic colonization."

At a time when government spending on classic military electronics has begun to drop, Dontot sees difficulties ahead in state-industry relations in research and development. From outright financing of prototypes of hardware needed for major equipment programs, the government recently has tended more and more toward "concerted actions" in which government and industry split the bill for research. Even though the sums French companies plow back into research often top—as a percentage of sales—the R&D money spent by American companies, Dontot considers the total funds available for research "greatly insufficient."

Broader base. Dontot, though, figures French companies could

Jacques Dontot now heads the French electronics trade association.

pour more money into research if they'd move more vigorously into export markets. In his opinion, they need immediate beachheads abroad since they don't have a huge domestic market—as do U.S. companies—to write off development costs of new products.

Dontot maintains FNIE members could learn much from their toughest competitors, American companies adept at market studies and product planning. To cope with what he terms "savage" competition, Dontot says the French industry should seek out openings in export markets where it can score. And even though FNIE runs a major components show every year [see related story p. 16], Dontot thinks sales managers should concentrate less on flashy, expensive exhibits and more on getting hustling salesmen out into export markets.

Japan

Color it rosy

This month, a spate of under-$500 color television sets started turning up in radio-tv dealers' showrooms throughout Japan, heralding the beginning of a color boom.

With the domestic market ready to take off and exports to the United States on the upswing, Japanese set makers now are geared up to turn out more than a million color receivers this year—double the 1966 figure. Largely as a result, the electronics industry is headed for a banner year.

The Electronics Industries Association of Japan now estimates that the 1967 output of electronics will total something like $3.16 billion. That's a gain of 22% over last year's $2.59 billion. Although color tv will show the strongest increase, the industry's rise will range across the board. In 1966, consumer electronics output was $1.23 billion, industrial electronics $625 million and components $735 million.

Star performers. Along with color tv, fast growth is forcast for auto radios, spurred by the demand from Japan's burgeoning auto industry. For other consumer products, production increases are estimated at somewhat less than 20%.

In industrial electronics, computers look to be the standout with an expected rise of about 35% over 1966. Video tape recorders and industrial tv equipment also are slated for strong gains, but are dwarfed in volume by computers.

Italy

Color it later

Prospects for Italian television-set producers paled considerably this month. In voting funds for the country's current five-year economic plan, the Chamber of Deputies tacked onto the appropriation bill an amendment banning any government spending for color tv through 1970.

The measure, first proposed last fall by Premier Aldo Moro's coalition government and fiercely fought by the industry since, hits set producers at a time when the market for black-and-white receivers shows signs of weakening. Tv sales have held at a level of about one million sets annually in recent years, but there's been a shift to low-priced sets during the past two years. Until the government decided color tv was a frill the country couldn't afford, set producers had counted on a lift from color sales starting in 1968.

Long-term worry. Along with their short-term worries, Italian tv firms are uneasy over the foreign competition they'll have when the state-owned broadcasting network finally gets around to colorcasting. Most Italian set makers can't afford to invest money now for color-receiver development with returns years off. Meanwhile, Dutch and German producers will be picking up manufacturing and sales know-how in their domestic markets and thus will have an edge over native producers when color tv comes to Italy.

Great Britain

Caught by a wave

Along with a lot of new material for night-club comics, the recent rash of large-scale robberies and jailbreaks in Britain has spawned a fully transistorized standing-wave protection system for warehouses and similar large buildings.

Standing-wave protection gear has been fairly common in the United States for some time but so far hasn't caught on in Britain. Telta Ltd., though, sees bright prospects for its new, small, ultra-high-frequency units. Telta claims it's made the system foolproof and every time a big robbery makes the headlines, Telta gets some free sales promotion. The basic system rents for about $850 a year.

Watchful. The equipment consists basically of a crystal controlled uhf transmitter that puts out a standing wave picked up by a separate receiver. When an intruder moves anywhere within a monitored space where nothing should be moving, he disturbs the standing wave. The receiver detects the disturbance and triggers an alarm.

Each transmitter-receiver pair can monitor up to about 200,000 cubic feet of space. Since most warehouses are larger than that, Telta has designed its equipment so several pairs can be used together to cope with big buildings.

Ordinarily, more than one transmitter working in a closed space would bring interference problems. Telta says it has solved the problem but won't say how because the system's antijamming circuitry is tied in with the interference rejection. For high selectivity between adjacent channels, the receivers are double superheterodyne types.

Discriminating. In addition to the capability of side-by-side operation of the receiver-transmitter pairs, Telta's standing-wave equipment has an analog memory circuit that distinguishes between unimportant movements like a crate falling and a significant movement like a man prowling inside a warehouse at night. The control on intensity of the uhf field is so close that no external shielding is needed on normal walls to prevent movements on the outside from triggering the alarm. The system also compensates for temperature changes over the range from 30°F to 100°F.

The transmitter and receiver units have twin power supplies. The system normally works on line voltage but has standby batteries to keep the protection in force during line-power failures. The transmitter unit measures 6½ by 5 by 3 inches and the receiver 6½ by 8 by 3 inches.

Poland

The collector

One of the most tedious tasks for laboratory assistants anywhere is collecting distillates, counting them drop by drop. For many Polish laboratory workers, laborious drop-counting will soon be a thing of the past now that the Experimental Establishment for Scientific Apparatus in Warsaw has developed equipment that does the job automatically.

The equipment marries an electronic drop-counter and timer to distilling gear with a servocontrolled revolving glass spout. Counting pulses are picked up by a photoresistor mounted in the spout. As each drop falls out of the spout, it interrupts a light beam played on the photoresistor and generates a pulse. The pulse is shaped and fed to a two-decade counter. The decade terminals are tied to rotary switches so that a preselected number of drops, ranging from 1 to 100, can be collected and the spout then shut off. A timer in the counting equipment provides for reset to zero after an interval of from 1 to 100 minutes.

The revolving spout can feed distillates into any of 240 standard test tubes arranged in five rings around the distilling column. Whenever a preset count is reached, the counter sends a signal to the spout servosystem which shuts off the spout and shifts it to the next test tube.

West Germany

Electronic St. Bernard

Each year, the delight of Alpine skiing suddenly becomes horror for hundreds of skiers buried under masses of snow by avalanches. Rescue teams guided by trained dogs find most victims in time but on the average, 70 lives are lost each winter.

Electronic rescue equipment that promises to reduce the death toll, however, now is finding its way into many European skiing areas. The equipment, basically a highly sensitive flux gate magnetometer, spots the small magnetic field of a tiny magnet sewn into a skier's clothing or worn as a pendant around his neck. The West German skiing association has mounted a campaign to get its members to wear the magnets whenever they're in avalanche country and skiing clubs in other Alpine countries are following suit.

Apres ski find. The idea of using magnetics to find skiers buried under snow first was hit upon in 1961 by a pair of scientists working for the Swiss subsidiary of Varian Associates. Varian proved the idea worked in tests first with a proton free-precession magnetometer and later with a rubidium gradiometer. Varian has sold a few $5,000 cesium magnetometers in Europe for use as avalanche-victim detectors. The Alpine market, though, is dominated by a small South German company—Institut Dr. Foerster—whose rescue equipment sells for $1,000 to $1,250, depending on how sophisticated the model.

Basically, the Foerster equipment consists of a 7-pound electronic unit carried on the rescuer's back and a 5-foot hollow aluminum pole with a sensor dangling from one end. The rescuer sweeps the sensor just above the snow. A meter on the pole shows when the sensor has passed over a magnet carried by a buried skier. A spotted magnet also is signalled by a 1,000-kilohertz tone from a small loudspeaker. The equipment can pick up magnets buried under snow as deep as 10 feet.

Alpine lifesaver. Sensor dangling from aluminum pole can spot skier buried under 10 feet of snow—if he's wearing tiny permanent magnet. Electronics pack carried on rescuer's back weighs just 7 pounds.

Sensitive. Actually, the basic operating principles of the device are similar to those that have been used for some time in magnetic detectors for finding mines or underground pipes. However, in the avalanche-victim detector, the sensitivity is much higher. The avalanche detector measures field strengths from 1 oersted to 10 microoersteds but nonetheless remains insensitive to the earth's 500 millioersted magnetic field.

The sensor is made up of a pair of probes interconnected so that the earth's field cancels out. Each probe has a high-permeability iron core that is saturated by a primary, or exciting, coil, plus a secondary measuring coil. An exciting current developed in a 10-khz stabilized oscillator magnetizes the core; and when the probe approaches the field of a skier's magnet, an output voltage proportional to the intensity of the detected field develops across the secondary coil. This voltage is filtered, amplified and rectified to deflect the meter and produce the 1,000-khz tone.

Second harmonic. The high sensitivity of the field strength measurement stems from the flux waveform of the iron core. It is magnetized to saturation by a field that varies sinusoidally. The flux curve, however, is not sinusoidal because of hysteresis. Fourier analysis shows that the flux waveform contains only the fundamental frequency and odd-numbered harmonics. This is because the hysteresis loop and the magnetizing field have point symmetry about the zero axis.

The symmetry, though, is upset whenever a small magnetic field (like that of a buried-skier's magnet) is superimposed on the sinusoidal core excitation. The flux curve then contains even-numbered harmonics and their amplitudes are a measure of the intensity of the external field. In the avalanche-victim detector, only the second harmonic is used as a gauge of field intensity. The other even harmonics are filtered out.

Faster forecasts

Although they still can't do anything about it, meteorologists in West Germany now can talk about the weather with more assurance than ever. For their forecasts, they're getting more data — and faster — over a new 3,000-hertz teleprinter link that joins the headquarters of the U.S. Weather Bureau in Washington to the West German central meteorological office in Offenbach, near Frankfurt.

The link, put into service last month, can move data at a rate of 1,050 bauds. It replaces 240-hertz, 75-baud equipment and can handle as much data in one hour as the old link could in 15. Even better, the new bandwidth makes possible facisimile transmission of weather charts, impossible before. Washington now transmits 96 charts a day to Offenbach. Offenbach sends Washington almost as much weather data, excluding charts, as comes in.

International. The faster data flow aids weather forecasters throughout Europe because the air masses that determine continental climatic conditions flow from West to East. To speed the spread of the information, direct lines tie Offenbach to Paris and Bracknell, near London. All West European weather bureaus use one of these three centers as their data source for long-range forecasting. Offenbach also serves as regional forecast headquaters for the International Civil Aviation Organization and transmits flight weather bulletins to airports in Northern Europe.

Let EDP do it. For the time being, the data fed into Offenbach over the new link is analyzed by meteorologists who then draw up charts that show existing weather conditions and what's likely to come. Later, probably starting this summer, computers will take over.

The computer system will evaluate data fed into it by punched tape, weeding out information that doesn't fit the general weather pattern. It will then print out weather charts showing current conditions and—if programed accordingly—produce charts showing the weather most likely to develop over the next few hours.

At the outset the Offenbach center will use the two Control Data Corp. computers it already has—a CDC 3400 and a CDC 3800—for the weather analysis. A CDC 1700 will be added later this year. A digital printer, to come from California Computer Products Inc., will make the charts.

Sweden

Talk-box takeover

The L.M. Ericsson Co., long the leader in Swedish telecommunications gear, this month moved to the forefront in intercommunication equipment as well.

In the Swedish electronics industry's biggest acquisition deal in years, Ericsson took over the intercom business of AB Gylling and Co., an expanding family-owned firm. Gylling last year had total sales of $20 million. Some $15 million came from intercom equipment, making Gylling a world leader in the field. The company's sales in the United States last year were $2 million.

Ericsson will merge Gylling's intercom operations and its own in a newly formed subsidiary, L.M. Ericsson Telemateriel AB. Telemateriel will now dominate the Swedish intercom market: Gylling's share was 60% and Ericsson's 20%. The only other producer of intercoms in the country is Standard Radio and Telephone AB, a subsidiary of the International Telephone and Telegraph Corp.

Pinched. Despite fast-rising sales that carried it from $2 million in 1965 to $20 million last year, Gylling, as a family-owned company, had trouble financing its expansion and for that reason sold its intercom operation to Ericsson. Neither company will disclose the price.

Gylling, though, will stay in business to produce components and radio and television sets. The company currently is the top Scandinavian producer of printed circuits. Gylling also handles Swedish sales for Japan's Sony Corp.

International

Well spaced

Success apparently breeds success in Europe's joint satellite program.

This month, a four-company consortium headed by France's Engins Matra won a $20 million contract to build two research satellites for the European Space Research Organization (ESRO). It was the largest contract yet awarded by ESRO and winning it meant a repeat performance for two companies in the consortium.

Matra was the major subcontractor for the first ESRO satellite, slated for launching next month. The British partner in the consortium, Hawker Siddeley Dynamics Ltd., was the main contractor. And whenever Matra and Hawker Siddeley have been involved in ESRO satellite contracts, so has the TRW Systems Group as an adviser. The other two companies in the consortium are West Germany's Entwicklungsring Nord and Saab AB of Sweden.

Heaviest. The $20 million contract covers a pair of 880-pound satellites, the fourth and fifth in ESRO's current 8-year program and the heaviest ordered so far. The first of the heavy satellites will be launched in the summer of 1970 during a period of intense solar activity. Its major mission will be gathering cosmic-ray data in the ionosphere. The other satellite is scheduled for launching in the spring of 1971 and will be instrumented for observation of infrared and ultraviolet radiation from stars.

The two satellites will be launched from the Vandenberg Air Force Base in California using Thor-Delta rockets supplied by the National Aeronautics and Space Administration. Esro has designated the satellites TD 1 and TD 2.

Around the world

Sweden. The prototype of the Viggen all-purpose supersonic aircraft was test-flown for the first time this month. The Viggen project will be a mainstay for the Swedish electronics industry during the next few years but not the bonanza first thought. The original $2 billion, 800-plane project most likely will be cut back to between 400 and 500 planes.

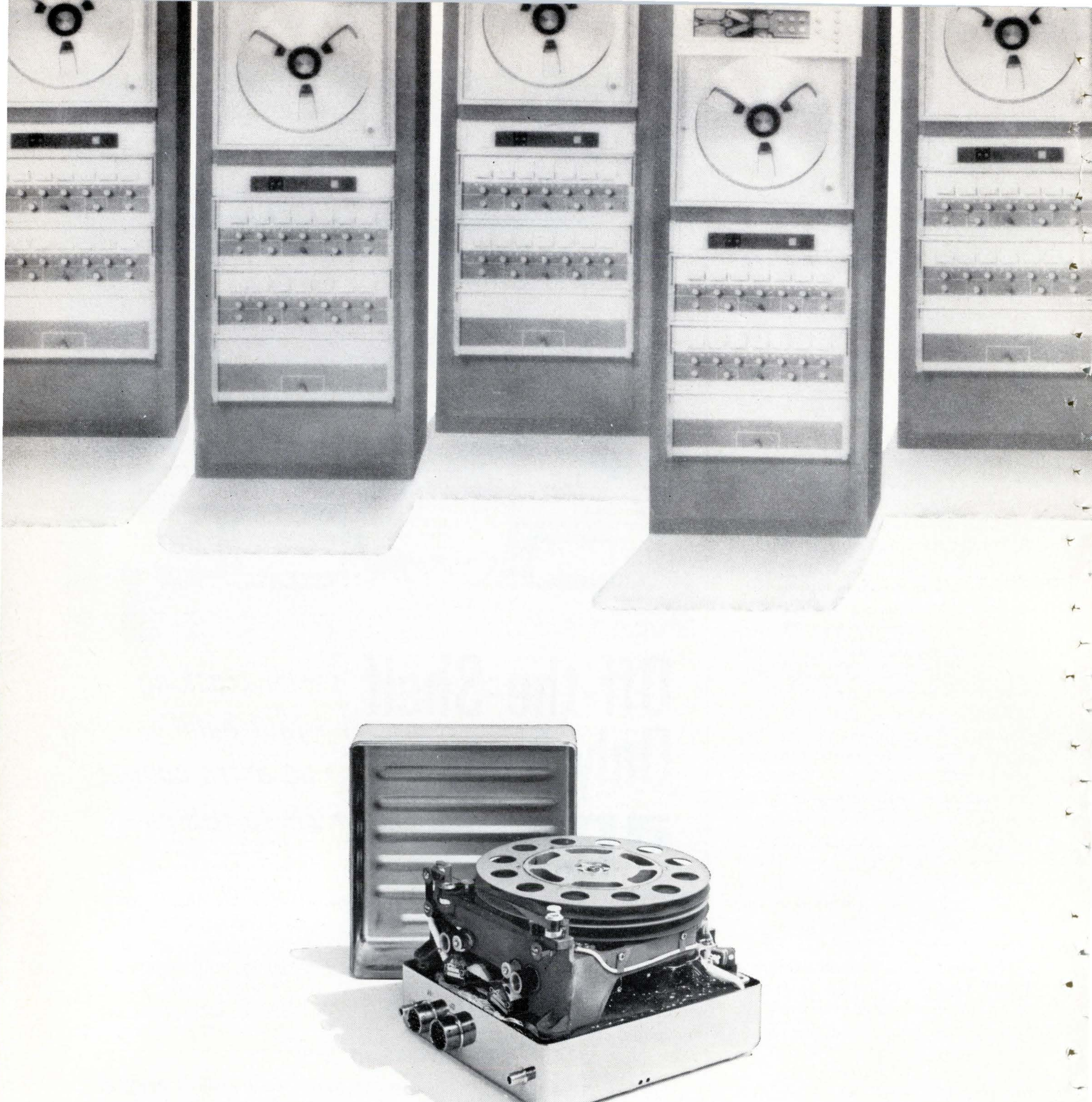
Austria. Like its West European neighbors, Austria has decided to adopt as its color television standard the West German PAL system. However, the ministry for telecommunications plans to continue backing an effort to develop a two-standard receiver compatible with the French Secam system. The reason: Austria's eastern frontier borders on Czechoslovakia and Hungary, both Secam countries.

Kenya. About $1 million of data processing equipment is slated to be delivered this year to Kenya. Most will come from Britain's International Tabulators & Computers Ltd. for use by government agencies. That company sees a market in the offing for business and industrial computers and to hold its dominant position in the country already has set up a programers school in Nairobi.

Norway. The David-Anderson Radio Co. of Oslo has begun to score in export markets with its riometer, an instrument that measures variations in the ionosphere. The company recently delivered 11 riometers to West Germany's Max Planck Institute and says it has other export orders on its books.

Holland. Philips Gloeilampenfabrieken NV has started producing color television sets for the Dutch market. The first sets will go on sale in mid-summer, priced about $780. Eastern Holland is within range of German stations that will begin colorcasts this autumn.

Czechoslovakia. An international center for research in use of computers for economic planning will be set up in Czechoslovakia, most likely in Bratislava, with financial support from the United Nations.



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