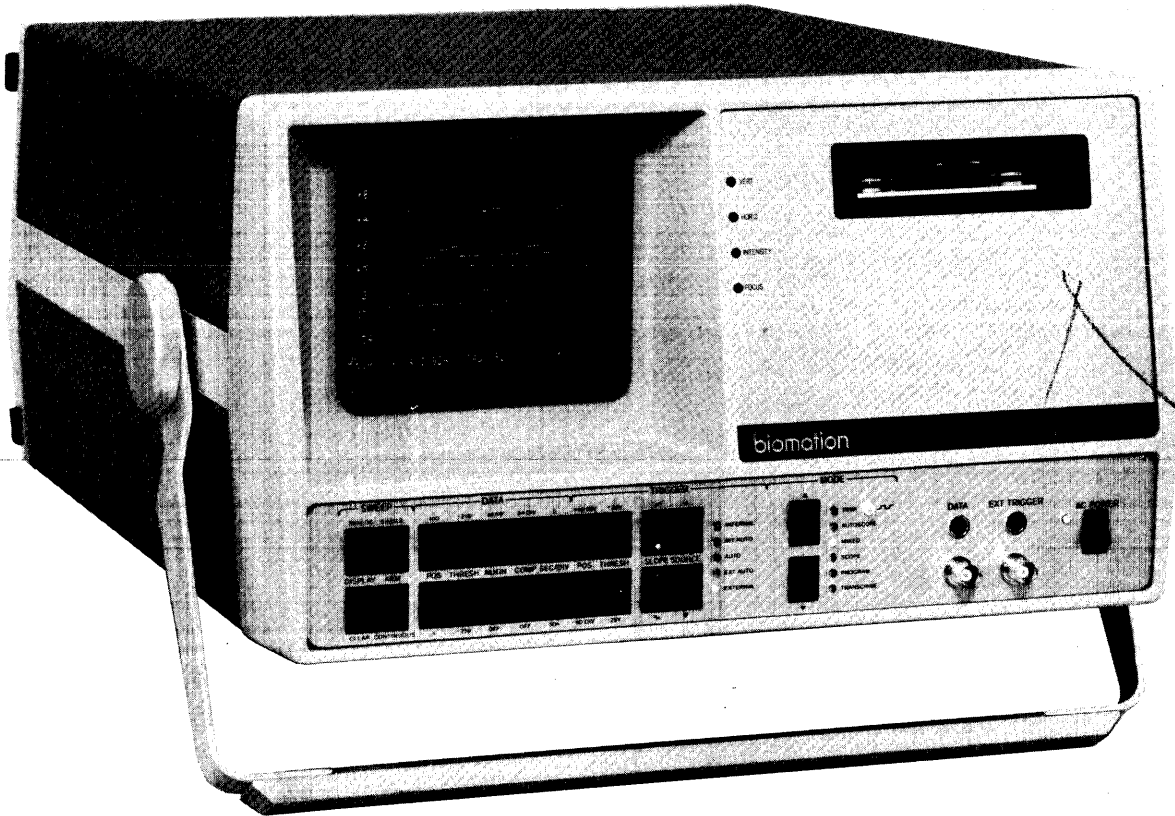# biomation

MODEL DTO-1
DIGITAL TESTING OSCILLOSCOPE

OPERATING AND SERVICE MANUAL

GOULD

OPERATING AND SERVICE MANUAL

MODEL DTO-1

Table of Contents

SECTION I

GENERAL INFORMATION

1.1   Certification

Gould Inc. certifies that this instrument was thoroughly tested and found to meet its published specifications when it was shipped from the factory.

1.2   Warranty

All Gould Inc. products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products that prove to be defective during the warranty period. If a unit fails within thirty days of delivery, Gould Inc. will pay all shipping charges relating to the repair of the unit. Units under warranty, but beyond the thirty day period, should be sent to Gould Inc. prepaid and Gould Inc. will return the unit prepaid. Units out of the one year warranty period, the customer will pay freight charges. IN THE EVENT OF A BREACH OF GOULD INC.'S WARRANTY, GOULD INC. SHALL HAVE THE RIGHT IN ITS DISCRETION EITHER TO REPLACE OR REPAIR THE DEFECTIVE GOODS OR TO REFUND THE PORTION OF THE PURCHASE PRICE APPLICABLE THERETO. THERE SHALL BE NO OTHER REMEDY FOR BREACH OF THE WARRANTY. IN NO EVENT SHALL GOULD INC. BE LIABLE FOR THE COST OF PROCESSING, LOST PROFITS, INJURY TO GOODWILL, OR ANY SPECIAL OR CONSEQUENTIAL DAMAGES. THE FOREGOING WARRANTY IS EXCLUSIVE OF ALL OTHER WARRANTIES, WHETHER EXPRESSED OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

1.3   Instrument Description

The Model DTO-1 Digital Testing Oscilloscope is a multipurpose instrument used for the design, test, and maintenance of digital equipment. Among its many features is the ability to compare automatically logic traces from a unit under test against prerecorded logic traces from a known good system.

The DTO-1 is basically a logic recorder that digitizes signals one at a time and displays up to eight logic traces on a common time scale. These logic traces can provide pretrigger and/or delayed information. Digitized signals and their associated attributes can also be stored on magnetic tape, then recalled for logic trace display at a later date. Logic traces from magnetic tape and logic traces from newly digitized signals can appear simultaneously on a common time scale. The "old" traces can be automatically expanded or compressed up to 25% to compensate for differences in clock rates between the "old" traces and the "new" traces. Each "new" trace can be automatically compared to a corresponding trace from magnetic tape to determine whether disagreements are within acceptable limits. The result of this comparison is indicated by PASS/FAIL LEDs. The exact areas of logical disagreement are also underscored on the display.

In addition, a signal can be digitized to one part in 39. The resulting analog waveform and up to three logic traces can be simultaneously displayed on a common time scale.

1.4 Specifications

INPUTS

Data (Referred to tip of probe).

Impedance. 10 MΩ, 15 pF.

Voltage range. $\pm$25 V, protected to $\pm$200 V.

Threshold voltage. $\pm$25 V, adjustable in 0.1 V steps, accurate to $\pm$100 MV $\pm$3% of reading.

Minimum pulse width. 10 ns when 50% or more of pulse height exceeds the threshold voltage.

Sample rate. 2 Hz to 100 MHz, accurate to 0.1%.

Number of bits stored. 1000 per trigger event.

Resolution[*] of stored bits. 50 ns to 1 μs/div -- 10 ns. 2 μs to 5 s/div -- $\frac{s/div}{100}$.

Trigger (Referred to tip of probe).

Impedance. 10 MΩ, 15 pF.

Voltage range. $\pm$25 V, protected to $\pm$200 V.

Threshold voltage. $\pm$25 V, adjustable in 0.1 V steps, accurate to $\pm$200 mV $\pm$3% of reading.

Minimum pulse width. 20 ns when 50% or more of pulse height exceeds the threshold voltage.

Source. Internal, Internal Auto, Auto, External Auto and External.

Slope. Positive or Negative.

Position (Referred to one division from left[*] side of display). -180[*] divisions to +180[*] divisions in 0.1 division steps, accurate to $\pm$0.1% of reading $\pm$2 samples.

COMPARE

Resolution[**]. 50 ns to 1 μs/div -- 40 ns. 2 μs to 5 s/div -- 4X $\frac{s/div}{100}$.

OUTPUT

Probe Calibration Signal. 1 kHz squarewave 0 to +4 V.

Auxiliary Power for Optional 10-TC Pod. +5 V $\pm$0.25 V, 360 mA; -5.2 V $\pm$0.2 V, 100 mA.

TIME BASE

Sweep Ranges. 50 ns per division to 5 s per division in 1-2-5 sequence, accurate to 0.1%.

DISPLAY (Biomation Model 350).

CRT.

Screen area. 8 x 20 cm.

Graticule. External, 8 x 10 divisions.

Deflection. Electrostatic.

Phosphor P31.

Characters.

Height. 0.25 cm.

Width. 0.20 cm.

Horizontal spacing. 0.25 cm on centers.

Logic Traces.

Height. 0.5 cm.

Length. 10 cm.

Horizontal resolution. 20 bits/cm.

Time resolution[*]. 50 ns to 0.2 μs/div -- 10 ns. 0.5 μs/div -- 25 ns. 1 μs to 5 s/div --5X $\frac{s/div}{100}$.

Analog Display Area.

Height. 3.9 cm.

Length. 10 cm.

Vertical resolution. 10 dots/cm, 39 total.

Horizontal resolution. 20 dots/cm, 200 total.

[*]$\pm$130 divisions in Program Mode.
[**] For trigger position from +7.0 to -130 divisions.

Sensitivity. 0.5 V/cm to 10 V/cm in 1-2-5 sequence.

Amplitude resolution. 1 part in 39.

MISCELLANEOUS

Memory.

Standard. 4K bytes.

Optional. 16K bytes.

Transcribe.

Records with standard memory. 22 per step, 5 steps maximum.

Records with optional memory. 100 per step.

Size (Excluding Handle).
　　　　Height. 8.7 in (22 cm).
　　　　Width. 15.7 in (40 cm).
　　　　Depth. 18.9 in (48 cm).

Weight (maximum). 48 lbs (22 kg).

Power. 200 W maximum 48 to 62 Hz/100, 120, 200 or 240 $\pm$10%volts RMS /2 A maximum at 100 V.

ACCESSORIES

Data Probe.

Impedance. 10 MΩ, 15 pF.

Attenuation. 10X.

Trigger Probe.

Impedance. 10 MΩ, 15 pF.

Attenuation. 10X.

DATA CARTRIDGE (3M Data cartridge DC100A)

Number of records. 100.

SECTION II

INSTALLATION

2.1   Introduction

This section contains information on un-packing, inspection, repacking, storage, and installation of the Model DTO-1.

2.2   Unpacking and Inspection

Inspect instrument for shipping damage as soon as it is unpacked. Check for broken knobs and connectors; inspect cabinet and panel surfaces for dents and scratches. If the instrument is damaged in any way or fails to operate properly, notify the carrier immediately. For assistance of any kind, including help with instruments under warranty, contact your local Gould Inc., Biomation Division, representative or the Gould Inc., Biomation Division factory.

2.3   Storage and Shipment

To protect valuable electronic equipment during storage or shipment, always use the best packaging methods available. Contract packaging companies in many cities can provide dependable custom packaging on short notice.

2.4   Power Connection

CAUTION: Before connecting the unit to AC power, be sure that the proper voltage has been selected.

The operating voltage is shown in the window beneath the fuse clips. See the following sketch.
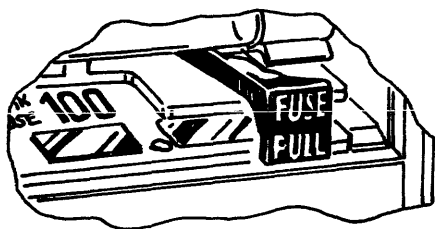
The Model DTO-1 has a line voltage selector that permits operation at four different nominal line voltages: 100, 120, 220, and 240 VAC. The unit will operate correctly at variations of + 10% from these nominal voltages, and at line frequencies for 48 to 62 Hz.

To select the operating voltage, perform the following steps.

1. Unplug line cord from rear of instrument.

2. Slide up clear plastic cover and remove fuse using built-in lever.

3. Remove the small circuit board inside the fuse holder using a small hook or screwdriver.

4. Install the circuit board, oriented so that the desired line voltage is visible beneath the fuse clips.

5. Replace the fuse and slide the clear plastic cover over it.

NOTE: When operating at 100 or 120 VAC, use a 2 A slo-blow fuse; at 220 or 240 VAC use a 1 A slo-blow fuse.

Power cable: The Model DTO-1 is equipped with a detachable three-wire power cable. Proceed as follows for installation.

1. Connect line-cord plug (three-socket connector) to AC line jack at rear of instrument.

2. Connect plug (two blades with round grounding pin) to three-wire (grounded) power outlet. Exposed portions of instrument are grounded through the round pin on the plug for safety.

2.5   Preparation for Use

The Model DTO-1 is an integrated, self-contained unit. With its standard accessories (data probe, trigger probe, data cartridge, and power cord) it is capable of performing all the functions covered in the operation section of this manual.

2.6   Initial Warm-Up

Except for the CRT, the Model DTO-1 is a solid-state instrument. Although the instrument is usable after CRT warm-up (approximately one minute), we recommend allowing approximately 10 minutes for the internal circuitry to reach thermal stablization.

2.7   Data Cartridge DC100A

OPERATION ENVIRONMENT

Temperature	32 to 122°F
	(0 to 50°C)
RH	20 to 80%
	non-condensing
Maximum Wet	79°F (26°C)
Bulb Temperature	

3M recommends that if the recipient of a data cartridge knows or suspects that the cartridge has been exposed to either the maximum or minimum temperature extreme, that it be rewound one complete cycle before using.
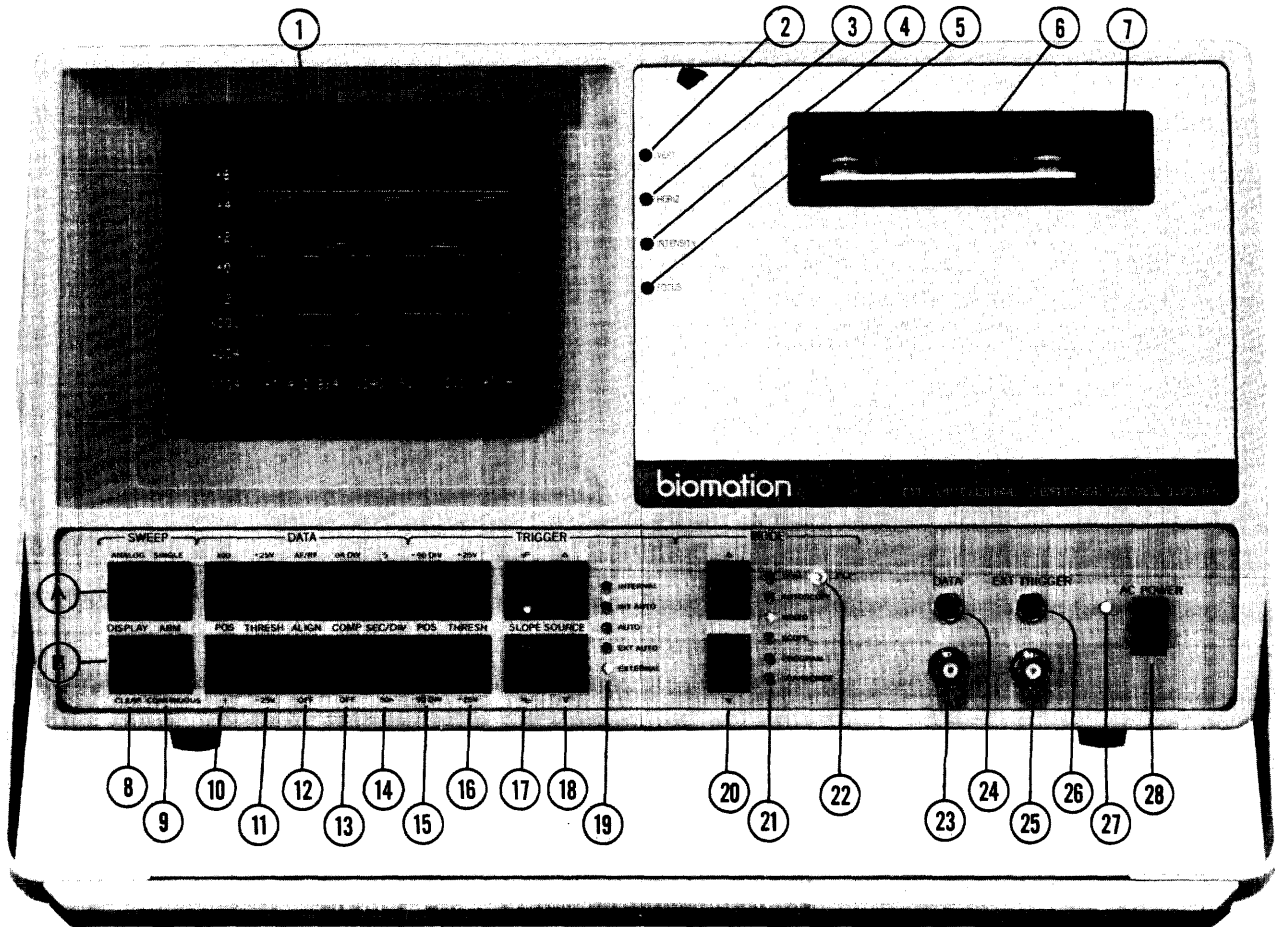
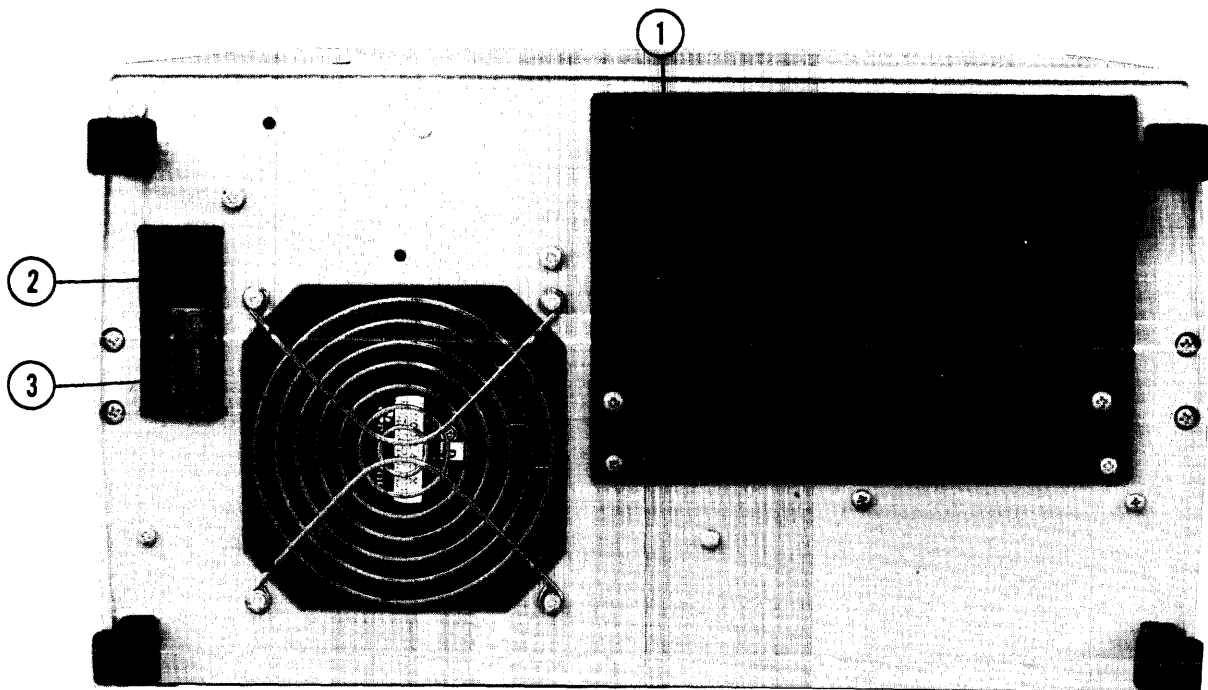Figure 3.1   Front Panel Functions

Figure 3.2   Rear Panel Functions

3.1 Introduction

This section identifies and describes front panel, rear panel and probe controls, and provides complete operational procedures.

3.2 Front Panel Controls, Connectors and Indicators

The front panel controls and other features are identified in Figure 3.1 and are described in Table 3.1.

3.3 Rear Panel Controls

The rear panel controls and other features are identified in Figure 3.2 and are described in Table 3.2.

3.4 Data Probe

The data probe controls and indicators are identified in Figure 3.3 and are described in Table 3.3.

3.5 Switches and Nomenclature

The user will quickly become accustomed to the feel and convenience of the pushbutton switches used in the DTO-1.

To understand the five different types of switch responses to momentary, repeated, and continuous depression, the user must first understand the nomenclature associated with the switches.

3.5.1 Nomenclature

The nomenclature between the rows of switches is associated with the nomenclature immediately above and below the switches. The nomenclature engraved on the switches is color keyed for use in certain modes of operation. There are two exceptions to the above. The "FAIL" and "PASS" engraving are only associated with the red and Green LEDs and there is no nomenclature between the mode △ and mode ▽ switches.

3.5.2 Switch Action
The five types of switch action are:

1. SINGLE
   A single or repeated depression, or continuous pressure on a pushbutton produces only a single change.

2. DUAL
   A single depression or continuous pressure on a pushbutton produces a single change of state. Repeated depressions produce an alternation between two states.

3. STEP SEQUENCE
   A single depression or continuous pressure on a pushbutton produces a single change of state. Repeated depressions produce stepping through a number of states until an "end" state is reached at which point repeated depressions produce no change.

4. STEP SEQUENCE, LOOP
   Same as Step 3., except that when "end" state is reached, repeated depressions cause cycle of states to repeat.

5. CONTINUOUS SEQUENCE
   A single depression produces a single step change toward some limit; repeated depressions produce additional step changes toward some limit; continuous pressure produces continuous step changes toward some limit at an increasing rate of change. When a limit is reached, additional depressions have no effect.

Table 3.4 identifies the type of action for each switch.

3.5.3 Switching Sequences

This paragraph describes the switching for switch types 2, 3, 4 and 5 as defined in paragraph 3.5.2 above. The sequences are described in Table 3.5.

INDEX NO. (Figure 3.1)	NAME	FUNCTION
1	CRT Display	Displays logic traces, analog waveforms, trace numbers, analog voltage scale data threshold, AF/RF ratio, compare tolerance, seconds/division, trigger position, trigger threshold, data error trace, and alphanumerics associated with the transcribe mode and messages to the operator.
2	VERT	Adjusts vertical position of display.
3	HORIZ	Adjusts horizontal position of display.
4	INTENSITY	Adjusts intensity of display.
5	FOCUS	Adjusts focus of display.
6	Receptacle	Receives data tape cartridge.
7	EJECT	Ejects data tape cartridge.
8a	SWEEP,DISPLAY, ANALOG	Displays analog voltage scale and readies unit for acquisition of an analog waveform display.
8b	SWEEP,DISPLAY, CLEAR	In Analog and Trim modes it clears the analog display area. In Autoscope mode it clears trace seven. In Mixed mode it clears trace six. In Scope and Program modes it clears trace 8.
9a	SWEEP, ARM, SINGLE	Arms unit for single sweep in all modes except Transcribe.
	LED	Lights when the unit is armed for single sweep and remains on until the sweep is complete and the trace is displayed.
	YES	Answers "Yes" to questions displayed in the Transcribe mode.
9b	SWEEP, ARM, CONTINUOUS	Automatically rearms unit after each sweep in all modes except Transcribe.
	LED	Lights when the unit is armed or sweeping. It goes off momentarily between sweeps.

Table 3.1 Front Panel Identification and Description

Table 3.1 (Con't)

INDEX NO. (Figure 3.1)	NAME	FUNCTION
	NO	Answers "No" to questions displayed in the Transcribed mode.
10a	DATA, POS, 100	Increments the trace numbers toward 100 in all modes except Trim, Analog and Transcribe. In the Transcribe mode it increments the tape record number toward 100.
	+25 V	In the Analog mode it increments the voltage scale toward +25 V. (NOTE: +24 V max at 2 V/cm and +20 V max at 10 V/cm.)
10b	DATA, POS, 1	Decrements the trace numbers toward 1 in all modes except Trim, Analog and Transcribe. In the Transcribe mode it decrements the tape record number toward 1.
	-25 V	In the Analog mode it decrements the voltage scale toward -25 V. (NOTE: -24 V max at 2 V/cm and -20 V max at 10 V/cm.)
11a	DATA, THRESH, +25 V	Increments the data threshold toward +25 V.
	10 V/DIV	In the Analog mode it increases the volts/division toward 10.
11b	DATA, THRESH, -25 V	Decrements the data threshold toward -25 V.
	0.5 V/DIV	In the Analog mode it decreases the volts/division toward 0.5.
12a	DATA, ALIGN, AF/RF	Tells unit to compute and display the AF/RF ratio and to reconstruct and redisplay the reference trace, on line 8, to that ratio. Used only in the Autoscope mode.
12b	DATA, ALIGN, OFF	Turns off Data Align. The AF/RF ratio disappears from the display and the trace on line 8 reverts back to recorded characteristics. Used only in the Autoscope mode.
13a	DATA, COMP, 0.04 DIV	Decreases the allowable disagreement towards 0.04* divisions.
	RED LED	The red LED lights in the Autoscope mode if the amount of continuous disagreement exceeds the compare limit displayed, or if the total disagreement exceeds 30% of the trace.

* These limits apply from 1 μs/div to 5 s/div. Below 1 μs/div the limits are inversely proportional to s/div.

Table 3.1 (Con't)

INDEX NO. (Figure 3.1)	NAME	FUNCTION
13b	DATA, COMP, OFF	Increases the allowable disagreement toward 1.0* division. Continuing past this point will turn the automatic compare mode off.
	GREEN LED	Lights in Autoscope mode if there is a compare limit displayed and if there is no continuous logical disagreement that exceeds that limit, and if the total disagreement does not exceed 30% of the trace.
14a	DATA, SECONDS/ DIVISION, 5	Changes time scale toward 5 s/div.
14b	DATA, SECONDS/ Division, 50 n	Changes time scale toward 50 ns/div.
15a	TRIGGER, POS, +180 DIV	Moves trigger position and displayed traces to the right.** Decreases delay and/or increases pretrigger time of data acquisition.
15b	TRIGGER, POS, -180 DIV	Moves trigger position and displayed traces to the left.** Increases delay and/or decreases pretrigger time of data acquisition.
16a	TRIGGER, THRESH, +25 V	Increases the trigger threshold voltage toward +25 V.
16b	TRIGGER, THRESH, -25 V	Decreases the trigger threshold voltages toward -25 V.
17a	TRIGGER, SLOPE ∫	Sets trigger to positive-going waveform and lights LED.
17b	TRIGGER, SLOPE ⌐	Sets trigger to negative-going waveform and lights LED
18a	TRIGGER, SOURCE △	Changes trigger source toward internal as indicated on adjacent LEDs (Index No. 19).
18b	TRIGGER, SOURCE ▽	Changes trigger source toward external as indicated on adjacent LEDs (Index no 19).
19	Trigger Source LEDs	Indicates the trigger source.
20	MODE △	Changes mode toward TRIM as indicated on LEDs (Index No. 21).

* These limits apply from 1 μs/div to 5 s/div. Below 1 μs/div the limits are inversely proportional to s/div.

** Zero (0.0) trigger position is located at one division from the left of the display. All trigger positions are referenced to this point.

Table 3.1 (Con't)

INDEX NO. (Figure 3.1)	NAME	FUNCTION
20b	MODE ▽	Changes mode toward TRANSCRIBE as indicated on LEDs (Index No. 21).
21	Mode LEDs	Indicates mode of operation.
22	Test Point ⊓⎍	Signal used for compensating probe.
23	DATA, BNC Connector	Data input connector for data probe.
24	DATA, Remote Connector	Provides for hook-up of the remote switches and indicators on the data probe.
25	EXT TRIGGER, BNC Connector	Trigger input connector for trigger probe.
26	EXT TRIGGER Power Connector	Provides power for 10-TC pod.
27	AC POWER, LED	Indicates presence of AC power in the unit.
28	AC POWER, SWITCH	Controls AC power to unit.

Table 3.2   Rear Panel Indentification and Description

INDEX NO. (Figure 3.2)	NAME	FUNCTION
1	Astigmatism Potentiometer	Adjusts display astigmatism.
2	Power Cord Receptacle	AC Power input.
3	Fuse	Protects AC power input.
	Voltage Selection PC Board	Selects AC power line voltage (see Section II, Paragraph 2.4).
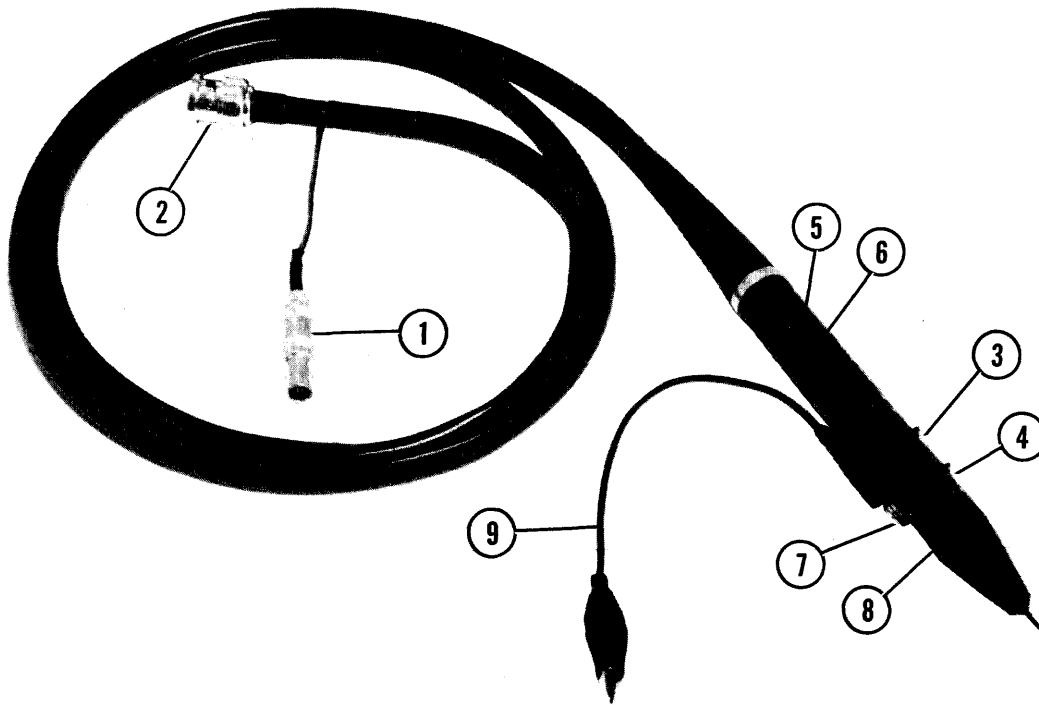
Figure 3.3 Data Probe Functions

Table 3.3 Data Probe Identification and Description

INDEX NO. (Figure 3.3)	NAME	FUNCTION
1	Remote Control Connector	Connects index numbers 3, 4, 5, and 6 to unit.
2	Data, BNC Connector	Connects probe to data input of unit.
3	Advance/Clear Pushbutton	Advances record number in Autoscope, Mixed, Scope and Program modes. Clears analog display in Analog mode.
4	Sweep Pushbutton	Arms unit for single sweeps.
5	LED, Green (2)	Indicates "PASS" condition.
6	LED, Red (2)	Indicates "FAIL" condition.
7	Ground Lug	Provides access to probe ground.
8	Probe adjust	Adjusts probe compensation capacitor.
9	Ground Lead	Connects probe ground to circuit ground.

Table 3.4   Identification of Switch Action

SWITCH	TYPE OF SWITCH ACTION (See Paragraph 3.5.2)				
	1 SINGLE	2 DUAL	3 STEP	4 STEP,LOOP	5 CONTINUOUS
STANDARD NOMENCLATURE					
DISPLAY ANALOG		X			
DISPLAY CLEAR	X				
ARM SINGLE	X				
ARM CONTINUOUS	X				
POS 100					X
POS 1					X
THRESH +25 V					X
THRESH -25 V					X
ALIGN AF/RF	X				
ALIGN OFF	X				
COMP 0.04 DIV					X
COMP OFF					X
SEC/DIV 5					X
SEC/DIV 50 n					X
POS +180 DIV					X
POS -180 DIV					X
SLOPE ∫	X				
SLOPE ⌐	X				
SOURCE △			X		
SOURCE ▽			X		
MODE △			X		
MODE ▽			X		
COLOR KEYED NOMENCLATURE					
ANALOG +25 V					X
ANALOG -25 V					X
ANALOG 10 V/DIV			X		
ANALOG 0.5 V/DIV			X		
TRANSCRIBE YES	X				
TRANSCRIBE NO				X	
PROBE					
SWEEP	X				
ADVANCE/CLEAR	X				

		Table 3.5 Switching Sequences	
SWITCH	TYPE (Table 3.4)	SEQUENCE	EXAMPLE
DISPLAY ANALOG	Dual	Switches unit in and out of the analog mode.	Analog Enabled, Analog Disabled, Analog Enabled, etc.
POS 100	Continuous Sequence	Sequentially increments record numbers toward 100.	2, 3---99,100.
POS 1	Continuous Sequence	Sequentially increments record numbers toward 1.	99,98---- 3, 2, 1.
THRESH +25 V	Continuous Sequence	Increments in 0.1 V steps toward +25 V.	-24.9 V, -24.8 V--- +24.9 V, +25 V.
THRESH -25 V	Continuous Sequence	Increments in 0.1 V steps toward -25 V.	+24.9 V, +24.8 V--- -24.9 V, -25 V.
COMP 0.04 Div	Continuous Sequence	Increments in 0.02 div steps toward lower limit.*	(At 1 μs/div) 1.0, 0.98, 0.96----0.06, 0.04.
COMP OFF	Continuous Sequence	Increments in 0.02 div steps toward upper limit* and then to off.	(At 1 μs/div) 0.06, 0.08, ------0.98, 1.0, OFF.
SEC/DIV 5	Continuous Sequence	Increments in 1-2-5 sequence toward 5 s/div.	0.1 μs, 0.2 μs, 0.5 μs, 1 μs, 2 s, 5 s.
SEC/DIV 50 n	Continuous Sequence	Increments in 5-2-1 sequence toward 50 ns/div.	2 s, 1 s, 0.5 s, --- 0.1 μs, 50 ns.
POS +180** DIV	Continuous Sequence	Increments in 0.1 div steps toward +180** div.	-179.9, -179.8---- +179.9, +180.0
POS -180*** DIV	Continuous Sequence	Increments in 0.1 div steps toward -180*** div.	+179.9, +179.8----- -179.9, -180.0
SOURCE △	Step Sequence	Increments lit LED toward internal.	Ext Auto, Auto, Int Auto, Internal
SOURCE ▽	Step Sequence	Increments lit LED external.	Int Auto, Auto, Ext Auto, External
MODE △	Step Sequence	Increments lit LED toward trim.	Program, Scope, Mixed, Autoscope, Trim.
MODE ▽	Step Sequence	Increments lit LED toward transcribe.	Autoscope, Mixed, Scope, Program, Transcribe

    *   See paragraphs 3.6.1 and 3.9.1.9.   -14-
    **   +130 in PROGRAM mode.
    ***   -130 in PROGRAM mode.

Table 3.5 (con't)

SWITCH	TYPE (Table 3.4)	SEQUENCE	EXAMPLE
ANALOG +25 V	Continuous Sequence	Increments in steps equal to the analog volts/division scale, toward the upper limit.**	(Most positive voltage; 1 V/div) -20 V, -19 V --+24 V, +25 V.
ANALOG -25 V	Continuous Sequence	Increments in steps equal to the analog volts/division scale, toward the lower limit.**	(Most negative voltage; 5 V/div) +5 V, 0 V, -5 V, -10 V, -15 V, -20 V, -25 V.
ANALOG 10 V/DIV	Step Sequence	Increment in 1-2-5 sequence toward 10 V/div.	1 V, 2 V, 5 V, 10 V.
ANALOG 0.5 V/DIV	Step Sequence	Increment in 5-2-1 sequence toward 0.5 V/div.	5 V, 2 V, 1 V, 0.5 V.
TRANSCRIBE NO	Step Sequence Loop	Increments in "rewind tape?", "read?", "erase?", "test tape?" sequence and then repeats cycle.	Read, Erase, Test Tape, Rewind Tape, Read, Erase, Etc.

** At 2 V/div, upper limit is +24 V and lower limit is -24 V.
At 10 V/div, upper limit is +20 V and lower limit is -20 V.

3.6 Special Relationships and Limitations

There are special relationships between switch settings that, in certain modes of operation or in certain sequences, do not allow these setting to be changed independently.

3.6.1 Time/Division

In the AUTOSCOPE COMPARE mode, the allowable disagreement is established with reference to a certain time/division. If the SEC/DIV is changed, the compare is changed to maintain the same allowable time limit.

For example, the initial COMPARE setting is 0.04 divisions and the sweep time is 1 μs/division. The compare time is 0.04 X 1^{-6} = 40 ns. If the trace is expanded by a factor of two, by changing the sweep time to 0.5 μs/division, the compare setting automatically changes by the same factor to 0.08 divisions. This maintains the established compare time; 0.08 X 0.5 $^{-6}$ = 40 ns.

3.6.2 Trigger Position

If the trigger position is not set at zero, expanding a trace changes the trigger position relative to the zero trigger reference point by the same ratio that the trace was expanded. Because the trigger position limits are ±180 divisions, no expansion can take place that would put the trigger position beyond these limits.

For example, the trigger position is at -40; sweep time is at 1 μs/cm. The first expansion is to 0.5 μs/cm, an expansion of two times. Two times the position of -40 would be -80. The second expansion would be to 0.2 μs/cm, an expansion of 2.5 or a total expansion of five times. This would put the position at 2.5 X -80 or 5 X -40, which equals 200. Because we cannot exceed -180, the unit does not respond to the second expansion.

3.6.3   Volts/Division

The analog voltage scale naturally changes when the volts per division is changed. However, the volts per division changed cannot be referenced to a particular point on that voltage scale. Therefore, any V/DIV change reestablishes 0 V on the third line from the top of the display. Whenever possible, it is recommended that the volts per division be set first and then analog voltage.

3.6.4   Trace Comparison

In the AUTOSCOPE COMPARE mode of operation it is the intent to compare traces that are acquired under common conditions. That is why the reference trace attributes are recorded on tape and those same attributes are automatically set up when a new trace is to be acquired. As a safeguard against inadvertently comparing traces recorded under different conditions, a new trace cannot be acquired and compared if either the SEC/DIV or POS controls are changed.

3.7   Trigger Modes

There are five trigger modes-Internal, Internal Auto, Auto, External Auto and External. When using the Biomation model 10-TC Probe Pod, there is a sixth "combinational trigger" mode of operation.

The trigger input connector is not used in the internal, internal auto, or auto modes of operation. There is no need, however, to disconnect the trigger probe from a signal when in these modes of operation.

When in the external auto, external, or external with combinational trigger, the trigger probe is connected to the trigger input connectors. When the 10-TC Probe Pod is used, the probe power is obtained through the trigger mini connector just above the trigger input BNC connector.

3.7.1   Internal

In the Internal position, the unit triggers off of the data signal.

3.7.2   Internal Auto

In the Internal Auto position, the unit triggers off of the data signal unless a data signal of sufficient amplitude is not present, in which case the unit triggers automatically.

3.7.3   Auto

In the Auto position, the unit triggers as soon as the unit is armed.

3.7.4   External Auto

In the External Auto position, the unit triggers off of the trigger signal unless a trigger signal of sufficient amplitude is not present, in which case the unit triggers automatically.

3.7.5   External

In the External position, the unit triggers off of the trigger signal.

3.8   Modes of Operation

The following paragraphs briefly describe the purpose of each mode of operation and then what can be done once the unit is in that mode. The step-by-step operating procedures are located in Section 3.9.

3.8.1   Trim Mode

The Trim mode is used to check probe calibration. There is a 0 to +4 V, 1 kHZ squarewave output on the front panel for this purpose. Although all front panel data and trigger switches are operational, they are seldom used in this mode of operation.

3.8.2   Autoscope Mode

The Autoscope mode is used for comparing logic traces. The reference trace from the data cartridge always appears on line eight of the display and the new trace always appears on line seven. All front panel data and trigger switches are operational (see paragraphs 3.6.1 and 3.6.4).

With the compare function off, a visual comparison can be made. With the compare function on, an automatic comparison is made. As long the SEC/DIV is not changed, the compare limits can be changed and still retain the automatic compare feature.

As long as the SEC/DIV is not changed, the align feature can be enabled. The align feature can be disabled at any time.

There can be up to six logic traces on lines one through six. The trace number prefix is either an "A" or an "R" depending

on whether the trace was acquired from the SUT or from tape storage. There is no prefix if there is no trace.

The mixed mode may be entered without losing any of the information displayed on the lower quarter of the CRT.

3.8.3   Mixed Mode

The Mixed mode is entered from the Autoscope mode to retain the logic traces on lines 7 and 8 while looking at other logic traces on lines 1 through 6; while looking at analog waveforms; or while looking at both logic traces and analog waveforms.

The Mixed mode is entered from the Scope mode to retain the logic traces on lines 7 and 8 while looking at other logic traces on lines 1 through 6; or while looking at both logic traces and analog waveforms. Entering the Mixed mode from any other mode simply allows acquisition of logic traces and analog waveforms on lines 1 through 6 with lines 7 and 8 remaining blank.

When in the Mixed mode all data and trigger switches are operational except for the Align and Compare functions. New logic traces are displayed on line 6.

The analog pushbutton must be depressed to display analog waveforms (see paragraph 3.8.5).

3.8.4   Scope Mode

The Scope mode is entered when the DTO-1 is to be used strictly as an oscilloscope or logic analyzer, or when it is desirable to display eight new traces or three new traces with an analog waveform.

When in the Scope mode all data and trigger switches are operational except for the Align and Compare functions.

The analog pushbutton must be depressed to display analog waveforms (see paragraph 3.8.5).

3.8.5   Analog Mode

The Analog mode is entered from the Mixed or Scope modes for the purpose of displaying analog waveforms while retaining up to three logic traces, on lines 6 through 8, from the previous mode.

Any number of analog waveforms may be displayed concurrently in the analog display area as long as none of the displayed attributes are changed between sweeps. Any change of operational data or trigger switch settings clears the analog display area.

The data position and threshold switches become analog voltage switches in the analog mode. All data and trigger switches are operational except for align and compare functions.

3.8.6   Program Mode

The Program mode is used to record logic traces on magnetic tape. A test program is recorded in this mode for recall at a later date in the Autoscope mode. Test programs or historical records of logic traces can be recalled for display in either the Autoscope or Program modes. All data and trigger switches are operational except for the align function.

3.8.7   Transcribe Mode

The Transcribe mode is used to duplicate or reorganize existing tapes, erase magnetic tape records, rewind tapes, or verify the correctness of magnetic tapes.

The "Yes", "No", and Data position pushbuttons are the only ones operational in this mode.

3.9   Operating Procedures

3.9.1   General Operating Information

To keep the step-by-step operating procedures as brief as possible, some of the redundant procedural steps, alternate steps, and special operations are treated separately below.

3.9.1.1   Data Align

DATA, ALIGN, AF/RF and OFF pushbuttons can be activated only in the Autoscope mode (see Table 3.1, index numbers 12a and 12b).

Once this function is enabled, it can be disabled only by entering the Trim mode or by depressing the DATA, ALIGN, OFF pushbutton when in the Autoscope mode.

Whenever a test procedure calls for a frequency alignment to be done and there is already an AF/RF ratio displayed, first depress the DATA, ALIGN, OFF pushbutton and then depress and release the DATA, ALIGN, AF/RF pushbutton.

3.9.1.2 Indexing Tapes

There are two methods for indexing a blank tape.

1. Enter the Program mode and insert tape.

2. Enter the Transcribe mode and ask the instrument to erase number 001-100. (See paragraph 3.9.2.6, steps 1 and 11-15.)

3.9.1.3 Probe and Ground Connections

Prior to acquisition of any signal:

1. Connect data probe ground lead to system under test.

2. Whenever using External Trigger mode of operation, be sure to connect trigger probe and trigger probe ground lead to the system under test.

3.9.1.4 Data Probe ARM, ADVANCE pushbuttons

In writing the step-by-step operating procedures, a standard X10 data probe was used with the DTO-1. When using the special data probe with ARM and ADV pushbuttons, the following procedure changes can be made.

1. The probe ARM pushbutton can be used wherever the SWEEP, ARM, SINGLE pushbutton is called out.

2. The probe ADV pushbutton can be used wherever the DATA, POS, 100 pushbutton is called out.

3. The probe ADV pushbutton can be used to clear the display when in the Analog mode of operation.

3.9.1.5 Clearing the Display

Analog Waveforms - In the Trim, Mixed/Analog and Scope/Analog modes of operation, newly acquired signals will be superimposed on any existing waveforms unless the display is first cleared.

Logic Traces - There is no need to clear the display prior to acquisition of a new signal. The displayed trace will automatically be cleared prior to display of a new trace.

3.9.1.6 Continuous Sweep

The Continuous Sweep mode can be used anytime SWEEP, ARM, SINGLE is called out; however, it is probably most useful in the Mixed or Scope mode during troubleshooting procedures.

Continuous sweep is obtained by depressing the SWEEP, ARM, CONTINUOUS pushbutton. There are two ways to disable the continuous sweep function.

1. Depress the CLEAR pushbutton until the LED on the continuous switch goes off. The appropriate display area will be cleared.

2. Depress the SWEEP, ARM, SINGLE pushbutton until the LED on the continuous switch goes off. Sweeping will stop at the end of the next complete sweep. None of the displayed information will be cleared.

    NOTE: No control settings can be changed during continuous sweep.

3.9.1.7 Changing the Control Settings

The control settings can be changed at anytime with the following exceptions:

1. As stated elsewhere in Section III of this manual.

2. While the instrument is carrying out a prior instruction.

3.9.1.8 Data Error Trace

In the Autoscope mode, the logic trace from the system under test is being compared

with the logic trace from the known good system. The exact areas of disagreement are underscored on the display. This underscoring is present whether or not the automatic compare (COMP) function is being used. It gives the operator a quick and accurate visual indication of where the disagreements are located.

The data error trace is expanded or compressed along with the logic traces when the time base is changed. It is also retained when going from the Autoscope to the Mixed mode.

3.9.1.9   Data Compare (COMP)

The compare limit, in display divisions, is one of the controls set up in the Program mode. (See Table 3.1, index number 13a and 13b.) In the Autoscope mode, this is the limit that sets the pass/fail indicators. It does this by comparing the data error trace against this limit. (See Table 3.1, index numbers 13a and 13b.)

The compare limit can be changed in the Autoscope mode.

The smallest compare limit that can be set is the larger of 0.04 divisions or the number of divisions representing 4 sampling bits of the internal clock. In all cases where the latter would be the larger of the two, the internal clock would be 100 MHz and the sampling interval would be 10 ns. Therefore, the compare limit cannot represent less than 40 ns. It follows that automatic comparisons connot be made to limits of less than 40 ns.

However, using a sweep time of 50 ns/DIV, a visual comparison can be made with a resolution of 10 ns and typical accuracy of 20 ns.

3.9.1.10   PASS/FAIL LEDs

Prior to acquisiton of a trace in the Autoscope mode, the read LED will be lit. This is a ready indication, or to put it another way, the operator is to take some action. Shoot a trace!

The read (FAIL) indication after acquisition of a signal also tells the operator to take action. In this case he should look at the display.

If no trace appears on line 8 in the Autoscope mode, the green LED will be lit. (You might say that nothing is being compared against nothing.) In this case the unit cannot be armed.

When there is a trace on line 7 and the COMP function is off, neither the red LED or the green LED will be lit.

The pass/fail LEDs operate only in the Autoscope mode except as noted in paragraph 3.9.1.11.

3.9.1.11   Self Test

Each time the unit is powered up or enters the Trim mode, it self-tests the major portions of the device including the MPU, firmware RAMs. If the microprocessor is unable to access the ROM or RAM, both the pass and the fail LEDs will become lit. The defective device can be located using Table 3.6 and Figure 3.4.

3.9.1.12   Offset Errors

If "OFFSET ERROR" is displayed, it means that the dc offset of the input circuitry exceeds 50 mV. If this should occur, depress the clear pushbutton and then proceed. The instrument will automatically calibrate itself to eliminate the offset.

3.9.1.13   Tape Errors and Dirty Heads

If any of the following messages appear on the display, you either have a dirty read/write head or a tape problem.

"READ or WRITE ERROR"
"READ ERROR at ***"
"INDEX ERROR"
"INDEX ERROR at ***"

Cleaning the head will usually solve a nonrepetitive type problem. If a read error repeats at a specific record, that record will have to be reprogrammed. If an index error repeats at a specific location, that record must be worked around or the entire tape must be reindexed and refreshed from your master tape.

In the Autoscope mode, an error can be worked around by depressing the CLEAR pushbutton and then proceeding. An "E" will be displayed in front of the record number containing the error.
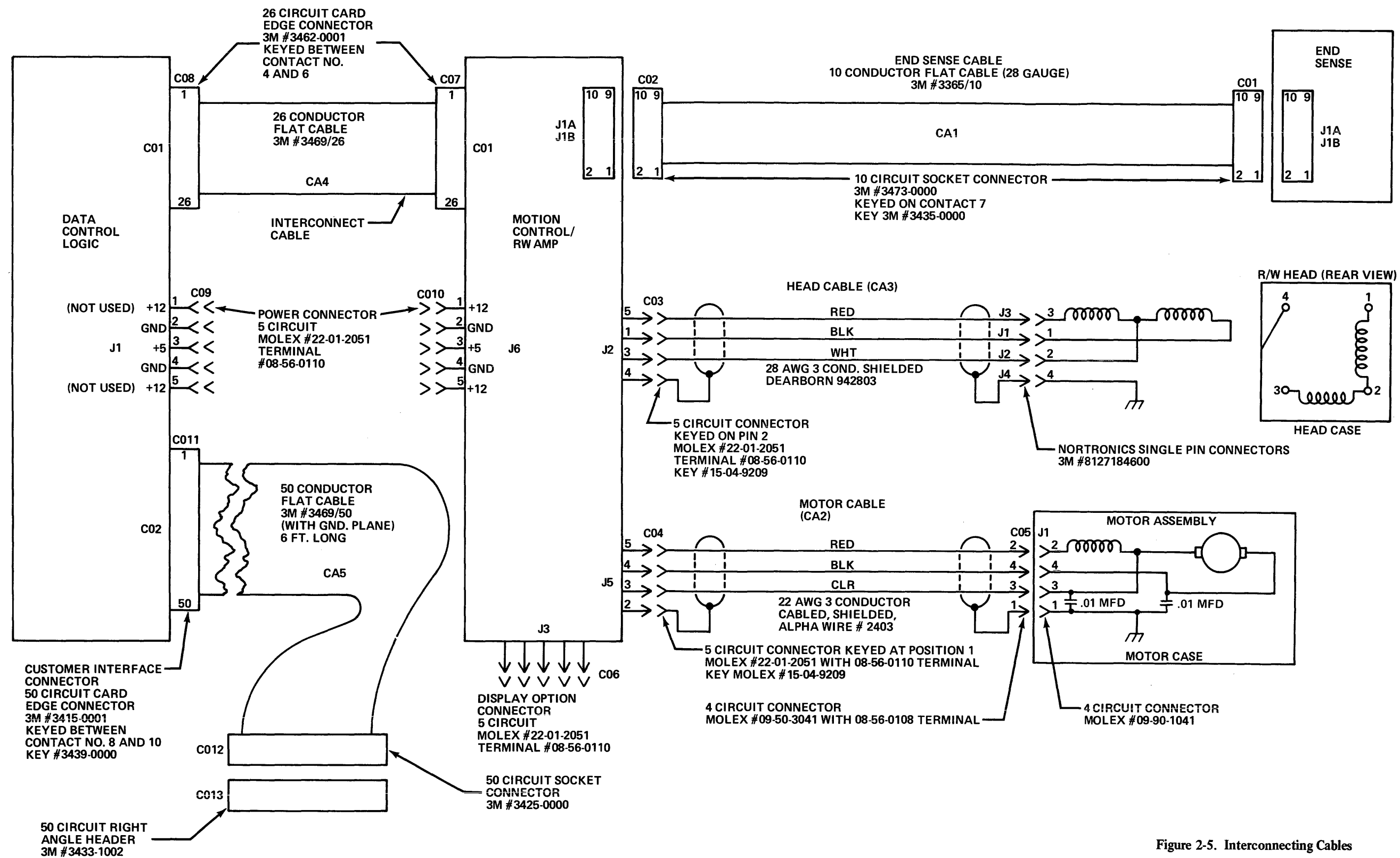
Figure 2-5. Interconnecting Cables

Table 3.6 Self Test - Diagnostic Error Identification

FRONT PANEL

FAIL

COMP

SLOPE

PASS

(0)◯INTERNAL
(1)◯INT AUTO
(2)◯AUTOMATIC
(3)◯EXT AUTO
(4)◯EXTERNAL

(0)◯TRIM
(5)◯AUTOSCOPE
◯MIXED
◯SCOPE
◯PROGRAM
◯TRANSCRIBE

(1) (2) (3) (4)

Both the PASS and FAIL LEDs (1) will light when there is a failure in the memory access routine.

One of the SLOPE LEDs (2) will light. The upper LED, ⊐⊏ , indicates that the failure is in one of the eight ROMs. The lower LED, ⊐⊏ , indicates that the failure is in one of the eight RAMs.

The weighted TRIGGER LEDs (3) and MODE LEDs (4) locate the defective chip. Add the weight, in parenthesis, of the one LED lit at (3) to the weight of the one LED (TRIM or AUTOSCOPE) lit at (4) . Locate the chip using the control board layout Figure 3.4.
(NOTE: The sum will not exceed 7.)

7 6 5 4 3 2 1 0

ROM

RAM

0
1
2
3
4
5
6
7

CONTROL BOARD

Figure 3.4

-20-

3.9.2   Step-by-step Operating Procedures

3.9.2.1 Trim Mode

STEP	PROCEDURE	INDICATION
1	Enter the TRIM mode.	A voltage scale will appear on the left side of the display and controls will be automatically set for acquisition of the probe calibration waveform.
2	Hold probe to be calibrated to the TRIM terminal. Press and release the SWEEP, ARM, SINGLE pushbutton.	Calibration signal will be displayed.
3	Adjust probe compensation capacitor if required.	
4	Press and release the CLEAR pushbutton.	Displayed signal is cleared.
5	Repeat steps 2, 3 and 4 until probe is properly compensated.	

3.9.2.2 Autoscope Mode

STEP	PROCEDURE	INDICATION
1	Insert prerecorded data cartridge and enter the AUTOSCOPE mode.	From two to seven index or record numbers will be displayed on the left side of the CRT. The numerical part of the number on line 8 will be duplicated on line 7. For those record numbers that have a logic trace recording on tape, an "R" prefix will appear in front of the record number. The records are numbered consecutively from top to bottom except for the duplication on lines 7 and 8. The control settings are displayed across the bottom of the CRT and on the front panel LEDs. The control settings will be those of the trace on line 8. If no trace appears on line 8, the most recently used settings will be displayed. The data align AF/RF ratio will normally be off when starting a new test sequence. (See Paragraph 3.9.1.1).
2	Place desired record number on line 8 of the display using the DATA, POS pushbuttons.	Desired logic signal appears on line 8. The controls will automatically be set for the trace on line 8.
3	Connect trigger probe and ground leads as required.	
4	Probe the test point that corresponds to the record number on line 8.	
5	Press and release the SWEEP, ARM, SINGLE pushbutton.	A logic signal will appear on line 7. An "A" will appear in front of the record number on line 7. The green, PASS, or the red, FAIL, LED will become lit. The "Data Error Trace" will appear immediately below the logic signal on line 7 if there is any logical disagreement between the traces on lines 7 and 8.

STEP	PROCEDURE	INDICATION
6	If no frequency alignment is to be done, proceed to step 7. If a frequency alignment is to be done (see paragraph 3.9.1.1), depress and release the DATA, ALIGN, AF/RF pushbutton.	The AF/RF ratio appeared on the display. The trace on line 8 was cleared from the display and then reappeared after being aligned to the clock or reference signal of the system under test.
7	If there was a "PASS" condition in the last step, the test is complete. Additional tests can be made by repeating steps 2-7. If there was a "FAIL" condition in the last step, either proceed to a preprogrammed subroutine, or enter the MIXED mode for manual trouble-shooting (See paragraph 3.9.2.3 Mixed Mode.)	

3.9.2.3 Mixed Mode

STEP	PROCEDURE	INDICATION
1	Enter the MIXED mode.	The trace number 001 will appear on line 6. Logic traces, if any, on lines 7 and 8, and control settings, will be holdovers from the previous mode.
3	Probe test point. Depress and release the SWEEP, ARM, SINGLE pushbutton.	A logic signal will appear on line 6. An "X" will appear in front of the trace number.
4	If the logic signal on line 6 is to be retained and a new logic signal is to be displayed, depress and release the DATA, POS, 100 pushbutton.	The trace number and trace move up to line 5 and the next consecutive number appears on line 6.
5	Repeat steps 2, 3 and 4 for each new logic signal to be displayed.	Same as above except in step 4 all traces above line 6 will move up one position and the trace on line 1, if any, will be lost.
6	If the analog waveform of the input signal is to be displayed, depress and release the ANALOG pushbutton.	The traces, if any, on lines 1 through 5 will disappear from the display. A voltage scale will appear on the left side of the display.
7	Probe test point. Depress and release the SWEEP, ARM, SINGLE pushbutton.	An analog waveform will be displayed. (NOTE: Probe must be held to the test point until complete waveform is displayed.)
8	To superimpose additional analog waveforms on the display, repeat step 7.	Additional waveforms will be superimposed on the existing waveforms.
9	If new analog waveforms are to be displayed by themselves, depress the CLEAR pushbutton. Repeat step 7.	The analog waveform will disappear from the display. Same as step 7.
10	To disable the analog function, depress and release the ANALOG pushbutton.	The voltage scale and analog waveforms will disappear from the display. Any logic traces that were present on lines 1 through 5 prior to entering the analog mode will reappear. The control settings will remain as they were in the analog mode.

STEP	PROCEDURE	INDICATION
11	In order to <u>return</u> to the autoscope mode, depress and release the MODE pushbutton.	Lines 1 through 6 will clear. Logic traces, if any, that were present on lines 1 through 6 prior to entering the mixed mode will be displayed, except that "A" traces will be replaced by "R" traces recalled from tape. Control settings will be recalled from tape for the trace on line 8.
12	In order to <u>return</u> to the scope mode, depress and release the MODE pushbutton.	Lines 1 through 6 will clear. Trace numbers, if any, that were present on lines 1 through 6 prior to entering the mixed mode will be displayed without prefixes or traces. Control settings will not change.

3.9.2.4 Scope Mode

STEP	PROCEDURE	INDICATION
1	Enter scope mode.	Display is clear except for the trace number 001 and controls settings. Control settings are holdovers from previous mode.
2	Probe test point. Depress and release the SWEEP, ARM, SINGLE pushbutton.	A logic trace will appear on line 8 and the prefix "S" will be added to the trace number.
3	If additional signals are to be displayed, depress and release the DATA, POS, 100 pushbutton.	The logic trace and trace number will move up to line 7 and the next consecutive number will appear on line 8.
4	Repeat steps 2 and 3 for each new signal that is to be displayed.	Same as above except that in step 3, all logic traces and trace numbers will move up one position. As traces move off the top of the display they will be lost.
5	If the analog waveform of an input signal is to be displayed, depress and release the ANALOG pushbutton.	Lines 1 through 5 of the display will be cleared. A voltage scale will appear on the left side of the display.
6	Probe the test point. Depress and release the SWEEP, ARM, SINGLE pushbutton.	An analog waveform will be displayed.
7	To superimpose additional analog signals on the display, repeat step 6.	Additional waveforms will be displayed.
8	To clear the display prior to acquisition of new analog signals, depress the CLEAR pushbutton. Repeat step 6.	The analog waveform(s) will be cleared. Same as step 6.
9	To disable the analog mode, depress and release the ANALOG pushbutton.	Lines 1 through 5 of the display will be cleared. Any logic traces and trace numbers that were present on lines 1 through 5 prior to entering the analog mode will be displayed.

3.9.2.5 Program Mode

STEP	PROCEDURE	INDICATION
1	Enter the PROGRAM mode and insert the data cartridge. NOTE: IT IS EXTREMELY IMPORTANT TO OBSERVE THE TRIGGER MODE LED DURING THE COURSE OF PROGRAMMING A TAPE. UNLESS A PREVIOUS PROGRAM HAS BEEN ERASED, THE TRIGGER INFORMATION FROM THAT PROGRAM MAY CHANGE YOUR INTENDED SETTING AND GO UNDETECTED. WHEN USING AN EXTERNAL TRIGGER, BE SURE THAT IT IS PROPERLY SELECTED. SHOULD THERE BE ANY DOUBT, DISPLAY THE LOGIC TRACE SEVERAL TIMES AND CHECK FOR REPEATABILITY BEFORE PUTTING IT IN TAPE STORAGE.	a) **Using unindexed tape.** The statement "INDEXING TAPE - WAIT 60 SEC" will appear on the display. When indexing is complete, the index numbers 093-100 will appear along the left side of the display. The most recently used control settings will appear across the bottom of the display and on the trigger slope and trigger source LEDs. b) **Using pre-indexed tape.** From one to eight consecutive index or "record" numbers will appear along the left side of the display. Where there is a logic signal stored on tape, the record number will have an "R" prefix. The stored signal, if any, may or may not be displayed as logic traces depending on the SEC/DIV and Trigger POS control settings. The control settings will be displayed across the bottom of the display and on the Trigger slope and Trigger source LEDs. The control settings will be those of the trace on line 8. If no trace is displayed on line 8, the most recently used settings will be displayed.
2	Using the DATA, POS pushbuttons, position the desired record number on line 8 of the display.	If a record position change was made, see step 1b above.
3	Set controls and connect ground leads and trigger probe as required.	
4	Probe test point. Depress and release the SWEEP, ARM, SINGLE pushbutton.	A logic trace will appear on line 8 of the display. The prefix "P" will appear in front of the record number on line 8. ("P" indicates it is a proposed trace.)
5	If the logic trace displayed is to be recorded on tape, proceed to step 6. If any change is made to the control settings, reacquire the logic trace before proceeding to step 6.	

STEP	PROCEDURE	INDICATION
6	Depress and release the DATA, POS, 100 pushbutton.	All displayed record numbers and traces moved up one division on the display. The prefix on the trace just recorded changed from "P" to "R". ("R" indicates that the trace has been recorded on tape.) The next consecutive number will appear on line 8. If there is a trace displayed on line 8, and if the SEC/DIV and TRIGGER, POS control settings have changed, the traces on lines 1 through 7 will be redisplayed to agree in both time and position with the new settings.
7	To record additional signals, repeat steps 2 through 6.	

3.9.2.6 Transcribe Mode

STEP	PROCEDURE	INDICATION
1	Enter the transcribe mode.	"REWIND TAPE?" appears on the display.
2	If the "Erase" operation is to be performed, proceed to step 14. If the "Test Tape" operation is to be performed, proceed to step 20. If records are to be transcribed to another tape or to a new position on the same tape, proceed to step 5. If the tape is to be rewound, proceed to step 3.	
3	Depress and release the "YES" pushbutton.	The tape will move forward to the end and then rewind back to the beginning. "REWINDING-WAIT" will appear on the display. When rewinding is complete, "REWIND TAPE AGAIN?" will appear on the display.
4	If another tape is to be rewound, insert that tape and repeat step 3. This completes the rewind procedure.	
5	Depress and release the "NO" pushbutton.	"READ 001?" appears on the display.
6	If the lowest record number to be transcribed is 001, proceed to step 4. If the lowest record number to be transcribed is not 001, use the DATA, POS pushbuttons to display the lowest number that is to be transcribed.	The number selected (XXX) will appear on the display. (READ XXX?)
7	Depress and release the "YES" pushbutton.	"READ XXX - XXX?" appears on the display.

3.9.2.6 Transcribe Mode (cont.)

STEP	PROCEDURE	INDICATION
8	If only a single record is to be transcribed, proceed to step 6. If a block of records is to be transcribed, use the DATA, POS pushbuttons to display the highest consecutive record number that is to be transcribed.	The number selected (YYY) will appear on the display. (READ XXX - YYY?)
9	Depress and release the "YES" pushbutton.	"READING - WAIT" will appear on the display. Then "WRITE XXX - YYY to XXX-YYY" will be displayed.
10	If the records are to be written onto a new tape at the same location, proceed to step 8. If the records are to be written to a new location, either on the same tape or on a new tape, use the DATA, POS pushbuttons to select the block of consecutive numbers at the new location.	The block of numbers selected (WWW - ZZZ) will appear on the display. (WRITE XXX - YYY to WWW-ZZZ?)
11	If the records are to be moved to a new location on the same tape, proceed to step 9. If the records are to be transcribed to another tape, remove the data cartridge and insert the other pre-indexed data cartridge.	
12	Depress and release the "YES" pushbutton.	The tape will move to the first record in the group to be transcribed. "WRITING-WAIT" will then appear on the display. When the writing is complete, "WRITE XXX-YYY to WWW-ZZZ again?" will appear on the display.
13	If the records transcribed in step 9 are to be recorded on additional tapes, repeat steps 8 and 9. This completes the transcribe procedure.	

STEP	PROCEDURE	INDICATION
14	Depress and release the "NO" push-button twice.	"ERASE 001?" appears on the display.
15	If the lowest record number to be erased is 001, proceed to step 13.	
	If the lowest record number to be erased is not 001, use the DATA, POS pushbuttons to display the lowest number that is to be erased.	The number selected (XXX) will appear on the display (ERASE XXX?)
16	Depress and release the "YES" push-button.	"ERASE XXX-XXX?" will be displayed.
17	If only a single record is to be erased, proceed to step 15.	
	If more than one consecutive record is to be erased, use the DATA, POS pushbuttons to display the highest consecutive number that is to be erased.	The number selected (YYY) will be displayed. (ERASE XXX-YYY?)
18	Depress and release the "YES" push-button.	The tape will move to the first record to be erased. "ERASING -WAIT" will then appear on the display. When the records have been erased, "ERASE XXX-YYY AGAIN?" will be displayed. NOTE: If the entire tape is being erased, records 001-100, instead of displaying "ERAS-ING - WAIT", "INDEXING TAPE - WAIT 60 SEC." will appear. After erasure is complete, "ERASE 001-100?" will be displayed.
19	If additional tapes are to have the same records erased, remove the tape just erased and insert the next tape to be erased. Repeat step 15. This completes the erase procedure.	

STEP	PROCEDURE	INDICATION
20	Depress and release the "NO push-button twice.	"ERASE 001?" will be displayed.
21	Depress and release the "NO" pushbutton.	"TEST TAPE?" will be displayed.
22	Depress and release the "YES" pushbutton.	"TESTING - WAIT" will be displayed. After testing, "TEST TAPE AGAIN?" will be displayed.
23	If additional tapes are to be tested, remove the tape just tested and insert the next tape to be tested. Repeat step 19.	

3.10   Programming Notes

3.10.1   Test Point Selection

For system or subassembly testing, the minimum number of test points should be selected that will validate the electrical performance.

For troubleshooting, test point selection should follow the troubleshooting tree format.

3.10.2   Test Procedure

A recommended test procedure or "test point listing" is shown in Figure 3.5, and a sample listing is shown in Figure 3.6. The system test sequence is shown as Record No.'s 001-010 in Figure 3.6. The troubleshooting sequences begin at Record No. 012.

3.10.3   Programming Steps

Steps 1 & 2   Sectionalize the system under test (SUT), and select test points. The order in which these two steps are done will depend to a great deal on the complexity of the SUT. In one case, the test points that will validate the system will be obvious, in which case that step will be done first. In another case, sectionalization of the system may be required in order to determine which points must be tested.

Sectionalization would be done on a functional basis, with grouping of the test points that require a common trigger. The idea is to keep the test operation as simple as possible. Testing all points that use a common trigger point, in sequence, will reduce the number of operations the user will have to perform.

Step 3.   If the signals at a group of test points have a time relationship to a specific clock, the clock, or a waveform derived from that clock, should be the first signal programmed in the sequence for that group of signals. To obtain the best frequency resolution in the ALIGN mode, a large number of transitions should be recorded. However, the pulse or data bit width should never be less than the COMPARE resolution.

TIP: The COMPARE resolution can be found by depressing the COMP, .04 DIV pushbutton until the minimum is reached.

Step 4.   Program the group of test points that have a timing relationship to the clock signal recorded in Step 3. These signals should be displayed with maximum display resolution commensurate with the minimum amount of displayed data required.

The purpose of having the waveforms displayed is to provide the user with information. Unless the user has good visual resolution, the display is of no value to him. Therefore, when large amounts of data are to be compared, record as much data as possible without losing good visual resolution and then make additional recordings at the same test point (different trigger position) to cover the additional data that must be compared.

Step 5.   Proceed to the next group of test points and repeat steps 3 and 4.

3.10.4   Setting the Controls

The DATA THRESHOLD AND TRIGGER THRESHOLD voltages are set for the logic family that is being tested. If you are programming a system using mixed technologies and are not sure about the logic levels, use the ANALOG mode to check the levels.

The TRIGGER POSITION should be set to 0.0 when recording the clock signal. Whenever possible, record the other signals as close to 0.0 trigger position as possible.

When recording a clock signal, the SEC/DIV should be set so that a large number of transitions will be displayed (see Step 3 above). For other recordings, the important thing is to have good visual resolution (see Step 4 above).

The following guidelines may be used for setting the COMPARE function.

1. If only looking for the presence of a pulse, the setting should be just small enough that the absence of a pulse would indicate an error. If the timing is unimportant and it does in fact vary to a large degree with reference to the compare setting, errors may often be indicated during testing. In such a case, it is better to show a FAIL condition when there is none than to show a PASS condition when there is no pulse. An instruction in the "test point listing" could tell the user when to disregard the FAIL indication.

2. If timing is important, the programmer will have to determine the maximum allowable deviation.

   For example: If there are 10 gates between the trigger source and the test point, and the propagation delay of each gate can vary from 8 to 15 ns, the total variation can be as much as (15-8) X 10 or 70 ns. If the time bases were set to 50 ns/DIV, the compare function would have to be set to 1.6 divisions or 80 ns minimum. In no case, however, should this setting exceed the pulse width or the width of one bit of data.

3. Specific limits may be dictated by the system specification or other circuit timing requirements. In this case, program in those limits unless they exceed the pulse or data bit time, in which case the setting should be at least one increment less than the pulse width or the time of one data bit.

4. If the user does not want to calculate his propagation delays, or he chooses to assume the delays will average out, he should use the following rule of thumb.

   Set the compare limit to the smaller of two times the minimum allowable setting or 1/2 the pulse of data width.

TEST PROCEDURE

FOR_____

Approved
By_____

Date_____

Test Equipment Required:

    Biomation DTO-1
    DTO Cartridge No._____

Cartridge No._____

RECORD NO.	DATA PROBE AT	TRIGGER PROBE AT	ON FAIL GO TO CARTR.	RECORD	REMARKS

Figure 3.5 Recommended Test Procedure

FOR _COFFEE VENDOR_
MODEL 120

Approved
By_____

Test Equipment Required:

Date _7/7/77_

Biomation DTO-1
DTO Cartridge No. ___120-1, 2, 3, & 4___

Cartridge No. ___120-1___

RECORD NO.	DATA PROBE AT	TRIGGER PROBE AT	ON FAIL GO TO CARTR.	RECORD	REMARKS
001	PCB7, A13-6	PCB7, A7-13			AUTO ALIGN LIMIT .93 to 1.07
002	PCB7, A7-13	PCB7, A7-13			
003	PCB7, E14-1	PCB7, A7-13		012	
004	PCB7, D3-2	PCB7, A7-13		091	
005	JUNCTION PCB1, R13-C6	PCB7, A7-13	120-2	010	
006	PCB3, C12-15	PCB3, B1-6	120-2	052	PRESS "CREAM ONLY"
007	PCB4, A3-2	PCB3, B1-6	120-2	081	PRESS "HOT CHOCOLATE"
008	PCB5, C1-7	PCB5, C1-2	120-3	001	
009	PCB6, J1-37	PCB5, C1-2	120-3	045	
010	PCB2, B13-3	PCB5, C1-2	120-4	010	END OF TEST PROCEDURE
011					
012	PCB7, E14-3	PCB7, A7-13		041	
013	PCB7, E14-5	PCB7, A7-13			
014	PCB7, E13-1	PCB7, A7-13			
015	PCB7, E13-11	PCB7, A7-13			
016	PCB7, B3-7	PCB7, A7-13		072	
017	PCB7, A1-6	PCB7, A7-13			
018	PCB7, B3-3	PCB7, A7-13			Figure 3.6 Sample Listing
019	PCB7, C2-1	PCB7, A7-13			-35-
020	PCB7, C2-2	PCB7, A7-13			

SECTION IV

PRINCIPLES OF OPERATION

4.1 Introduction

This section provides a basic functional description and a detailed circuit description of the DTO-1.

4.2 Basic Functional Description

For the discussion that follows, refer to the block diagram, Figure 4.1.

4.2.1 Front Panel Boards

Front panel and data probe switch information is made available to the Control board. The data and trigger settings are then stored in RAM.

Instrument status information from the Control board is displayed via front panel and data probe LEDs.
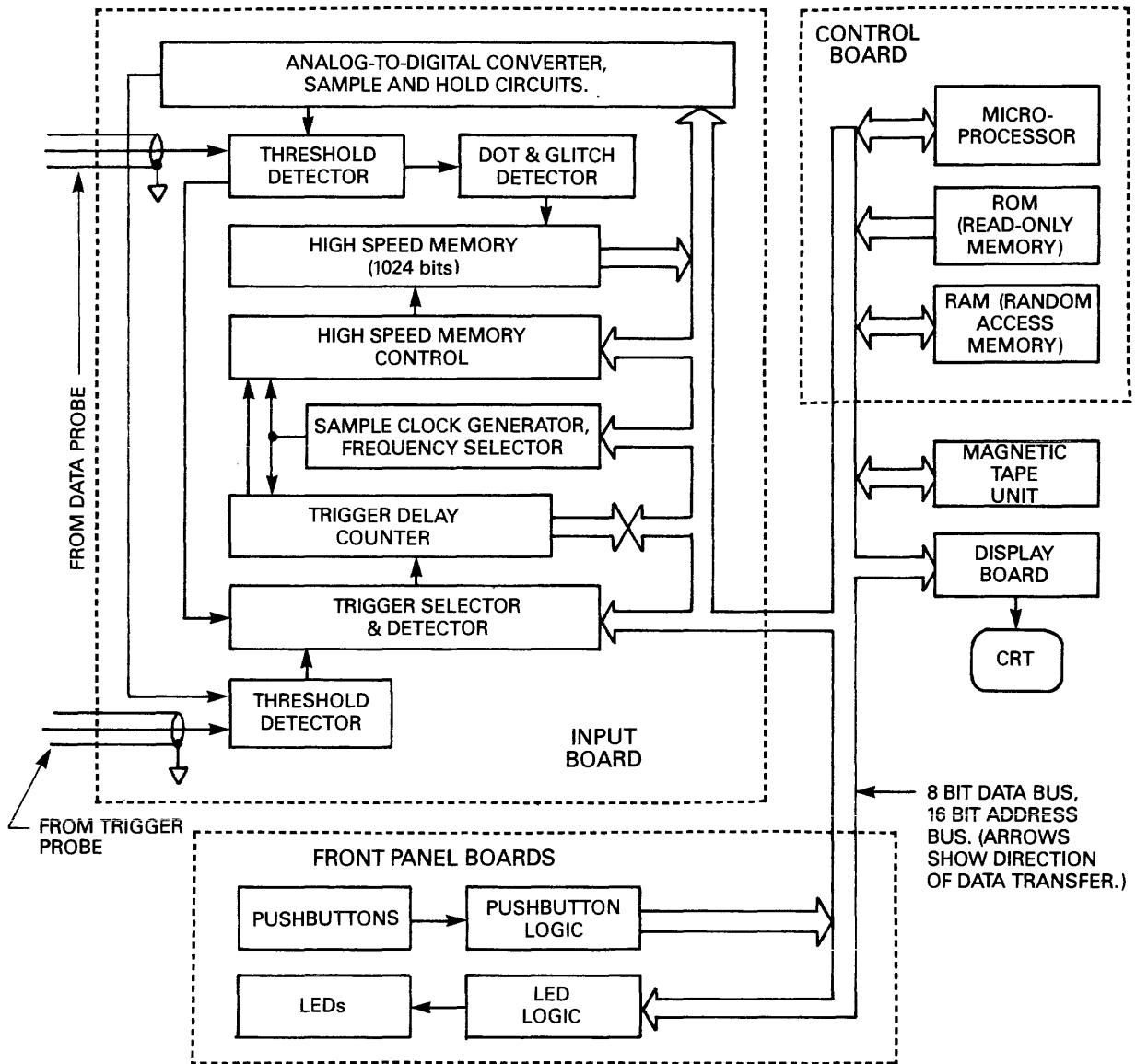

Figure 4.1 DTO-1 Block Diagram

4.2.2 Control Board

The Control board controls all operations directly or indirectly performed by the DTO-1. Front panel switches read by the Control board are translated into the control signals required to perform the assigned task. The Control board contains a Motorola 6800 microprocessor, Read Only Memory (ROM), Read-Write Memory (RAM), and a Direct Memory Access (DMA) controller, all connected together by an address and data bus and synchronized by a timing generator.

4.2.3 Display Board

Data representing the information to be displayed on the CRT is stored in the microprocessor RAM. The Display board reads this data through the DMA channel and converts it to three analog signals for the CRT display unit.

4.2.4 Input Board

The input board is, in essence, a variable speed analog-to-digital converter. The Analog Input signal is converted to a digital data stream that is stored in memory. The Data or External Trigger input can identify when the conversion is to take place.

Before the input signal can be digitized, the Input board must be initialized by setting the sample clock frequency, the trigger delay counter, the trigger source, the mode "analog" or "digital", and the input threshold voltages. The microprocessor controls these circuit functions by writing data into latches and counters on the Input board. The microprocessor can also test the results of processes by reading the status of the Input board.

4.2.5 Signal Acquisition, Storage and Display

Signal acquisition is accomplished by sampling the input at rates up to 100 MHz. For logic recording, a string of "1's" and "0's", relative to the data threshold level, are continually stored in a 1024-bit high-speed memory. When a trigger event occurs and a trigger event countdown is complete, the 1024-bit high-speed memory is halted and the most recently stored 1000 bits are transferred to a low-speed RAM area.

High speed analog waveform recording is handled in a similar manner except that the process is repeated 39 times, looking at different threshold levels or windows on each pass. The high-speed memory again stores 1024 bits for each scan and transfers this information to RAM. Closely spaced threshold voltages are established for each scan with a logic "1" recorded only if the input is within that window during the associated sampling interval. After 39 scans, bits describing the complete waveform reside in RAM.

For low-speed analog waveform recording, only one occurrence of the signal is required. A successive approximation digitization is made during each sampling interval, and the appropriate column of the 39 row by 200 column memory matrix is developed.

The stored data, for both logic and analog recordings, includes the control settings at which those recordings were made. This data is continually read by the display circuitry to provide X, Y and Z signals to the CRT where the logic traces and waveforms appear.

A logic trace always consists of 200 display bits. Depending upon the SEC/DIV and TRIGGER POSITION settings, anywhere from 40 to 1000 of the 1000 stored bits are used to make up the display bits. Whenever the number of stored bits to be displayed exceeds the number of display bits (200), an algorithm is used to process the stored bits in such a manner that a change of state during any display interval will always be detected and displayed.

Once a logic trace is in RAM and displayed, it can be transferred to tape storage. This can be accomplished only in the PROGRAM mode and only for the most recently acquired logic trace. Except for the bit transfer in and out of the high-speed memory, all other data transfers are in bytes; i.e., RAM to display, RAM to tape, tape to RAM.

Each displayed logic trace is stored in RAM twice. Once as it was originally acquired and once as it is displayed. The 1000 bits in the first location never change, while the display bits in the second location

change as the display parameters are changed; i.e., SEC/DIV, TRIGGER POSITION, AUTO ALIGN.

When the automatic align feature is enabled, the AF/RF ratio must be determined. This is accomplished by counting the total number of bits between the first and last transition for the total number of complete cycles recorded. The total number of bits is divided by the number of complete cycles to yield the number of bits per cycle. Doing this for both the "A" and "R" traces yeilds the frequency ratio.

The number of display bits per cycle of the "R" trace is then increased or decreased to agree with the number of bits per cycle of the "A" trace.

In the automatic COMPARE mode, the bits stored in RAM for both the "A" and "R" logic traces are compared bit by bit. Where there is logical agreement, there will be a "O" logic level, and a disagreement will produce a logic "1". This data is stored in RAM and is displayed as an underscoring of the "A" trace. Only the logic "1" bits are intensified and, therefore, visible on the display.

Another function of the processor is to take these logic "1" areas of disagreement and make a PASS/FAIL decision. It compares the number of consecutive errors against the allowable predetermined limit. If the consecutive errors exceed this limit, the FAIL LED is lit. If the total number of error bits exceeds 30% of the recorded bits, there will also be a FAIL indication. If neither of these limits is exceeded, the PASS LED is lit.

In storing a record on magnetic tape, the 1000 logic bits, the associated 120 control setting bits, and the 8-bit CRC (cyclic redundancy check) are automatically recorded twice in succession. The CRC is a hamming code obtained when the complete string of 1120 bits is divided by a nine term polynomial.

When reading a record, the record index number (1 to 100) is first verified, then the first group of 1120 bits is read into RAM. If a CRC byte developed as described above agrees with the CRC byte from magnetic tape, the 1120 bits are retained in RAM.

If the first of the two test-record copies fails the CRC, the second is read and checked. If both fail, these redundant checks are made up to three more times by rewinding and rereading the two records.

If all eight CRCs fail, the micro-processor displays the message READ ERROR AT XXX (the record index number). Pressing the clear button results in the trace being displayed with an E instead of its normal R prefix.

4.3 Detailed Description

This part of Section IV gives a detailed, circuit-by-circuit description of the Model DTO-1.

4.3.1 Front Panel Circuitry

The Front Panel circuitry performs three functions. It displays instrument status information via LEDs, sends control switch information to the processor, and couples switch and pass-fail information to the probe.

The processor controls all front panel operations through the Data Bus, Address Bus and the WP signal, which originate on the Control board. To illuminate one or more LEDs, the processor addresses either U6 or U7 by setting either A0 or A1, and puts the appropriate information on the data bus and pulses WP high. The low levels from the data bus are latched into U6 to light the PASS, FAIL, ARM SINGLE, ARM CONTIN-UOUS, TRIGGER SLOPE or TRIGGER SLOPE as required. A 3-bit binary code latched into U7 1Q, 2Q and 3Q selects one of the mode LEDs through U8. Also a 3-bit code on U7 4Q, 5Q and 6Q selects one of the trigger source LEDs through U9. To determine if one of the panel switches is depressed, the processor selects one of the four banks of switches by the binary code of A0, A1 acting through gates U4-6, U4-3, U4-11 or U4-8 to bring the switch commons low. If a switch is closed, a low level is coupled through U1 to the data bus when the processor brings RP low. If one of the Data Input Probe switches is depressed, a low level is coupled through U5-3 and Q2 or U5-11 and Q1 to U1.

The Pass and Fail lights on the Data Input Probe are turned on by either a positive or negative current into the reverse con-

nected LED pairs. To turn on the Pass LEDs, a low is latched into U6-1Q (as before for the panel Pass LED) turning on Q3 and Q4. Q4 conducts current from ground in the probe through the two green LEDs to-5.2 V. To turn on the probe Fail LEDs, a low is latched into U6-2Q turning Q5 on. Q5 conducts currents from +5 V through the red LEDs in the probe.

4.3.2   Input Board

The Input board is, in essence, a variable speed analog-to-digital converter. The Analog Input signal is converted to a digital data stream that is stored in memory. The Data or External Trigger input can identify when the conversion is to take place. Refer to Figure 4.2, block diagram, before reading the following detailed description.

4.3.2.1   Initialization

Before the input signal can be digitized, the Input board must be initialized by setting the sample clock frequency, the trigger delay counter, the trigger source, the mode "analog" or "digital", and the input threshold voltages. The microprocessor controls these circuit functions by writing data into latches and counters on the Input board. The microprocessor can also test the results of processes by reading the status of the Input board. Refer to Table 4.1 for the signals under the control of the microprocessor.

The 100 MHz oscillator (7K-15) is divided by decades to 10 Hz. One of the decade frequencies is selected by SCA, SCB and SCC through multiplexer 8J. The output of 8J is further divided by two and five by
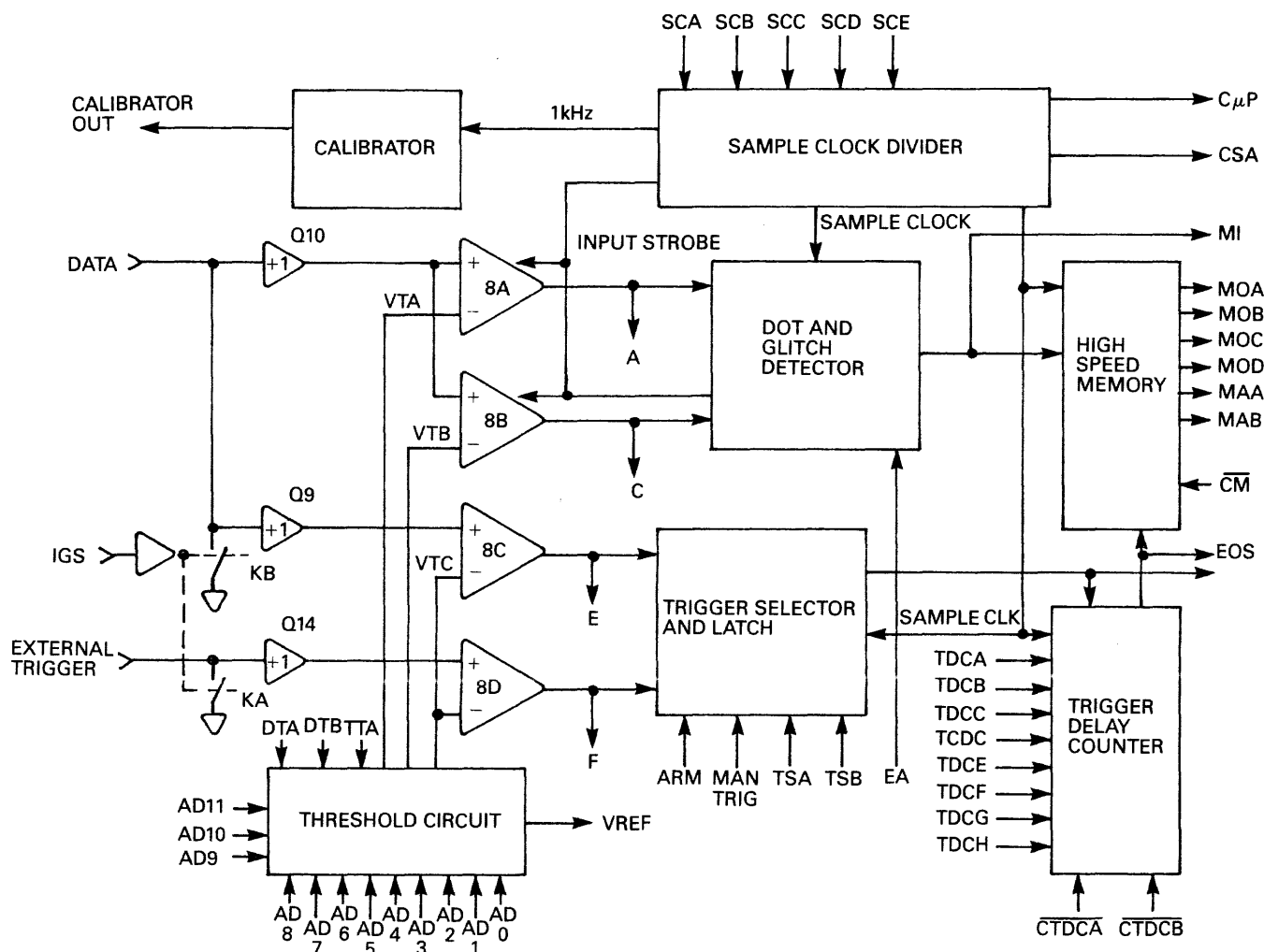
Figure 4.2 Input Board Block Digram

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Table 4.1 Signals Under Control of the Microprocessor

Write	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	-	-	AD5	AD4	AD3	AD2	AD1	AD0
1	0	0	1	-	-	AD11	AD10	AD9	AD8	AD7	AD6 TTL
2	0	1	0	-	-	-	-	IGS	TTA	DTB	DTA
3	0	1	1	-	-	EA	SCE	SCD	SCC	SCB	SCA
4	1	0	0	-	-	-	MAN TRIG	ARM	-	TSB	TSA
5	1	0	1	TDC7	TDC6	TDC5	TDC4	TDC3	TDC2	TDC1	TDC0 (CTDC A)
6	1	1	0	TDC15	TDC14	TDC13	TDC12	TDC11	TDC10	TDC9	TDC8 (CTDC B)
7	1	1	1	*	*	*	*	*	*	*	* ($\overline{CM}$)

* The high speed memory is clocked independent of the data.

READ	A3	A2	A1	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	A	-	MAB	MAA	MOD	MOC	MOB	MOA
1	0	0	1	C	-	MAB	MAA	MOD	MOC	MOB	MOA
2	0	1	0	E	-	MAB	MAA	MOD	MOC	MOB	MOA
3	0	1	1	F	-	MAB	MAA	MOD	MOC	MOB	MOA
4	1	0	0	T	-	MAB	MAA	MOD	MOC	MOB	MOA
5	1	0	1	EOS	-	MAB	MAA	MOD	MOC	MOB	MOA
6	1	1	0	$\overline{CSA}$	-	MAB	MAA	MOD	MOC	MOB	MOA
7	1	1	1	MI	-	MAB	MAA	MOD	MOC	MOB	MOA

7H. SCD and SCE select either the undivided output or the output divided by two or five. The selected frequency at the common output of 7F is the sample clock frequency and is delayed and buffered by 8F-2 and 7E for use throughout the Input board.

The trigger delay counter 3F, 4F, 3E, and 4E is preset with the 16-bit complement of the number of sample clock pulses to be counted after the trigger event. The data bus, buffered by 3H and 4H and shifted to ECL levels, is clocked into 3F and 4F by $\overline{CTDCA}$ and into 3E and 4E by $\overline{CTDCB}$.

The trigger source, one of the four outputs of 8C and 8D, is selected by TSA and TSB through multiplexer 7D to the clock of 6D-15. The trigger source is thus selected as either the positive or negative slope of the DATA or EXTERNAL TRIGGER input.

Input data may be taken in any one of four ways depending on the front panel controls.

1. High Frequency Digital
2. Low Frequency Digital
3. High Frequency Analog
4. Low Frequency Analog

If an Analog mode is selected, the Dot and Glitch detector is configured to detect Dots by E_A; otherwise, E_A is set low, configuring the Dot and Glitch detector to detect glitches. In both Analog modes, with E_A high comparators 8A and 8B are strobed by the sample clock. In the Digital modes the comparator outputs are active at all times.

The threshold voltages required by the comparators as references for detecting the input signals are established by the microprocessor. Before setting the threshold voltages, the offsets of the input amplifiers Q9, Q10 and Q14, and of the comparators are measured by the processor through the threshold circuit. To measure the offsets the microprocessor sets IGS high, grounding the Data and Trigger Inputs through KA and KB. The microprocessor then determines the voltage required at VTA, VTB and VTC to produce a change of level at comparator outputs A, C, and E or F. If one of the inputs requires more than ± 50 mV, the corresponding input is not calibrated and one or more "INPUT OFFSET ERROR" messages will show on the CRT. With the offsets determined, the microprocessors adjust the voltages set at VTA, VTB and VTC to one-tenth of the required threshold voltages.

The threshold circuit consists of +10 V reference 10E, registers 11H and 10H, digital-to-analog converter 11F, output amplifier 11E, three switch 10D holding capacitors C13, 19 and 25, and amplifiers 10B, 10A and 10C. During a measurement the microprocessor automatically controls the DAC inputs and switches to maintain the required threshold voltage VTA, VTB, and VTC.

With DTA, DTB and TTA low, the processor loads registers 10H and 11H with the binary value of the voltage to be set as threshold voltage VTA. The output of digital-to-analog converter 11F is a current proportional to the binary input. Amplifier 11E produces a voltage proportional to the 11F output current that, when acting through resistors internal to 11F between 11F 10 and 11F 9 and 11, hold pins 11E-8, 9, and 11 at ground. Table 4.2 shows the expected output voltage at 11E-6 for selected binary inputs to 11F.

After the voltage at 11E-6 has stabilized, DTA is set high turning on CMOS switch 10D-3,4. Capacitor C13 charges to the desired threshold voltage until DTA is set back low and the switch opens. In a similar manner, voltages VTB and VTC are set and held on capacitors C19 and C25.

The process of repeatedly charging capacitors C13, 19 and 23 maintains the required threshold voltages stable at the inputs to unity gain buffer amplifiers 10B, 10A and 10C. The outputs of the unity gain buffers are filtered to remove any high frequency noise, presenting clean, stable, and accurate threshold voltages to the inputs of the comparators.

Comparators 8A through 8D compare the reference voltages on their negative (-) input to the buffered Data or External Trigger inputs. When the Data or External Inputs are more positive than the corresponding reference voltage, an ECL high level is present on pin 7.

Table 4.2 Selected Digital-To-Analog Output Voltages												
AD												Output Voltage
11	10	9	8	7	6	5	4	3	2	1	0	11 E-6
0	0	0	0	0	0	0	0	0	0	0	0	-2.56000
0	1	1	1	1	1	1	1	1	1	1	1	-0.00125
1	0	0	0	0	0	0	0	0	0	0	0	0.00000
1	0	0	0	0	0	0	0	0	0	0	1	+0.00125
1	1	1	1	1	1	1	1	1	1	1	1	+2.55875

The incoming signal is processed by the DTO-1 in one of four ways depending on the front panel control settings. The processing is dependent on the sample clock frequency and whether an analog or digital trace is to be displayed. The four conditions are shown in Table 4.3.

The most common mode of signal processing is High Speed Digital. To initiate the recording of a digital trace, the SWEEP ARM SINGLE or SWEEP ARM CONTINUOUS is depressed and the processor initializes the input circuitry as described previously. The processor then sets ARM (9J-10) high so that data prior to a trigger event can be loaded into memory.

In the digital recording modes the threshold voltage at 8A-3 and 8B-3 are separated by 20 mV to provide hysteresis. Whenever the input signal at 8A-2 is more positive than the upper threshold level at 8A-3, 6B-2 is set. Whenever the input signal at 8B-2 is less positive than the lower threshold voltage at 8B-3, 6B-2 is reset.

Brief pulses or glitches either momentarily high or low occurring between rising edges of the clock are latched into 6B-2 if the output of 6B-2 and 6B-15 are the opposite state of the glitch. As an example, suppose the signal had been less positive than the threshold voltage for several clock cycles causing 6B-2 and 6B-15 to be low. If the signal becomes more positive than the threshold for more than 10 ns, 6B-2 is preset high by 6A-2. Then, regardless of the sample clock frequency, the high state on 6B-2 is clocked into 6B-15 and then into the high speed memory. A negative-going glitch after being high resets 6B-2 through 6A-15 and is latched

Table 4.3		
Processing Method	Sample Clock Frequency	Seconds/Division*
Low Speed Digital	20 Hz to 500 Hz	0.5 to 5
High Speed Digital	1 kHz to 100 MHz	50 ns to 0.1
Low Speed Analog	100 Hz or 200 Hz	0.5 to 5
High Speed Analog	500 Hz to 100 MHz	50 ns to 0.2

*Assumes trigger position < +7.1 divisions.

into 6B-15 on the next rising edge of the clock. A continuous series of glitches produces alternating highs and lows from the glitch detector indicating that a noisy input signal or too low a sample frequency has been selected. With E_A low the $\overline{Q}$ output 6B-15 is gated through 5C-2 to the Dot and Glitch Detector output register 5D-2, which is also clocked by the sample clock. The output of the Dot and Glitch Detector is connected to the High Speed Memory.

The active high and active low data inputs to the High Speed Memory are translated from ECL to TTL levels by 4C-4 and 4C-5. The sample clock is divided by 2D-2 and 2D-15 to form a four phase clock for the memories. These four ECL level clocks are translated to TTL by 1D. Because the TTL memories 1B, 1F, 2B and 2F cannot store data at 100 MHz, the data stream is demultiplexed into four separate memories, each with its own address counter and input register. The clock phases and timing for memory 1B are shown in Figure 4.3, timing diagram.
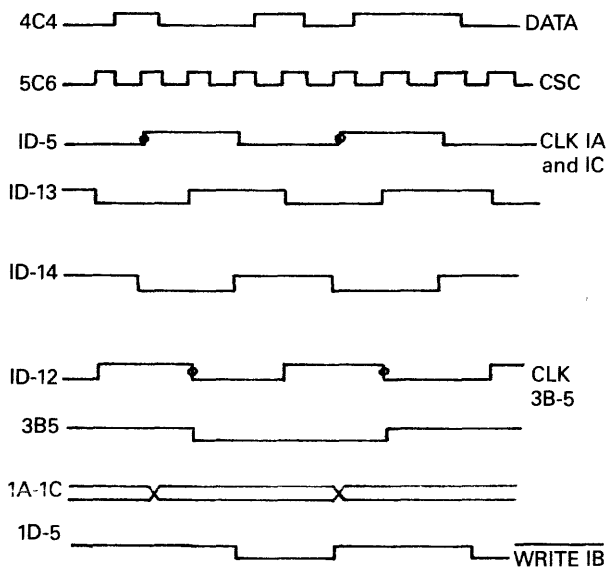

Figure 4.3   High Speed Memory Timing Diagram

Because the memory address counters and clock register 2D are not preset prior to accepting new data, the data is stored sequentially until the trigger event occurs and the Trigger Delay counter stops the high speed memory. Then the data is clocked out of the memory in the same sequence as it was entered. This is possible because the address counter repeats the same address sequence every 256 clocks regardless of where they start. The first, fifth and ninth data bits are clocked into 3B-9 then stored in successive addresses of 2B; the second, sixth, and tenth bits are clocked into register 3C-5 then stored in successive addresses of 2F; the third, seventh, and eleventh bits are clocked into 3B-5 then stored in 1B and so forth until the required pretrigger data has been stored in memory.

Low Speed Digital traces are detected in the same manner as High Speed Digital traces through the input amplifiers, comparators, and the Dot and Glitch Detector; however, the high speed memory is not used. To permit the trace data to be displayed on the CRT as it is being recorded, the processor monitors the sample clock signal through multiplexer 6C-13 and transfers the data directly to the processor memory from the output of the Dot and Glitch Detector at 5D-2.

4.3.2.2   Input Amplifier Circuits

The External Trigger and Data Inputs are coupled to the DTO-1 through X10 probes similar to conventional oscilloscope probes. The signal is attenuated by the ratio of the 9 MΩ resistor in the probes and the 1 MΩ resistors (R50 and R82) in the DTO-1. The variable capacitors in the probe compensate the probe cable and DTO-1 input capacitances. Diodes CR1, CR2, CR3 and CR4 clamp any out-of-range input signals to plus and minus 3 V to prevent damage to the DTO-1 input circuitry. Resistors R46 and R80 limit current into the protection diodes. FET matched pairs Q10, 9, and 14 form unity gain voltage amplifiers with low output impedances to drive the voltage comparators. Two amplifiers are used on the Data Input to isolate the data and trigger comparator circuits so that trigger comparator noise doesn't degrade the signal to the data comparators 8A and 8B.

High Speed Analog signals are recorded using a unique 1-bit conversion technique (patent application pending). At the start of the conversion, threshold VTA is set to a voltage equal to the highest voltage to be displayed on the CRT and VTB is set to a

voltage one-tenth of a division lower. At the falling edge of CS a 2 ns pulse briefly enables comparators 8A and 8B. If the DATA INPUT signal is more positive than the threshold voltages, the comparator outputs latch high; if the DATA INPUT is more negative than VTA or VTB one of the corresponding outputs latches low. The output of 8A is latched into register 6B-2 and the output of 3B is latched into register 6B-15 on the rising edge at the sample clock. Gate circuitry 5B-3, 5B-15, 5B-2 and 5C-15 output a high level to latch 5D-2 only if the signal was between or has just crossed the threshold voltages. Data from the Dot and Glitch Detector is clocked into the High Speed Memory just as it is in the High Speed Digital mode. After the trigger event and count down have occurred, the data indicating when the signal was in the first "window" is transferred from the high speed memory to the processor memory. Threshold

voltage VTA is then decreased by two-tenths of a division creating a new window and new data. The windows are leapfrogged down and data is transferred to the processor memory until 39 200-bit lines are stored in the processor memory. These 39 200-bit lines of data are used to intensify dots on the CRT screen to produce the High Speed Analog Display.

A Low Speed Analog Display is recorded by a successive approximation routine. Rather than requiring 39 repetitions of a low speed analog signal, the waveform is digitized completely as it occurs. After each rising edge of the sample clock, the processor digitizes the signal according to the routine shown in Figure 4.4.

The Threshold voltage is initialized to the mid-value of the analog display area, the raster number (R) is set to 20 (equivalent to
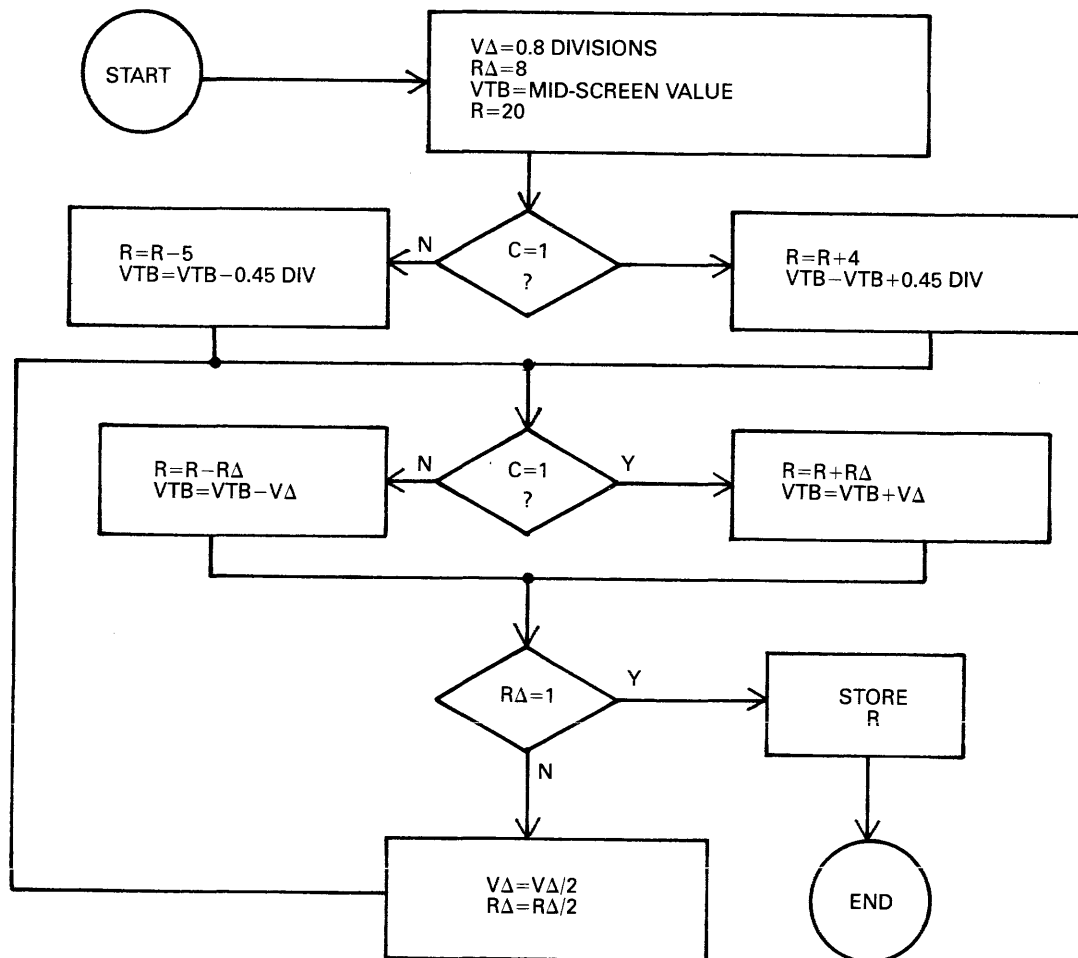

Figure 4.4 Diagram of Low Speed Analog Conversion

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the mid-value), the change in raster is set to 8 and the change in VTB (VA) is set to 0.8 divisions. The first decision about C (the output of 8B) determines if the signal is above or below the mid-value, then adjusts R and VTB accordingly. The second decision is made four times, each time adjusting VTB and R toward the signal value and the dot position to be intensified on the display. When the C=1? decision has been made the last time, the value of R is stored in the processor memory. After digitization is complete, the processor fills in the rising and falling edges of any vertical discontinuities in the displayed waveform. Signal frequencies higher than one-fourth the sample frequency can cause erroneous displays.

4.3.2.3 Trigger Circuit

The recording of a trace while initiated by a high ARM signal, is terminated by the Trigger Circuit. After sufficient pretrigger data has been recorded, the processor sets ARM low, then recording continues until a trigger occurs and the trigger delay counter counts up to FFFF HEX. The trigger event can come from either the DATA INPUT, the EXTERNAL TRIGGER or the processor. The EXTERNAL TRIGGER is attenuated to one-tenth its actual value by the 9 MΩ input resistor of the probe and the 1 MΩ resistor R82 in the DTO. The resulting signal is buffered by Q14 so that it can drive the comparator circuit. The (-) input to comparator 8D is threshold voltage VTC and the (+) input is the attenuated and buffered EXTERNAL TRIGGER voltage. If the EXTERNAL TRIGGER is selected, TSB is high enabling 8D outputs 7 and 8.

If a positive slope, external trigger is selected 8D-7 is connected through 7D to 6D-11. When a positive transition with respect to the threshold voltage occurs, flip-flop 6D-15 is set. A small portion of the output of comparators 8C and 8D are fed back to the (+) inputs of 8C and 8D to prevent oscillations. Negative slope transitions are coupled through 7D and 8D-8. Internal triggers are obtained from the DATA INPUT through buffer Q9 and comparator 8C in a similar manner to external triggers. After 6D-15 is set, the trigger is recognized on the next rising edge

of CS by 6D-2. When 6D-3 goes low, gates 6E-3 and 6E-2 are enabled and the sample clock begins incrementing the Trigger Delay Counter. When the Trigger Delay Counter reaches its top count (FFFF), 3D-3 goes high and on the next sample clock 5D-15 goes high, stopping the High Speed Memory by inhibiting 5E-2. The processor detects the end of the recording process by testing EOS at 6C-12.

After EOS, the processor transfers the contents of the high speed memory to the processor memory. Memory outputs MAA and MAB identify which of the memory data outputs MOA, MOB, MOC or MOD is active at each location. The processor identifies the first bit, reads it, writes it into the processor memory, then advances to the next High Speed Memory location by bringing $\overline{CM}$ (3J7) low momentarily. This process is repeated until all the required bits have been transferred.

4.3.3 Display Board

Refer to the back diagram in Figure 4.5. Data representing the information to be displayed on the CRT is stored in the microprocessor RAM. The Display board reads this data through the DMA channel and converts it to three analog signals for the Model 350 CRT display unit. The X output controls the horizontal position of the electron beam, the Y output controls the vertical position of the electron beam, and the Z output controls whether the beam is turned on or off. By modulating the X, Y, and Z signals, the display board paints a new picture on the CRT 50 times per second.

The Display board sequences through three display modes during each display cycle. The three modes are Digital Trace, Analog Trace and Character Display. When power is first applied to the DTO, $\overline{POP}$ is low and the circuit is reset; when $\overline{POP}$ returns high the Digital Trace mode is entered.

Each mode is indicated by a flip-flop. During the Digital Trace mode, T (2E-6) is high; during the Analog Trace mode, A (2E-9) is high; during the Character Display mode, W (2F-9) is high. When trace descriptions or characters are being transferred through the DMA channel from RAM, M (3F-9) is high. Figure 4.6 shows the time relationships of these signals.
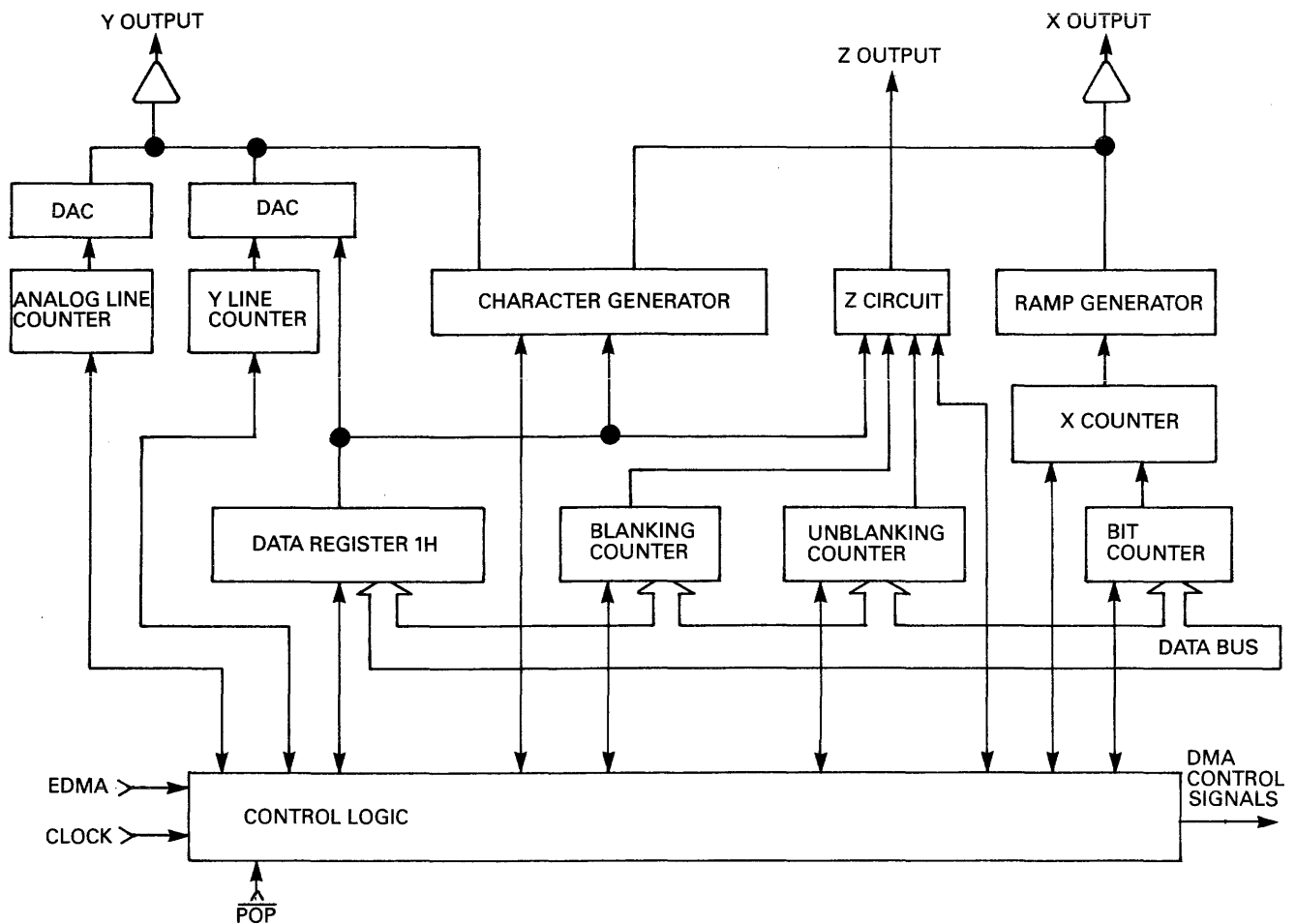
Figure 4.5   Display Board Block Diagram
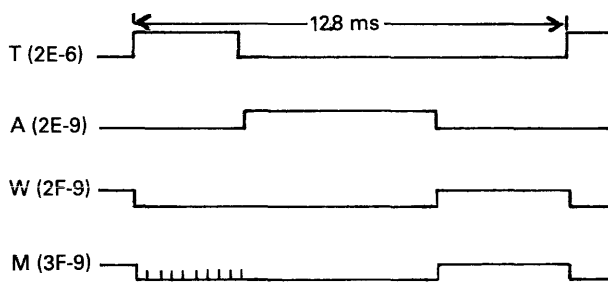
Figure 4.6   Signal Time Relationships

To display the first trace at the top of the CRT, the DMA channel is activated and the unblanking, blanking, and data location are read from RAM. Unblanking time is loaded into 2K and 3K, banking time is loaded into 4K and 5K and the starting bit location is loaded into 1K. The start word and page locations are loaded into the 12-bit DMA address counter on the Control board. The first word of trace data is read from the RAM address indicated by the 12-bit DMA address counter. The data is transferred from RAM via the data bus to 1H. The data bits in 1H are scanned by counter 1E and multiplexer IF, but the X sweep is not enabled until the start bit is reached as indicated by 1K. When the last bit in the first data word has been displayed, the DMA channel reads the next memory location into 1H and each bit is read. As each bit is read the unblanking and blanking counters are incremented. When the unblanking counter reaches all ones, the beam is turned on. When the blanking counter reaches all ones, the beam is turned off. As the data bits are read the X counter 6D and 6E is incremented.

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The data multiplexed through 1F-5 modulates the Y output to produce the high-low logic diagram. As the X counter is counting up, the ramp generator is enabled and current source Q17 charges C39 producing a linear voltage ramp at 8J-6. The Y digital signals, including the Y line counter input, are converted to an analog level by 7J to produce the voltage step necessary for the Y output. At the end of the digital trace the X counter is reset, the X ramp is reset, the Y line counter is incremented, a new trace description is obtained from RAM and the whole process is repeated until the eighth trace. During the eighth trace the data modulates the Z output rather than the Y to underline the seventh trace as required. After the eighth trace the bottom trace is developed as usual.

During the second display mode, the analog trace, if any, is displayed. After the Digital Trace mode is completed, the Display board picks up the Analog Trace description. The blanking word is loaded into 4K and 5K and blanks the analog trace completely unless the word is all one's. The unblanking word is loaded into 2K and 3K but is not used. The address of the first word of trace data is loaded into the 12- bit DMA address counter on the Control board. The Y output is set down one division, the analog line counter 6F and 6G is set to 1, the X ramp is reset, and the X counter is reset. The first data word is accessed from RAM and

loaded into 1H. The X ramp and X counters are enabled and each bit of the data word is read in sequence through the multiplexer to intensify modulate the beam. When the 200 bits of the 25 data words have been read and the X counter reaches 200, the beam is turned off, the X ramp is reset and the Y output is moved down one-tenth of a division. When the X counter reaches 208, it is reset to 1 and the next line of data is displayed. After 39 lines of data the analog line counter indicates the end of the Analog Display mode.

During the third display mode, the characters and symbols (see Table 4.4) are written on the CRT. Each character is read in sequence from the RAM address indicated by the 8-bit address counter on the Control board and stored in 1H. The Y line counter and DAC position the beam for the first character.

The 32-word character generator ROM 1G is addressed by the word in 1H. The output 1G controls the stroke circuit. the ROM output can cause the spot on the CRT to move in any one of eight directions with the beam on and any one of seven directions with the beam off, or reset the beam to its point of origin. Once the character is loaded into 1H, counter 1E, 1C-6, 1C-9 addresses in sequence the 32 strokes to make the required character or symbol. After the last stroke (S31) the beam is positioned to the next origin by the X ramp generator and Y counter and DAC.

Table 4.4	Display	Words	and	Symbols			
00$_H$	"BLANK"	08	8	10	P	18	?
01	1	09	9	11	R	19	+
02	2	0A	0	12	S	1A	-
03	3	0B	A	13	T	1B	C
04	4	0C	E	14	W	1C	D
05	5	0D	G	15	u	1D	.
06	6	0E	I	16	n	1E	F
07	7	0F	N	17	m	1F	X

Four characters or symbols are generated in the first division of the first seven lines and forty on the bottom line. If the most significant bit of the word in 1H is a one the character or symbol is shifted down 3/32 of a division.

4.3.4   Control Board

The Control board controls all operations directly or indirectly performed by the DTO-1. Front panel switches read by the Control board are translated into the control signals required to perform the assigned task. The Control board contains a microprocessor, Read Only Memory (ROM), Read-Write Memory (RAM), and a Direct Memory Access (DMA) controller, all connected together by an address and data bus and synchronized by a timing generator. Refer to the block diagram in Figure 4.7.

4.3.4.1   Timing Generator

The Timing Generator breaks the 1 μs system cycle into several time intervals. Each 1 μs interval is divided so that it shares the RAM between the DMA Channel and the microprocessor.
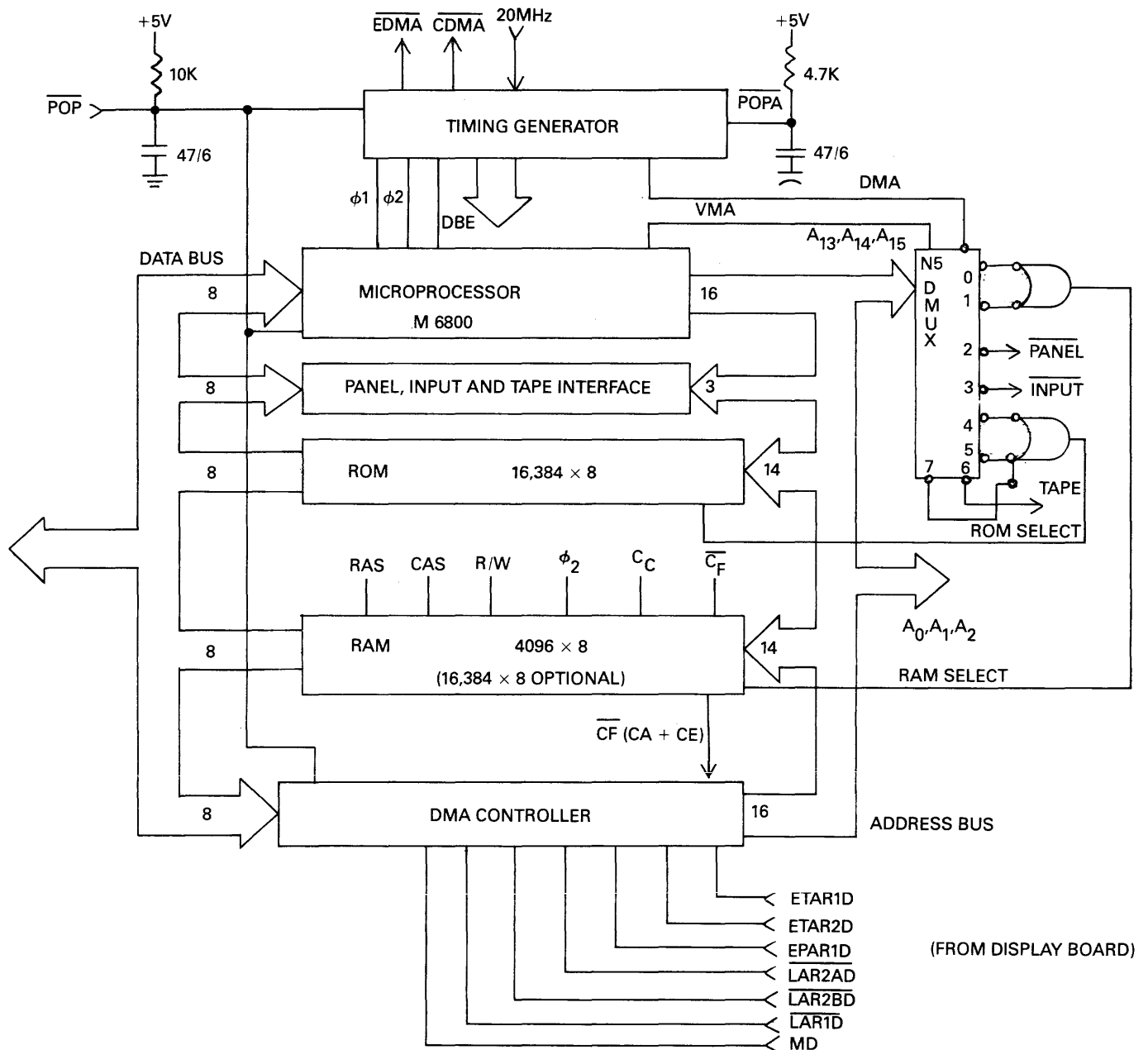
Figure 4.7   Control Board Block Diagram

-48-

When power is applied to the system flip-flops H2-5, H2-9, L2-5, L2-9, L3-5 and L3-9 are reset to zeroes during the R15, C42 charging time constant. Then the 20 MHz Clock from the Input board increments the 20 state feedback register H2-5 through L3-5 and toggles L3-9, dividing each 1 µs into 20 states. Refer to the timing diagram in Figure 4.8.

The following signals are derived from this counter:
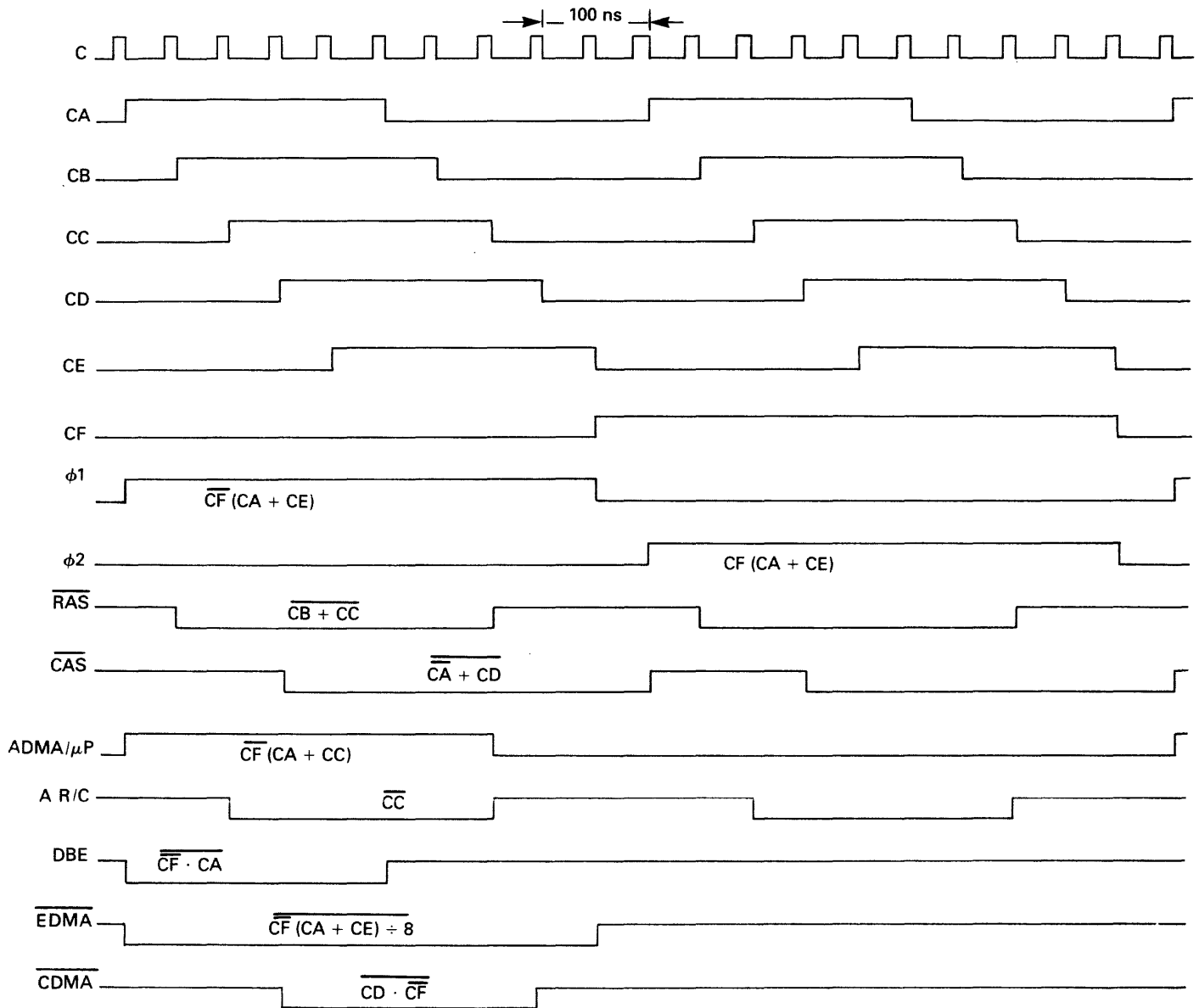
Figure 4.8   Cycle Sharing Timing Diagram

A. Microprocessor

    1. Ø1 Clock   H4-11
    2. Ø2 Clock   H4-8
    3. DBE   H4-3

B. RAM

    1. $\overline{RAS}$ N11-8
    2. $\overline{CAS}$ N11-10
    3. WRITE   H1-8
    4. $\overline{ROE}$ N11-6
    5. CC   L2-5
    6. $\overline{CC}$ L2-6

C. Data Bus Control

    1. CF   L3-9

D. DMA

    1. $\overline{EDMA}$ H3-12
    2. $\overline{CDMA}$ E4-11

Counter N4 gates EDMA so that it occurs once every 8 μs.

The microprocessor is a Motorola type M6800 (refer to M6800 product brochures for detailed information). The processor receives instructions and data from the ROM, writes data to and reads data from the RAM, and controls the other functional blocks. When power is applied to the DTO, R12, C25 holds $\overline{RESET}$ (K2-40) low to initialize the 6800. The timing generator provides DBE, and clocks Ø1 and Ø2 through inverting transistor drivers. The processor outputs ROM, RAM and I/O addresses through 16 address lines A0 and A15. The processor reads and writes instructions and data through data lines D0 through D7. Output VMA indicates valid information is on the address bus and R/W indicates whether the processor is reading or writing data through the data bus. The other processor inputs and outputs are not used. Circuits H6, H5, L5 and L6 buffer the processor from the address and data buses.

The eight ROMs A2 through A9 are connected directly to the address bus to select one of the 2048 words in each ROM. If the processor is reading a word from ROM (indicated by H3-8 high) one of the ROMs will be selected by C1 and it will output a word onto the data bus through B1.

Trace data, display data and numerous temporary variables are stored in the dynamic RAMs D4, E1, F1, H8, J1, K4, L7 and M2. These memories may be accessed twice during each processor cycle. During the first half cycle the RAMs are connected to the data bus for a DMA read (DMA is always a read) and during the second half for a processor read or write. Each RAM access requires the sequential application of the low and high order address bits through B2 and A10. The low order addresses are strobed by $\overline{RAS}$ and the high order by $\overline{CAS}$; if the processor requests a write, WRITE will be low during the second $\overline{RAS}$ - $\overline{CAS}$ cycle. Refer to the Timing Generator in Figure 4.7. Data from the RAMs drive the data bus through H7. The DMA channel provides the memory refresh.

Memory block decoder N5 divides the 65K word address space into eight segments shown in Table 4.5. N5 outputs are active only when VMA and $\overline{DMA}$ (L3-7) are true.

1. Front Panel Interface. $\overline{RP}$ (N7-6) selects reads of the front panel switches. WP (N7-4) selects writes to the front panel LEDs.

2. Input PCB Interface. $\overline{RI}$ (N8-6) selects reads of the Input PCB status and data. $\overline{WI}$ (N8-8) selects writes to the input PCB.

3. Tape Unit Interface. Refer to Appendix (X) for functions of specific Tape Unit signals.

See Table 4.6 for tape unit control signals.

4. Read Bus Enable T. (L1-6) enables the output of data from the Tape unit to the data bus (D0 through D7). L1-12 puts tape unit status information on the bus via M1.

5. DMA Counters. The display unit accesses RAM every 8 us through the DMA channel. The word to be accessed is determined by either one of two counters, 8-bit counter E5, E6 for control bytes and display characters or the 12-bit counter E8, E10, E9, for trace information. The 8-bit counter is reset at the start of each display cycle by $\overline{LARID}$ and

		Table 4.5				
	Address					
Output	A15	A14	A13	VMA	$\overline{DMA}$	
0	0	0	0	1	1	RAM 0 to 8K
1	0	0	1	1	1	RAM 8K to 16K
2	0	1	0	1	1	Front Panel Switches and Lights
3	0	1	1	1	1	Input Board Control and Data
4	1	0	0	1	1	ROM 0 to 8K
5	1	0	1	1	1	ROM 8K to 16K
6	1	1	0	1	1	Tape Unit
7	1	1	1	1	1	ROM - Restart Vector for µP

		Table 4.6	Tape Unit Control Signals			
N1 Output	A2	A1	A0	Signal	Function	
0	0	0	0	$\overline{LD\ W\ BUF\ T}$	Load Write Buffer	
1	0	0	1	$\overline{RES\ T}$	Reset Tape Unit	
2	0	1	0	$\overline{RUN\ T}$	Run Tape	
3	0	1	1	$\overline{STOP\ T}$	Stop Tape	
4	1	0	0	-	Set Read Latch	
5	1	0	1	-	Reset Read Latch	
6	1	1	0	-	Set Forward Latch	
7	1	1	1	-	Reset Forward Latch	

is incremented as required when ETAR1D and MP are high. The lower 8 bits of the 12-bit counter (E8, E10) are preset from the data bus by LAR2AD. The 12-bit counter increments as required when EPAR2D and ETAR2D are high. MD(J2-22) selects whether the 8 or 12 bit counter is connected to the address bus during a DMA cycle.

4.3.5   Power Supply

The Power Supply supplies seven voltages and two control signals to the DTO circuits. The seven voltages and current ratings are:

Voltage		Current
+5 V $\pm$ 0.25 V	at	8 A
-2 V $\pm$ 0.08 V	at	0.7 A
-5.2 V $\pm$ 0.2 V	at	2.3 A
+15 V $\pm$ 0.6 V	at	0.2 A
+15 V (Tape)	at	1 A pulse
+12 V $\pm$ 0.5 V	at	0.4 A
-15 V $\pm$ 0.6 V	at	0.2 A

Refer to the schematic in Section VIII. Power to the DTO is supplied by conventional utility service and may be 100 to 240 V and 50 or 60 Hz. The input power module is used to connect the appropriate primary winding of T1 via an integral printed circuit board, protect the DTO from damage by a replaceable fuse, and reject power line noise with the integral filter. Proper fan voltage is also selected by the input module. The secondaries of T1 are rectified by CR1, 3, 4, 5, and 6 to provide the following approximate voltages:

Voltage	Filter Capicitor
+9 V	C1
-10 V	C2
+20 V	C3
-20 V	C9

The filter capacitors reduce the ripple to the regulators. Six regulators are used to produce the seven output voltages. All but the +5 V regulator are three-terminal integrated circuit devices that set the output voltage to the required value and limit their output current to prevent their destruction and protect the load.

The +5 V regulator conducts current to the load through Q1. The output voltage is compared to the -5.2 V output by resistors R6 and R11 and operational amplifier U1-1. If the output voltage is too low, U1-1 output goes positive increasing the current in Q2 and Q1 until the output is high enough. In the event that excessive current is required by the load, sufficient voltage is dropped across resistor R3 to cause U1-7 to go positive, forward biasing CR2. Current through CR2 increases the voltage at U1-2 so that U1-1 decreases the current in Q2 and Q1. The current limit is set to "fold back" so that less current is supplied into a short circuit than +5 V.

To prevent the DTO from being used with faulty power supplies, the circuitry associated with U2 holds the power on preset line ($\overline{POP}$) low whenever the +12 V, +5 V, -2 V, or -5.2 V supply is unusually low. Each voltage is compared to the voltage of the 5.1 V zener CR9. If one of the voltages is low the corresponding output of U2 will forward bias the diode (CR10, 11, 12 or 13) and turn on Q10.

It is possible for current to flow through the read/write head in the tape drive if the +5 V supply goes low before the +15 V to the tape unit. To prevent this, the +5 V supply is compared to the voltage of 5.1 V zener diode CR7. If the +5 V supply goes low, Q8 will turn on, which in turn turns on Q9. The collector of Q9 is connected into the Tape drive electronics to disable the write circuitry.

SECTION V

CALIBRATION PROCEDURES

5.1   Recalibration of Internal Circuits

The following calibration procedures are intended to be used in recalibrating the internal circuits of the Model DTO-1. The entire circuitry was calibrated before shipment and should not require any recalibration for at least six months or 1000 hours of operation. Refer to the schematics and assembly drawings in Section VII for additional help in locating devices referenced in this procedure. The display used in the DTO-1 is a Biomation Model 350. If failure of display occurs, refer to the Model 350 Operating and Service Manual (consult factory if no manual is supplied).

The Model 350 has two versions: -10 (standard) and -20 (DTO). Use -20 for DTO-1 references. To calibrate the Model 350, a signal input adapter is needed to route X, Y, Z in.

5.2   Required Test Equipment

The following test equipment are required to calibrate the DTO-1.

1. 250 MHz Oscillator (Tektronix 475).

2. Digital Voltage Meter (Dana 4200).

3. DTO-1 Data Probe or Biomation X10 Probe.

4. 3M DCD-1 Alignment kit (contact factory).*

   (a) Speed calibration cartridge.
   (b) Azimuth Alignment cartridge.

   *NOTE: Usage of the cartridges should be limited to total replacement of a Tape Drive System. Tape drive boards (3M) are calibrated with a specific tape head by serial numbers. See Tape Adjustment section.

5.3   Power Supply Verification

Before recalibrating any circuit in the DTO-1, it is necessary to check power supplies. Remove the bottom cover of the DTO-1, and stand the unit up on its rear feet. Turn power to on; unit should come up in TRIM mode. On the Mother Board, check the voltages with a DVM. Connect (-) lead of DVM to the chassis. See Figure 5.1 and refer to Table 5.1.

Table 5.1

A.   Tape Drive
(Edge of Tape Boards)

Pins (J6 - Top)		(J6 - Bottom)
1	+15 V	N/C
2	GND	GND
3	+5 V	+5 V
4	GND	GND
5	+15 V	N/C

B.   Input Board
(Edge Connector)

	Voltage Range
J1-16	-1.92 to -2.08 V
J1-22	-5.0 to -5.4 V
J1-18	4.75 to 5.25 V
J1-25	14.4 to 15.6 V
J1-CC	-14.4 to -15.6 V
J1-5	9.9 to 10.1 V

C.   Filter Capacitor

13.5 to 15.6 V

5.4   Display Adjustment

Put display board on extender with power off. Turn power to on. Enter SCOPE mode. Connect probe to trim point and press ARM.

TOP VIEW

REF

(4 PLCS) (2 PLCS)

(2 PLCS)

(8 PLCS)

THRU 350
INTO DTG

AZIMUTH
ADJUSTMENT
(HEX NUT)

(4 PLCS)
THRU F.P. CASTING
TO TAPE DRIVE BKT.

(4 PLCS)

POWER
SUPPLY ASSY

16 POS CONNECTOR FROM
MOTHER BD ASSY

6 POSITION CONNECTOR FROM CAP ASSY

BOTTOM VIEW

THIS SIDE
AGAINST
FRONT PANEL

TAPE DRIVE

-02 VERSION

01 VERSION

REMOVE MOUNTING
BRACKETS THAT COME
WITH TAPE DRIVE

(3 PLCS)

SIDE VIEW

(4 PLCS)

(4 PLCS)

CAPACITOR ASSY NOT
SHOWN FOR CLARITY

CRT ASSY

(2 PLCS)

INSIDE BACK LIP

(2 PLCS)

8 PLCS

FRONT END PCB

DISPLAY PCB

CONTROL PCB

INPUT BD.

**DC VOLTAGE
MEASUREMENTS**

WIRE FROM TEST POINT
ON FRONT PANEL

REF
FRONT END PCB
COMPONENT SIDE

(8 PLCS)

STACKED RIBBON
CABLE FROM FRONT
PANEL

MOTHER BD ASSY

(4 PLCS)

GRAY RIBBON CABLE
COAX CABLE
STRANDED

3 PLCS

(2 PLCS)

(9 PLCS)

(6 PLCS)

HOLDS SUPPORT TRAY AND
CARD CAGE.

C9

**FILTER CAPACITOR
VOLTAGE MEASUREMENT**

CABLE LIES
ON SUPPORT
TRAY PLUGS INTO
BOTTOM BOARD

(4 PLCS)

THIS CONNECTOR HAS 5 WIRES
BOTTOM CONNECTOR HAS 3
CONNECTORS COME FROM MOTHER BD.

ADD JUMPER WIRE, 24 AWG SOLID
FROM CENTER TO J8-6

BEND POST 90° AS SHOWN

ADD JUMPER WIRE TO PIN 25 ON FAR SIDE

RE: TAPE DRIVE (J6)
TOP/BOTTOM CONNECTORS

FIGURE 5.1

-54-

A squarewave trace should appear on the screen.

Use Trace Rotation (on side of 350, inside DTO-1) to level trace on display. Using DTO-1 Horizontal and Vertical controls, set display "S" and trace to touch left graticule line (See Figure 5.2).
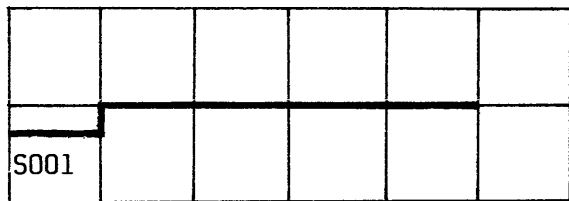

Figure 5.2

Use R3 (Display Board) to adjust trace to just touch right graticule line (see Figure 5.3).
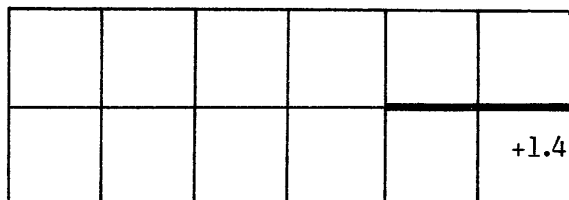

Figure 5.3

Use R49 to set the four of the +1.4 V Trigger Threshold to touch the right graticule as in Figure 5.3.

Using Sweep Arm Single and Data Position 100 (to scroll data up), obtain eight traces of the trim signal (S001 through S008). Using DTO-1 vertical control, set S001 on the second horizontal graticule line from the top, and at top of squarewave trace set S001 to touch first horizontal graticule line.

Use R2 to set S008 on the bottom line of display.

Press ANALOG and set the analog voltage scale to 0.5 V/DIV with +3 V at the top of the display area (see Figure 5.4). Change SEC/DIV to 5 m, and shoot trace of calibration signal. Use DTO-1 Horizontal control to line the left side of the raster with graticule line.

Use R53 to adjust the right side of the raster to touch right graticule line.

Use R1 to adjust raster so that it is evenly spaced between the second and sixth horizontal graticule lines (see Figure 5.4).
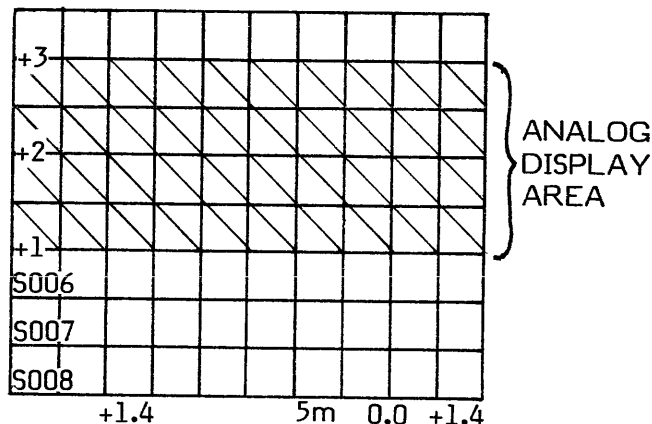
Figure 5.4

Turn off DTO, and replace the display board.

5.5   100 Mc Oscillator Adjustment

Connect oscilloscope to CALIBRATION TEST POINT. The signal should be 1 + 0.5 kHz. Adjust C41 on the Input Board to obtain the proper frequency. Turn power off then on, and verify a 1 kHz waveform.

5.6   Tape Drive Azimuth Alignment

Refer to DCD-1 Data Cartridge Drive Instruction Manual sections 3-1-2-4 and 3-2-12 for complete details on alignment. The alignment normally does not need to be changed except if a new or replacement assembly is used.

SPECIAL
NOTE: To properly use a DTO-1 tape in any machine, it should be rewound at least once before using (TRANSCRIBE mode).

Head Alignment (Azimuth) can cure READ, INDEX, and WRITE **errors** between two different DTOs if the tape can be read on the DTO. After alignment is obtained, a spot of "goop" or screw locking liquid should be used.

SECTION VI

MAINTENANCE

6.1 Introduction

This section covers the DTO-1 self-diagnosis routine within the instrument. The diagnostic routine checks the microprocessor ROM and RAMs using a CRC checking method. Repair of other boards (Display and Input) can be performed with the aid of the technical description or additional information from the factory.

Drawings in Section VII have been included to aid service personnel who wish to troubleshoot to the component level. Additional assistance in a particular problem can be obtained by contacting the Customer Service Department at the factory: Phone (408) 988-6800, TWX 910-338-0509.

In summary, there are two methods of service available:

1. Return the entire unit to the factory or service center for repair.

2. Troubleshoot the problem to the component level with the aid of the Technical Description and schematics or with the aid of factory personnel.

6.2 Diagnostic Routine and Indications

Place the DTO-1 on a bench with the display facing the user. Power up the DTO-1 and note that the TRIM mode is displayed. The LEDs on the front panel will be as follows:

Key Front Panel Lights

	Diagnostic Check	ROM Error	RAM Error
PASS		X	X
FAIL		X	X
_∫_	X	X	
‾↘_			X
(0) INTERNAL	X		

	Diagnostic Check	ROM Error	RAM Error
(1) INT AUTO			
(2) AUTO			
(3) EXT AUTO			
(4) EXTERNAL			
(0) TRIM	X		
(5) AUTOSCOPE			
MIXED			
SCOPE			
PROGRAM			
TRANSCRIBE			

> NOTE: See coding for error detection in ROM and RAM.

Coding for error detection:

Note the numbers to the left of the Trigger Source and Mode LEDs. When ROM or RAM failure occurs, add the values of these LEDs together to determine the location of the fault (see Figure 6.1).
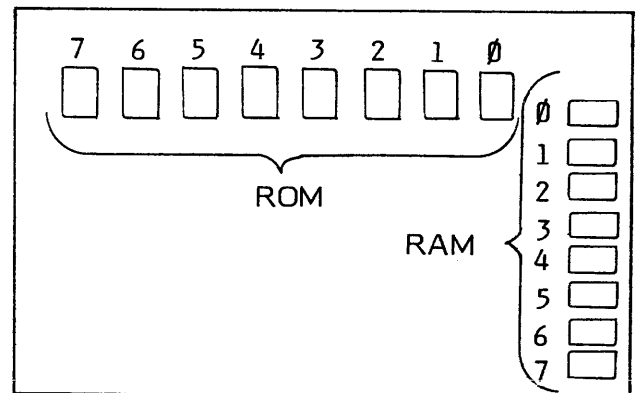
Figure 6.1 Control Board

The diagnostic routine can be called up (performed) any time. When the DTO-1 is powered up or when MODE is in any operation other than TRIM, then return it to TRIM.

SECTION VII

SCHEMATICS AND ASSEMBLY DRAWINGS

7.1   Introduction

This section contains the schematics and assembly drawings for the Model DTO-1. Parts lists are also included.

7.2   List of Drawings

7.3 __Parts Lists__

The materials in the following lists are subject to change without Gould Inc.'s prior notification. For list verification, contact the Customer Service Department at the factory: Phone (408) 988-6800, TWX (910) 338-0509.

7.3.1 List of Parts Lists
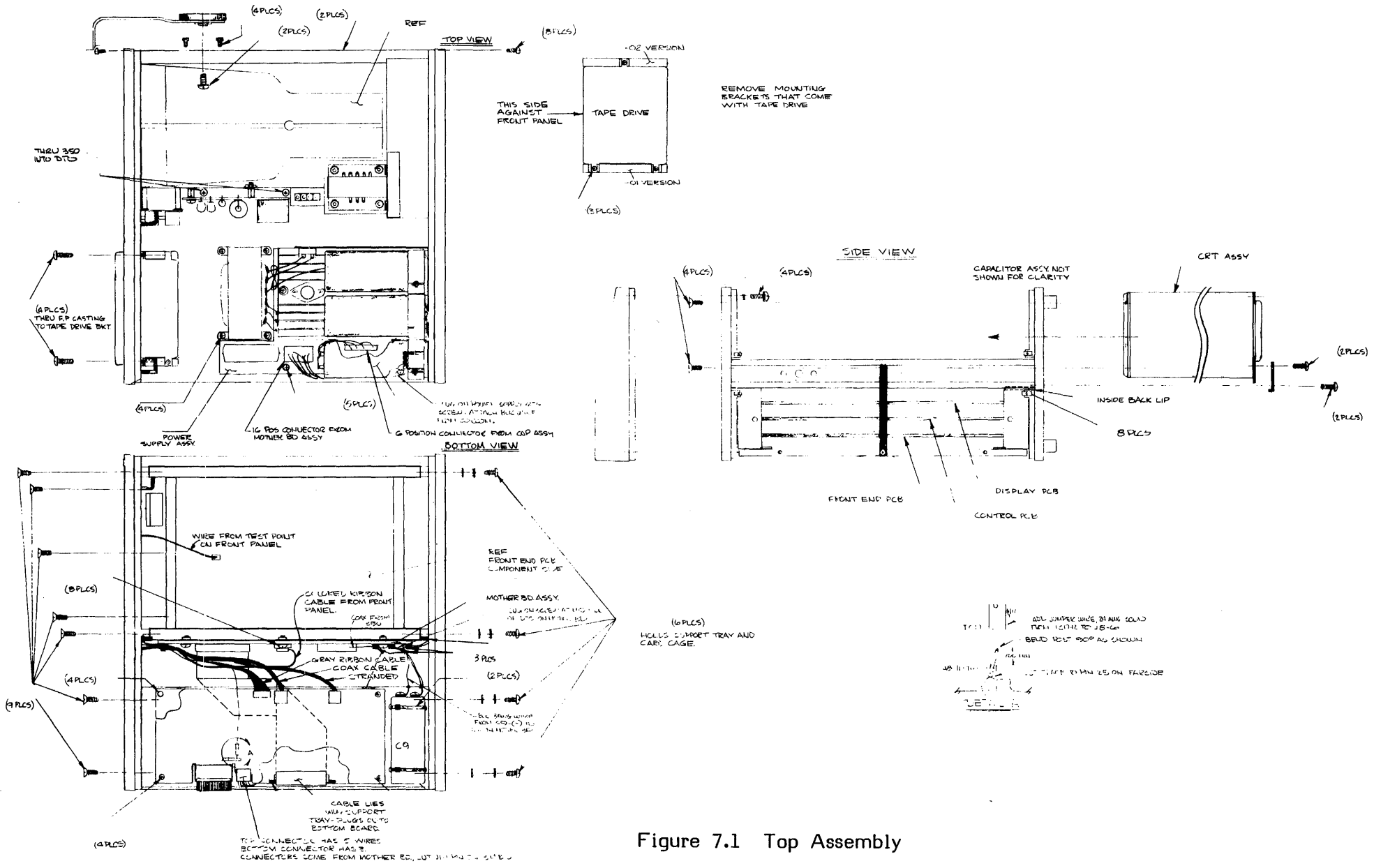
Figure 7.1 Top Assembly

SIDE VIEW   REAR VIEW

INSULATING WASHERS

SWITCH PC BD.   LOGIC PC BD.

COMPONENT SIDE

COMPONENT SIDE

#6KEI-NUT (6PLCS)

PLUG TOGETHER AFTER ASSY.

P2

P1

CONNECTOR FROM TEST POINT.
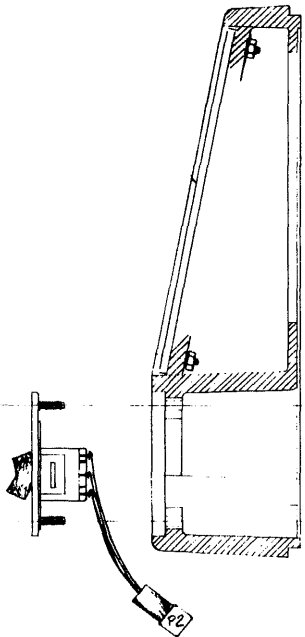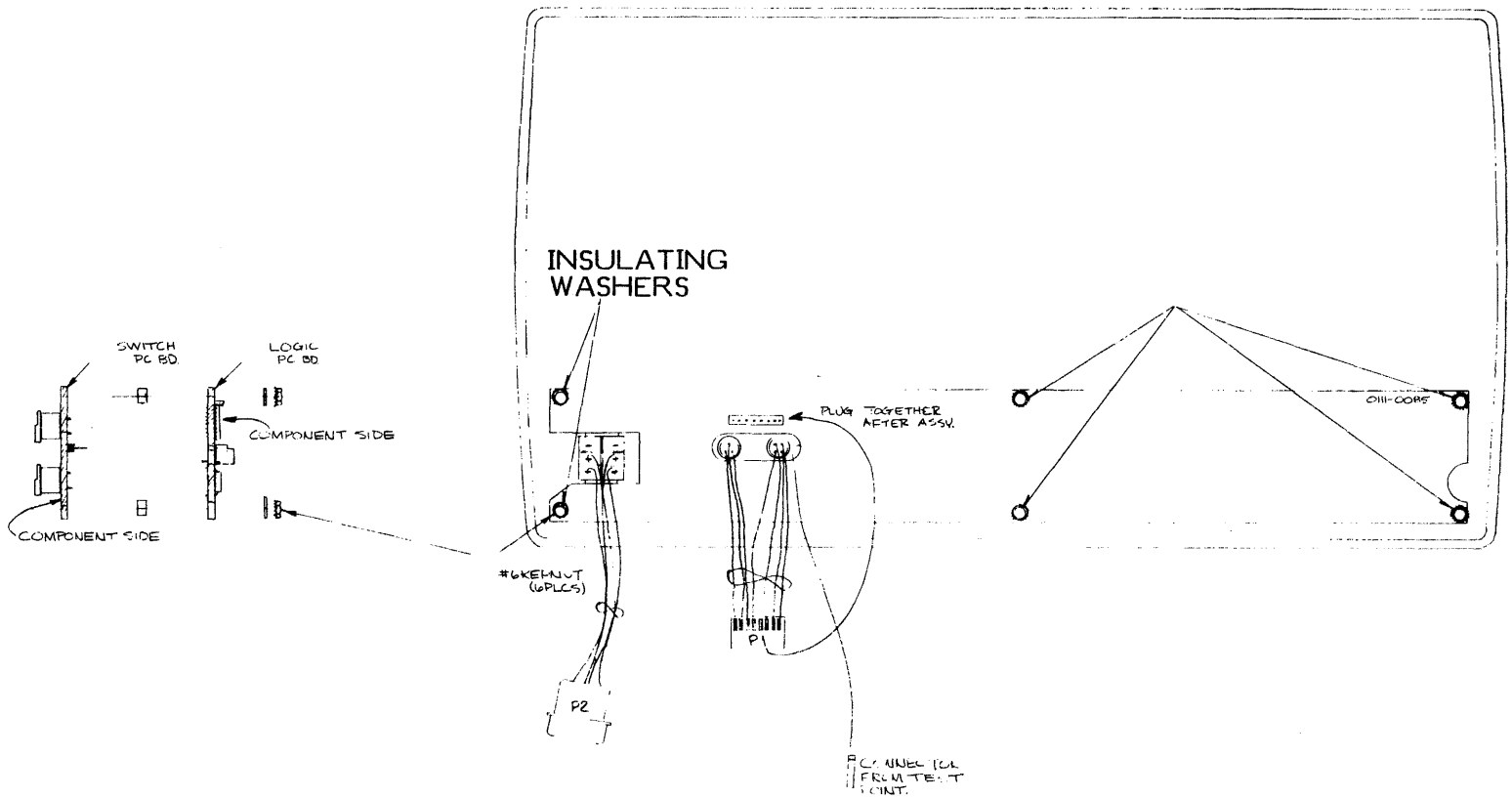
Figure 7.2   Front Panel Assembly

-60-

	ITEM		A2
P3-1	ITEM		#2
P2-5	S1	GRN/YEL	#22

LEMO	P1	COLOR	AWG
1	1	WHT	#16
2	2		
3	3		
4	NOT USED		
1	5		
2	6		
3	7		
4	8	WHT	#16

EXT. TRIGGER (rows 1–4)

DATA (rows 1–4)

S1	P2	COLOR	AWG
2	2	BLK/...	#22
4	4	GRN/...	22
1	3	B.../...	22
5	1	WHT/...	22

KEY PIN 4

8½"

7"

TWIST

SHRINK SLEEVING

P2

S1

1 2 3

DATA   EXT TRIGGER   AC POWER
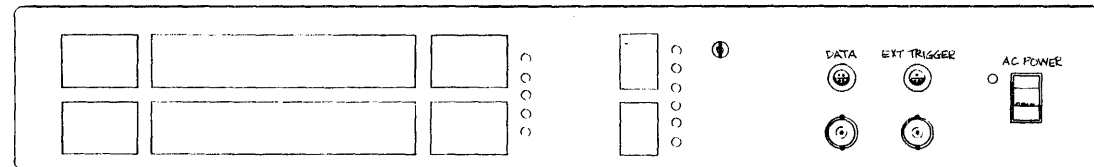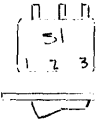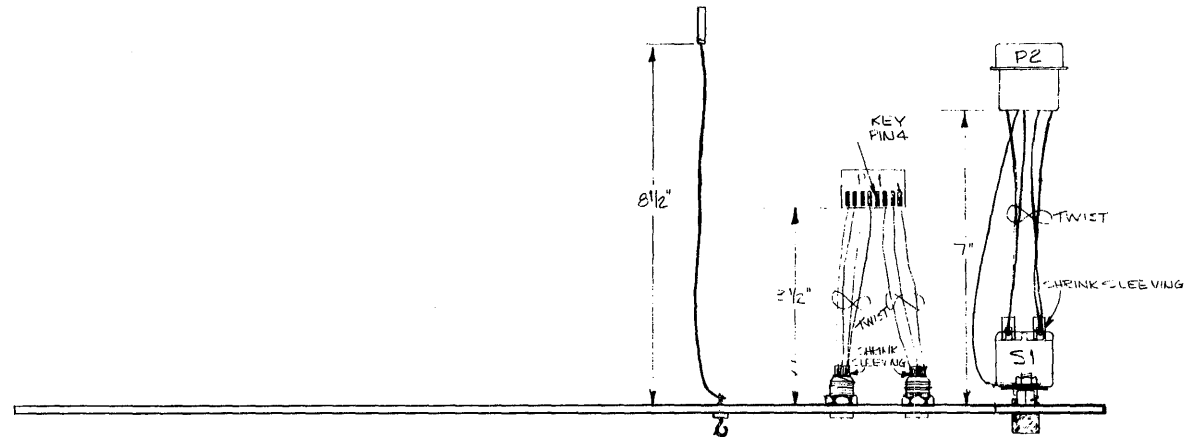
NOTES:

① SOLDER
   SHIELD OF COAX TO GND LUG.

② ALL WIRES ARE 26 GAUGE.

③ INSTALL ITEM 10 PER CABLEWEAVE
   SYSTEMS CAT # 201 PIGGI. USE TOOL
   N° T-15.

④ USE 2 DROPS (ITEM 46) EACH LOCATION
   ON THREADS AT BACK OF NUTS.

⑤ INSULATE BNC FROM PANEL
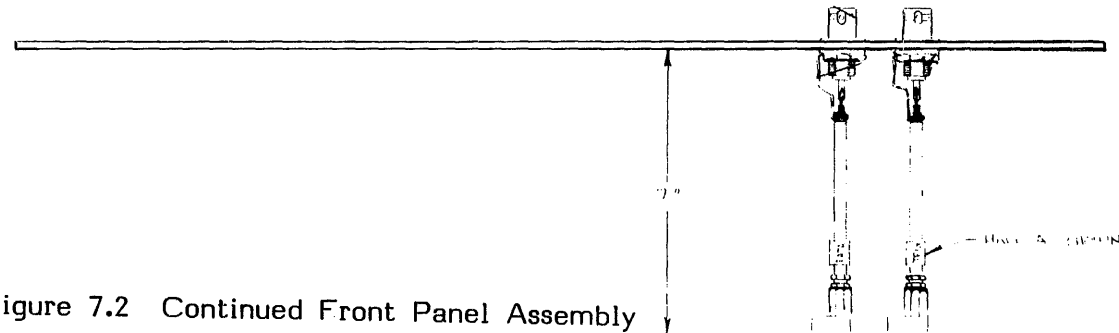
Figure 7.2 Continued Front Panel Assembly

-61-
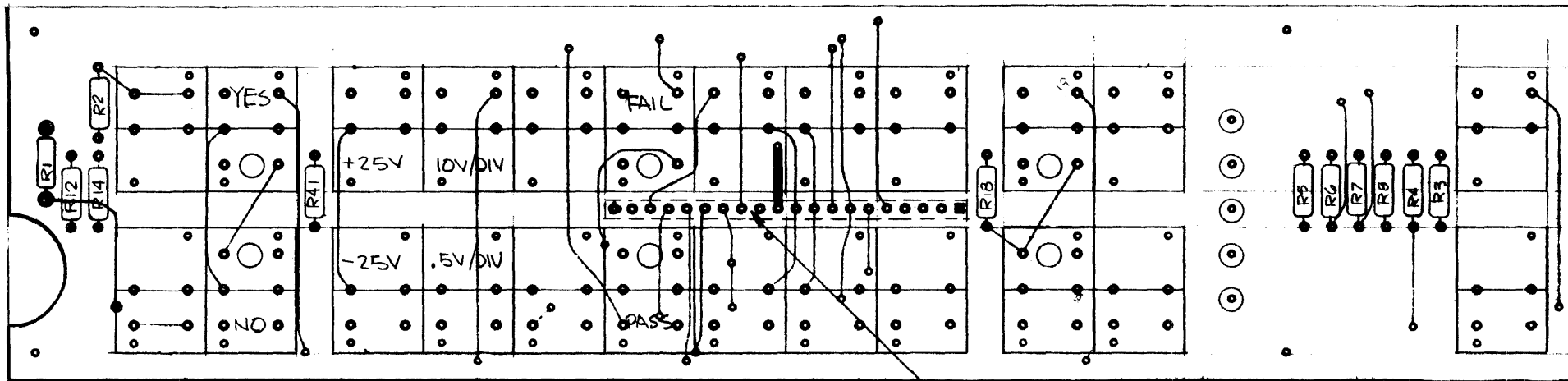
MOUNTED FROM
FAR SIDE. SHORT PINS
THRU BD.

Figure 7.3 Front Panel Switch Assembly
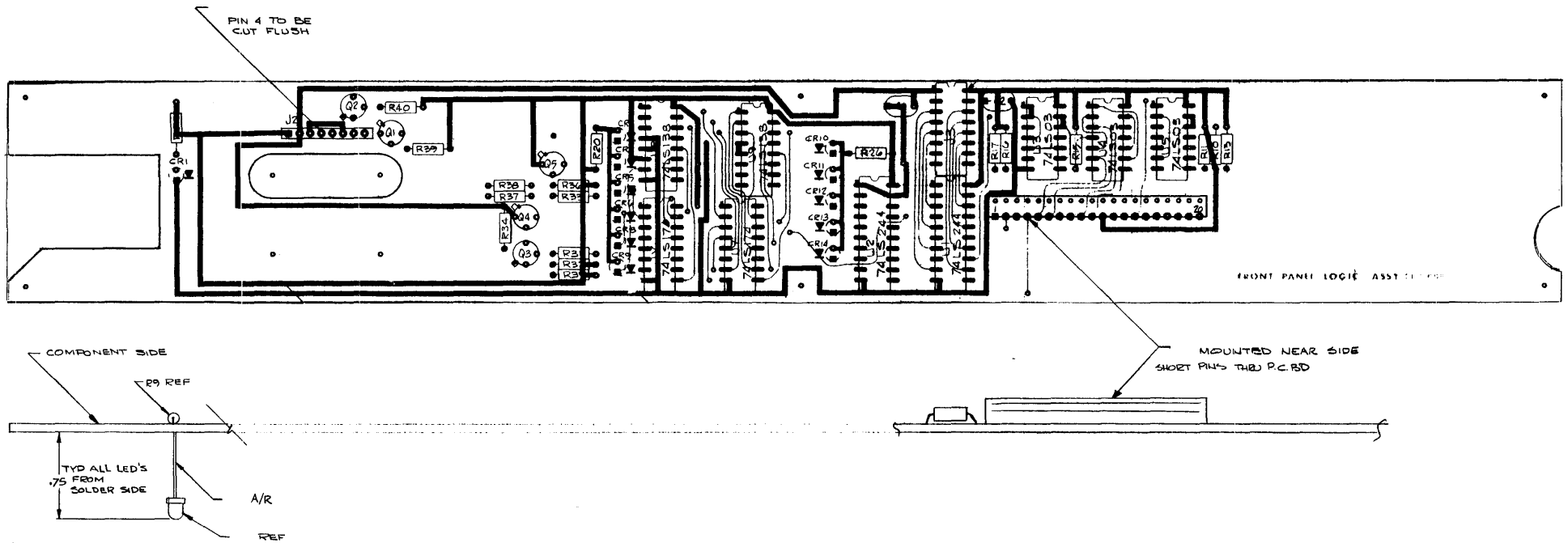
Figure 7.4 Front Panel Logic Assembly
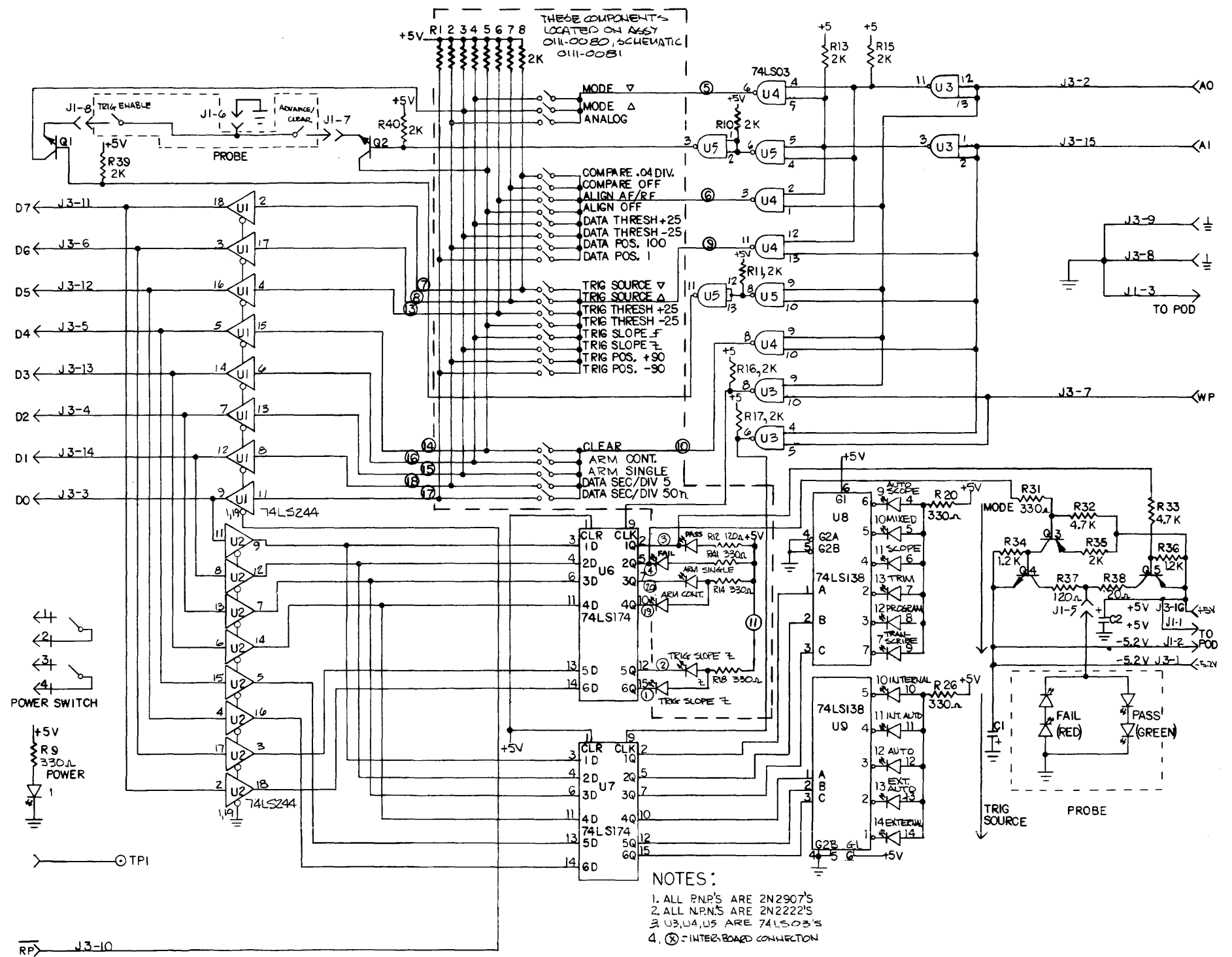
Figure 7.5 Front Panel Switch and Lamp Schematic
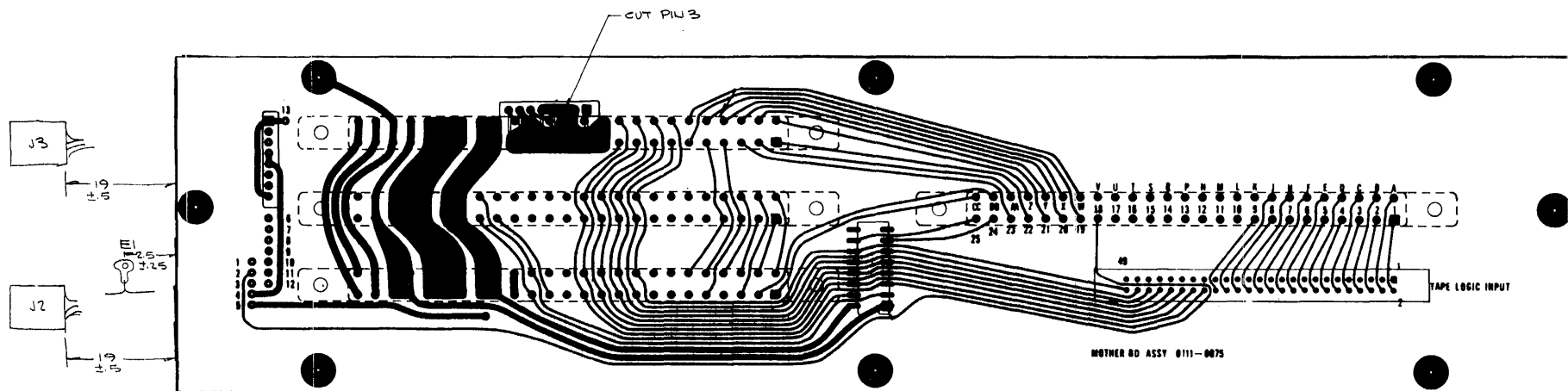
COMPONENT SIDE

WIRE LIST - 10

FROM	TO	COLOR AWG	
J2-1	6	YEL	18
J2-2	10	VIO	18
J2-3	11	BLK/WHT	18
J2-4	12	ORN	18
J2-5	E1	ORN	18
J3-1	1	BLK	18
2	2	WHT	18
3	3	RED	18
4	4	RED	18
5	5	GRY	18
6	7	BLU	18
7	8	BLK	18
J3-8	9	BLK	18
E1	13	ORN	18

WIRE LIST - 20

FROM	TO	COLOR AWG	
J2-15	6	YEL	18
J2-11	10	VIO	18
J2-6	11	BLK/WHT	18
J2-13	12	ORN	18
J2-4	E1	ORN	18
J2-3	1	BLK	18
J2-9	2	WHT	18
J2-12	3	RED	18
J2-10	4	RED	18
J2-5	5	GRY	18
J2-1	7	BLU	18
J2-16	8	BLK	18
J2-14	9	BLK	18
E1	13	ORN	18

Figure 7.6   Mother Board Assembly

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DISCREET WIRING

⏚	1		
RESET	2	11	⏚
+5	3	12	+15
+5	4		
-2	5		
+12	6		
-5.2	7		
⏚	8		
⏚	9		
-15	10		

TAPE DRIVE POWER

+15	1
⏚	2
+15	3
+5	4
+5	5
⏚	6
⏚	7
+15	8

13	+15

350 DISPLAY

X	8
◁	7
Y	6
◁	5
◁	4
◁	3
◁	2
Z	1

INPUT

Left	#	Ltr	Right
+15	25	CC	-15
◁	24	BB	◁
-5.2	23	AA	-5.2
-5.2	22	N	-5.2
⏚	21	Y	⏚
⏚	20	X	⏚
⏚	19	W	⏚
+5	18	V	+5
+5	17	U	+5
-2	16	T	-2
A_0	15	S	A_1
A_2	14	R	—
—	13	P	—
D_0	12	N	D_1
D_2	11	M	D_3
D_4	10	L	D_5
D_6	9	K	D_7
—	8	J	—
—	7	H	—
◁	6	F	CμP
+10	5	E	◁
—	4	D	◁
—	3	C	$\overline{WI}$
—	2	B	$\overline{RI}$
—	1	A	—

CONTROL

Left	#	Ltr	Right
+12	25	CC	+12
-5.2	24	BB	-5.2
⏚	23	AA	⏚
⏚	22	N	⏚
+5	20	X	+5
+5	19	W	+5
A_0	18	V	A_1
A_2	17	C	—
—	16	T	—
—	15	S	—
—	14	R	—
—	13	P	—
D_0	12	Z	D_1
D_2	11	M	D_3
D_4	10	L	D_5
D_6	9	K	D_7
—	8	J	R/W
—	7	H	—
—	6	F	$\overline{CDMA}$
—	5	E	—
CμP	4	D	◁
+10	3	C	◁
$\overline{WI}$	2	B	—
$\overline{RI}$	1	A	—

DISPLAY

Left	#	Ltr	Right
+15	25	CC	+15
-15	24	BB	-15
◁	23	AA	◁
-5.2	22	N	-5.2
⏚	21	Y	⏚
⏚	20	X	⏚
⏚	19	W	⏚
+5	18	V	+5
+5	17	C	+5
◁	16	T	X
◁	15	S	◁
◁	14	R	Y
◁	13	P	◁
◁	12	Z	Z
◁	11	M	◁
D_0	10	L	D_1
D_2	9	K	D_3
D_4	8	J	D_5
D_6	7	H	D_7
—	6	F	$\overline{ETAR2D}$
$\overline{CDMA}$	5	E	ET ARID
+10	4	D	EP AR2D
$\overline{EDMA}$	3	C	$\overline{LAR2AD}$
$\overline{LARID}$	2	B	LAR2BD
MD	1	A	POP

FRONT PNL

Left	#	#	Right
+5	9	8	⏚
$\overline{RP}$	10	7	WP
D_7	11	6	D_6
D_5	12	5	D_4
D_3	13	4	D_2
D_1	14	3	D_0
A_1	15	2	A_0
⏚	16	1	-5.2

TAPE LOGIC

Left	#	#
D_7	50	49
D_6	48	47
D_5	46	45
D_4	44	43
D_3	42	41
D_2	40	39
D_1	38	37
D_0	36	35
—	34	33
—	32	31
BOT	30	29
RD BUF FULL	28	27
INC CHAR	26	25
IRG	24	23
W BUF EMPTY	22	21
READY	20	19
READ BUS ENABLE T	18	17
STOP T	16	15
$\overline{RES\,T}$	14	13
FOR/REV T	12	11
R/W CONT	10	9
SEL1	8	7
—	6	5
LD W BUF	4	3
RUN	2	1

CONTROL

Left	#	Ltr	Right
$\overline{RP}$	25	CC	—
WP	24	BB	—
$\overline{EDMAD}$	23	AA	LARID
MD	22	N	POP
$\overline{LAR2BD}$	21	Y	LAR2AD
ED AR2D	20	X	ET ARID
—	19	W	ET AR2D
$\overline{RESET}$	18	V	—
—	17	C	—
—	16	T	—
—	15	S	—
—	14	R	—
—	13	P	—
—	12	Z	—
—	11	M	—
—	10	L	—
—	9	K	—
BOT	8	J	RD BUF FULL
INC CHAR	7	H	IRG
W BUF EMPTY	6	F	READY
READ BUS ENABLE	5	E	—
$\overline{RES\,T}$	4	D	STOP T
R/W T	3	C	FOR/REV T
—	2	B	SEL1
RUN	1	A	LD W BUF

Figure 7.7 Mother Board Schematic
-66-

Figure 7.8   Input Board Assembly

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Figure 7.9 Input Board Schematic   Sheet 1 of 2
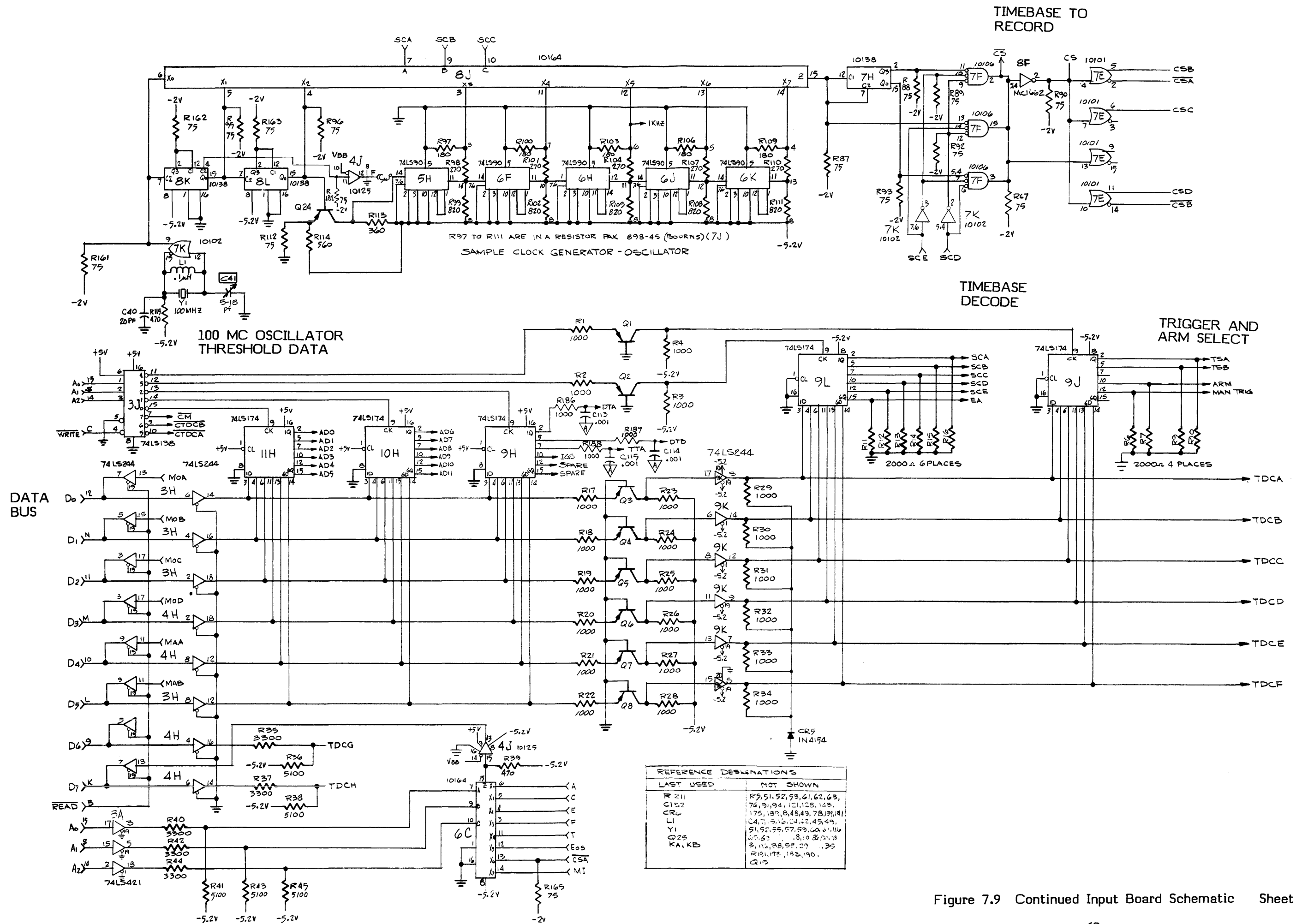
Figure 7.9 Continued Input Board Schematic   Sheet 2 of 2

Figure 7.10   Control Board Assembly
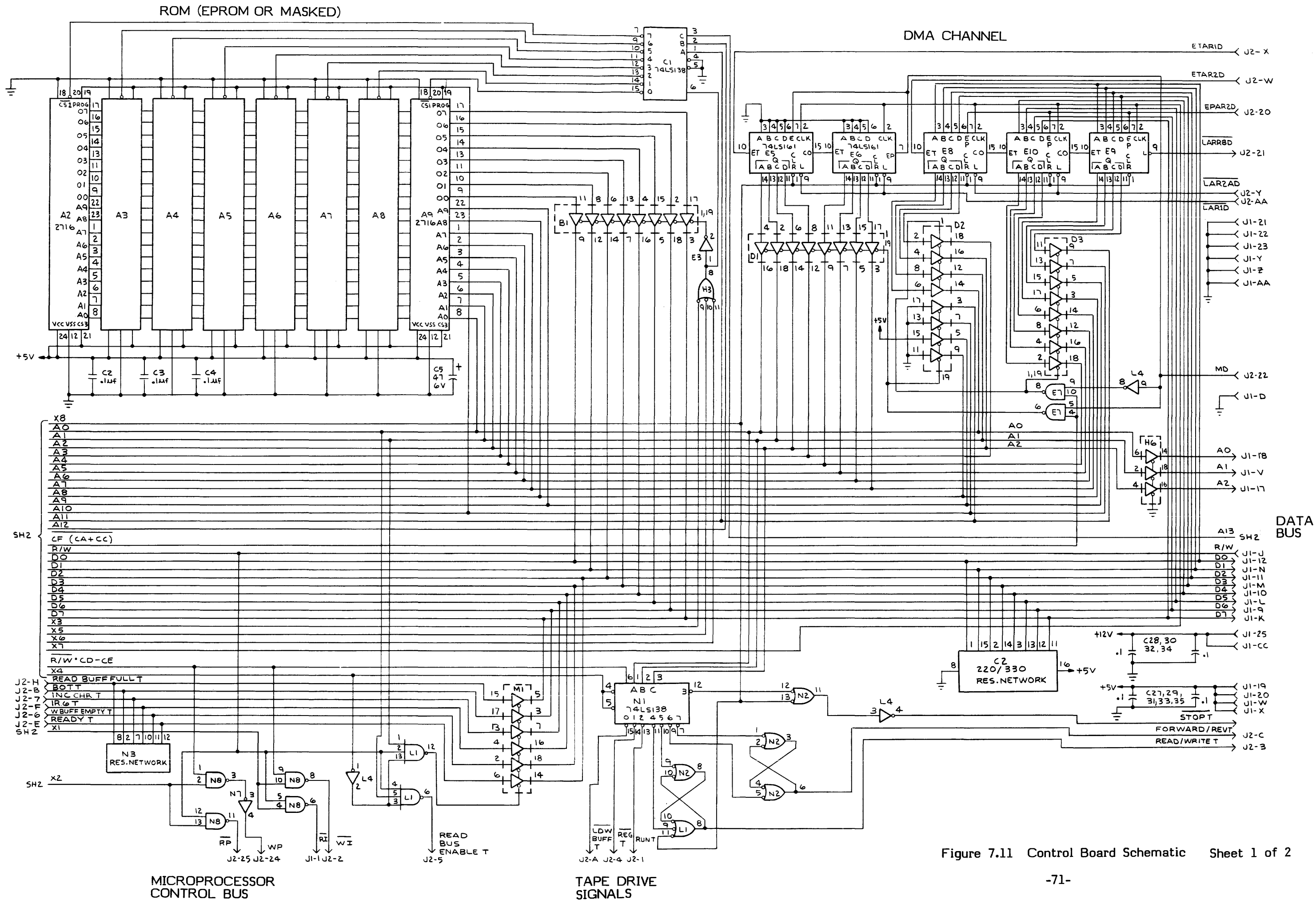
Figure 7.11 Control Board Schematic   Sheet 1 of 2
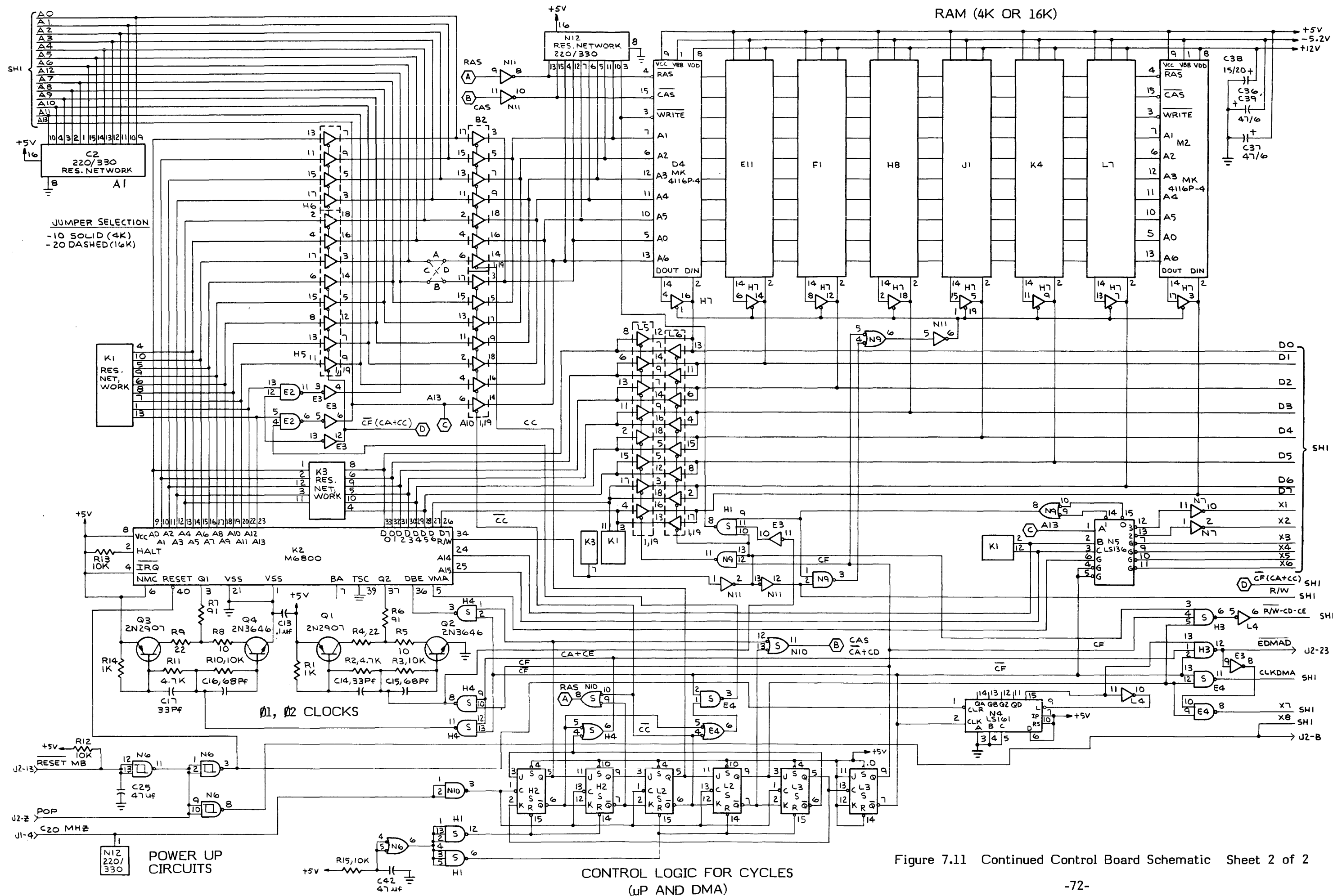
Figure 7.11   Continued Control Board Schematic   Sheet 2 of 2
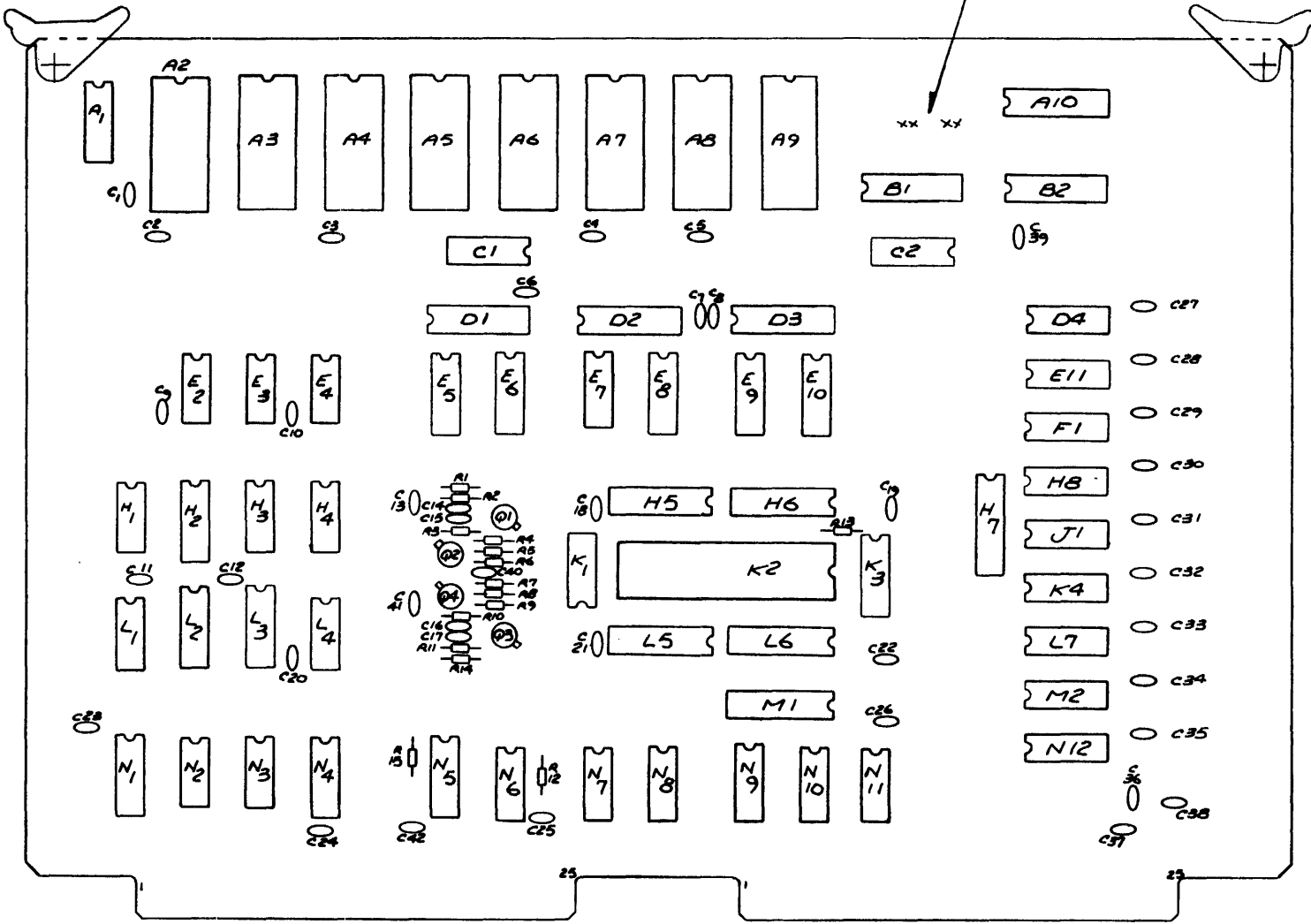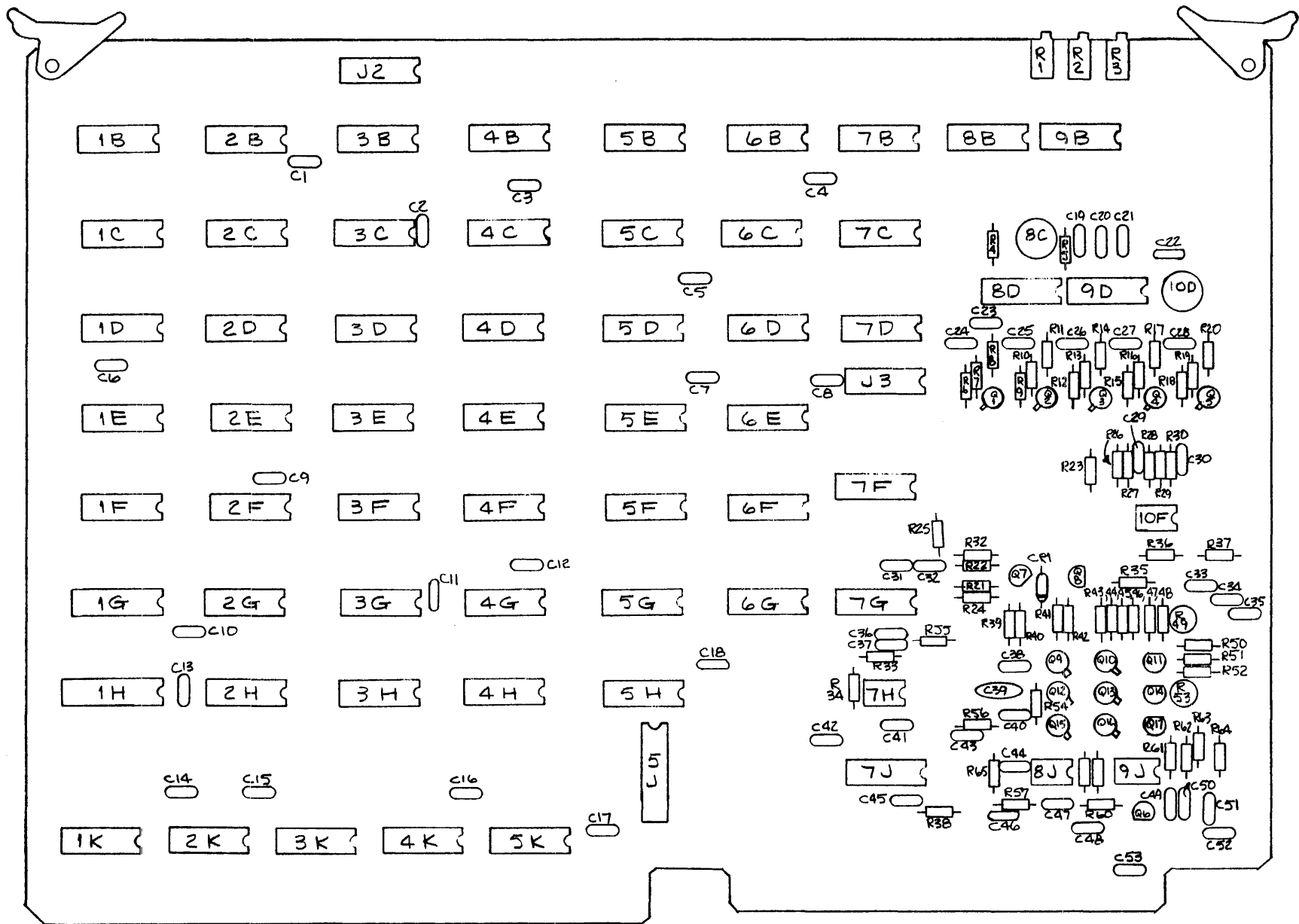
Figure 7.12 Display Board Assembly
-73-
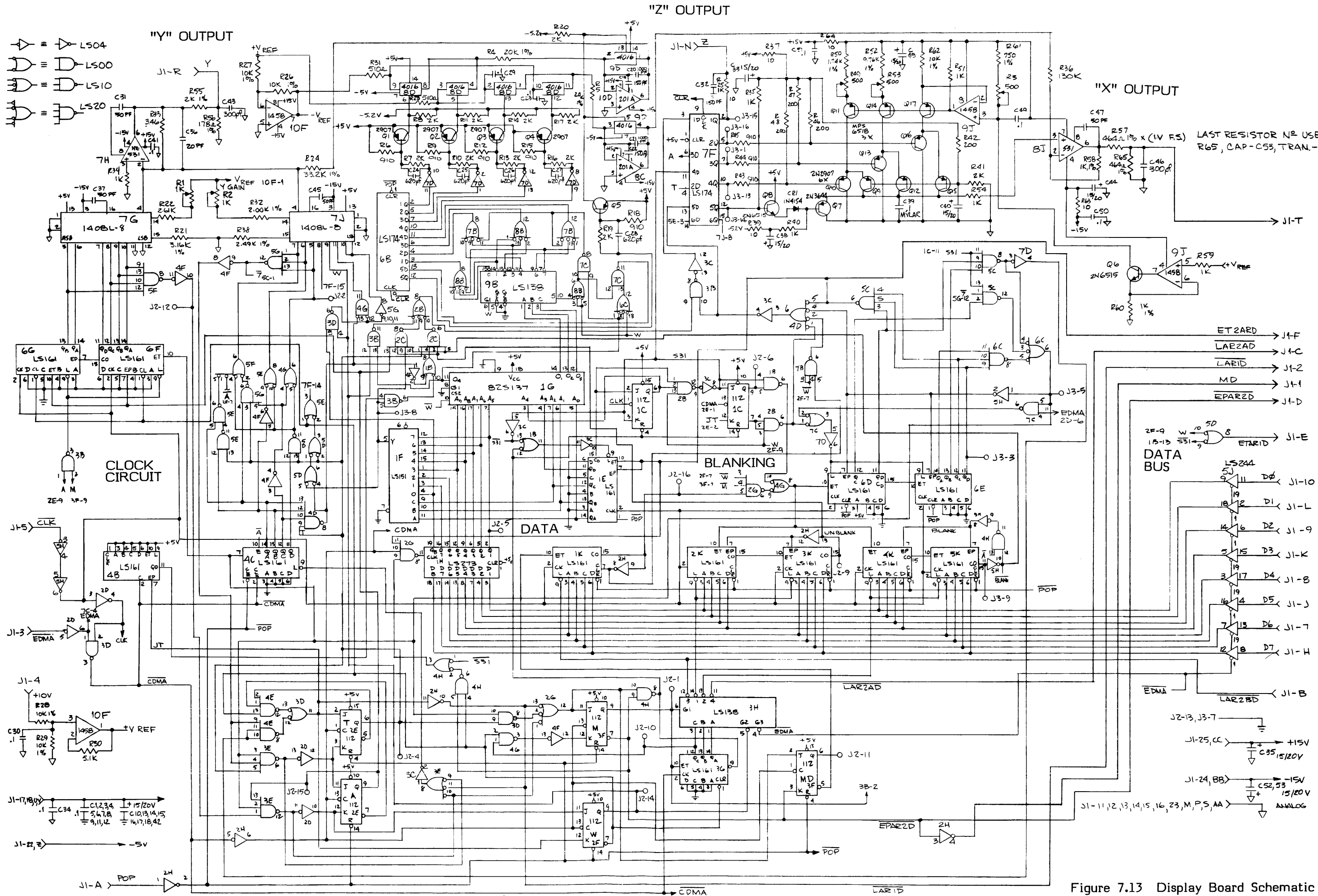
Figure 7.13 Display Board Schematic
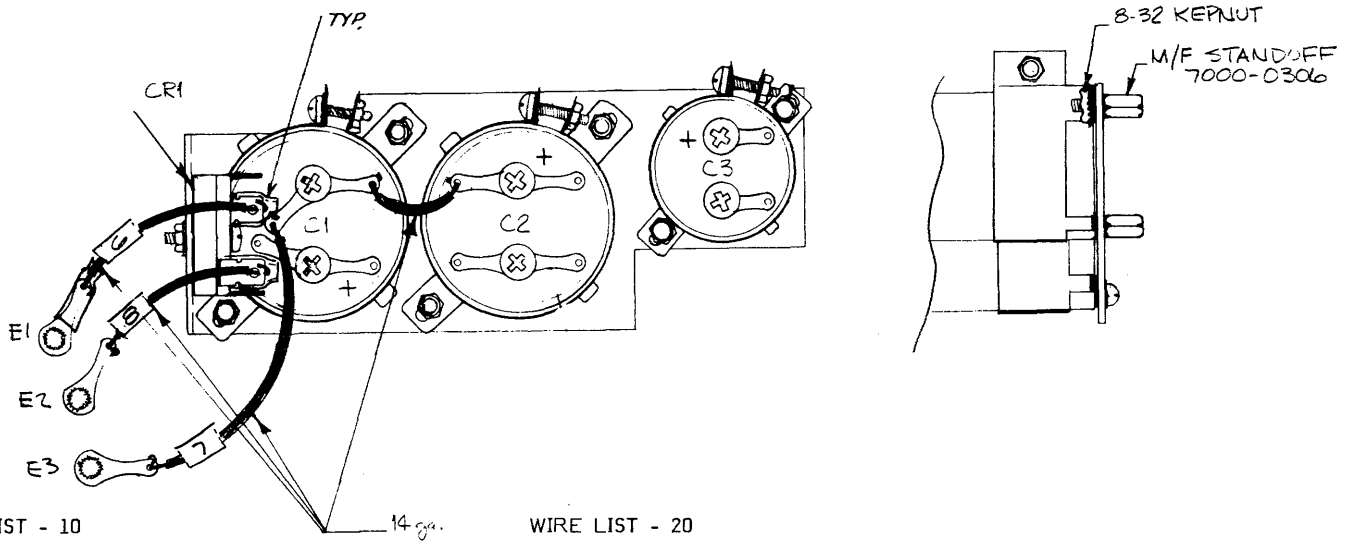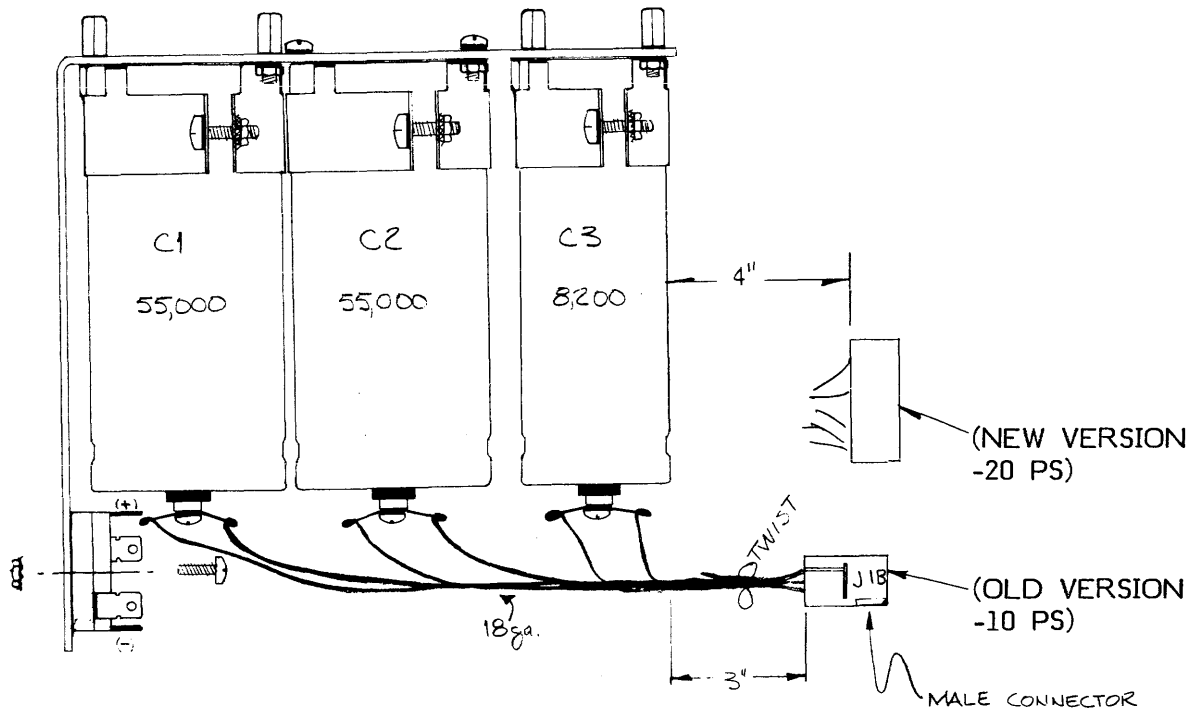
TIMING GENERATION CIRCUIT

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WIRE LIST - 10

FROM	TO	COLOR	AWG
E1	CR1∼	WHT/RED	14
E2	CR1∼	WHT/RED	14
E3	C1-(-)	BLK	14
C1-(-)	C2-(+)	BLK	14
CR1-(+)	C1-(+)	ORN	18
C1-(+)	J1-1	ORN	18
CR1-(-)	C2-(-)	ORN	18
C2-(-)	J1-2	ORN	18
C2-(+)	J1-3	RED/YEL	18
C3-(+)	J1-4	GRN	18
C3-(-)	J1-5	BLU	18

WIRE LIST - 20

FROM	TO	COLOR	AWG
E1	CR1∼	WHT/RED	14
E2	CR1∼	WHT/RED	14
E3	C1-(-)	BLK	14
C1-(-)	C2 -(+)	BLK	14
CR1-(+)	C1-(+)	ORN	18
C1-(+)	J1-3	ORN	18
CR1-(-)	C2-(-)	ORN	18
C2-(-)	J1-6	ORN	18
C2-(+)	J1-1	RED/YEL	18
C3-(+)	J1-4	GRN	18
C3-(-)	J1-5	BLU	18

NOTE:

[1] APPLY THERMAL COMPOUND BETWEEN DIODE BRIDGE & BRACKET.

[2] SOLDER (3) WIRES TO #8 GND LUGS, TO BE ATTACHED LATER TO XFMER,
LENGTH OF WIRES - 5'.

Figure 7.14   Capacitor Assembly
-75-

(4 PLCS)

-20
-10

(4 PLCS)

(2 PLCS)

CASTING
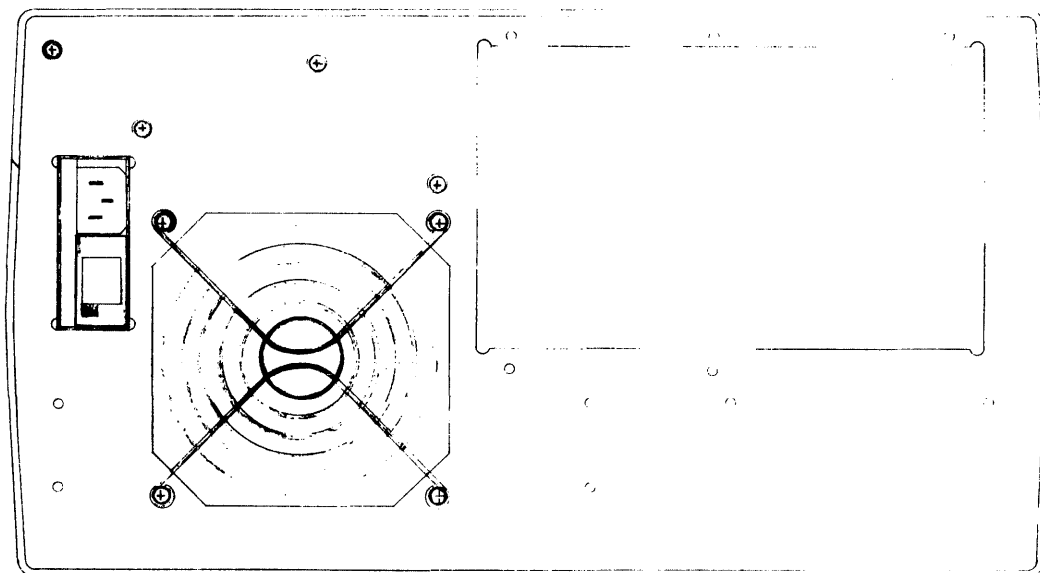
REAR PANEL ASSY

-10
-20

NOTE:

1. FAN WIRING

CORCOM	FAN	XFMER
C	2	1
E	1	3
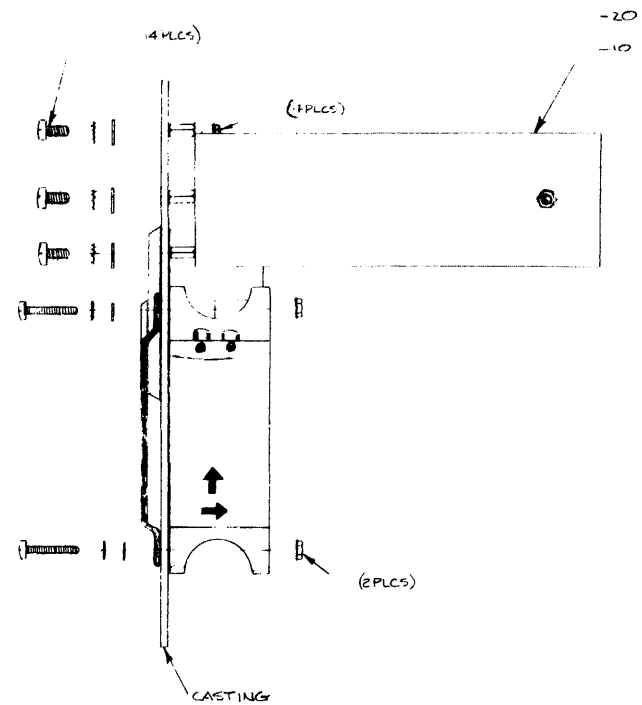
Figure 7.15 Rear Panel Assembly

WIRE LIST

FROM	TO	COLOR
A1-A	E 2	BLU/BLK
A1-B	P1-4	WHT/BRN
A1-C	E 1	BLK
A1-D	E 4	GRN/BLK
A1-E	E 3	YEL/BLK
A1-F	E 5	RED/BLK
A1-L	P1-1	WHT/BRN
A1-N	P1-2	BLK/BLU
A1-m	E6	GRN/YEL
A1-F	P1-3	BLK/BLU
A1-m	P1-5	GRN/YEL
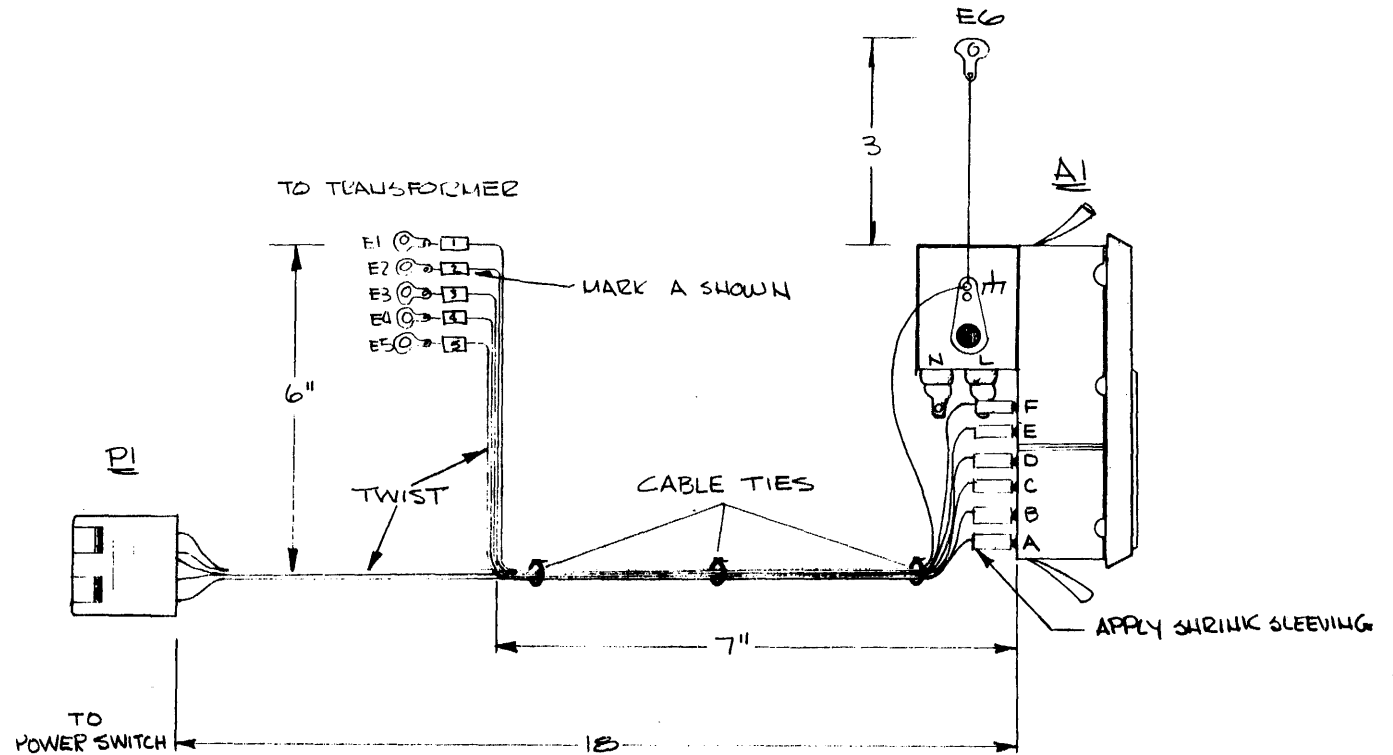
Figure 7.16   AC Wiring from Rear Panel (AC Corcom)

(T1-1) E1 ⊙☐—☐1

(T1-2) E3 ⊙☐—☐3
(T1-3) E4 ⊙☐—☐4
(T1-4) E5 ⊙☐—☐5

J1A

LENGTH TO REACH TO
POWER CONNECTOR FROM
350 ASSY (5.00±.5)
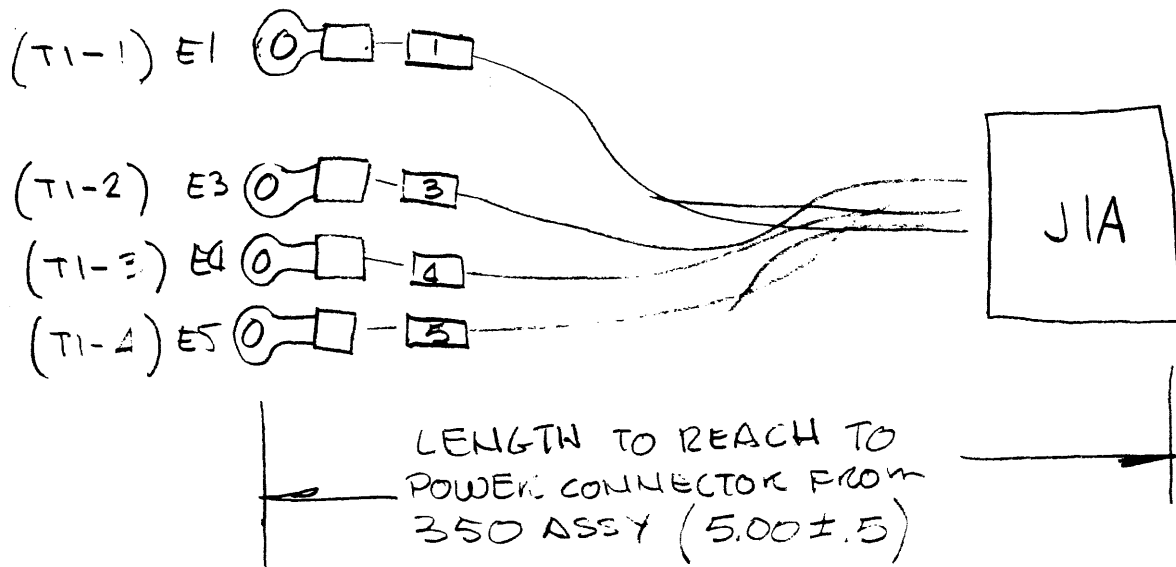
FROM   TO   COLOR/AWG

J1-1   E1   RED/WHT   20 AWG

   2   E2   WHT

   3   E3   RED/BLK

J1-4   E4   BLK   20 AWG

Figure 7.17   Cable Assembly 350 Power

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16.00 ± .50

KEY PIN 1

J1

USE MOLEX CONNECTOR # 22-01-2051
AND PIN 08-50-0114 AS SUPPLIED
WITH 3M TAPE DRIVE, BIOMATION P/N 9000-0014

J2

J6

SPOT TIE
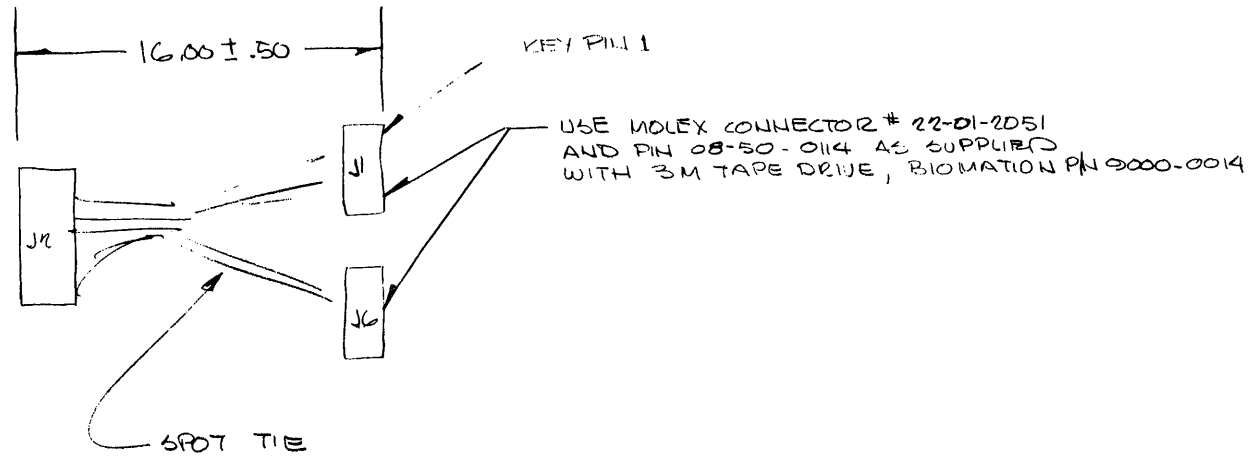
FROM	TO	COLOR/AWG
J2-1	J6-1	WHT/22AWG
2	J1-2	
3	J1-4	
4	J1-3	
5	J6-3	
6	J6-2	
7	J6-4	
J2-8	J6-5	WHT/22AWG

Figure 7.18 Cable Assembly Tape Power

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Figure 7.19   Power Supply Assembly
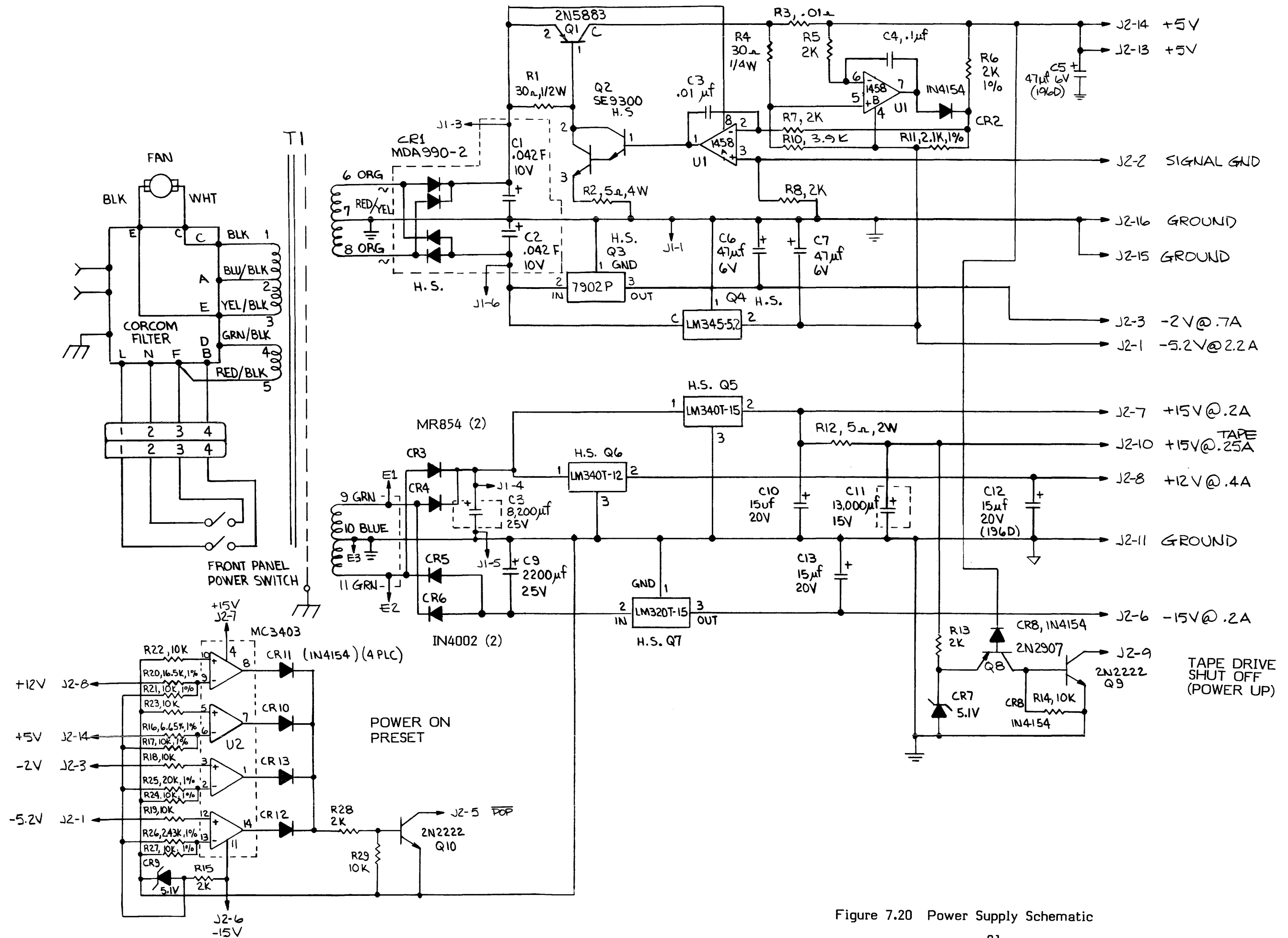
Figure 7.20 Power Supply Schematic

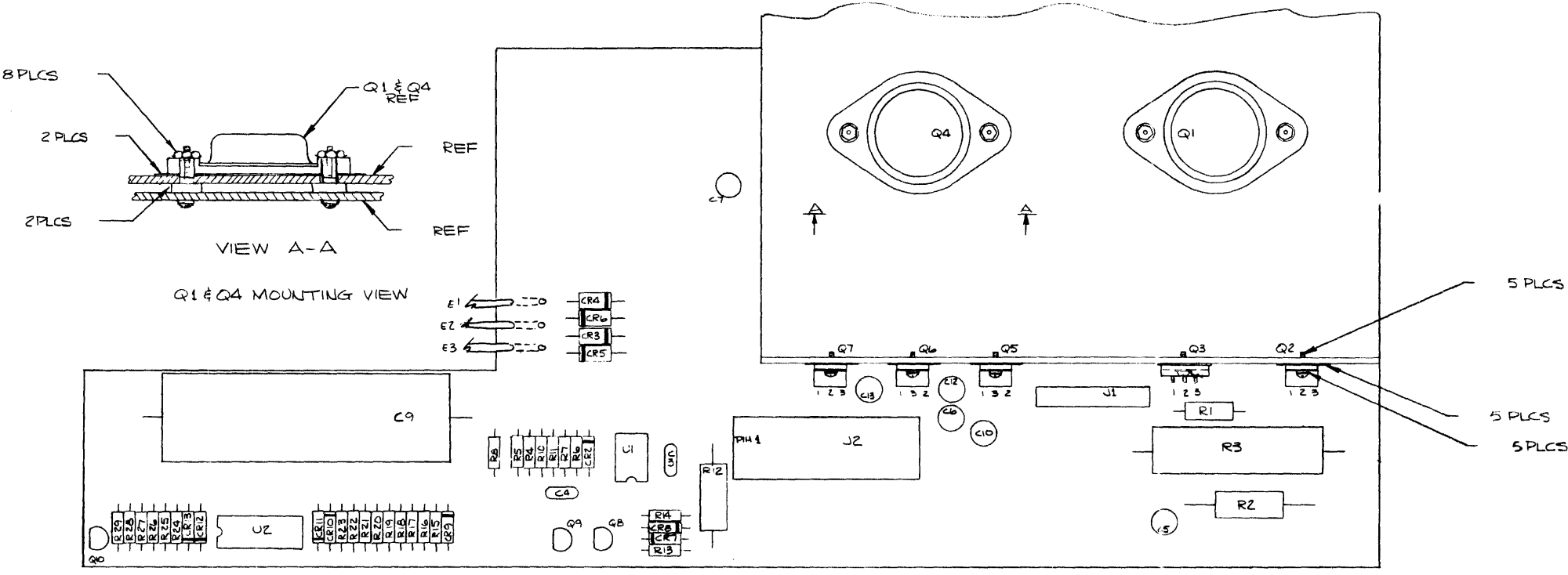| ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
1					1	1	0350-0001-20	CRT				L/M
2												
3					1	1	0111-0647	CRT BKT-BOT				
4					6	6	7000-0326-05	SCREW-TAPTITE	THRU REAR CASTING		#6 X 5/16 PH	
5					4	4	———	SCREW	THRU FRONT CASTING		#6 X 5/16 FH	
6					1	1	7200-0019	ADHESIVE CLAMP				
7					1	1	9000-0014	TAPE DRIVE				
8					1	1	9000-0015	TAPE CARTRIDGE				
9					1	1	0111-0006-10	REAR PNL ASSY				L/M
10					4	4	———	SCREW	THRU FRONT CASTING TO TAPE DRIVE BKT.		6-32X3/8 PH	
11					7	7	—	SCREW			6-32X5/16 PH	
12					1	1	0111-0005	FRONT PNL ASSY				LM
13					4	4	———	SCREW			6-32X1/2 PH	
14					10"	10"	7200-0024	GROMMET			RICHCO SPGS-1	
15					1	1	0111-0054-02	FRONT BEZEL				
16					1	1	0111-0053-01	BRACKET,TAPE				
17					1	1	0111-0053-02	BRACKET,TAPE				
18												
19					—	1	0111-0036	CARD CAGE				
20					—	1	0111-0075-10	MOTHER BD ASSY				L/M
21					8	8	———	SCREW	THRU MOTHER BD		#6 X1/4 PH	
22					1	1	0111-0042	CARD RETAINER				
23					1	1	0111-0026	TRANSFORMER				
24					4	4	———	SCREW	THRU XFMR		#8 X 1/4 PH	
25					—	1	0111-0065	POWER SPLY ASSY				L/M
26					5	4	———	SCREW	THRU SUPPLY ASSY		#6 X 1/4 PH	
27					9	9	———	SCREW	(CARD CAGE & SUPPORT TRAY) THRU FRONT CASTING		#6 X 1/4 FH	
28					6	6	———	SCREW	THRU REAR CASTING & CARD CAGE		#6 X 5/16 PH	
29					3	3	7000-0268	CABLE CLAMP	MOTHER BD.			
30					1	1	0111-0035	SUPPORT TRAY-TAPE LOGIC				
31					4	4	7000-0129	SPACER			#4 X 5/8 PH	
32					4	4	———	SCREW	THRU SPACERS		#4 X 1 PH	
33												
34					1	1	———	SCREW	THRU CARD RETAINER		6-32X1/4 PH	
35					24	24	———	LOCK WASHER			#6	
36					20	20	———	FLAT WASHER			#6	

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
37					2	2	0111-0044	SIDE RAILS				
38					8	8	7000-0328-10	SCREW-TAPTITE	THRU CASTING INTO RAILS		#8 X 5/8 PH	
39					2	2	————	SCREW	INTO HANDLE		1/4-20 X 5/8 PH	
40					4	4	7000-0331	SCREW SOCKET HD CAP SCREW	AS STOPS FOR HANDLE		#10-32 X 5/16	
41					1	1	0111-0100	CABLE MOD			26 COND	
42					1	1	0111-0101	CABLE MOD			50 COND	
43					1	1	0111-0102	CABLE ASSY				
44					1	1	0111-0009	BAIL ASSY				L/M
45					1	1	————	TAPE LOGIC B.D.		833640-2536 C1	COMES WITH TAPE DRIVE	
46					1	1	————	TAPE LOGIC BD.		833640-253AC1	COMES WITH TAPE DRIVE	
47					4	4	————	LOCK WASHER	GOES ON SUPPORT TRAY SPACERS		#4	
48					4	4	————	FLAT WASHER	"		#4	
49					1	1	0111-0103	CABLE ASSY			350 PWR	
50					1	1	0111-0070	CONTROL P.C.BD ASSY				L/M
51					1	1	0111-0060	FRONT END PCBD ASSY				L/M
52					1	1	0111-0090	DISPLAY P.C.BD ASSY				L/M
53					A/R	A/R	0111-0095	EXTENDER SINGLE COLN				L/M
54					A/R	A/R	0111-0100	EXTENDER DUAL COLN				L/M
55					—	1	0111-0040-10	COVER				
56					—	1	0111-0040-20	COVER				
57					8	8	—	SCREW	ON COVERS		#8-32 X 5/8 100° FH	
58												
59					8	8	7000-0334	CLIP ON RECEPTACLE	ON CASTING			
60					—	4	7000-0233	FEET	ON BOT COVER			
61					—	4		SCREW	@ FEET		#6 X 5/8 PH	
62					—	4		NUT	@ FEET		#6	
63												
64					2	2		CABLE STRAIN				
65					1		4400-002	CAPACITOR	C3		300µf 1V ALUM	
66												
67												
68												
69					1	1	7100-0054	POWER CORD			BELDEN KH8574	
70					1	1		SOLDER			#3	
71					1	1	0111-0021					
72					1	1	0111-0075					
73					1	—	0111-0112	CARD CAGE				
74					1	—	0111-0075-20	MOTHER BD ASSY				
75					1	—	0111-0105	PWR SPLY ASSY				
76					1	—	0111-0111-10	COVER-TOP				
77					1	—	0111-0111-20	COVER-BOT.				
78					1	—	0111-0006-20	REAR PNL ASSY				
79												
80												

Front Panel Assembly

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
1						1	0111-0034	BEZEL				
2						1	0111-0004	FRONT PNL SUB ASSY				L/M
3						1	0111-0051	FRONT PNL-UPPER				
4						1	0111-0080	SWITCH P.C.BD				L/M
5						1	0111-0085	LOGIC P.C.BD				L/M
6												
7						10	————	KEPNUT			#6	
8												
9												
10												
11						2	7000-0253	SPACER			6-32 X 3/16	
12						4	7000-0341	SPACER			6-32 X 1/8	
13						4	7000-0073	WASHER - INSULATIN			#6	

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
1						1	0111-0062	P.C. Board				
2						6	3000-5106	RESISTOR	R55-59, 69		51Ω ¼W 5%	
3						67	3000-7506	↑	R65-67,71,87-90,92 93,95,96,112,116-120		75Ω ↑ ↑	
4									122-127,129-142,146-150 152-166,176-180,182,184,185,192			
5						1	3000-2000		R73		200Ω	
6						1	3000-3600		R113,		360Ω	
7						2	3000-4700		R39,115		470Ω	
8						9	3000-1006		R68,144,151,174, 181,210,211,197,198		10Ω	
9						1	3000-6200		R75		620Ω	
10						25	3000-1001		R1-4, R17-34 186,187,188		1000Ω	
11						17	3000-2001		R6,7,9-16,167-170 199,202,205		2000Ω	
12						4	3000-2401		R84,85,193,194		2400Ω	
13						5	3000-3301		R35,37,40,42,44		3300Ω	
14						3	3000-5100		R60 145,173		510Ω	
15						5	3000-5101		R36,38,41,43,45		5100 Ω	
16						1	3000-5601	↓	R81		5600Ω ↓ ↓	
17						1	3000-6201	RESISTOR	R72		6200Ω ¼W, 5%	
18												
19						1	3000-5600	RESISTOR	R114		560Ω, ¼W, 5%	
20						6	3100-1000	↑	R47,54,83,86 195,196		100Ω, ⅛W, 1%	RN55
21						1	3100-4640		R74		464, ⅛W, 1%	RN55
22						2	3100-1002	↓	R46,80		10K, ⅛W, 1%	RN55
23						2	3100-1004	RESISTOR	R50,82		1 Meg, ⅛W, 1%	RN55
24						5	3000-2402	RESISTOR	R200,203,206,171,172		24K, ¼W., 5%	
25						1	3700-0028	RESISTOR PAK TTL-ECL	R97-R111(7J.)	BOURNS 898-45	180,270,820Ω ±2%, TRANSLATOR	
26						1	3000-6206	RESISTOR	R212		62Ω 5% ¼W	
27						61	4000-0025	CAPACITOR	C2,5,6,7,11,12,17,18 21-23,27,28,31-33,36		.1µF, 50V	
28									37,39,43,44,46-48,50,53,54,56,62, 66-74,79,85,87,117,123	63,64,109-112, 124,125,130,131,138		
29						3	4100-0005		C9,121,122		10PF, 5%, 500V	
30						1	4100-0006		C40,		20PF, 5%, 500V	
31						3	4000-0030		C1,34,118		.002UF/1KV	
32												
33						3	4200-0006		C13,19,25		.01µF, 10%, 250V	
34						4	4000-0005	↓	C14,20,26,30		.01UF, 100V	
35						17	4300-0025	CAPACITOR	C91-97,99-101 104-108,126,128		47µF, 10%, 6V	
36						1	4600-0001	CAP. VARIABLE	C41		5-18 PF	

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
37						1	2100-0014	INDUCTOR	L1		.1µH	
38						4	1000-0017	DIODE	CR1,2,3,4		1N458A	
39						1	5100-0004	CRYSTAL	Y1		100 MHz	
40						1	6000-0195	CONNECTOR		MOLEX 22-05-2051	WAFER, 5 PIN	
41												
42												
43						15	1400-0001	TRANSISTOR	Q1-8,16,17,18,19, 20,21,24		2N2907	
44						3	1500-0006	TRANSISTOR	Q9,14,10		2N5912	
45						2	6000-0134	JACK, ST COAX		700209	50Ω	
46												
47					-	2	2600-0001	RELAY	KA, KB	ELECTROL RA 3038-1051		
48												
49						1	1800-0193	INTEGRATED CIRCUIT	3J		74LS138	
50						5	1800-0190		9H,9L,9J,10H,11H		74LS174	
51						5	1800-0118		6F,5H,6H,6J,6K		74LS90	
52						2	1800-0039		3B, 3C		74S112	
53						8	1800-0102	INTEGRATED CIRCUIT	1A,2A,1C,2C, 1E,2E,1H,2H		93S16	
54						2	1000-0002	DIODE	CR6, 5		1N4152	
55						4	1800-0240	INTEGRATED CIRCUIT	3A,3H,4H,9K	SIGNETICS	74LS244	
56						3	1850-0009		5A,8E,8F	MOTOROLA	MC1662L	
57						1	1850-0037		7E		10101	
58						3	1850-0002		6E,7K,5E		10102	
59						3	1850-0025		5B,5C,7F		10106	
60						1	1850-0003		4D		10105	
61						1	1850-0021		5F		10124	
62						3	1850-0014		1D,4C,4J		10125	
63						1	1850-0006		2D		10131	
64						3	1850-0041		7H,8L,8K		10138	
65						3	1850-0042		6C,7D,8J		10164	
66						1	1820-0022		10D		4016	
67						4	1850-0055		3E,4C,3F,4F		10016	
68						1	1900-0008		11F	ANALOG DEVICE	AD562KD	
69						4	1850-0001		8A,B,C,D		AM685	
70						4	1700-0071		10A,B,C,11E	NATIONAL SEMI	LF356	
71						4	1800-0127		1B,1F,2B,2F		27LS01F	
72						1	1700-0063	INTEGRATED CIRCUIT	10E	PRECISION MONOLITHICS	REF 01	

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
73						3	4000-0013	CAPACITOR	C113,114,115		.001 UF, 500V	
74						2	4100-0003	CAPACITOR	C119,120		1 PF	
75						4	4300-0026	CAPACITOR	C102,103,127,129		15 UF, 20V	
76						3	1850-0019	I C.	5D,6B,6D		10231	
77						3	3000-4702	RESISTOR	R201,204,207		47K, 1/4W, 5%	
78						2	3000-9102	RESISTOR	R208,209		31K, 1/4W, 5%	
79						1	3100-1001	RESISTOR	R70		1000, 1/8W, 1%	
80						2	1850-0008	I C.	3D,6A		1660	
81						1	1700-0051	VOLTAGE REG.	Q22		7805	
82						1	1700-0052	VOLTAGE REG.	Q23		7905	
83												
84						2	7000-0164	CARD EJECTOR				
85												

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
1					1	1	0111-0072	P.W. BOARD				
2					8	—	1800-0229	I.C.	E11,D4,F1,H8,J1,K4,L7 M2	HK4116P-4		
3					2	2	1400-0001	TRANSISTOR	Q1,Q3	2N2907		
4					2	2	1300-0003	TRANSISTOR	Q2,Q4	2N3646		
5					3	3	1800-0107	INTEGRATED CIRCUIT	E3,N7,L4	74LS04		
6					4	4	1800-0105	↑	N8,N9, E2,E7	74LS00		
7												
8					—	8	1800-0230		E11,D4,F1,H8,J1, K4,L7,M2	MK4027P4		
9					3	3	1800-0039		H2,L2,L3	74S112		
10												
11					3	3	1800-0193		C1,N1,N5	74LS138		
12					6	6	1800-0125		E5,E6,E8,E9, E10,N4	74LS161		
13					1	1	1800-0199		N6	74LS132		
14					12	12	1800-0240		A10,B1,B2,D1,D2,D3 H5,H6,H7,L5,L6,M1	74LS244		
15					4	4	1800-0031		N2,E4,H4,N10	74S00		
16					3	3	1800-0060		H1,3,L1	74S10		
17					1	1	1800-0201	INTEGRATED CIRCUIT	K2	M6800		
18												
19					3	3	3700-0005	RESISTOR NETWORK	K1,K3,N3		2K	
20					3	3	3700-0029	RESISTOR NETWORK	A1,C2,N12		220/330Ω	
21					31	31	4000-0016	CAPACITOR	C2-C13 C26-35 C18-C24 C40,41		.1μf	.2
22					2	2	4100-0013	↑	C14,17		33pf	.25
23					2	2	4100-0024	↓	C15,16		68pf	.25
24					6	6	4300-0025	CAPACITOR	C1,C25,36,37 39,42		47μf,6V	.1
25					1	1	4300-0026	CAPACITOR	C38		15Uf,20V	
26					1	1	1800-0092	I.C.	N11		74S04	
27												
28					1	1	6100-0072	SOCKET	K2		40PIN	
29					8	8	6100-0046	SOCKET	E11,D4,F1,H8,J1 K4,L7,M2			
30					5	5	3000-1002	RESISTOR	R3,10,12,13,15		10K,1/4w,5%	
31					2	2	3000-4701	↑	R2,11		4.7K,1/4w,5%	
32					2	2	3000-2206		R4, 9		22Ω,1/4w,5%	
33					2	2	3000-1001	↓	R1,14		1K,1/4w,5%	
34					2	2	3000-1006	RESISTOR	R5,8		10Ω,1/4w,5%	
35					2	2	3000-9106	RESISTOR	R6,7		91Ω5% 1/4w	
36					2	2	7000-0164	EJECTOR		S-200	SCANBE	

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
37					1	1	0111-0025-10	MASKED ROM	A9			
38					1	1	-11		A8			
39					1	1	-12		A7			
40					1	1	-13		A6			
41					1	1	-14		A5			
42					1	1	-15		A4			
43					1	1	-16		A3			
44					1	1	0111-0025-17	MASKED ROM	A2			
45												

Display Board Assembly

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1						1	0111-0092	PWB				
2						8	1800-0105	IC	1E,3B,7C,3D,5D, 5E,4G,4H	74LS00		
3						6	-0107	↑	7D,2D,2H,3C, 4F,5H	74LS04		
4						9	-0110		6C,8B,2B,2G, 3E,4E,5C,5G,7B	74LS10		
5						3	-0111		2C,4D,5F	74LS20		
6						1	-0240		5J	74LS244		
7						4	1800-0068		1C,2E,2F,3F	74LS112		
8						1	0111-0024		1G	82S137		
9						2	1800-0193		3H,9B	74LS138		
10						1	-0181		1F	74LS151		
11						1	-0231		1H	74LS273		
12						13	-0125		1E,1K,2K,3G,3K,4C,4K, 5K,6D,6E,6F,6G,4B	74LS161		
13						2	1800-0190		6B,7F	74LS174		
14						2	1820-0022		8D,9D	4016		
15						2	1900-0006		7J,7G	1408L-8		
16						2	1700-0036		8C,10D	LM201A		
17						2	1700-0019	↓	7H,8J	NE531		
18						2	1700-0018	IC	10F,9J	1458		
19						1	1000-0008	DIODE	CR1	1N4154		
20												
21												
22						2	1300-0005	"	Q6,8	2N6515		
23						11	1400-0001	"	Q1-5,9,10,12, 13,15,16	2N2907		
24						1	1400-0015	"	Q7	2N3644		
25						3	1400-0024	"	Q11,14,17	MPS6518		
26												
27						4	3000-1006	RESISTOR	R37,39,63,64		10Ω ¼w 5%	
28												
29						4	3000-2000	"	R42,46,47,48		200 Ω	
30						8	3000-9100	"	R6,9,12,15,18, 43-45		910 Ω	
31						7	3000-1001	"	R25,34,35,40,51, 54,55		1K	
32						11	3000-2001	"	R7,8,10,11,13,14, 16,17,19,20,41		2K	
33						1	3000-5101	"	R30		5.1K	
34						2	3000-5100	"	R31,R23		510Ω	
35												
36												

Continued Display Board Assembly

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
37												
38						1	3100-3322	RESISTOR	R24		33.2K 1% 1/8W	
39						1	-1303	"	R36		130K 1% 1/8W	
40						1	-1780	"	R56		178 Ω 1% 1/8W	
41						2	-1001	"	R58,60		1.0K 1/8W 1%	
42						2	-2001	"	R32,55		2.0K	
43						1	-2491	"	R38		2.49K	
44						1	-1741	"	R50		1.74K	
45						1	-3831	"	R21		3.83K	
46						1	-3161	"	R33		3.16K	
47						1	-9761	"	R52		9.76K	
48						5	-1002	"	R26-29,62		10.0K	
49						2	-2002		R4,5		20.0K	
50						1	-7500	"	R61		750Ω	
51						1	-2611	"	R22		2.61K 1/8W 1%	
52						2	3100-4640	"	R57,R65		464Ω 1/8W 1%	
53						1	3300-0060	RES VAR	R3		500Ω 20T	
54						2	3300-0073	"	R1,2		1K 20T	
55						2	3300-0034	RES. VAR	R49,53		500Ω 1T	
56												
57						3	4100-0011	"	C19,22,32		150 PF	
58						1	4100-0006	"	C36	DM10	20PF	
59						4	4100-0019	"	C31,37,45,47	"	50PF	
60						16	4300-0026	"	C10,3,4,5,6,17,8,33,35,38,40,42,		15/20V	
61						—	—	"	44,48,52,53		"	
62						2	4100-0015	"	C20,21		1000PF	
63						1	4200-0004	"	C39		.1 MYLAR	
64						19	4000-0025	CAP	C1,2,3,4,5,6,7,8,9,11,12,23,29,30,34,41,		.1 µf	
65						—	—	"	49,50,51		"	
66												
67						2	4100-0042	CAP	C43,46		300 pf	
68						5	4100-0032	CAP	C24,25,26,27,28		620 pf	
69						2	7000-0164	EJECTOR			SM. STYLE	

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
1						1	0111-0049	FRONT PANEL				
2						2	— —	KEPNUT			#4	
3						1	6000-0181	CONNECTOR 3 PIN			LEMO	
4						1	6000-0058	CONNECTOR 4 PIN			LEMO F/RA 0.304 NYLS/4.2	
5						1	6000-0187	CONNECTOR 8 PIN			MOLEX # 22-01-2081	
6						8	6000-0188	CONNECTOR PIN			MOLEX # 08-50-0114	
7						1	6000-0189	CONNECTOR KEY			MOLEX # 15-04-9209	
8						2		GROUND LUG			(BNC)	
9						2	6000-0003	CONNECTOR BNC				
10						2	6000-0215	CONNECTOR COAX				
11						A/R	—	COAX			RG 188	
12						1	6600-0082	SWITCH ROCKER	BLACK ROCKER		C&K 9201-J1 BLK WITH .190 MTG HOLES	
13						1	6100-0016	CONNECTOR 6 PIN		AMP 1-480076-0		
14						5	6100-0005	CONTACT SOCKET (F)		AMP 61173-1		
15						1	6800-0008	TEST POINT		SEALECTRO 011-6054		
16						2	7000-0253	SPACER	FOR POWERS		#6 X 3/16	
17												
18						4	7000-0007	INSULATING WASHER			BNC	
19						A/R		WIRE - WHT			26 AWG	
20						A/R			BLK/BLU			22 AWG	
21						A/R		WIRE - WHT/BRN			22 AWG	
22						A/R		WIRE - GRN/YEL			22 AWG	
23						1		GND LUG			#4	
24						1	6100-0112	HOUSING				
25						1	6100-0111	CONTACT				
26						A/R	8200-0007	LOCKTITE	TO MT. LEMO'S		#242	

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
1						1	0111-0107	P.C. BD				
2						1	0111-0027	HEATSINK				
3												
4						1	1700-0018	I.C	U1	N5558 1458		
5						1	1700-0033	I.C	U2	MC 3403		
6						1	1700-0066	TRANSISTOR	Q3	MOTOROLA 7902CP		
7						1	1700-0050	TRANSISTOR	Q4	NATIONAL LM345-5.2		
8						1	1700-0047	TRANSISTOR	Q5	NATIONAL LM340T-15		
9						1	1700-0072	TRANSISTOR	Q6	NATIONAL LM340T-12		
10						1	1700-0048	TRANSISTOR	Q7	NATIONAL LM320T-15		
11						1	1300-0020	TRANSISTOR	Q2	FAIRCHILD SE9300		
12						1	1400-0030	TRANSISTOR	Q1	2N5883		
13						6	1000-0008	DIODE	CR2,CR8,10-13	IN4154		
14						4	1200-0001	DIODE	CR3-CR6	IN4002		
15						2	1100-0003	ZENER DIODE	CR7, CR9	IN751A	5.1V	
16						2	1300-0001	TRANSISTOR	Q9, Q10	2N2222		
17						1	1400-0001	TRANSISTOR	Q8	2N2907		
18												
19												
20						1	4000-0038	CAPACITOR	C3		.01uf, 100V	
21						1	4000-0016	CAPACITOR	C4		.1 μf,	
22						3	4300-0025	CAPACITOR	C5,C6,C7	(196D)	47μf, 6V, TANT	
23						1	3050-3006	RESISTOR	R1		30Ω 1/2W	
24						1	4400-0023	CAPACITOR	C9		2200μf, 25V, ALUM	
25						3	4300-0026	CAPACITOR	C10,C12,C13	(196D)	15μf, 20V, TANT	
26						1	6000-0221	HEADER	J1		6 POS	
27						1	6000-0218	HEADER	J2		16 POS	
28						1	3200-0037	RESISTOR	R3		.01Ω	
29						1	3000-3006	RESISTOR	R4		30Ω, 1/4W	
30						1	3200-0019	RESISTOR	R2		5Ω, 4W	
31						3	6200-0031	RING TONGUE TERMINAL	E1,2,3		PANDUIT #10 BLUE	
32						6	3000-2001	RESISTOR	R5,7-8,13,15,28		2K, 1/4W, 5%	
33						1	3100-2001	RESISTOR	R6		2K, 1/4W, 10%	
34						1	3000-3901	RESISTOR	R10		3.9K, 1/4W 5%	
35						1	3100-2101	RESISTOR	R11		2.1K, 1/4W, 10%	
36						1	3080-5007	RESISTOR	R12		5Ω, 2W	

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
37						6	3000-1002	RESISTOR	R14,18,19,22,23,29		10K, 1/4W, 5%	
38						1	3100-6651	RESISTOR	R16		6.65K, 1/4W 1%	
39						4	3100-1002	RESISTOR	R17,21,24,27		10K, 1/4W, 1%	
40						1	3100-1652	RESISTOR	R20		16.5K,1/4W, 1%	
41						1	3100-2002	RESISTOR	R25		20K,1/4W, 1%	
42						1	3100-2431	RESISTOR	R26		2.43K,1/4W, 1%	
43												
44						4	————————	SCREW, PAN HD			#6 X 5/8 LG	
45						4	7000-0316	SHOULDER WASHER				
46												
47												
48						A/R	————————	WIRE	E1,E2,E3		16 GAUGE	
49						4	————————	KEP NUT			#6	
50												
51						5	————————	SCREW			#4 X 1/4 LG	
52						5	————————	SHOULDER WASHER				
53						2	7200-0016	TO-3 INSULATOR	Q4, Q1	CHOMERICS 60-11-4996-1666		
54						5	7200-0017	INSULATOR	Q2,3,5,6,7	CHOMERICS 60-11-4969-1666		

APPENDIX

DCD-1 DATA CARTRIDGE DRIVE

The following DCD-1 instruction manual is reproduced by permission of 3M Company, Mincom Division, Saint Paul, Minnesota.
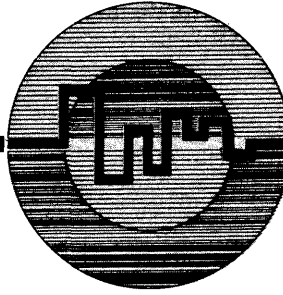
DCD-1
DATA CARTRIDGE DRIVE
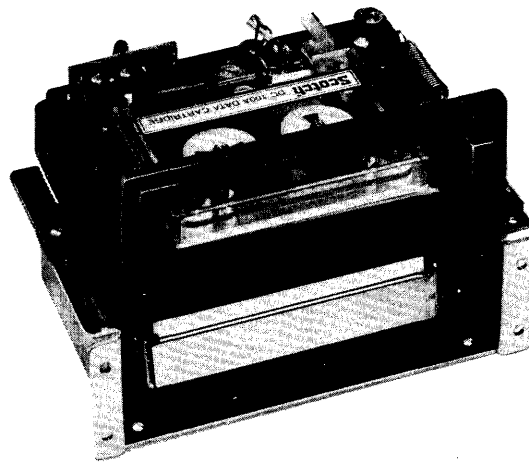
INSTRUCTION MANUAL

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SECTION I. INTRODUCTION

1-1 SCOPE

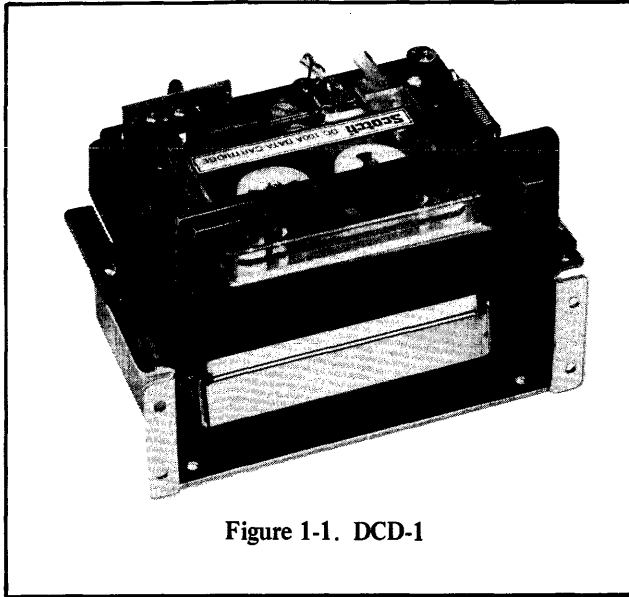This manual describes the DCD-1 Data Cartridge Drive along with its operation, interface, use, mounting, and maintenance.

Figure 1-1. DCD-1

This manual is divided into 4 sections each of which describes specific aspects of the drive.

SECTION I. INTRODUCTION

This section provides general information and specifications for the drive system as a whole.

SECTION II. GENERAL OPERATING PROCEDURES

This section describes the mounting, interface, use and scheduled maintenance requirements of the DCD-1 Cartridge Drive.

SECTION III. SUBASSEMBLY DESCRIPTIONS

This section describes the operation of the various subassemblies which comprise a DCD-1 Cartridge Drive.

SECTION IV. PARTS LISTS, SCHEMATICS, AND PC BOARD LAYOUTS

This section contains the engineering documentation for the system.

1-2 GENERAL DESCRIPTION

The DCD-1 Data Cartridge Drive has been designed for use with the "Scotch" Brand DC100A Data Cartridge. The drive and cartridge provide a tape storage system capable of recording and reading approximately 100,000 eight bit bytes in a physically small, highly reliable unit.

The DCD-1 consists of three major subassemblies. These subassemblies are:

1-2-1 MECHANICAL ASSEMBLY

The Mechanical Assembly includes those items necessary to position and hold a cartridge within the drive, to sense the presence of a cartridge within the drive, to detect the position of the cartridge File Protect Slide Switch, and to detect the tape position holes located on the cartridge tape. The mechanical assembly also includes a motor, a tape head, and a light source used in detection of tape position holes.

1-2-2 READ/WRITE AMPLIFIER AND SERVO ELECTRONICS PC ASSEMBLY

This PC Assembly includes the circuitry necessary (1) to maintain tape speed and direction according to input command; (2) to interlock all tape motion commands with tape position status so that improper commands (such as requesting REWIND when tape is at BOT) will not cause activation of the drive motor; (3) to accept TTL Compatible Serial data to be written which places flux transitions on the tape for each change of logic state in the input; and (4) to accept low level read data from the tape head and convert it to a TTL compatible serial data which is identical to the input used when writing data.

This assembly also contains select circuitry which allows up to four units, consisting of a mechanical assembly, read/write amplifier and servo electronics PC Assembly, to be connected to one Encode/Decode PC Assembly.

1-2-3 ENCODE/DECODE PC ASSEMBLY

This assembly consists of that circuitry necessary to accept 8 bit bytes (bit parallel) as a data input and decode a serial TTL bit stream for use by the write amplifier. This assembly also accepts a serial TTL bit stream from the read amplifier and decodes an 8 bit byte read output for the user.
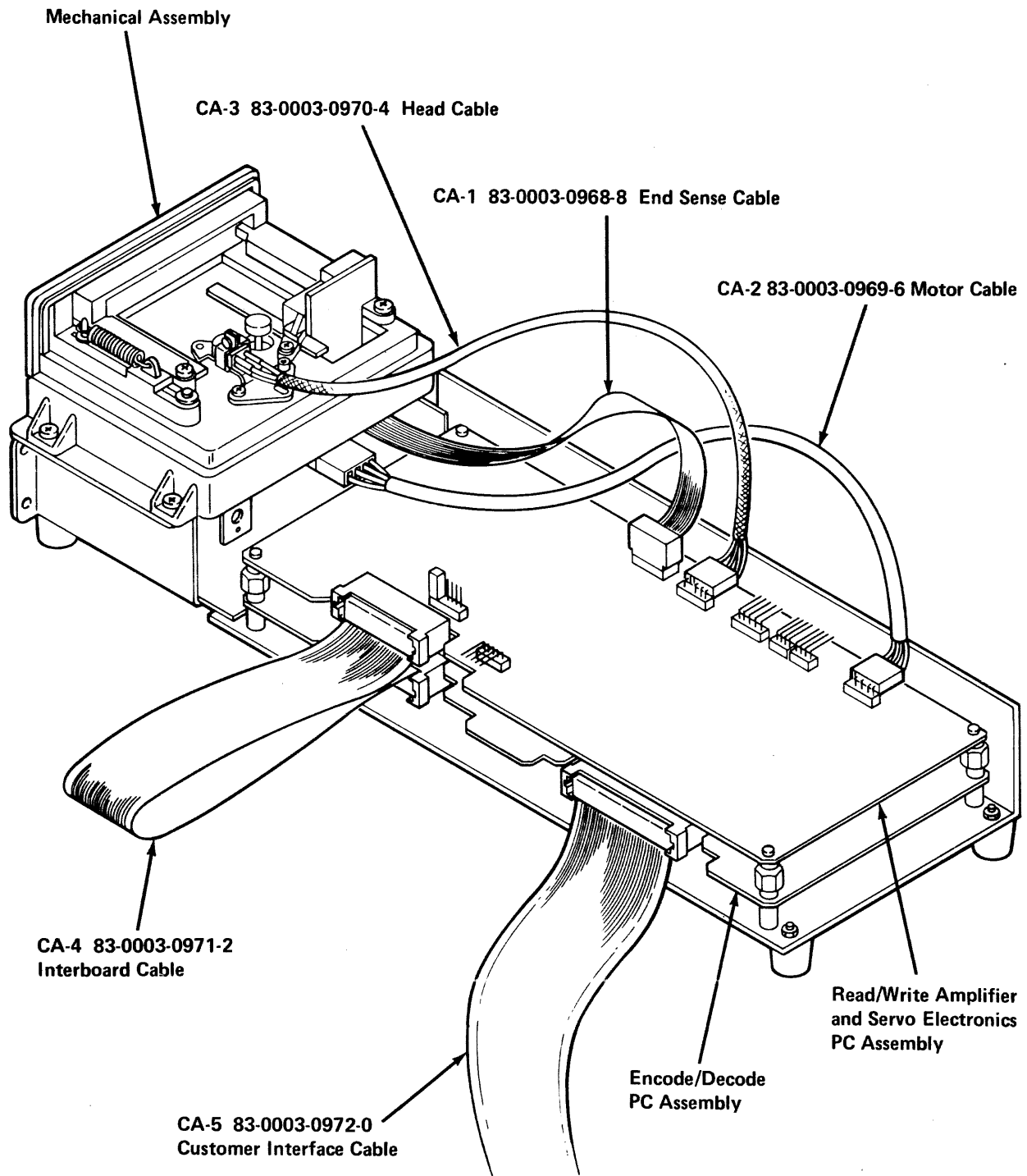
Mechanical Assembly

CA-3 83-0003-0970-4 Head Cable

CA-1 83-0003-0968-8 End Sense Cable

CA-2 83-0003-0969-6 Motor Cable

CA-4 83-0003-0971-2
Interboard Cable

Read/Write Amplifier
and Servo Electronics
PC Assembly

Encode/Decode
PC Assembly

CA-5 83-0003-0972-0
Customer Interface Cable

Figure 1-2. Assembly Locations

1-3 SPECIFICATIONS

The specifications of the DCD-1 Data Cartridge are as given below:

Cartridge	Uses the "Scotch" Brand DC100A Data Cartridge
Operating Speeds	FORWARD: 30 ips (76.2 cmps) REVERSE: 30 ips (76.2 cmps) or 60 ips (152.4 cmps)
Tape Head	Single channel, single gap, full width
Recording Format①	Variable Cell Width Recording②
Transfer Rate	2400 bytes/second, average
Cartridge Capacity	102,400 bytes, average (256 bytes per block, 1 inch IRG)
Start Delay	27 milliseconds
Stop Delay	5 milliseconds
Interface Logic	TTL compatible
Power	+5 VDC ±5%, 1.5 amps; +12 VDC (+10.8 VDC to +15 VDC), 1 amp average, 3 amps peak (20 msec duration) while running; 250 ma idle
Duty Cycle	7 start/stop operations per second maximum
Ambient Temperature	0°C to 50°C
Relative Humidity	20% to 80%, noncondensing

Size	Drive
	    5-3/4" wide (14.6 cm)
	    4" high (10.2 cm)
	    4-1/2" deep (11.4 cm)
	Electronics
	    Two 5" x 12" cards
	    (12.7 x 30.48 cm)

Weight	3-1/4 pounds maximum (1.47 kg)
Finish	All metal surfaces finished per best commercial practices.

NOTES:

① See Section 3.3.2 for description.

② PATENT PENDING

SECTION II. GENERAL OPERATING PROCEDURES

Before applying power to or attempting to use the DCD-1, the user should become familiar with this section of the manual.
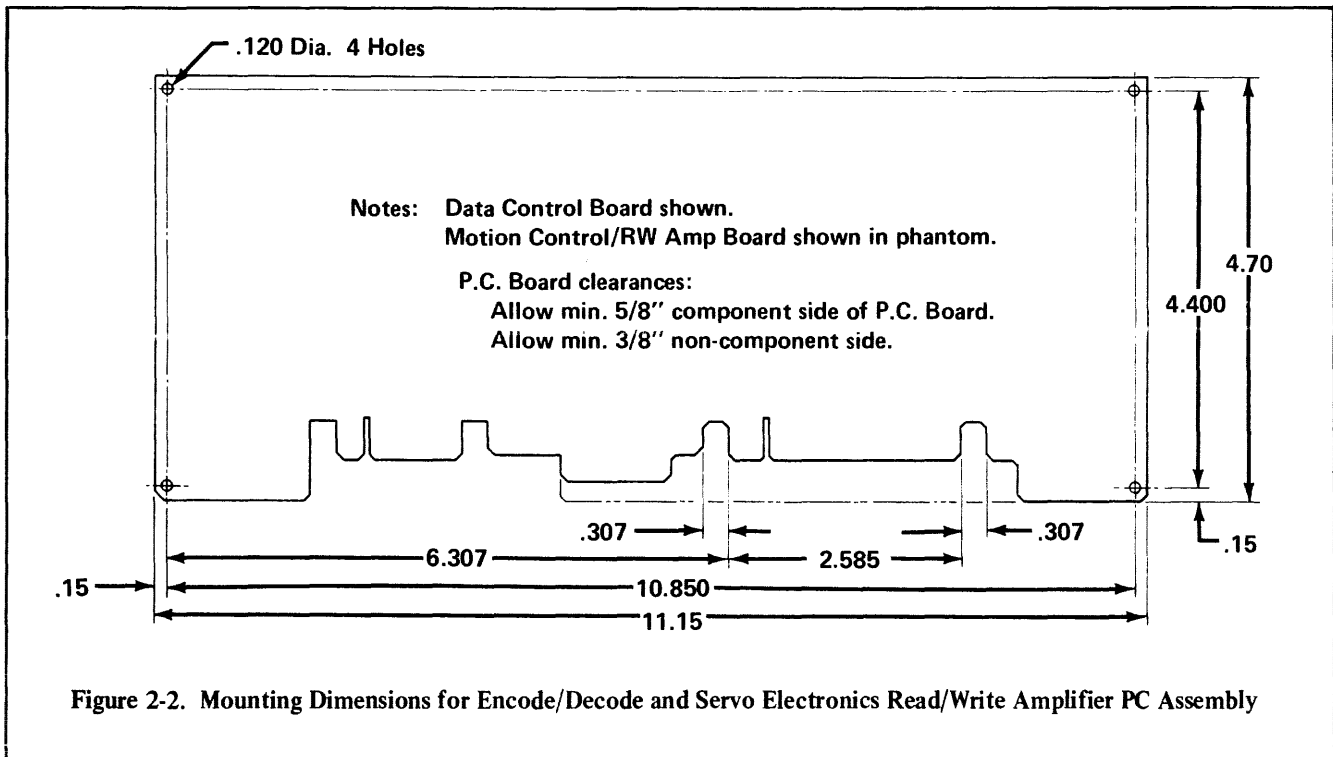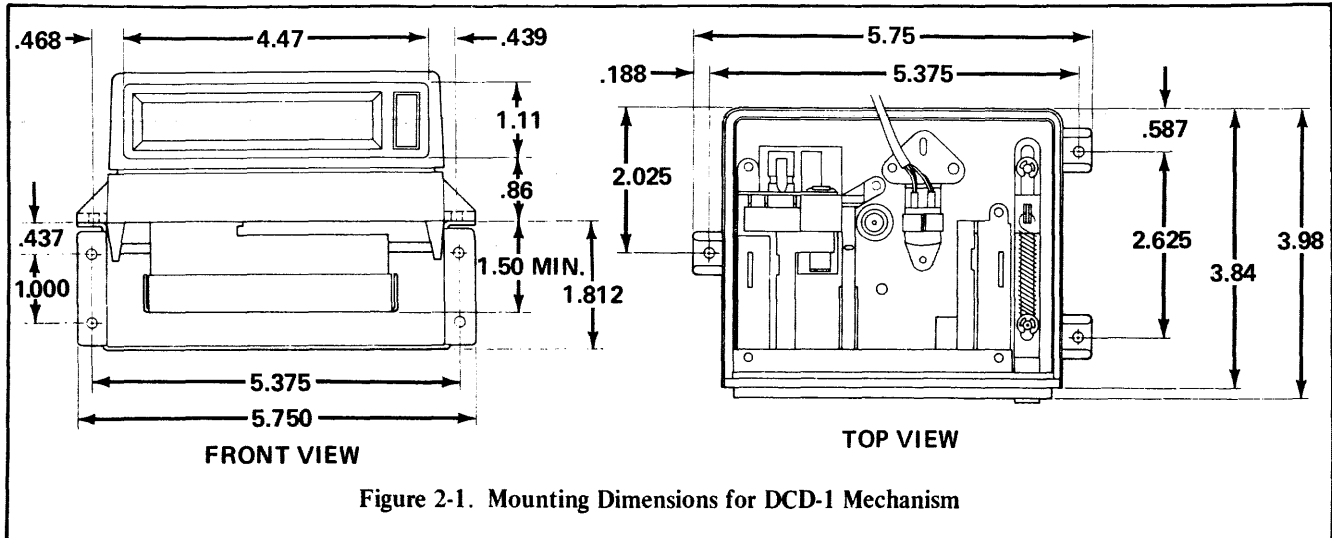
2-1 INSTALLATION

When unpackaging a DCD-1, the user should insure that the following items were received:

1 each   Mechanical Assembly
1 each   Read/Write Amplifier and Servo Electronics PC Assembly

1 each*   Encode/Decode PC Assembly
1 each*   Interboard Cable
1 each*   Interboard Connector
1 each*   6' Interface Cable and Connector Header
3 each*   PC Card Power and Display Connectors
2 each**   PC Card Power and Display Connectors
1 each   Instruction Manual

* Included with master drive units only
** Included with slave drive units only

Figure 2-1. Mounting Dimensions for DCD-1 Mechanism

Notes: Data Control Board shown.
Motion Control/RW Amp Board shown in phantom.

P.C. Board clearances:
Allow min. 5/8″ component side of P.C. Board.
Allow min. 3/8″ non-component side.

Figure 2-2. Mounting Dimensions for Encode/Decode and Servo Electronics Read/Write Amplifier PC Assembly
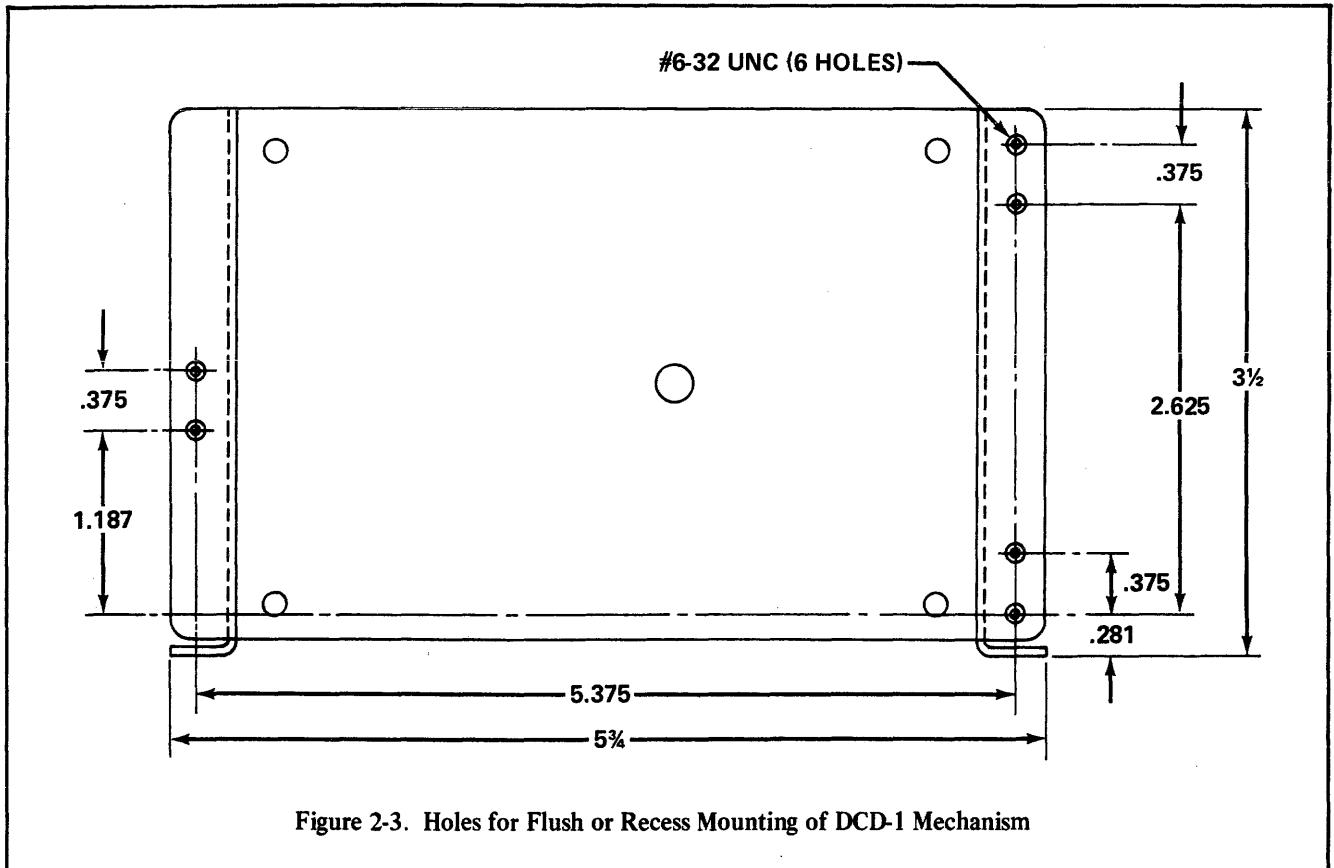
Figure 2-3. Holes for Flush or Recess Mounting of DCD-1 Mechanism

The DCD-1 mechanical assembly may be mounted in any attitude. As shown in Figure 2-1, the unit may be secured at the three ears of the top plate casting. Or if desired, the shipping bracket, used to protect the motor, may be used as a mounting frame. Location of holes for mounting in this frame are shown in Figure 2-1 and 2-2. Note that the top plate casting can be secured to the mounting frame in two different positions as shown in Figure 2-3. In the forward position, the frame can be attached to a front panel by through-bolting. In the recessed position, the frame can be attached to studs welded to the back of a front panel.

Figure 2-4 illustrates cable modification procedure for connecting one or more salve units to a master. Electrical interconnection of the three subassemblies is accomplished as shown in Figure 2-5. The two PC Assemblies may be mounted up to 12 inches away from the mechanical assembly. All connectors are keyed to prevent improper interconnection.

2-2 POWER APPLICATION

When applying power to the DCD-1, the +12 VDC power should be applied prior to application of the +5 VDC power

input. This prevents any possibility of motor movement during the power up cycle. When removing power, turn off the +5 VDC input first.

2-3 INTERFACE LOGIC

All inputs and outputs of the DCD-1 are TTL compatible with 0 to +0.8 VDC = logic 1 = low and +2.5 VDC to +5.0 VDC = logic 0 = high. The read data output is from 74125 tri-state drivers. The write data input goes directly to 74100 latches. All other outputs are from either 7416 or equivalent open collector buffer drivers. All inputs go to 7404 or equivalent gates. Except for select 0 and 1, which go to a 74155 2 line to 4 line decoder.

Recommended logic interfaces for the DCD-1 are as shown in Figure 2-6. When less than 4 feet of cable is used, the 220 ohm/330 ohm resistor terminations may be replaced with 1K ohm pull ups if desired.

2-4 INTERFACE SIGNALS

The interface signals of the DCD-1 and their functions are as described below. Details concerning the use of these signals are presented in various sections dealing with specific operations.
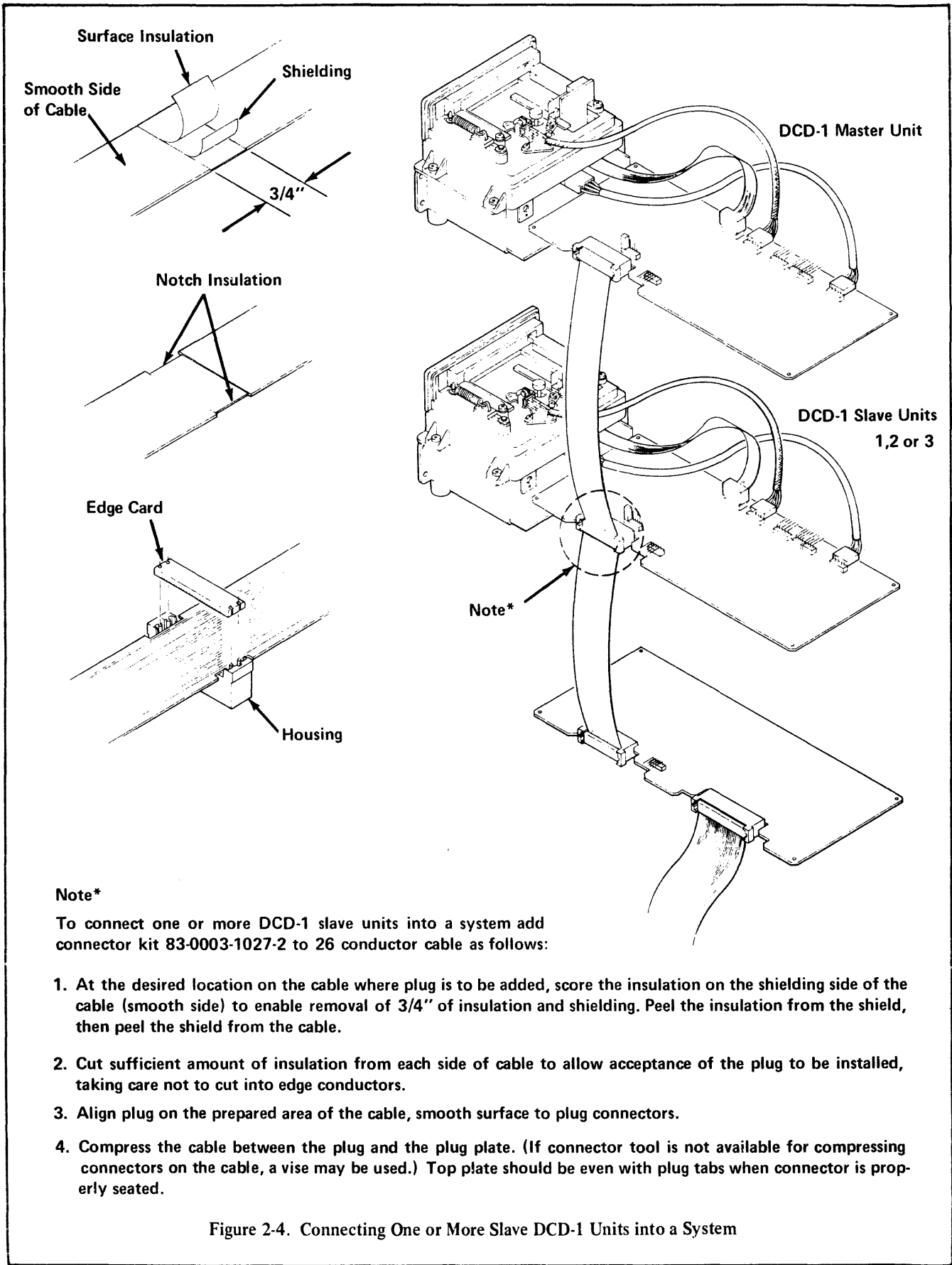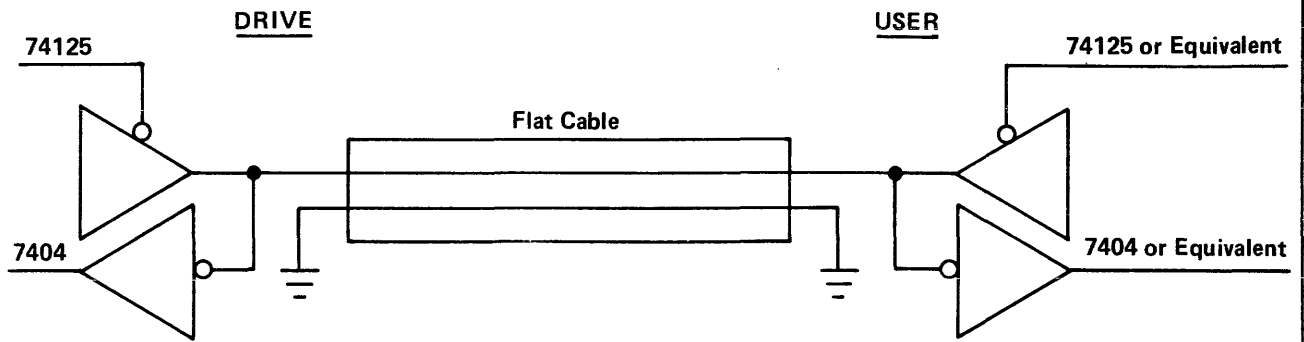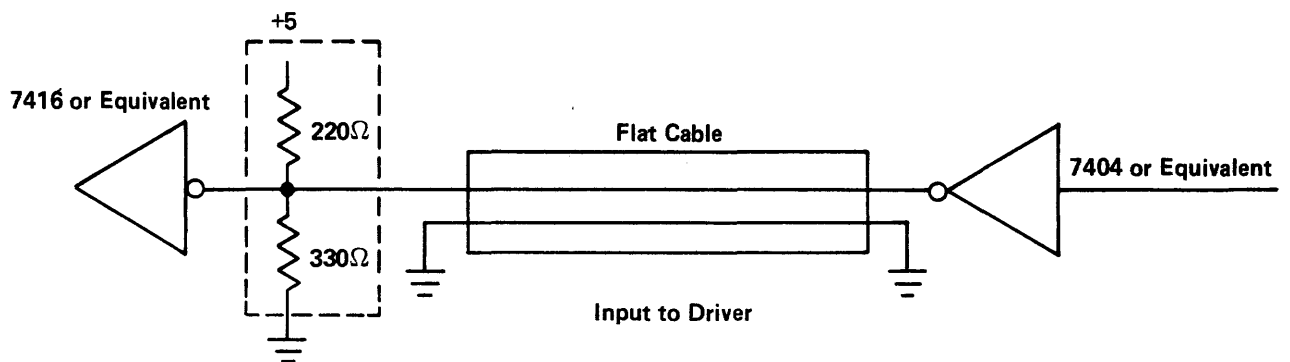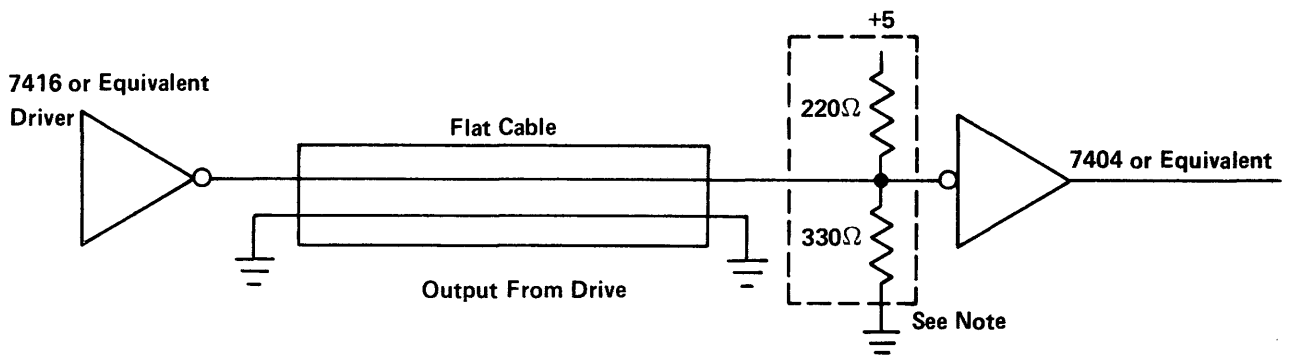
Note*

To connect one or more DCD-1 slave units into a system add connector kit 83-0003-1027-2 to 26 conductor cable as follows:

1. At the desired location on the cable where plug is to be added, score the insulation on the shielding side of the cable (smooth side) to enable removal of 3/4" of insulation and shielding. Peel the insulation from the shield, then peel the shield from the cable.

2. Cut sufficient amount of insulation from each side of cable to allow acceptance of the plug to be installed, taking care not to cut into edge conductors.

3. Align plug on the prepared area of the cable, smooth surface to plug connectors.

4. Compress the cable between the plug and the plug plate. (If connector tool is not available for compressing connectors on the cable, a vise may be used.) Top plate should be even with plug tabs when connector is properly seated.

Figure 2-4. Connecting One or More Slave DCD-1 Units into a System

DRIVE   USER

74125   74125 or Equivalent

Flat Cable

7404   7404 or Equivalent

NOTE: For short line (<4 feet) these lines could be driven from a MOS tri-state driver.
        Such as is used in some microprocessor systems.

7416 or Equivalent
Driver   +5

                    Flat Cable   220Ω

                                                          7404 or Equivalent

                    Output From Drive   330Ω

                                            See Note

        +5

7416 or Equivalent

        220Ω   Flat Cable

                                                          7404 or Equivalent

        330Ω

                                Input to Driver

NOTE: For short lines (<4 feet) each line may be pulled up with a single 1K resistor to
        +5V and driven by a MOS or standard TTL output. (Remove the 220 — 330 ohm
        network in tape drive (RN1) and replace with a 1K network.)

Figure 2-6. Recommended Interface Circuits

2-4-1 STATUS OUTPUTS

Two lines which give data relating to tape position and operational status of the drive. These outputs are:

2-4-1-1 BEGINNING OF TAPE (BOT)

A low level output that occurs when tape is at BOT. A reverse direction motion command will not be accepted when tape is at BOT.

2-4-1-2 READY

An output that is low during read operations when tape is between LOAD POINT and EARLY WARNING. See Figure 2-8. During write operations, the cartridge file protect slide switch must be in the RECORD position and the tape must be between LOAD POINT and EARLY WARNING for READY to go low.

2-4-2 TAPE MOTION COMMANDS

The DCD-1 Data Cartridge Drive has four input lines to control tape motion. These inputs are interlocked to the various drive status and tape position outputs to prevent motions which might damage the cartridge, such as giving a reverse command when the cartridge is already at beginning of tape.

2-4-2-1 FORWARD/REVERSE (F/R)

The status of this line determines the direction of tape motion. A high level causes forward motion and a low level causes reverse motion when the RUN input pulse is applied.

2-4-2-2 RUN

A low going pulse of 500 nanosecond minimum, maximum of 200 microsecond duration on this line causes tape motion to commence in the direction determined by the state of the FORWARD/REVERSE input. Motion commences upon the low to high transition. Minimum of 200 microseconds before most drives will start.)

2-4-2-3 STOP

A low going pulse on this line of 50 nanosecond minimum duration causes tape motion to stop. The STOP input overrides the RUN input, so that if both RUN and STOP are simultaneously low no tape motion will result.

2-4-2-4 RESET

A low going pulse on this input causes the READY input to go low regardless of tape position. This line is used to clear drive logic after a power interrupt. If tape is in motion when the RESET pulse is applied, tape motion will halt. RESET should be a pulse of 500 nanoseconds minimum duration and should be held low until power is completely up. Note that RESET clears system logic and forces the READY output to the true (low) state. Consequently, improper use of the RESET input (stopping at EOT, applying a reset pulse, commanding forward tape motion, and repeating this sequence) could cause damage to the cartridge. It is therefore recommended that after applying a RESET command, the cartridge be rewound to BOT before commencing further operations.

2-4-3 SELECT 0 AND SELECT 1

These two lines are used to select the active drive in multiple drive systems according to the following table:

Table 2-1. Active Drive Selection

SELECT 0	SELECT 1	SELECTED DRIVE
High	High	0
Low	High	1
High	Low	2
Low	Low	3

2-4-4 DATA 0 THROUGH DATA 7

Eight lines which form the data bus (used in both read and write operations). DATA 0 is the least significant bit, DATA 7 is the most significant bit.

2-4-5 READ/WRITE CONTROL

A level input which controls mode of operation. This line is held low to perform a write operation (enables head current) and held high to perform a read operation. During write operations, READ/WRITE CONTROL should be set low prior to initiating tape motion and held low until tape motion ceases to insure the writing of clean interrecord gaps.
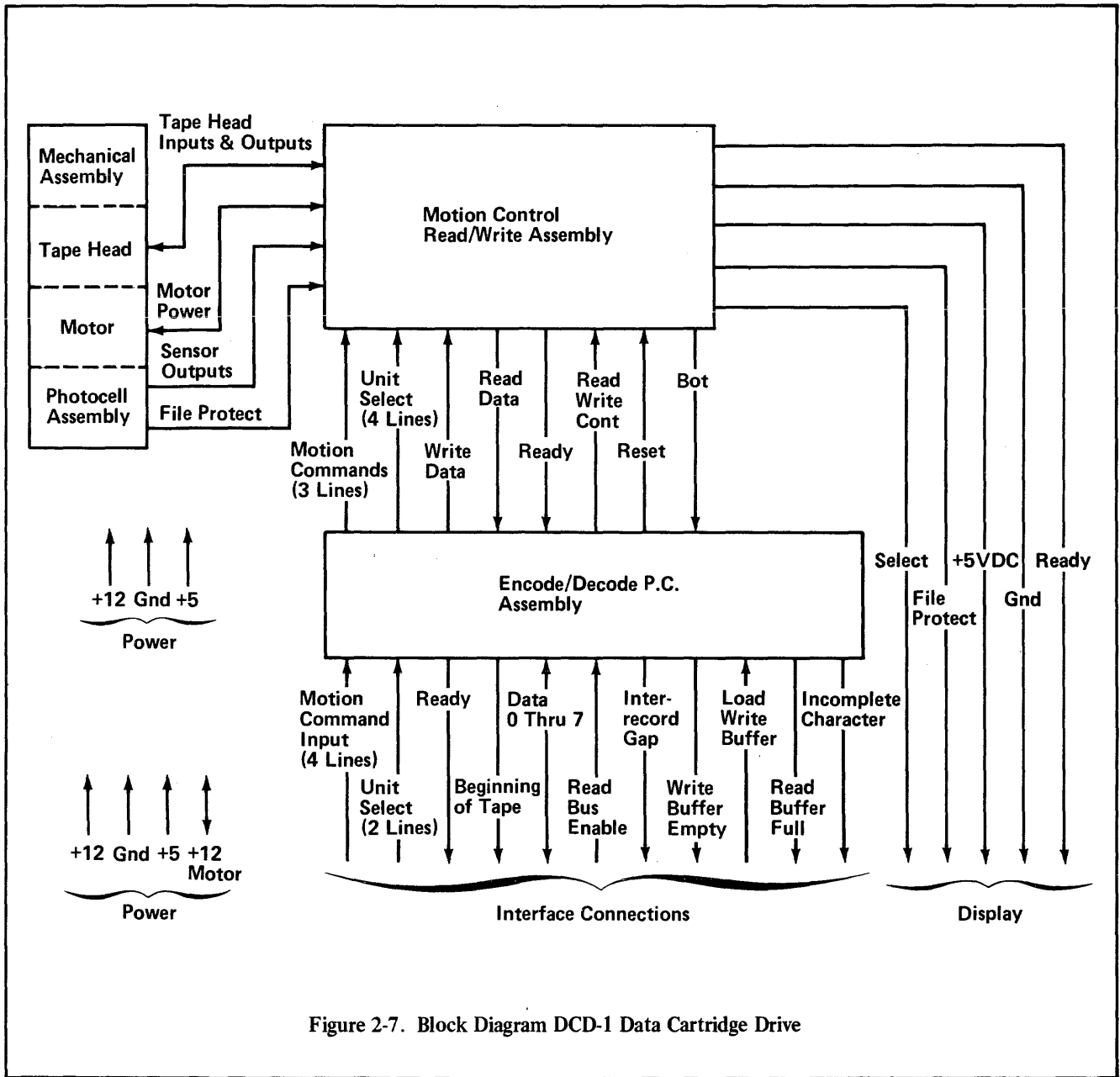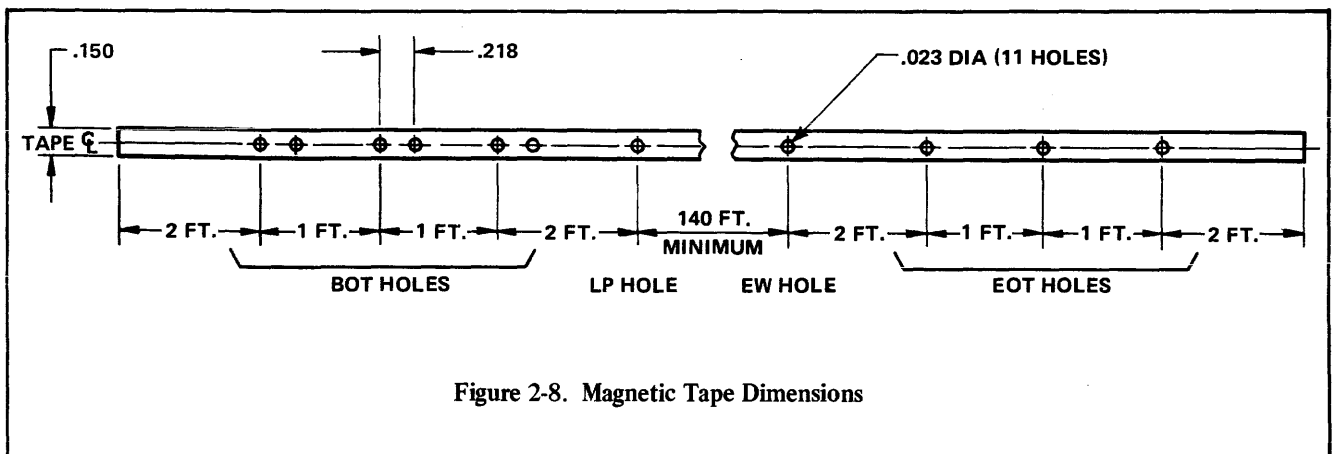
Figure 2-7. Block Diagram DCD-1 Data Cartridge Drive

Figure 2-8. Magnetic Tape Dimensions

2-4-6 READ BUS ENABLE

When this line is pulsed low, the contents of the read buffer are shifted onto the data bus. This pulse also clears the READ BUFFER FULL and INCOMPLETE CHARACTER flags.

The READ BUS ENABLE pulse must be at least 50 nanoseconds in duration and must occur no sooner than 20 nanoseconds after READ BUFFER FULL goes low. The READ BUS ENABLE pulse must return high within 200 microseconds of READ BUFFER FULL going low to avoid missing data, and must be held high during write operation.

2-4-7 INTERRECORD GAP

An output that goes low each time an interrecord gap is detected. This output is active when tape is moving in either the forward or reverse direction.

2-4-8 WRITE BUFFER EMPTY

This is an output flag that goes low to indicate that the write buffer is empty and ready to accept another byte of data.

When the first byte of a block is loaded, WRITE BUFFER EMPTY will go low again within from 16.7 microseconds to 83.5 microseconds, depending upon internal logic timing. After going low for the second byte, WRITE BUFFER EMPTY will go low no sooner than every 350 microseconds.

2-4-9 LOAD WRITE BUFFER

A low going pulse on this input causes information on the data bus to be strobed into the write buffer. This pulse must be at least 500 nanoseconds but no greater than 1.5 microseconds long. (The LOAD WRITE BUFFER pulse must occur less than 320 microseconds after WRITE BUFFER EMPTY goes low.) The LOAD WRITE BUFFER pulse also clears the WRITE BUFFER EMPTY output flag.

2-4-10 READ BUFFER FULL

This is an output flag that goes low when the read buffer contains a data byte. This flag will stay low until cleared by a READ BUS ENABLE input flag. READ BUFFER FULL will go true no sooner than every 200 microseconds.

In order to discriminate against false transitions in the interrecord gap, one 8 bit byte must be read before this flag becomes active.

2-4-11 INCOMPLETE CHARACTER

This is an output flag that goes low if a complete 8 bit byte is not contained in the read buffer when the READ BUFFER FULL output goes low. All bytes containing fewer than 8 bits will result in this flag going low thus indicating an error condition caused typically by tape dropouts. In order to discriminate against false transitions in the interrecord gap, one 8 bit byte must be read before this flag becomes active. A READ BUS ENABLE pulse clears this flag; therefore the status of this flag should be checked after READ BUFFER FULL goes low but before the READ BUS ENABLE input is issued.

Table 2-2. DCD-1 Power Connector Pin Assignments (SERVO ELECTRONICS AND READ/WRITE AMPL PC ASSEMBLY)	
Pin	Function
1	+12 VDC 10.8 VDC to 15.0 VDC, 1 Amp Avg. 3 Amps Peak (20 msec duration) while running; 250 ma idle
2	Ground
3	+5 VDC ±5%, 0.5 amps
4	Ground
5	+12 VDC

Table 2-3. DCD-1 Power Connector Pin Assignments (ENCODE/DECODE PC ASSEMBLY)	
Pin	Function
1	+12 VDC (Not Used)
2	Ground
3	+5 VDC ±5% 1.5 Amps
4	Ground
5	+12 VDC (Not Used)

Logic interface connection to the DCD-1 is via a 50 pin, PC card edge connector, "Scotchflex" No. 3415-0001 or equivalent, keyed between contacts 8 and 10. For "Scotchflex" connectors, use key No. 3439-0000.

Power connection is via two Molex connectors, No. 22-01-2051 with contacts No. 08-56-0114. One connector is used for each PC card.

Table 2-4. Interface Connector Pin Assignments

Function	Pin
Run	2
Load Write Buffer	4
Select 0	6
Select 1	8
Read/Write Control	10
Forward/Reverse	12
Reset	14
Stop	16
Read Bus Enable	18
Ready	20
Write Buffer Empty	22
Interrecord Gap	24
Incomplete Character	26
Read Buffer Full	28
Beginning of Tape	30
Not Used	32
Not Used	34
Data 0	36
Data 1	38
Data 5	40
Data 4	42
Data 2	44
Data 3	46
Data 7	48
Data 6	50
Common	All Odd No. Pins 1-49

2-5 CARTRIDGE LOADING

Loading the cartridge requires inserting a cartridge into the drive and positioning tape at Load Point.

The cartridge is installed in the drive by inserting it into the rectangular slot in the drive facade. With respect to the top plate, the cartridge is inserted with its metal base plate next to the drive top plate and with the cartridge edge containing head door and belt capstan being inserted first (this is the only cartridge orientation that will permit cartridge loading). The cartridge should be pushed fully into the drive; an audible click will be heard and the EJECT button protrudes from the front of the mechanism when the cartridge is engaged by the drive. Should difficulty be encountered, be sure the EJECT button is fully depressed before inserting the cartridge. To remove a cartridge from the drive, depress the EJECT button on the front facade of the drive.

Once the cartridge has been inserted into the drive, the first command issued must be for reverse motion (this is the

only command that will be accepted until BOT is reached). When tape motion stops at BOT, command forward motion until Load Point is reached (the READY output will go true). The drive and cartridge are now initialized and ready for subsequent read/write operations.

2-6 INTERRECORD GAP TIMING

To insure the writing of proper length interrecord gaps, the following delays should be employed:

(a) After commanding forward tape movement, delay 27 milliseconds before entering the first data byte.

(b) After writing (or reading) the last data byte, delay 5 milliseconds before commanding a STOP. During read operations, the INTERRECORD GAP output indicates the end of a data block.

2-7 WRITING A DATA BLOCK

It is recommended that an initial gap of 7-1/2 inches or longer be used between the LOAD POINT hole and the first data record. (Approximately 275 ms delay following the READY signal at LOAD POINT will produce this initial gap.)

When writing data, the following sequence of events should be used:

1. Set the READ/WRITE CONTROL input to the low logic state.

2. Check the READY output (assuming that tape is between LOAD POINT and EARLY WARNING). If it is low, proceed. If it is high, remove the cartridge, place the file protect slide switch in the RECORD position, reinsert the cartridge, set READ/WRITE CONTROL high, rewind to BOT, come forward until READY goes low, stop tape motion, and commence operation again at Step 1.

3. Set the FORWARD/REVERSE input high.

4. Apply a pulse to the RUN input.

5. Delay 27 milliseconds during which time the first byte to be written should be placed on the data bus.

6. After 27 milliseconds apply a LOAD WRITE BUFFER pulse.

7. Monitor the WRITE BUFFER EMPTY output. When this output goes true place the next byte to be writ-

ten on the data bus and issue another LOAD WRITE BUFFER pulse. Continue this process until all required bytes have been written.

8. Five milliseconds after the last LOAD WRITE BUFFER input, apply a STOP pulse.

9. Allow 20 milliseconds for tape motion to stop.

10. If the next operation to be performed is a write, leave READ/WRITE CONTROL low. If a read or rewind is to be performed next, set READ/WRITE CONTROL high.

2-8 READING DATA

The reading of data is accomplished per the following procedure:

1. Set the FORWARD/REVERSE input high.

2. Apply a pulse to the RUN input.

3. Apply a pulse to the READ BUS ENABLE input to clear the READ BUFFER FULL and INCOMPLETE CHARACTER flag circuits. This pulse should occur before data is encountered.

4. Monitor the READ BUFFER FULL output. For the first byte, it will go low about 27 milliseconds after the RUN pulse is applied. Thereafter it will go true approximately every 350 microseconds.

5. When READ BUFFER FULL goes low check the level of the INCOMPLETE CHARACTER output to determine if an error has occurred.

6. Set the READ BUS ENABLE input low. The data byte will have settled on the data bus within 50 nanoseconds of this input. Read data is only on the bus as long as this input is low.

7. After the byte has been captured by the user's circuitry, set READ BUS ENABLE high.

8. Alternate between monitoring the READ BUFFER FULL and INTERRECORD GAP flags.

9. If READ BUFFER FULL goes low, return to Step 5.

10. If INTERRECORD GAP goes low, wait 5 milliseconds and apply a pulse to the STOP input. Wait 20 milliseconds for tape motion to stop before issuing further commands. A continuous read is accomplished by not issuing the STOP pulse.

Table 2-5. Display Connector Pin Assignments

FUNCTION	SYMBOL USED ON SCHEMATIC	PIN
Select	SEL	1
+5 VDC	+5 VDC	2
File Protect	FP	3
Ground	GND	4
Ready	RDY	5

2-9 DRIVE UNIT SELECTION

As noted in paragraph 1-2-2, the DCD-1 is available in multiple drive configurations. When 2 or more drives are present, the SELECT 0 and SELECT 1 inputs must be used to determine which drive shall be operative during execution of a given function. Selection is accomplished according to the following table:

Table 2-6. Drive Unit Selection

DRIVE	SELECT 0	SELECT 1
0	High	High
1	Low	High
2	High	Low
3	Low	Low

2-10 RECOMMENDED MAINTENANCE

The only periodic maintenance required on the DCD-1 is cleaning of the tape head and motor drive roller.

These items should be cleaned with ethyl alcohol and a cotton swab every 1,000 to 1,500 cartridge cycles. A cycle is defined as tape movement from BOT to EOT and back to BOT.

In harsh environments cleaning may be required more frequently.

SECTION III. SUBASSEMBLY DESCRIPTIONS

3-1 MECHANICAL ASSEMBLY

3-1-1 DESCRIPTION

The Mechanical Assembly consists of those items necessary to position and hold a cartridge for READ/WRITE OPERATION, to apply rotary power to the cartridge bolt capstan to create motion, to detect the presence of a cartridge within a drive, to determine the status of the cartridge file protect plug, and to detect the tape position holes of the cartridge.

The major components of the assembly are the top plate, the motor-tachometer, the tape head, and the photocell amplifier PC Assembly.

3-1-2 MAINTENANCE

DCD-1 Alignment Kit 80-9700-0167-5 is available from the 3M Company. The kit contains one 80-9700-0168-3 DC100A Azimuth Alignment Tape, one 80-9700-0169-1 DC100A Speed Tape and instructions.

3-1-2-1 HEAD AND PUCK CLEANING

The only periodic maintenance required on the mechanical assembly is cleaning of the tape head and the drive puck. This cleaning operation should be accomplished every 1,000 − 1,500 tape cycles. In harsh environments, cleaning on a more frequent basis may be required.

Cleaning should be accomplished with a cotton swab moistened with ethyl alcohol by gently rubbing the head and then the drive puck.


NOTE

The useful life of the DCD-1 Data Cartridge Drive is estimated at 40,000 tape cycles. At this point, the head and/or motor may be near failure, and the user may elect to change these components.

It is recommended, however, that only the volume user with formalized depot programs and facilities attempt to replace these components in the Mechanical Assembly. Other users are advised to return the unit to the factory for replacement of these items.

Replacement of the EOT/BOT bulb is the one procedure which does not require specialized tools and fixtures.

3-1-2-2 EOT-BOT BULB REPLACEMENT

1. Remove the two front bezel mounting screws.

2. Remove the front bezel.

3. Unplug the cable from the EOT/BOT PC Board.

4. Remove the two rail mounting screws (left rail).

Figure 3-1. EOT/BOT Bulb Replacement
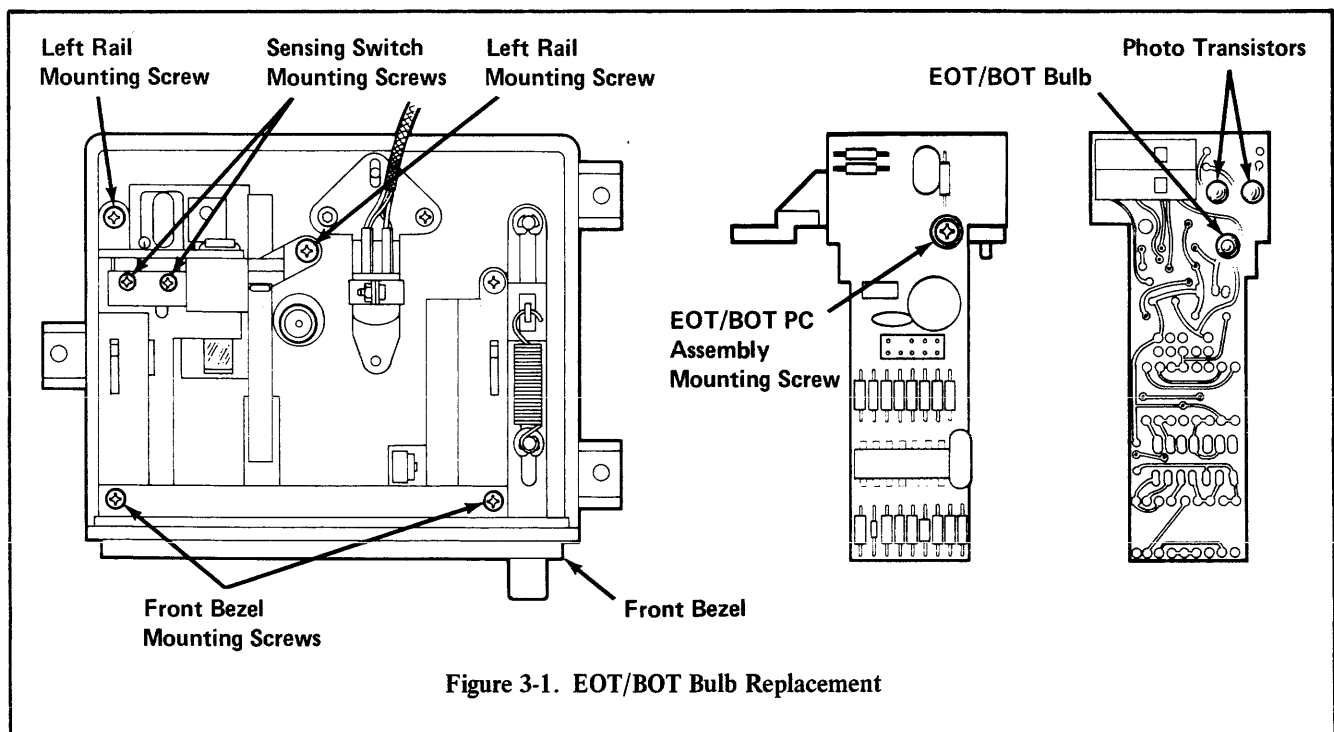
5. Remove the left rail and the EOT/BOT PC Assembly from the mechanism.

6. Remove the two sensing switch mounting screws.

CAUTION

Hex nuts are free in block depression.

---

7. Remove Phillips mounting screw and plastic insulation washer from the EOT/BOT PC Assembly.

8. Remove the EOT/BOT PC Board and switch assembly from the block.

9. Unsolder the old bulb from the board and clean the solder from the holes.

10. Place the new bulb leads through the holes and insert the bulb fully into the block as the PC board is again fitted to the block. Secure with the Phillips mounting screw and insulating washer.

11. Solder bulb leads with the bulb located all the way into the block.

12. Reverse the disassembly procedure from Step 6 through Step 1.

3-1-2-3 MOTOR REPLACEMENT
See Figure 3-2

1. Remove the deck from the mounting base.

2. Remove the power cable from the motor.

3. Remove the two motor pivot mounting screws.

4. Remove the motor assembly. Retain the pivot pins.

5. Insert the pivot pins into the new motor mounting.

6. Remount the motor using the screws and pivot hold down clamps.

7. No end play is permissible in the motor pivot mount. Secure one pivot clamp and force the other pivot pin into the motor mount, tighten the second pivot clamp. If end play is not completely removed, loosen one pivot clamp and force the pivot pin in, then re-tighten the clamp screw.

See maintenance section for motor control alignment procedure.

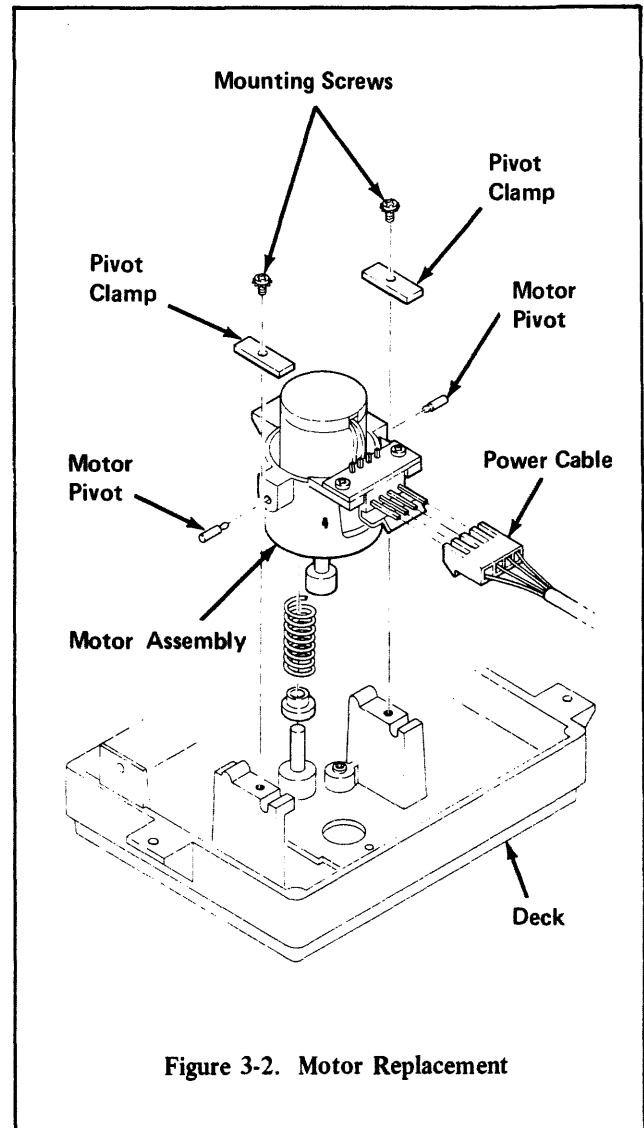8. Whenever a motor is replaced the Servo Electronics *MUST BE REBALANCED.*

Figure 3-2. Motor Replacement

3-1-2-4 HEAD REPLACEMENT
See Figure 3-3

1. Loosen the head clamp screw sufficiently to allow the head to be removed.

2. Be sure the new head has one wrap of mylar tape around the body of the head to give insulation between head and the mounting bracket.

3. Slide the new head into place and tighten the mounting screw lightly so that head position can be changed with finger pressure.

4. Position the head so that the head will push the tape .055" to .065" into the cartridge when a cartridge is inserted fully into the deck. This may be done by measuring the distance from when the head first contacts the tape as a cartridge is inserted, and when the cartridge is firmly in position.

5. Align the two mating surfaces of the head clamp and tighten the head clamp firmly.

6. Install azimuth alignment cartridge 3M Number 80-9700-0168-3 into the drive and adjust the azimuth screw for maximum output at TP3.

CAUTION

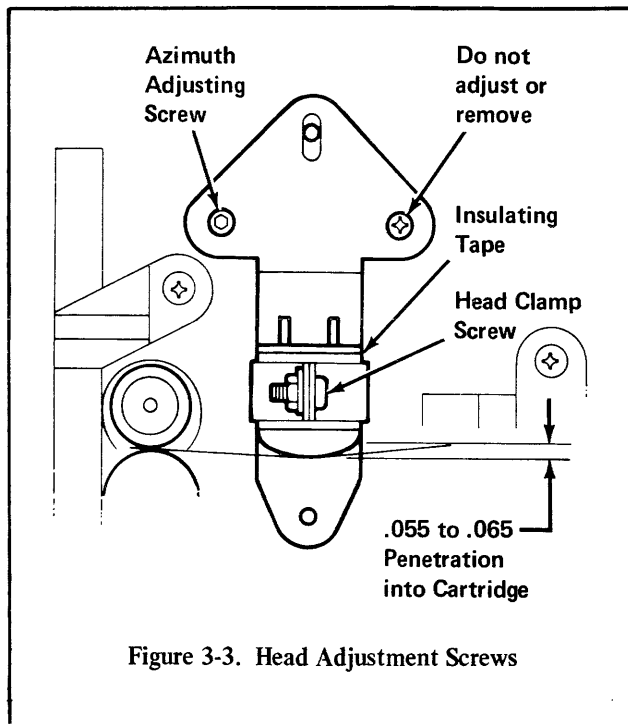When installing a new head degauss the head before using the azimuth test tape.

Figure 3-3. Head Adjustment Screws

3-2 SERVO ELECTRONICS AND READ/WRITE AMPLIFIER PC ASSEMBLY

This assembly is comprised of the major subfunctions listed below. See Block Diagrams, Figure 3-4 and 3-5.

3-2-1 DRIVE SELECT LOGIC

This circuitry consists of the select jumper plug which enables only the selected drive command input gates and output gates.

3-2-2 DIRECTION CONTROL LOGIC

This circuitry is comprised of two sections.

1. The Status Logic section monitors cartridge related factors such as tape position, file protect status, and cartridge in place status.

2. The Command-Status Interlock section prevents acceptance of motion commands which could harm the cartridge (rewinding from BOT, etc.).

3-2-3 SERVO ELECTRONICS

This circuitry consists of several sections which operate in unison to control the direction and speed of tape motion (by controlling motor input voltage). Jumper J7 allows user the choice of 30 ips or 60 ips reverse.

3-2-4 WRITE CIRCUITRY

This circuitry consists of a write enable transistor switch which only permits head current to flow when the READ/WRITE Control input is low, and the write head drivers.

3-2-5 READ CIRCUITRY

This circuitry consists of Operational Amplifiers for Read, Threshold Detector, and Peak Detector.

3-2-6 DRIVE SELECT LOGIC
See Figures 3-4 and 3-5

One of four ENABLE inputs is connected through a jumper plug at connector J8 to IC16, pin 9. This signal is routed through 2 inverter stages and then enables negative and gates for input signals (RUN, STOP, READ/WRITE CONTROL, WRITE DATA, FORWARD/REVERSE, and RESET). The same signal also enables tri-state gates for output signals (BOT, READY, and READ DATA). The signal at IC16, pin 8 is also inverted to provide a SELECT output at IC20, pin 2. This output can sink 40 ma at +5 VDC.

3-2-6-1 LOGIC INTERFACE CONNECTIONS

The interface connections of the drive select logic portion of the read/write amplifier and servo electronics PC Assembly and their use is as described below:

3-2-6-2 ENABLE 0, 1, 2 AND 3

One to four drives may be used in a system. Selection of one of four drives is performed on the data control logic PC Electronic Assembly. This will hold either EN 0, EN 1, EN 2, or EN 3 to ground and thereby selects the proper drive.

3-2-6-3 UNIT DESIGNATE

J8 requires a jumper plug to select the proper drive. Place the jumper plug in the 0 position when only one drive is used. When multiple drives are used designate the drive number by placing the jumper plug in positions 0, 1, 2, or 3.
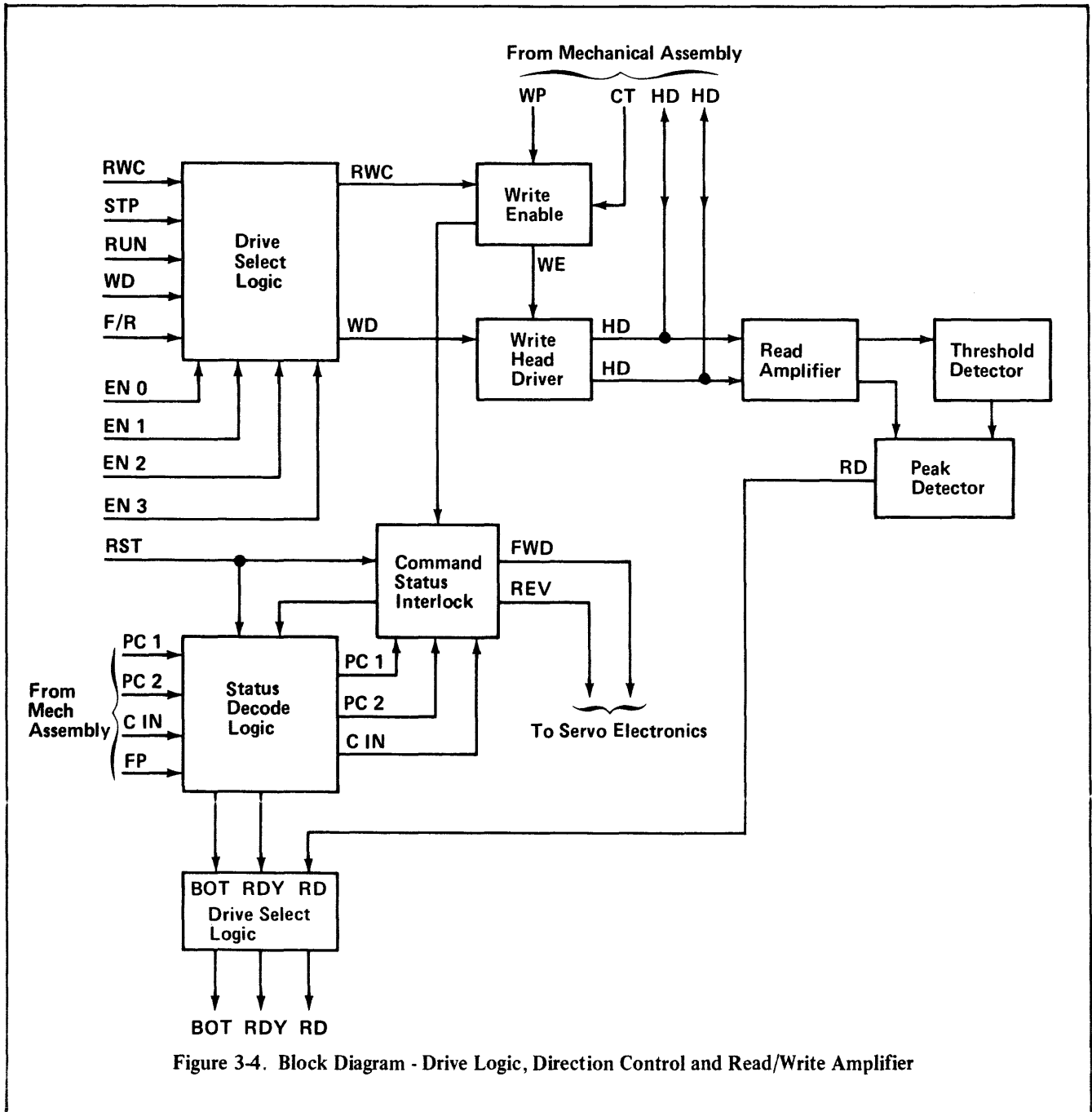
Figure 3-4. Block Diagram - Drive Logic, Direction Control and Read/Write Amplifier

3-2-6-4 FORWARD/REVERSE

The status of this line determines the direction of the tape motion. A high level causes forward motion while a low causes a reverse motion when the RUN input pulse is applied.

3-2-6-5 RUN

A low going pulse of 500 nanosecond minimum, maximum of 200 microsecond duration on this line causes tape motion to commence in the direction determined by the state of the FORWARD/REVERSE imput. Motion commences upon low to high transition.

3-2-6-6 STOP

A low going pulse of 500 nanosecond minimum duration on this line causes tape motion to stop. The STOP input overrides the RUN input, so, if both RUN and STOP are simultaneously low, no tape motion will result.

3-2-7 STATUS DECODE LOGIC

3-2-7-1 CARTRIDGE IN (CIN)

A switch on the mechanical assembly senses the presence of the data cartridge. When the cartridge is out this line clears the 4 bit bidirectional shift register (IC3) and sets the set/reset flip flop (IC10) to the initialization state.

3-2-7-2 PHOTOCELL 1 (PC1)

An input from the Photocell Amplifier PC Assembly. Momentarily high when a hole passes by the Photosensor. Used along with Photocell 2 to develop the various tape position outputs. A hole in the tape passes by Photocell 1 before Photocell 2 when the tape is moving in the forward direction.

3-2-7-3 PHOTOCELL 2 (PC2)

An input from the Photocell Amplifier PC Assembly. Momentarily high when a hole passes by the Photosensor. Used with Photocell 1 to develop the various tape position outputs.

3-2-7-4 FILE PROTECT

An input from the file protect switch of the photocell amplifier PC Assembly. During write operations the file protect switch on the DC100A Cartridge must be in the record position. If it is not in the Record position and RWC (Read/Write Control) is forced true, RDY will go false indicating the drive is not in the proper mode for writing. Forward and reverse motion can still take place with RDY false, but no writing will occur since the write current is disabled whenever the record switch on the DC100A is not in the record position.
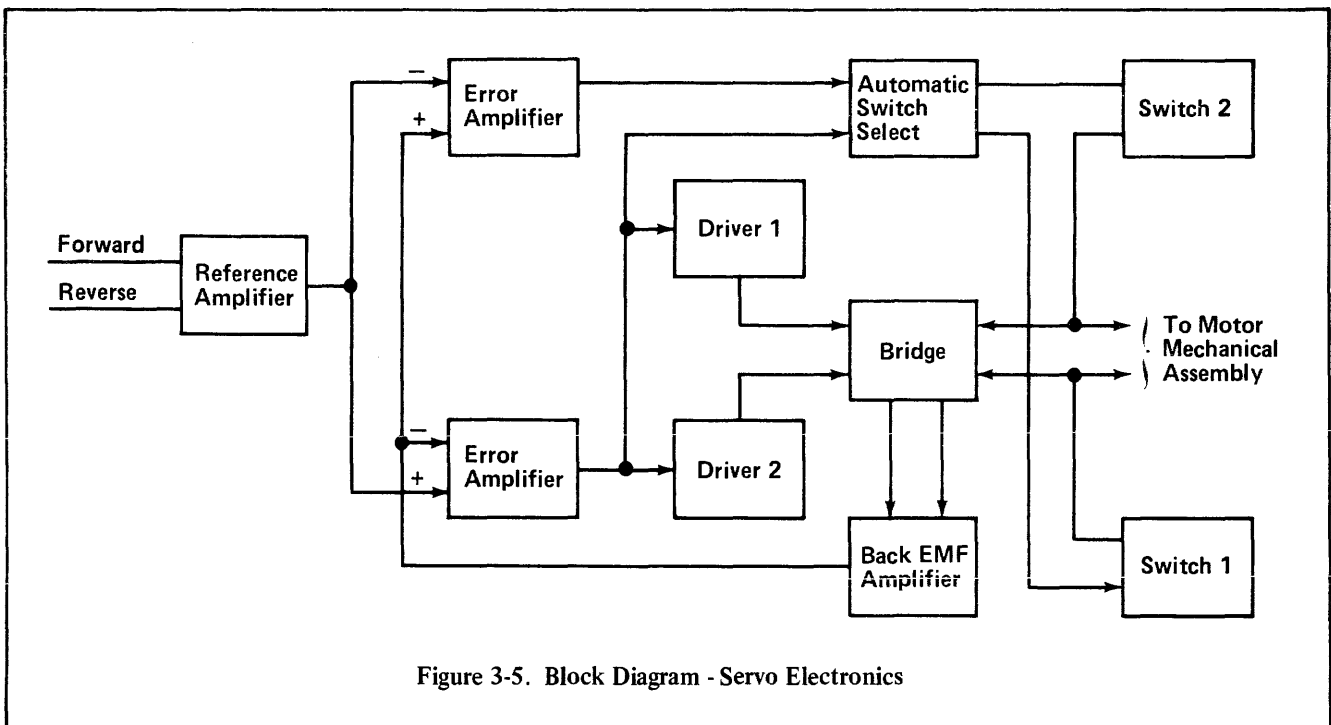

Figure 3-5. Block Diagram - Servo Electronics

3-2-7-5 RESET (RST)

A low going pulse on this line forces the status decode logic to the Ready (RDY) state regardless of actual tape position. In the ready state either Forward or Reverse Commands will be accepted. Reset Commands should be used in only these cases.

1.   If it can be determined, the tape in the DC100A is actually between LP and EW. The determination of this fact would have to be based on past cartridge history.

2.   To determine whether or not a cartridge is actually in the drive. A Reset Command will have no effect if there is no cartridge in the drive. Thus, issuing a Reset Command and sensing ready indicates the presence of a cartridge. A Reverse Command to BOT should then be given to properly locate the cartridge.

Using of Reset during power fail restart situation: When power restart occurs the reset line should be held true until power is stable. Appropriate action can then be taken depending on the cartridge tape position before the power failure occurred.

3-2-8 COMMAND-STATUS INTERLOCK

The command status interlock circuitry utilizes the four unique locations on the tape which are determined by the punched holes on the DC100A Cartridge. See Figure 2-8. These positions are Beginning of Tape (BOT), Load Point (LP), Early Warning (EW), and End of Tape (EOT). The photosense and direction control logic use these tape positions to generate the two drive status indications BOT and RDY. In the Forward direction, RDY is true between (LP) and (EW). At (EW) in the forward direction RDY will go false. Drive motion in the forward direction can continue until (EOT) is sensed. At (EOT) all forward motion is inhibited and any attempt to command forward motion at (EOT) is ignored. In the reverse direction, RDY is true between (EW) and (LP). At BOT, RDY will go false and BOT will go true. When BOT is true all reverse motion is inhibited and any attempt to command reverse motion is ignored. The forward and reverse commands are captured by the run command flip flop (IC2). This flip flop is conditioned by the F/R input and is clocked by the run input. The output of this flip flop controls the mode of the 4 bit bidirectional shift register. (i.e. In forward the status bit is shifted to the right, in reverse the status bit is shifted to the left.)

The forward and reverse lines to the servo (IC11 pin 6 is forward, IC6 pin 4 is reverse) are controlled by the command flip flop and are gated by the appropriate status

signals to produce proper tape motion. (This gating mainly takes place in IC12).

Forward = (Forward Command · (PC1 ·PC2 + 7 ms one shot) · RUN · EOT · INIT)

Reverse = (Reverse Command · (PC1 · PC2 + 7ms one shot) · RUN · BOT)

The two one shots (IC1) are used for determining whether the photosensors are detecting the status holes in the tape or sensing whether the tape has run off the end in the cartridge. This is accomplished by the 7 ms and 15 ms timing. IC10 is an initialization flip flop. It sets on COT, which blocks all forward motion, resets on BOT or RST.

3-2-9 SERVO ELECTRONICS

The servo electronics consists of Reference Amplifier, Back EMF Amplifier, Switch Select, Switches, Error Amplifiers, and Drive Amplifiers. The Reference Amplifier provides speed reference voltage and proper voltage waveform for acceleration and deceleration on command from the Motion Control circuitry. The Back EMF Amplifier accepts the motor speed information from the motor bridge and provides output voltage level proportional to the motor speed. The Error Amplifiers, one and two, compare voltage levels from the reference and back EMF Amplifiers and provides output voltage levels proportionate to the difference between them. The Switch Select compares voltage levels from Error Amplifiers one and two and determines which Error Amplifier is on and sets the appropriate two stage transistor switch to the On position. Only one switch is on according to the comparison. The Driver Amplifiers one and two are two stage transistor amplifiers series regulator drivers which are driven by the Error Amplifiers. The output of these amplifiers drive the motor. The switches provide the complete path to ground.

3-2-10 WRITE CIRCUITRY

The Write Enable Section accepts the READ/WRITE Control signal from the Drive Select Logic (IC17, pin 13). If the READ/WRITE Control signal is low, drive is provided at the base of Q1 to drive it into conduction and write current is provided at the head center tap from the emitter of Q1. Collector voltage is provided through the normally open contact of the Write Protect switch; therefore, head current can flow only if the cartridge slide switch is in the record position, regardless of the status of the READ/WRITE control input.

The Write Enable section also inverts the READ/WRITE Control input (IC16, pin 12) and uses this signal to enable

the READ DATA output (IC13, pin 6) only if the READ/WRITE Control input is high.

The Write Head Driver section consists of two "AND" gates, which are enabled if the write mode is selected.

One gate is provided with the WRITE DATA and the other with WRITE DATA. The output of those two gates (IC11, pin 11, IC11, pin 3) are then routed to the open collector drivers (IC17, pin 9 and pin 11) which drive the tape head.

3-2-11 READ CIRCUITRY

The Read Amplifier section accepts the low level read data from the tape head and amplifies this signal to a nominal 2.0 V P-P level (IC18, pin 6).

This amplified data is then clipped at a 28 percent level by the threshold detector (IC19, pin 14) to remove any background noise from the signal.

The peak detector senses peaks in the amplified signal and produces a TTL compatible reproduction of the data (IC19, pin 1).

Table 3-1. Connector Pin Assignments Servo Electronics and READ/WRITE Amplifier PC Assembly C01 Connector

SIGNAL	ABBREVIATION USED ON SCHEMATIC	PIN
Beginning of Tape	BOT	1
Ready	RDY	3
Read Data	RD	5
Run	Run	7
Stop	STP	9
Read/Write Control	RWC	11
Write Data	WD	13
Forward/Reverse	F/R	15
Reset	RST	17
Enable Drive 0	EN0	19
Enable Drive 1	EN1	21
Enable Drive 2	EN2	23
Enable Drive 3	EN3	25
Ground	GND	2-26

Table 3-2. Connector Pin Assignments Servo Electronics and READ/WRITE Amplifier PC Assembly J1A J1B Photocell Connector

SIGNAL	ABBREVIATION USED ON SCHEMATIC	PIN
Photocell 2	PC2	2
Photocell 1	PC1	4
Cartridge IN	CIN	3
File Protect	FP	5
Ground	GND	1
+12V Endsense	+12V	9
Key	Key	7
+5V	+5V	6
Write Protect	WP	10
Cartridge	COT	8

Table 3-3. Connector Pin Assignments Servo Electronics and READ/WRITE Amplifier PC Assembly J2 Head Connector

SIGNAL	ABBREVIATION USED ON SCHEMATIC	PIN
Center Tap	CT	3
Head	HD	5
Head	HD	1
Shield	SHLD	4
Key	Key	2

Table 3-4. Connector Pin Assignments Servo Electronics and READ/WRITE Amplifier PC Assembly J3 Display Connector

SIGNAL	ABBREVIATION USED ON SCHEMATIC	PIN
Select	Select	1
+5 VDC	+5 VDC	2
File Protect	File Protect	3
Ground	GND	4
Ready	Ready	5

**Table 3-5. Connector Pin Assignments
Servo Electronics and R/W Amplifier PC Assembly
J4A J4B Test Point Connector**

SIGNAL	ABBREVIATION USED ON SCHEMATIC	PIN
Ground	TP1	1
Reference Amp Output	TP2	2
Read Amp Output	TP3	3
Back EMF Amp Output	TP4	4
Fwd Driver Amp Output	TP5	5
Rev. Driver Amp Output	TP6	6
Motor Bridge Output	TP7	7
Motor Bridge Output	TP8	8

**Table 3-6. Connector Pin Assignments
Servo Electronics and R/W Amplifier PC Assembly
J5 Motor Connector**

SIGNAL	ABBREVIATION USED ON SCHEMATIC	PIN
Motor	MTR	4
Motor	MTR	5
Shield	SHLD	2
Sensing Coil	SENS	3
Key	Key	1

3-2-12 MAINTENANCE
See Figure 3-6

3-2-12-1 Motor Control Alignment Procedure
Motor Balance Adjustment

(a) Connect Motor cable to motor and motion control PC Board connector (J5).

(b) The following test fixture should be constructed to properly balance the Servo Bridge.

(c) The motor must be locked while balancing the Servo Bridge. This may be accomplished by inserting a cartridge into the deck.

(d) With the test fixture applied to test points adjust R71 balance pot to obtain zero volts on the VTVM readout (±0.5 mv should be easily achieved). Rotate the motor shaft to insure balance is not at high resistance point. Remove power from the circuit board while making this adjustment.

*Either of two types of Drive motors may be used on this drive. Measure the dc resistance of the motor to determine the correct parallel resistor. Measure between TP6 and TP7. For Motors having 3.6 ohms dc resistance use 120 ohms 1/4w resistor. For Motors having 2.4 ohms dc resistance use a 80 ohm resistor to achieve proper balance.

The Servo Null Pot (R69) and the Motor Speed Adjust Pot (R70) will require adjusting whenever components are changed in the Reference or Back EMF Amplifiers. Whenever these adjustments are made, they should be made *after* the motor balance adjustment has been made.

Reference Amplifier Null Adjust

1. Connect a VTVM or digital voltmeter between test points TP2 and TP4, at J4 on the motion control board.

2. Adjust R69 for zero volts (±5 mv) while the servo system is operational. Whenever the Null R69 is adjusted, the speed adjustment should be checked.

The speed of the motor may be measured by using a speed cartridge 3M Number 80-9200-0169-1 and a counter. Adjust R70 to give 24 KHz at pin 5 on the CO1 connector. Another method is to use a stop watch to time the length of the READY status output, while running a cartridge from BOT to EOT. 56 seconds is the proper time interval.
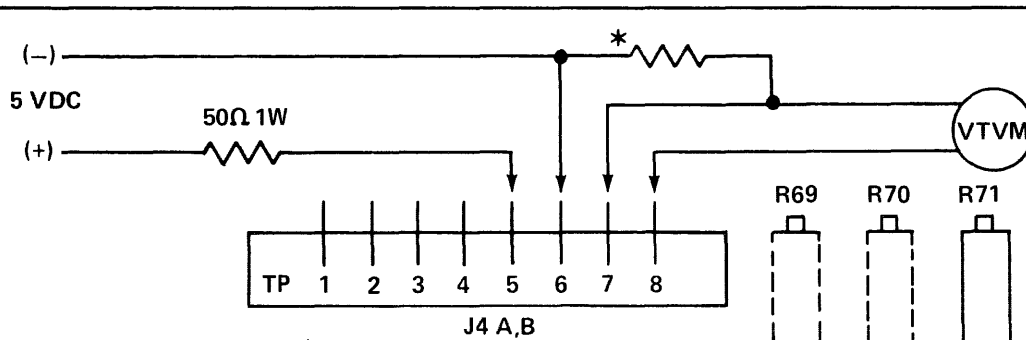

Figure 3-6. Motion Control R/W Amp Circuit Board, Test Points and Adjustment Potentiometers
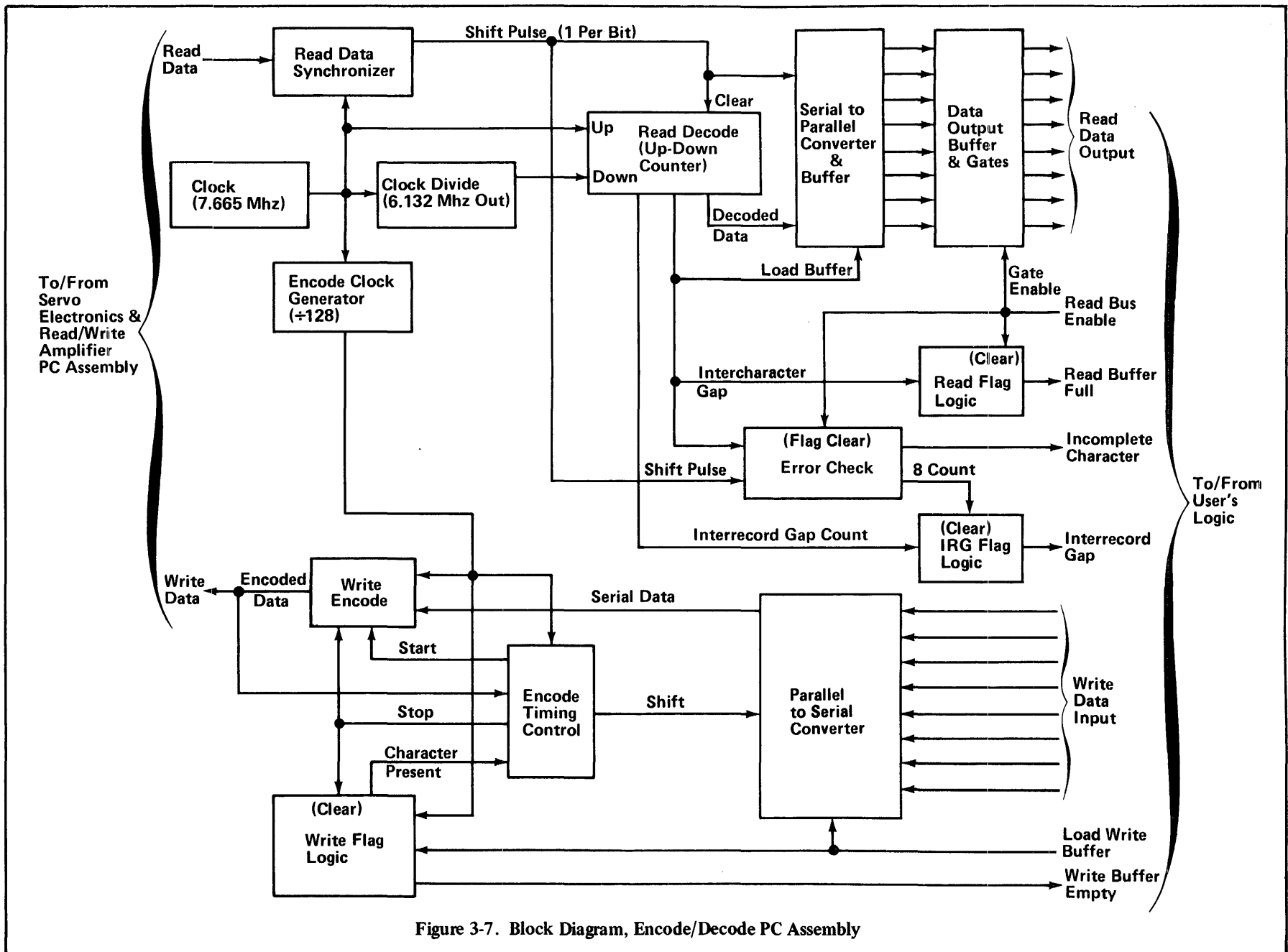
Figure 3-7. Block Diagram, Encode/Decode PC Assembly

Table 3-7. Interface Pin Assignments
C02 on Encode/Decode PC Assembly

FUNCTION	SYMBOL USED ON SCHEMATIC	PIN
Data 0	DATA 0	36
Data 1	DATA 1	38
Data 2	DATA 2	44
Data 3	DATA 3	46
Data 4	DATA 4	42
Data 5	DATA 5	40
Data 6	DATA 6	50
Data 7	DATA 7	48
Read Bus Enable	RDBEN	18
Interrecord Gap	IRG	24
Write Buffer Enable	WBE	22
Load Write Buffer	LWRTE	4
Read Buffer Full	RBF	28
Incomplete Character	ICC	26
Ready	RDY	20
Beginning of Tape	BOT	30
Reset	RST	14
Forward/Reverse	F/R	12
Run	RUN	2
Stop	STP	16
Read Write Control	RWC	10
Select 0	SEL-0	6
Select 1	SEL-1	8

3-3   ENCODE/DECODE PC ASSEMBLY

3-3-1   DESCRIPTION
See Figure 3-7

The Encode/Decode PC Assembly provides a serial byte oriented (eight bit parallel) data interface for the user. During write operations the assembly accepts bytes to be written and converts these bytes to a serial bit stream in Variable Cell Width format (described in paragraph 3-3-2) for use by the Read/Write Amplifier PC Assembly.

During read operations, the assembly accepts data from the Read/Write Amplifier PC Assembly in a TTL compatible, Variable Cell Width format and decodes this information into an eight bit byte (high for a "Zero", low for a "One") for output to the user.

Further, the assembly contains an Interrecord Gap Detector and Error Detector with associated output flags.

Also, the assembly contains a Select Decode function which allows one Encode/Decode Assembly to operate with up to

four Read/Write Amplifier Assemblies. The assembly also contains 220/330 ohm input line terminators and line drivers for all user input/output signals. See Figure 2-6.

3-3-2   VARIABLE CELL WIDTH RECORDING

Variable cell width recording derives its name from the fact that a given bit cell varies in width according to whether a "1" or a "0" is being recorded. As shown in Figure 3-8, a bit cell consists of two pulses, a timing pulse of length t followed by a data pulse of length t if the bit is a "0" or length 2t if the bit is a "1".
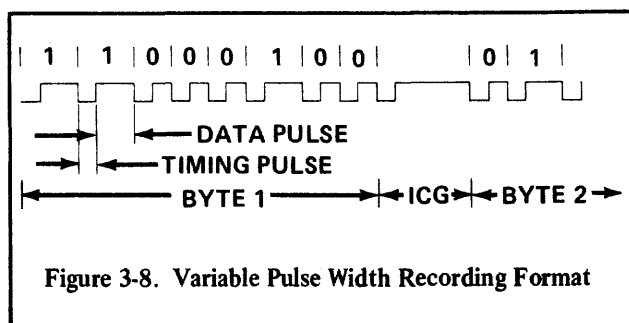

Figure 3-8. Variable Pulse Width Recording Format

When writing data, the length of the timing and data pulses is derived from a crystal oscillator. Implementation of the read decode function is as follows:

1. When the first transition of the timing pulse occurs, a counter is cleared and begins counting in a positive direction at frequency f (7.665 mHz).

2. At the next transition, which ends the timing pulse, the counter begins counting in a negative direction at frequency 0.8f (6.132 mHz).

3. At the final transition of the bit cell, the counter contents are sampled. Since counting in the negative direction is accomplished at a lower frequency when counting up, the counter will contain a positive number if the recorded bit was a "0" and a negative number if the recorded bit was a "1".

This encode/decode technique can tolerate a total speed variation of ±20% in the drive mechanism without causing subsequent read errors or impairing the ability to interchange data between drives.

As shown in Figure 3-8, each stream of recorded data ends with a timing pulse so that this encode/decode technique may permit read reverse operation. Although read reverse is

not implemented in the DCD-1, the presence of this final pulse permits a form of error checking. During write operation, the DCD-1 generates an intercharacter gap after each 8 bits; this gap has a length 4 times that of a timing pulse. During read operations, the counter contents are monitored and when the negative count indicates a data pulse of at least 2-1/2 times the length of the timing pulse, an intercharacter gap is indicated. At this point the number of decoded bits in the output register is sensed. If less than 8 bits are present the incomplete character flag is set to indicate the presence of a read error to the user. Reading may continue, however, as the decode function is resynchronized after each intercharacter gap. If the negative count indicates a data pulse of at least 6-1/4 times the length of a timing pulse, the interrecord gap flag is set.

Table 3-8. Connector Pin Assignments Encode/Decode PC Assembly

C01 SIGNAL	SYMBOL USED ON SCHEMATIC	PIN
Write Data	WD	13
Read Data	RD	5
Ready	RDY	3
Reset	RST	17
Forward/Reverse	F/R	15
Run	RUN	7
Stop	STP	9
Read Write Control	RWC	11
Encode 0	EN0	19
Encode 1	EN1	21
Encode 2	EN2	23
Encode 3	EN3	25
Ground	GND	2-26

Table 3-9. Power Connector Pin Assignments Encode/Decode PC Assembly

J1 SIGNAL	SYMBOL USED ON SCHEMATIC	PIN
+5 VDC	+5 VDC	3
Ground	GND	2 & 4

The maximum packing density used by the DCD-1 is 2000 frpi (a byte consisting of 8 "0's"); however, because of the nature of variable cell width recording, further discussion of cartridge capacity and drive data transfer rate is required. The following tables show these characteristics as a function of recorded data.

Table 3-10. Cartridge Capacity as a Function of Data (256 Bytes/Block, 1 Inch IRG)

DATA	CAPACITY
All Zeroes	116,480 Bytes
All Ones	91,136 Bytes
50% Zeroes, 50% Ones	102,400 Bytes

Table 3-11. Drive Transfer Rate as a Function of Data (30 ips Tape Speed)

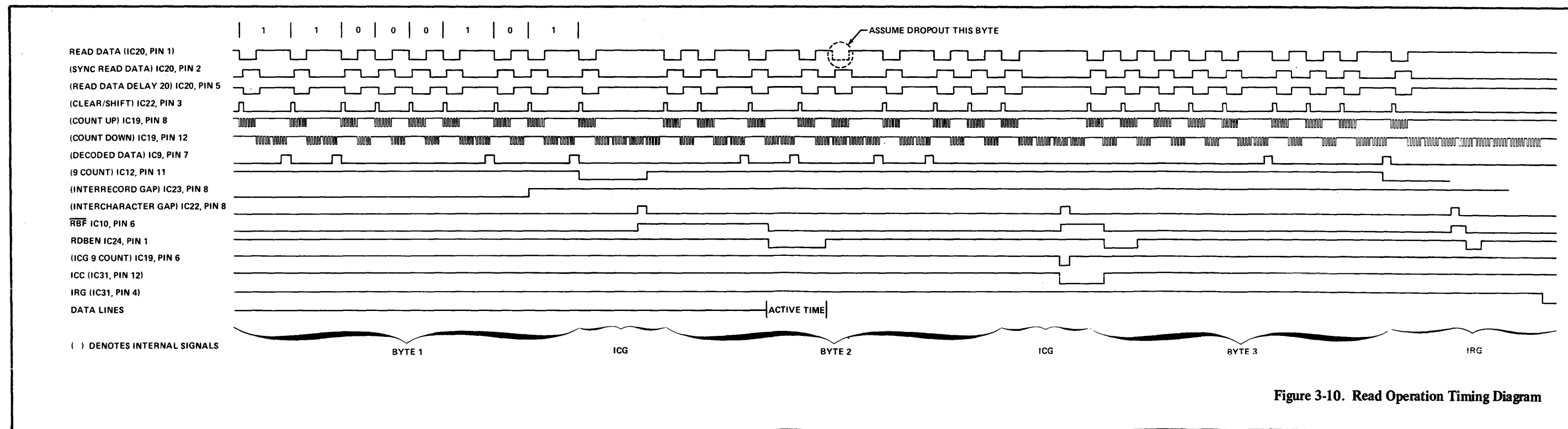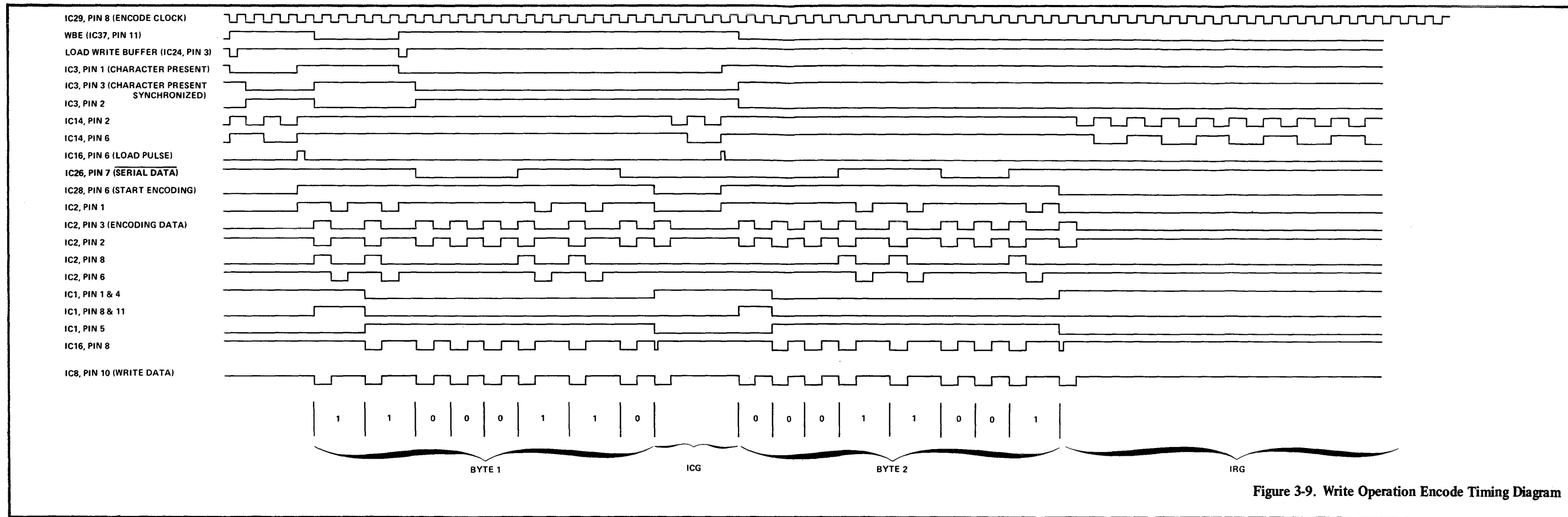| DATA	TRANSFER RATE
All Zeroes	2857 Bytes/Sec.
All Ones	2069 Bytes/Sec.
50% Zeroes, 50% Ones	2400 Bytes/Sec.

3-3-3 OPERATION (Refer to Fold Out Schematic, (Figure 4-7)

The encode/decode PC assembly operates as described below. A write operations timing diagram (Figure 3-9) and a read operations timing diagram (Figure 3-10) are included to aid the reader.

3-3-3-1 WRITE ENCODE

1. When the WRITE BUFFER EMPTY output flag is low the user places an 8 bit byte (high for a "Zero" bit, low for a "One") on the input and applies a low going pulse on the LOAD WRITE BUFFER input (IC24, pin 3).

2. This pulse is inverted (IC24, pin 4) and is used to strobe the input byte into a buffer register (IC36). The same pulse is inverted again and used as an input to (IC16) the write buffer empty set reset latch, causing the output pin 3 to go low. This low level causes the WRITE BUFFER EMPTY output (IC37, pin 11) to go high and applies a low level to the J input of flip flop IC3.

3. On the next clock transition, the Q and $\overline{Q}$ outputs of the flip flop (IC3, pins 3 and 2, respectively), change state. The resultant low level on pin 3 is used (IC37, pin 12) to insure that the WRITE BUFFER EMPTY output remains high. The resultant high level on $\overline{Q}$ (IC3, pin 2) is used as a gate enable at IC16, pin 4.

Figure 3-9. Write Operation Encode Timing Diagram

Figure 3-10. Read Operation Timing Diagram

4. Up to this point, IC14 has been a free running counter whose output was used to generate a short duration pulse at IC15, pin 6 every four clock periods. When IC3, pin 2 goes high, this pulse is gated through IC16 giving pin 6 a short duration low going pulse. This pulse clears IC27 and QD (IC27, pin 11) goes low, disabling the free running counter (IC14). The pulse at IC16, pin 6 is also used as a latch reset for IC16, pin 2 and as the load input enable for the parallel to serial shift register (IC26). The input data in the buffer (IC36) is thus loaded into the shift register (IC26). One clock period after the pulse occurs at IC16, pin 6, IC3, pin 3 goes high and the WRITE BUFFER EMPTY output is enabled at IC37, pin 13.

5. When IC27 is cleared, its low output at pin 11 is in-inverted at IC28, pin 6. This high level is used as a gate enable at IC15, pin 2 and at IC17, pin 1 to start the encode function.

6. When the encode circuit is enabled, IC2, pin 3 is low and IC2, pin 6 is high. This latter signal is fed back to IC2, pin 1 via an AND gate (IC15, pin 11). One clock period later, the flip flop output (IC2, pin 3) changes state to the high level. If a "Zero" is to be written, IC26, pin 7 will be low. This level is inputted to IC17, pin 13. The resultant high output is inverted at (IC28, pin 8) and the J input to the JK flip flop (IC2, pin 8) is held low and IC2, pin 6 remains high. The resultant high input to IC2, pin 3 causes IC2, pin 3 to change state once each clock period. This signal is inverted (IC28, pin 10) to form the Variable Cell Width Recording pattern for a "Zero" as described in Paragraph 3-3-2.

If a "One" is to be recorded IC26, pin 7 will be high and the state of IC2, pin 8 will correspond to the level output at IC2, pin 3. In this instance, when IC2, pin 3 goes high, IC2, pin 8 also goes high. This causes IC2, pin 6 to switch low after one clock period. Because during the first clock period (starting from IC26, pin 7 switching high) IC2, pin 6 (and consequently IC2, pin 1) is high, IC2, pin 3 also switches low at the end of the first clock period according to the rules of operation for a J-K flip flop.

This low level is applied to IC2, pin 8 and consequently IC2, pin 6 returns high at the end of the second clock period. Since IC2, pin 1 is low during second clock period, IC2, pin 3 does not switch at the end of the clock period 2 but remains low. The high input at IC2, pin 1 during clock period 3 causes IC2, pin 3 to switch low at the end of the third period. The signal at IC2, pin 3 is inverted at IC28, pin 10 to form the variable Cell Width Recording pattern

for a "One" as described in Paragraph 3-3-2. This signal is low for one clock period then switches high for 2 clock periods before switching low again.

7. The compliment of the signal at IC2, pin 3 (IC2, pin 2) is routed to a shift enable circuit consisting of IC1 (Dual J-K flip flop) and NAND gate IC16 (pin 8). At the second low going transition on IC2, pin 2 (which occurs at the end of the first data bit) IC1, pin 5 goes high to enable the NAND gate at pin 10, IC16. The low level occurring at IC1, pin 6 is fed back to IC1, pins 1 and 4 to prevent further flip flop operation as a result of changes in logic state at IC2, pin 2. Thereafter, each time IC2, pin 3 goes high, a low level occurs at IC16, pin 8. The low going excursions occurring at IC16, pin 8 are used to step the 8 bit counter, IC27, and to shift excessive bits out of the parallel to serial shift register (IC26).

8. After eight low going transitions (IC16, pin 8) the counter output (IC27, pin 11) goes high. This high level allows the counter comprised of the dual JK flip flop, IC14, to count at the clock rate. Every four clock periods IC14, pin 6 switches high and a high going pulse is produced at IC15, pin 6. If during writing of a given byte, a second byte is entered into buffer register IC36, IC15, pin 4 will have been set high and the pulse at IC15, pin 6 will be gated through to IC16, pin 6. The low pulse at IC16, pin 6 causes operation to begin on the second input byte, commencing at step 4 above. The four clock period delay generates the required intercharacter gap between successive bytes. If another byte had not been entered during writing of the previous byte, IC16, pin 4 will remain low, no further operation will be initiated and the WRITE DATA output to the Read/Write Amplifier PC Assembly will remain at the high logic state as required during an interrecord gap.

3-3-3-2 READ OPERATIONS

1. The READ DATA input from the read amplifier is applied to the read data Synchronizer (IC20, pin 1). Its compliment is applied to IC20, pin 4. The synchronizer circuit generates a positive going pulse (IC22, pin 3) for each low going transition on the READ DATA input line. This circuit further interlocks transitions of the READ DATA input to the output of the crystal clock so that subsequent read decode functions occur in proper timing sequence.

2. The high going pulse at IC22, pin 3 clears the read decode counters (IC's 7, 8, and 9 (all outputs go

low)); it pulses the shift input of serial to parallel converter (IC25, pin 8); and the low going trailing edge of the pulse steps the 9 bit counter (IC13, pin 14) of the Error Check Logic circuit.

3. When the first low going transition on the READ DATA input is shifted through the synchronizer, IC20, pin 2 goes high and the 7.665 MHz clock is enabled at IC18, pin 8. This clock output, when enabled, is applied to the count up input of the up-down counters of the read decode circuit. The counters then count up at the clock frequency until the READ DATA input returns high.

4. When READ DATA returns high, IC20, pin 3 goes high and the output of the clock divide circuit (IC15, pin 8) is enabled (IC19, pin 12). The clock divide circuit creates a low level (IC17, pin 8) every fifth period of the clock. This low level is applied to IC15, pin 10 to prevent every fifth clock pulse from appearing at IC15, pin 8. The net result is that the clock used at the count down input of the up-down counters contains, per unit time, 0.8 the number of clock transitions as the count up clock input.

5. During the timing pulse of a data bit, as described in Paragraph 3-3-2, the up-down counters (IC's 7, 8, and 9) will be counting up at the clock frequency. When the READ DATA input returns high at the end of the timing pulse, the counters will begin to count down at a rate which is 0.8 that of count up operation. At the end of the data pulse, when READ DATA switches low, counter output (IC9, pin 7) is inverted and strobed into the serial to parallel register (IC25, pins 1 and 2) by the pulse generated at IC22, pin 3. This pulse also resets the counters.

If the input bit to be decoded was a "Zero" the timing pulse and data pulse would be of the same length as described in Paragraph 3-3-2. In this instance, the contents of the counters would be positive at the end of the data pulse and IC9, pin 7 would be at a low logic level. If the input bit was a "One", the data pulse would be twice as long as the timing pulse; at the end of the data pulse, the counter would contain a negative number and IC9, pin 7 would output a high level.

6. When the ninth high going pulse occurs at IC22, pin 3, both the 2^0 and 2^3 output bits of counter IC13 in the error check circuit go high. The high level at the 2^3 output (pin 11) resets the interrecord gap latch and IC23, pin 8 goes high. This high level enables gates at the inputs to the latches for the READ BUFFER FULL and INCOMPLETE CHARACTER flags.

Since these latches are not enabled until the first full byte is read, immunity to interrecord noise is provided and precludes noise from appearing as data on the Read Data bus.

7. The ninth pulse at IC22, pin 3 occurs at the start of the intercharacter gap, a timing pulse followed by a data pulse which is 4 times the length of the timing pulse. When IC's 7, 8 and 9 reach a count of -128 (all counter outputs are high except for a low on IC8, pin 7) a low level appears at NAND gate IC21, pin 8 which in turn, creates a high level at IC22, pin 8. This high level causes buffer register (IC33) to be loaded with the contents of serial to parallel shift register. It also sets the read flag latch causing IC10, pin 6 to go high; this level is inverted to form the low going READ BUFFER FULL output.

If the counter (IC13) had not reached a count of 9 (eight bits were not present in the byte) when the intercharacter gap is sensed IC22, pin 8 goes high (as assumed in byte 2 of Figure 3-4), a low level is generated at IC19, pin 6. This low level sets the error flag SET/RESET latch and IC10, pin 8 goes high. This level is inverted at IC31, pin 12 to form the INCOMPLETE CHARACTER output flag. Sensing the intercharacter gap (high level at IC22, pin 8) also causes a high going pulse to occur at IC12, pin 6. This pulse clears the 9 bit counter (IC13) of the error circuit.

8. If the timing pulse in 7 above is at the end of a record, the counters, IC's 7, 8 and 9 will continue in a negative direction. When a count of -512 occurs (all counter outputs are high except for a low on IC9, pin 2), a low level occurs on IC23, pin 3 which sets the interrecord gap latch and IC23, pin 6 goes high. This level is inverted at IC31, pin 4 to form the low going INTERRECORD GAP, output. The low output at IC23, pin 3 also disables the clock inputs to the up down counters at IC19, pin 2 and at IC19, pin 9.

9. After the READ BUFFER FULL output goes low, the user must apply a low going pulse of at least 50 nanoseconds duration to the READ BUS ENABLE input. This pulse enables the tri-state data output gates (IC's 32 and 34) and resets the read flag and error flag latches.

3-3-4 INTERRECORD GAP TIME CONSIDERATIONS

To insure the writing of proper length interrecord gaps, the following delays should be used.

1. After commanding forward tape movement, delay 27 milliseconds before entering the first data byte.

2. After writing (or reading) the last data byte, delay 5 milliseconds before commanding a stop.

3-3-5 WRITE FLAG TIMING

When writing data, the following timing restrictions must be considered:

1. When the first byte of data is strobed in, WRITE BUFFER EMPTY will go low again within from 16.67 microseconds to 83.5 microseconds, depending on internal logic timing.

2. The LOAD WRITE BUFFER input must be a pulse of at least 50 nanoseconds but no greater than 1.5 microseconds. The LOAD WRITE BUFFER input must occur no sooner than 4 microseconds but prior

to 340 microseconds after WRITE BUFFER EMPTY goes low.

3-3-6 READ FLAG TIMING

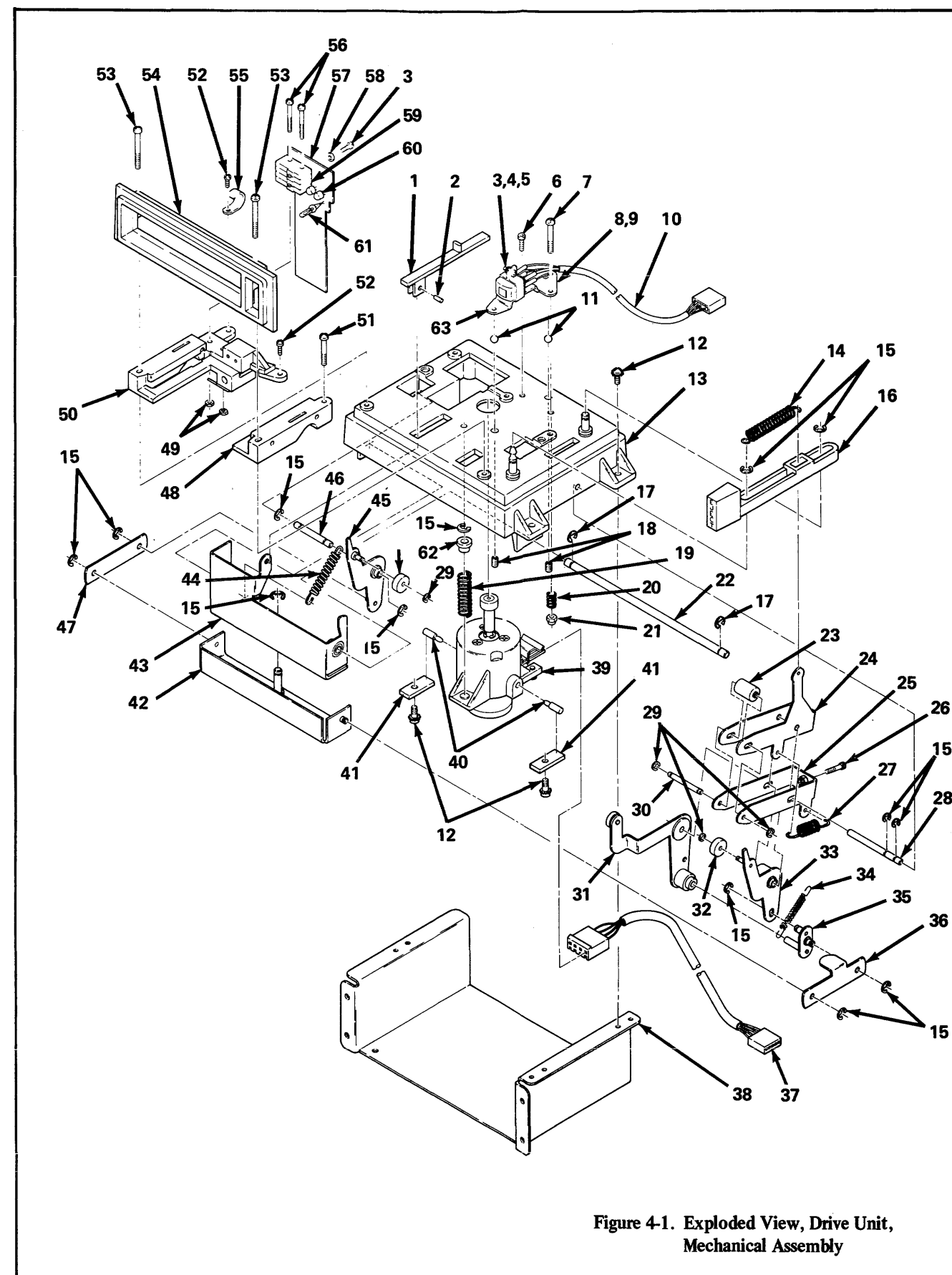When reading data, the following timing restrictions must be considered:

1. After the first byte is decoded, subsequent bytes will occur on the average, every 350 microseconds.

2. The READ BUS ENABLE input must be held true for at least 50 nanoseconds for valid data to appear on the data bus. This input must occur no sooner than 20 nanoseconds after READ BUFFER FULL goes low. READ BUS ENABLE should return high within 200 microseconds of READ BUFFER FULL going low.

NOTES

	Parts List, DCD-1 Mechanism Assembly		
INDEX NUMBER	PART NUMBER	DESCRIPTION	QTY.
1	81-1530-9670-6	Ejector Slide	1
2	81-0930-9770-7	Spiral Pin — 3/32 DIA x 3/16 L	1
3	83-9260-4501-0	Screw — Mach., Pan Hd., 2-56 x 3/16	2
4	83-9261-4201-5	Washer — Lock, Flat, Int. Tooth, #2	1
5	83-9260-2001-3	Nut — Hex, Plain 2-56 x .188 WD	1
6	83-9261-2132-4	Screw — Cap, Skt. Hd., 4-40 x 5/16	1
7	83-9260-4507-7	Screw — Mach., Pan Hd., 2-56 x .625	1
8	81-2716-1860-5	Head — Single Track R/W	1
9	81-1630-9870-0	Head Insulating Tape	1
10	83-0003-0970-4	Cable Assy. Head	1
11	81-0934-3480-1	Ball — Azimuth Adjust	2
12	81-1432-6660-9	Screw 6-32 x 5/16 Pan Head	5
13	83-0003-0993-6	Mechanism Base Assy.	1
14	81-1330-9880-6	Spring — Eject Release Slide	1
15	83-7270-0878-7	Ring — Retng., Ext., .113 Free Dia.	13
16	81-0150-0008-6	Eject Button Assy.	1
17	81-0930-9540-4	Ring — Retaining, Reinforced E	2
18	83-9261-0071-6	Setscrew — Cup Pt., 8-32 x 3/8	2
19	81-1330-9720-4	Motor Spring	1
20	81-1332-1000-5	Spring — Azimuth	1
21	81-0934-4680-5	Nut — Stop, 2-56	1
22	81-0430-9620-5	Whiffle Tree Shaft	1
23	81-0430-9790-6	Roller — Detent Lock Arm	1
24	81-0330-9440-0	Release Rocker Arm	1
25	83-0003-0985-2	Detent Lock Arm Assy.	1
26	83-9261-2003-7	Screw — Cap, Skt. Hd., 4-40 x 1/2	1
27	81-1317-7120-6	Spring Bank Item	1
28	81-0430-9750-0	Shaft — Right Lock Arm	1
29	83-7270-0876-1	Ring — Retng., Ext., .072 Free Dia.	4
30	81-0430-9780-7	Shaft — Detent Lock Arm	1
31	83-0003-0988-6	Rear Lock Arm Assy.	1
32	81-0430-9570-2	Roller	2
33	83-0003-0987-8	Right Lock Arm Assy.	1
34	81-1330-9930-9	Spring — Rear Lock Arm	1
35	83-0003-0984-5	Right Lock Cross Bar Assy.	1
36	81-0330-9830-2	Link Right Lock Arm	1
37	83-0003-0969-6	Cable Assy. Motor	1
38	81-0330-9480-6	Bottom Cover	1
39	83-0003-0994-4	Motor Assy.	1
40	81-0430-9550-4	Motor Pivot Shaft	2
41	81-0334-3350-9	Retainer — Motor Pivot	2
42	83-0003-0990-2	Transfer Bracket Assy.	1
43	83-0003-0989-4	Transfer Pivot Bkt. Assy.	1
44	81-1330-9900-2	Return Spring — Transfer Bkt.	1
45	83-0003-0986-0	Left Lock Arm Assy.	1
46	81-0430-9760-9	Shaft — Left Lock Arm	1
47	81-0330-9400-4	Link — Lock Arm	1
48	83-0003-0992-8	Right Guide Rail Assy.	1
49	83-9260-2001-3	Nut — Mach. Screw Hex 2-56	2
50	83-0003-0991-0	Left Guide Rail Assy.	1
51	83-9260-4519-2	Screw — Mach., Pan Hd., 4-40 x 5/8	1

INDEX NUMBER	PART NUMBER	DESCRIPTION	QTY.
52	83-9260-4514-3	Screw — Pan Hd., 4-40 x 5/16	2
53	83-9260-4522-6	Screw — Mach., Pan Hd., 4-40 x 1	2
54	81-1530-9640-9	Front Bezel	1
55	83-9630-0085-2	Lug	1
56	81-1434-4820-7	Screw — Pan Hd., 2-56 x 3/4	2
57	83-4930-3905-7	End Sense Assembly (includes item 50)	1
58	81-0884-2440-8	Washer #4 Plastic	1
59	83-1550-6166-2	Switch — Snap Action	2
60	81-2712-7041-5	TSTR — SI NPN Photo Sens FPT100A	2
61	81-2712-1310-0	Lamp — 2.5V Lens End TS1748	1
62	81-0430-9520-7	Washer — Shoulder	1
63	83-0003-1016-5	Head Clamp Assy.	1

Table title: Parts List, DCD-1 Mechanism Assembly (Cont.)

Figure 4-1. Exploded View, Drive Unit,
Mechanical Assembly
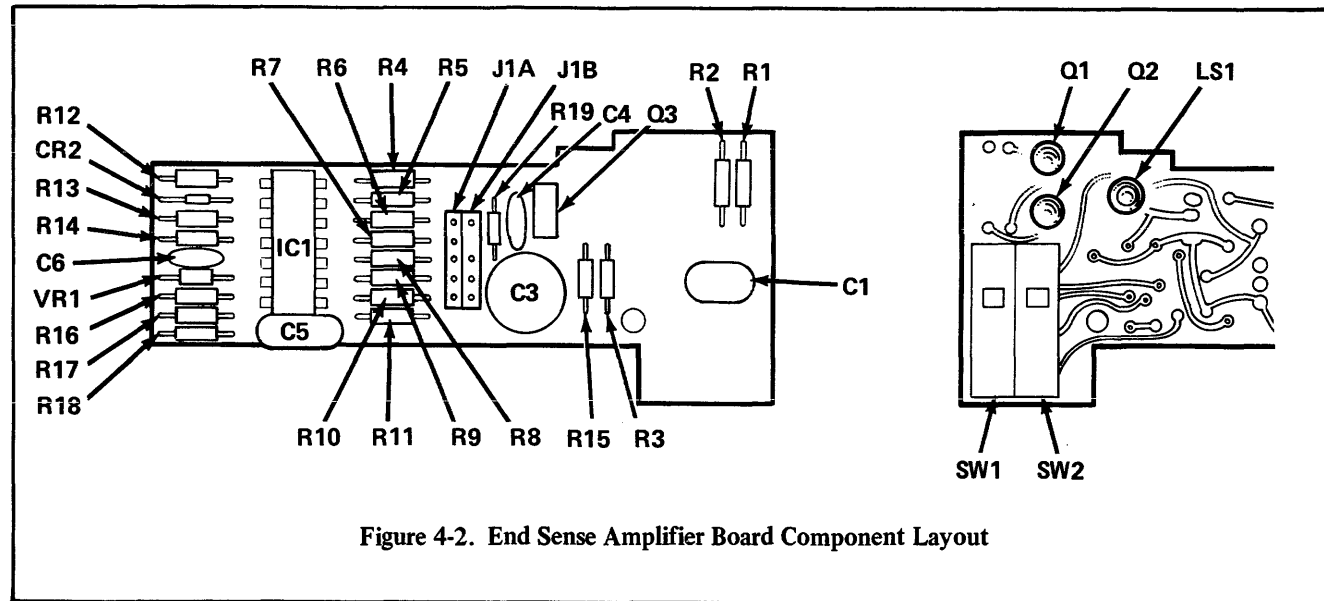
Figure 4-2. End Sense Amplifier Board Component Layout

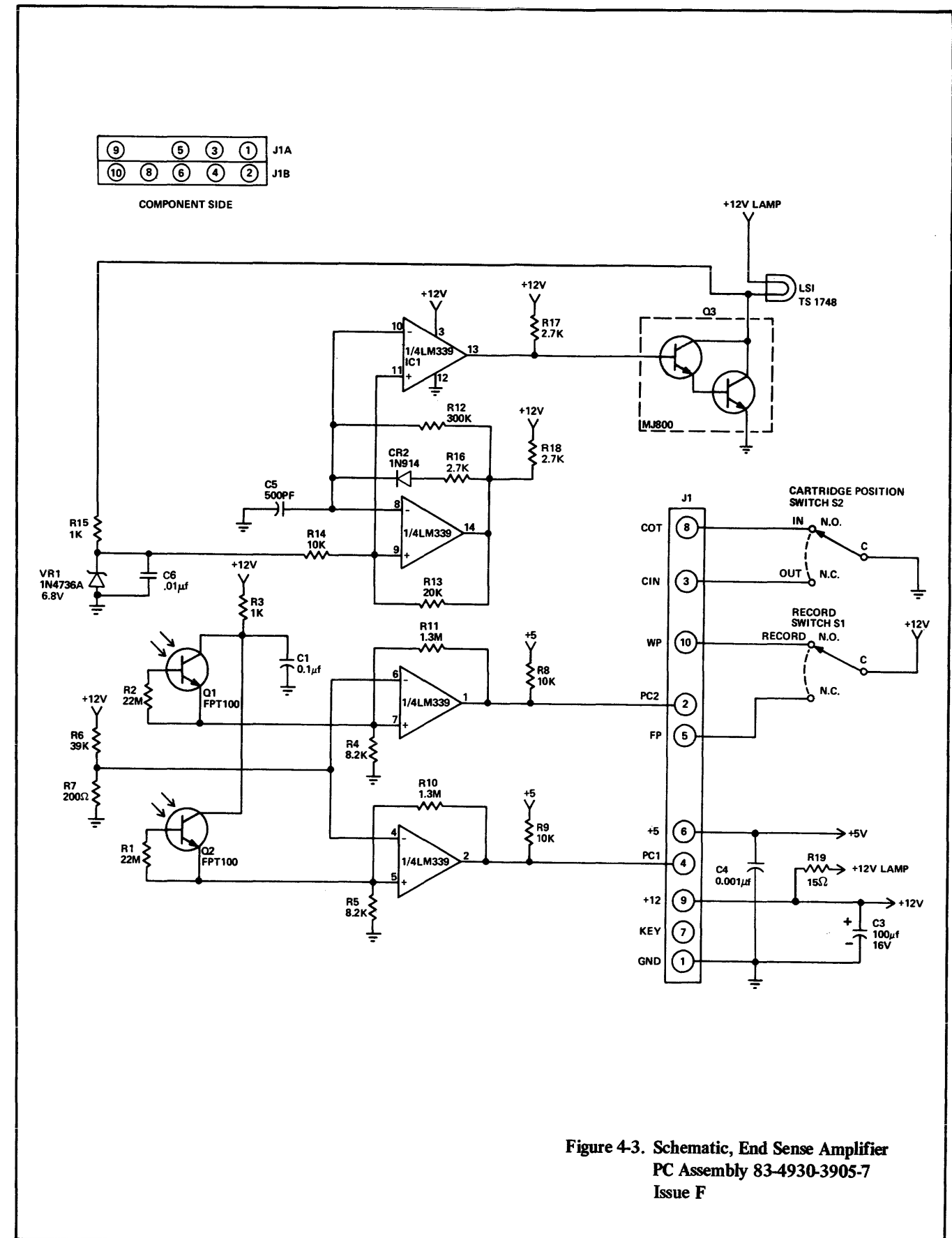| Parts List, End Sense Amplifier PC Assembly, 83-4930-3905-7, Issue F			
INDEX NUMBER	PART NUMBER	DESCRIPTION	QTY.
C1	83-1510-4648-5	Capacitor – Fixed, Film, 1 UF 100V 10%	1
C3	83-1510-2354-2	Capacitor – Fixed, Elc, 100 UF 16V	1
C4	83-1510-1024-2	Capacitor – Fixed, Ceramic, 1000 PF 1000V 10%	1
C5	83-1510-5120-4	Capacitor – Fixed, Mic, 500 PF 500V 5%	1
C6	81-1510-1075-4	Capacitor – Fixed Ceramic, .01 UF 10V	1
CR2	83-1530-0083-7	Diode – SI Switching 1N914	1
IC1	83-1530-8307-2	IC – Quad Comp LM339N	1
J1A, 1B	83-1610-1912-6	Connector – 5 Contact	2
LS1	81-2712-1310-0	Lamp – 2.5V Lens End TS1748	1
Q1, Q2	81-2712-7041-5	Transistor – SI, NPN Photo-Sens FPT100A	2
Q3	83-1530-2434-0	Transistor – SI, NPN Power-Darl MJE800	1
R1, 2	83-9520-2223-0	Resistor – Fixed, Comp, 22M Ohm 1/4W 5%	2
R3, 15	83-9520-2088-7	Resistor – Fixed, Comp, 1K Ohm 1/4W 5%	2
R4, 5	83-9520-2089-5	Resistor – Fixed, Comp, 8.2K Ohm 1/4W 5%	2
R6	83-9520-2167-9	Resistor – Fixed, Comp, 39K Ohm 1/4W 5%	1
R7	83-9520-2132-3	Resistor – Fixed, Comp, 200 Ohm 1/4W 5%	1
R8, 9, 14,	83-9520-2112-5	Resistor – Fixed, Comp, 10K Ohm 1/4W 5%	4
R10, 11	83-9520-2195-0	Resistor – Fixed, Comp, 1.3M Ohm 1/4W 5%	1
R12	83-9520-2182-8	Resistor – Fixed, Comp, 300K Ohm 1/4W 5%	1
R13	83-9520-2162-0	Resistor – Fixed, Comp, 20K Ohm 1/4W 5%	1
R16, 17, 18	83-9520-2098-6	Resistor – Fixed, Comp, 2.7K Ohm 1/4W 5%	3
R19	83-9520-2238-8	Resistor – Fixed, Comp, 150 Ohm 1/4W 5%	1
SW1, 2	83-1550-6166-2	Switch – Snap Action	2
VR1	83-1530-0465-6	Diode – SI Zener 6.8V	1
Not shown	83-0003-0991-0	Guide Rail, Left, Assy	1
	83-9260-4501-0	Screw Pan Head 2-56 x 3/16	1
	81-1434-4820-7	Screw Pan Head 2-56 x 3/4	2
	83-9620-2001-3	Nut Mach, Screw Hex 2-56	2
	81-0884-2440-8	Washer #4	1

Figure 4-3. Schematic, End Sense Amplifier
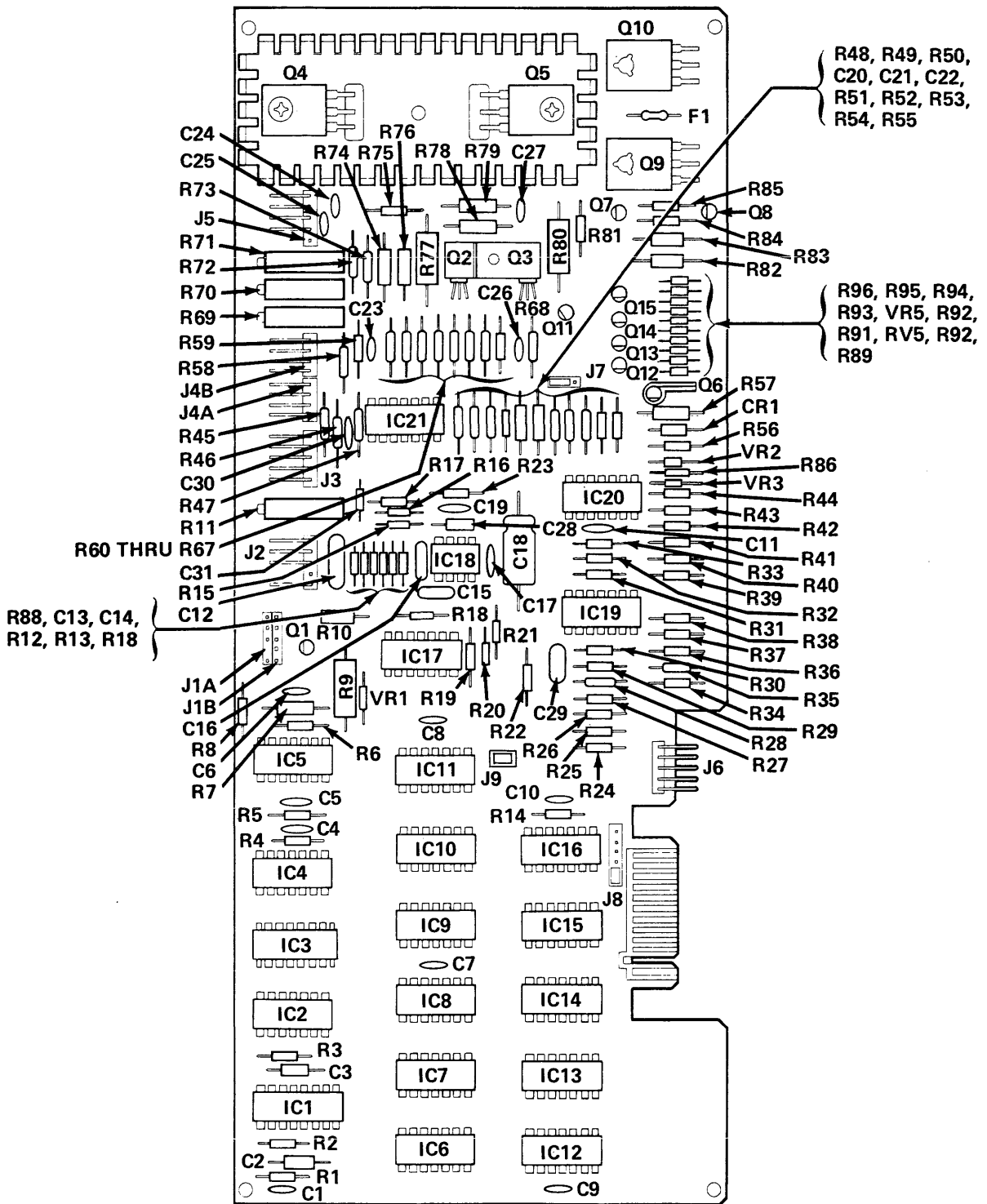PC Assembly 83-4930-3905-7
Issue F

Figure 4-4. Servo Electronics and Read/Write Amplifier Board Component Layout

Parts List, Servo Electronics and Read/Write Amplifier PC Assembly 83-4930-3904-0, Issue F			
INDEX NUMBER	PART NUMBER	DESCRIPTION	QTY.
C1, 6-10	83-1510-2307-0	Capacitor – Fixed, Ceramic, .05 UF 10V	6
C2	83-1510-6415-7	Capacitor – Fixed, Tan, 2.2UF 35V 10%	1
C3, 28	83-1510-6413-2	Capacitor – Fixed, Tan, 1.0 UF 35V 10%	2
C4, 5, 11	83-1510-1024-2	Capacitor – Fixed, Ceramic, 1000 PF 1000V 10%	3
C12	83-1510-5108-9	Capacitor – Fixed, Mic, 2000 PF 500V 10%	1
C13, 14	83-1510-1187-7	Capacitor – Fixed, Ceramic, .1 UF 50V	2
C15	83-1510-5164-2	Capacitor – Fixed, Mic, 150 PF 500V 5%	1
C16	83-1510-5263-2	Capacitor – Fixed, Mic, 2 PF 500V	1
C17, 19, 30	83-1510-1075-4	Capacitor – Fixed, Ceramic, .01 UF 50V	3
C18	83-1510-2355-9	Capacitor – Fixed, Elc, 100 UF 16V	1
C20	83-1510-6411-6	Capacitor – Fixed, Tan, .47 UF 35V 10%	1
C21, 22	83-1510-6126-0	Capacitor – Fixed, Tan, .18 UF 35V 10%	2
C23-27	83-1510-4649-3	Capacitor – Fixed, Film, .01 UF 100V 10%	5
C29	83-1510-5028-9	Capacitor – Fixed, Mic, 470 PF 500V 10%	1
C31	83-1510-1151-3	Capacitor – Fixed, Ceramic, .01 UF 10%	1
CR1	83-1530-0151-2	Diode – Rectifier 1N4004	1
F1	83-7550-8159-9	Fuse – 2 Amp, Microfuse	1
HS1	81-0930-9710-3	Heat Sink	1
IC1	83-1530-8162-1	IC – Dual One Shot SN74123N	1
IC2	83-1530-8163-9	IC – Dual J-K SN74107N	1
IC3	83-1530-8171-2	IC – Shaft Req SN74194N	1
IC4, 6, 16	83-1530-8142-3	IC – Hex Inverter SN7404N	3
IC5, 7	83-1530-8060-7	IC – Quad 2 Input NAND SN7400N	2
IC8, 12	83-1530-8069-8	IC – Dual 4 Input NAND SN7420N	2
IC9, 10	83-1530-8143-1	IC – Tri 3 Input NANDD SN7410N	2
IC11	83-1530-8168-8	IC – Quad 2 Input AND SN7408N	1
IC13, 15	83-1530-8333-8	IC – Quad 2 Input OR SN7432N	2
IC14	83-1530-8356-9	IC – Hex, Tri-State SN74125N	1
IC17, 20	83-1530-8174-6	IC – Hex, Inverter Buf SN7406N	2
IC18	83-1530-8358-5	IC – Op Amp 8 Pin Dip SN72748P	1
IC19	83-1530-8307-2	IC – Quad Comp LM339N	1
IC21	78-8032-2739-2	IC – Quad Op Amp LM324N	1
J1A, 1B	83-1610-1912-6	Connector – 5 Circuit	2
J2, 3, 5, 6	83-1610-1913-4	Connector – 5 Circuit	4
J4A, 4B	83-1610-1914-2	Connector – 4 Circuit	2
J7	83-1610-1915-9	Connector – 3 Circuit	1
J8	83-1610-1916-7	Connector – 6 Circuit	1
J9	81-2817-4620-6	Connector – 2 Circuit	1
P1, 2	83-1610-1907-6	Plug – Jumper	2
Q1, 7, 8, 12 13, 14, 15	81-2712-5290-0	Transistor – SI, NPN Low Power 2N3416	7
Q2, 3, 6	81-2712-5530-9	Transistor – SI, NPN 7553A	5
Q4, 5	83-1530-2424-1	Transistor – SI, PNP High Power MJE2955	2
Q9, 10	83-1530-2425-8	Transistor – SI, NPN High Power MJE3055	2
Q11	83-1530-2155-1	Transistor – SI, PNP Low Power 2N3638A	1
R1, 3	83-9520-2164-6	Resistor, Fixed, Cmp, 24K Ohm 1/4W 5%	2
R2, 8, 14, 19 24, 44, 54, 55, 59, 67	83-9520-2088-7	Resistor – Fixed, Cmp, 1K Ohm 1/4W 5%	10
R4	83-9520-2099-4	Resistor – Fixed, Cmp, 82 Ohm 1/4W 5%	1
R5, 86	83-9520-2107-5	Resistor – Fixed, Cmp, 180 Ohm 1/4W 5%	2

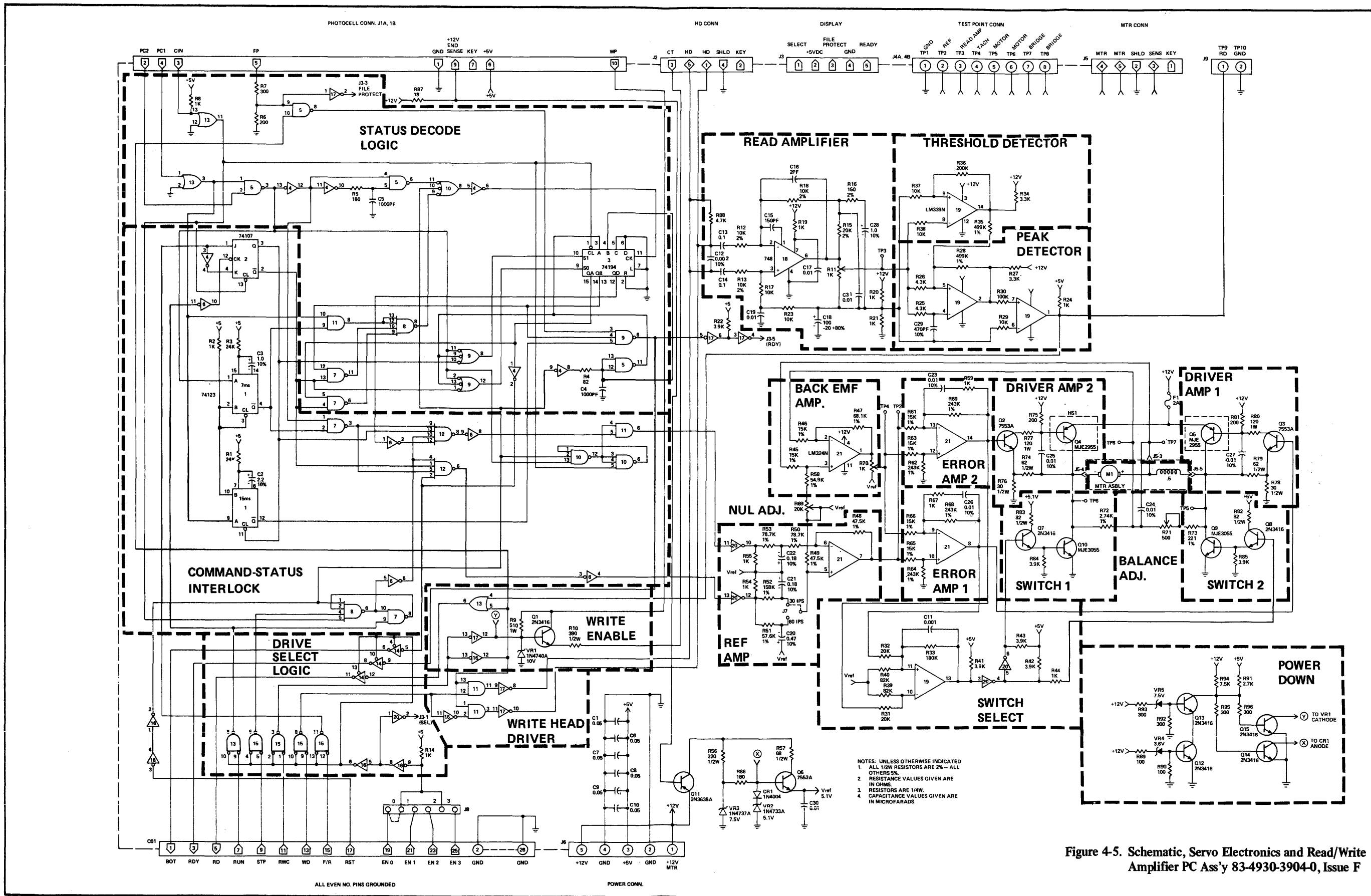|	Parts List, Servo Electronics and Read/Write Amplifier PC Assembly (Cont.)		
INDEX NUMBER	PART NUMBER	DESCRIPTION	QTY.
R6, 75, 81	83-9520-2132-3	Resistor — Fixed, Cmp, 200 Ohm 1/4W 5%	3
R7	81-1520-7349-6	Resistor — Fixed, Film, 300 Ohm 1/2W 2%	1
R9	83-9520-4144-6	Resistor — Fixed, Cmp, 510 Ohm 1W 5%	1
R10	83-1520-7174-8	Resistor — Fixed, Film, 390 Ohm 1/2W 2%	1
R11, 70	83-1520-1574-5	Resistor — Variable, Ceramic, 1K Ohm	2
R12, 13, 18	83-1520-7308-2	Resistor — Fixed, Film, 10K Ohm 1/4W 2%	3
R15	83-1520-7259-7	Resistor — Fixed, Film, 20K Ohm 1/4W 2%	1
R16	83-1520-0356-8	Resistor — Fixed, Film, 150 Ohm 1/4W 2%	1
R17, 23, 29 37, 38	83-9520-2112-5	Resistor — Fixed, Cmp, 10K Ohm 1/4W 5%	5
R20, 21	83-1520-7282-9	Resistor — Fixed, Film, 1K Ohm 1/4W 2%	2
R22, 41-43, 84, 85	83-9520-2096-0	Resistor — Fixed, Cmp, 3.9K Ohm 1/4W 5%	6
R25, 26	83-9520-2152-1	Resistor — Fixed, Cmp, 4.3K Ohm 1/4W 5%	2
R27, 34	83-9520-2095-2	Resistor — Fixed, Cmp, 3.3K Ohm 1/4W 5%	2
R28, 35	83-1520-0500-1	Resistor — Fixed, Film, 499K Ohm 1/4W 1%	2
R30	83-9520-2119-0	Resistor — Fixed, Cmp, 100K Ohm 1/4W 5%	1
R31, 32	83-9520-2162-0	Resistor — Fixed, Cmp, 20K Ohm 1/4W 5%	2
R33	83-9520-2179-4	Resistor — Fixed, Cmp, 180K Ohm 1/4W 5%	1
R36	83-9520-2180-2	Resistor — Fixed, Cmp, 200K Ohm 1/4W 5%	1
R39, 40	83-9520-2172-9	Resistor — Fixed, Cmp, 82K Ohm 1/4W 5%	2
R45, 46, 61, 63, 65, 66	83-1520-0501-9	Resistor — Fixed, Film, 15K Ohm 1/4W 1%	6
R47	83-1520-0502-7	Resistor — Fixed, Film, 68.1K Ohm 1/4W 1%	1
R48, 49	83-1520-0503-5	Resistor — Fixed, Film, 47.5K Ohm 1/4W 1%	2
R50, 53	83-1520-0504-3	Resistor — Fixed, Film, 78.7K Ohm 1/4W 1%	2
R51	83-1520-0505-0	Resistor — Fixed, Film, 57.6K Ohm 1/4W 5%	1
R52	83-1520-0506-8	Resistor — Fixed, Film, 158K Ohm 1/4W 1%	1
R56	83-1520-7220-9	Resistor — Fixed, Film, 220 Ohm 1/2W 2%	1
R57	83-1520-7340-5	Resistor — Fixed, Film, 68 Ohm 1/2W 2%	1
R58	83-1520-0507-6	Resistor — Fixed, Film, 54.9K Ohm 1/4W 1%	1
R60, 62, 64, 68	83-1520-0508-4	Resistor — Fixed, Film, 243K Ohm 1/4W 1%	4
R69	83-1520-1568-7	Resistor — Variable, Ceramic, 20K Ohm	1
R71	83-1520-1573-7	Resistor — Variable, Ceramic, 500 Ohm	1
R72	83-1520-0509-2	Resistor — Fixed, Film, 2.74K Ohm 1/4W 1%	1
R73	83-1520-0510-0	Resistor — Fixed, Film, 221 Ohm 1/4W 1%	1
R74, 79	83-1520-7339-7	Resistor — Fixed, Film, 62 Ohm 1/2W 2%	2
R76, 78	83-1520-7332-2	Resistor — Fixed, Film, 30 Ohm 1/2W 2%	2
R77, 80	83-9520-4132-1	Resistor — Fixed, Cmp, 120 Ohm 1W 5%	2
R82, 83	83-1520-7342-1	Resistor — Fixed, Film, 82 Ohm 1/2W 2%	2
R87	83-9520-2242-0	Resistor — Fixed, Cmp, 18 Ohm 1/4W 5%	1
R88	83-9520-2111-7	Resistor — Fixed, Car, 4.7K 1/4W 5%	1
R89, 90	83-9520-2094-5	Resistor — Fixed, Car, 100 Ohm 1/4W 5%	2
R91	83-9520-2098-6	Resistor — Fixed, Car, 2.7K 1/4W 5%	1
R92, 93, 95, 96	83-9520-2135-6	Resistor — Fixed, Car, 300 Ohm 1/4W 5%	4
R94	83-9520-2156-2	Resistor — Fixed, Car, 7.5K 1/4W 5%	1
VR1	83-1530-0389-8	Diode — Zener 10.0V 1N4708A	1
VR2	83-1530-0377-3	Diode — Zener 5.1V 1N4733A	1
VR3,5	83-1530-0376-5	Diode — Zener 7.5V 1N4737A	2
VR4	83-1530-0428-4	Diode — Zener 3.6V 1N4729A	1

Figure 4-5. Schematic, Servo Electronics and Read/Write
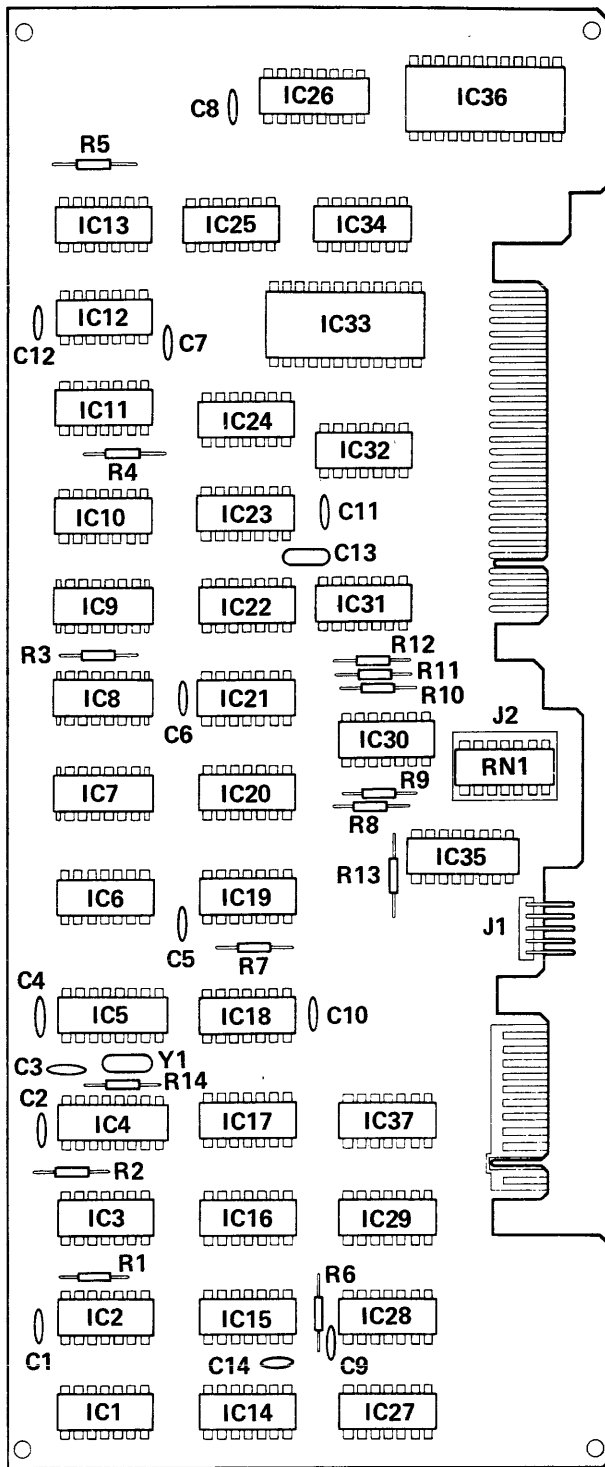Amplifier PC Ass'y 83-4930-3904-0, Issue F

Figure 4-6. Encode/Decode Board Component Layout

INDEX NUMBER	PART NUMBER	DESCRIPTION	QTY.
C1, 2, 6, 8, 10-12	83-1510-2307-0	Capacitor – Fixed, Ceramic, .05 UF 10V	7
C3, 4	83-1510-1077-0	Capacitor – Fixed, Ceramic, .1 UF 10V	2
C5	83-1510-1095-2	Capacitor – Fixed, DSC, 100 PF 1000V 20%	1
C7	83-1510-1158-8	Capacitor – Fixed, Ceramic, 220 PF 1000V 10%	1
C9	83-1510-1151-3	Capacitor – Fixed, Ceramic, .01 UF 200V 10%	1
C13	83-1510-5103-0	Capacitor – Fixed, Mic, 330 PF 500V 5%	1
C14	83-1510-1024-2	Capacitor – Fixed, Ceramic, 1000 PF 1000V 10%	1
IC1-3, 14, 20	83-1530-8163-9	IC – Dual J-K SN74107N	5
IC4	78-8005-8300-3	IC – 4 Bit Synchronizer Counter SN74163N	1
IC5	83-1530-8359-3	IC – Crystal Oscillator MC12061P	1
IC6, 11, 24, 28	83-1530-8142-3	IC – Hex Inverter SN7404N	4
IC7-9	83-1530-8357-7	IC – 4 Bit Synchronizer Counter SN74193N	3
IC10, 12, 16, 23	83-1530-8060-7	IC – Quad 2 Input NAND SN7400N	4
IC13, 18, 27, 29	83-1530-8066-4	IC – 4 Bit Counter SN7493N	4
IC15, 22	83-1530-8168-8	IC – Quad 2 Input AND SN7408N	2
IC17, 19	83-1530-8143-1	IC – Tri 3 Input NAND SN7410N	2
IC21	83-1530-8061-5	IC – 8 Input NAND SN7430N	1
IC25	83-1530-8320-5	IC – Shift Register Parl Out SN74164N	1
IC26	83-1530-8172-0	IC – Shift Register Parl Load SN74165N	1
IC30	83-1530-8271-0	IC – Hex Buffer Driver SN7417N	1
IC31	83-1530-8189-4	IC – Hex Inverter Driver SN7416N	1
IC32, 34	83-1530-8356-9	IC – Quad Tri-State SN74125N	2
IC33, 36	83-1530-8355-1	IC – Latch 8 Bit BSTBL SN74100N	2
IC35	83-1530-8242-1	IC – Decoder Dual 2LN-4LN DM74155N	1
IC37	83-1530-8341-1	IC – Quad 2 Input NAND SN7438N	1
J1	83-1610-1913-4	Connector – 5 Circuit	1
J2	81-2817-4590-1	Socket – 14 Pin Dip	1
R1-3, 5, 8-13	83-9520-2088-7	Resistor – Fixed, Comp, 1K Ohm 1/4W 5%	9
R4, 6, 7	83-9520-2107-5	Resistor – Fixed, Comp, 180 Ohm 1/4W 5%	3
R14	83-9520-2139-8	Resistor – Fixed, Comp, 510 Ohm 1/4W 5%	1
RN1	83-1520-0492-1	Resistor – Fixed, Network, 330/220 Ohm	1
Y1	81-2716-6011-0	Crystal, 7.665 MHz Fund Serial Resistor	1
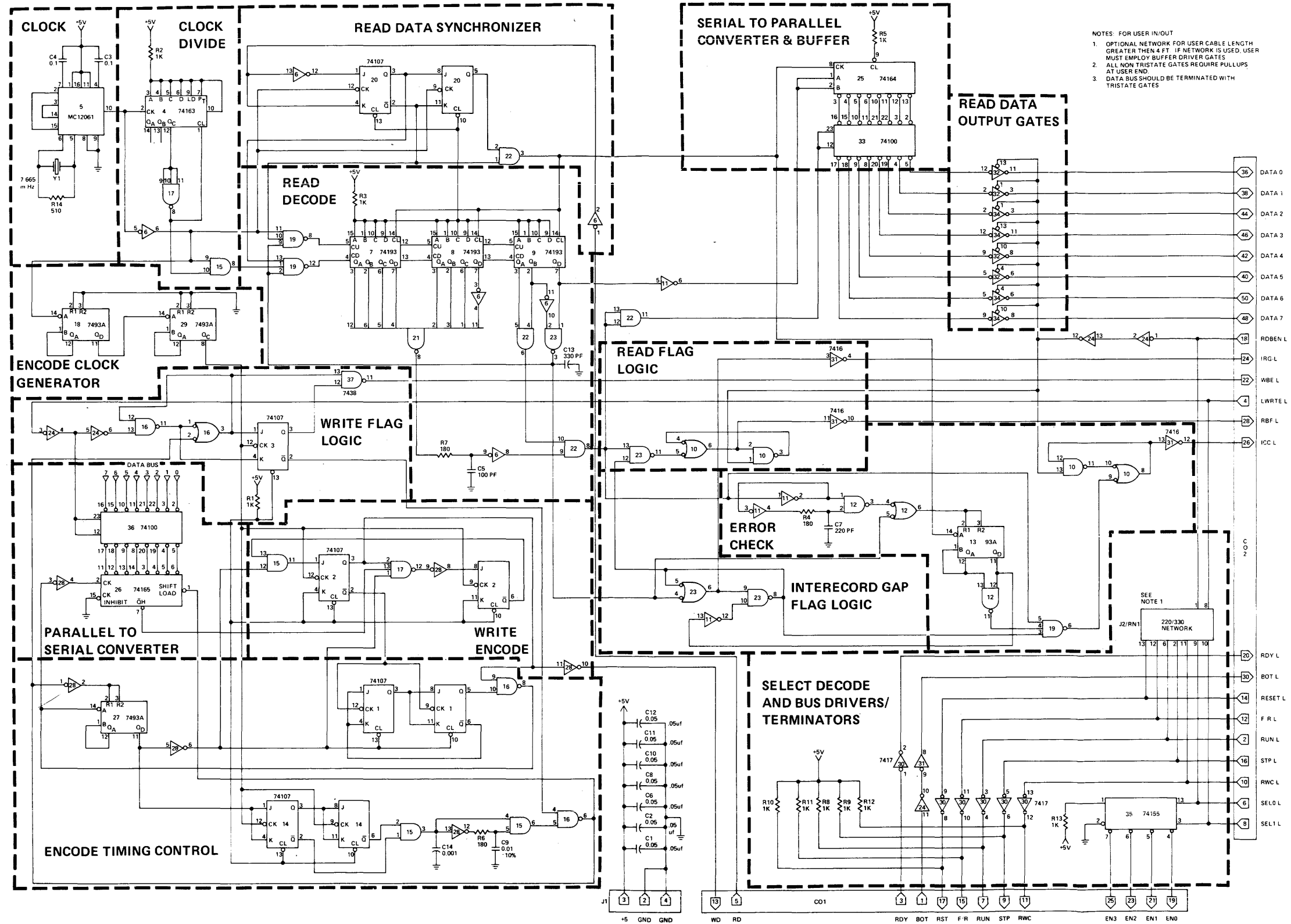
Parts List, Encode/Decode PC Assembly 83-4930-3906-5, Issue C

NOTES

Figure 4-7. Schematic, Encode/Decode PC Assembly
83-4930-3906-5, Issue C

APPENDIX I. WARRANTY

DCD-1 DATA CARTRIDGE DRIVE WARRANTY

MINCOM DIVISION/DATA PRODUCTS, MINNESOTA MINING & MANUFACTURING CO. HEREINAFTER REFERRED TO AS 3M, WARRANTS THE EQUIPMENT COVERED HEREBY TO BE FREE FROM DEFECTS IN MATERIAL AND WORKMANSHIP FOR TWELVE (12) MONTHS FROM DATE OF ORIGINAL SHIPMENT TO PURCHASER. DURING THIS WARRANTY PERIOD 3M WILL REPAIR OR REPLACE DEFECTIVE EQUIP- MENT FOB ITS PLACE OF BUSINESS WITHOUT CHARGE TO PURCHASER.

THIS WARRANTY APPLIES TO DEFECTS ARISING OUT OF NORMAL USE AND SERVICE OF THE EQUIP- MENT AS SPECIFIED BY 3M. THIS WARRANTY DOES NOT COVER ABNORMAL OPERATION OF THE EQUIPMENT, ACCIDENT, ALTERATION, NEGLIGENCE, MISUSE AND REPAIRS OR SERVICING PER- FORMED BY OTHER THAN 3M AUTHORIZED REPRESENTATIVES. PURCHASER SHALL UPON REQUEST BY 3M FURNISH REASONABLE EVIDENCE THAT THE DEFECT AROSE FROM CAUSES PLACING A LIABILITY ON 3M. IF THE DEFECT DID NOT ARISE FROM CAUSES PLACING A LIABILITY ON 3M, PUR- CHASER SHALL REIMBURSE 3M FOR EXPENSES INCURRED IN INSPECTING THE EQUIPMENT AT THE REQUEST OF PURCHASER.

THE OBLIGATION OF 3M UNDER THIS WARRANTY IS LIMITED TO REPAIR OR REPLACEMENT OF THE DEFECTIVE EQUIPMENT AND IS THE ONLY WARRANTY APPLICABLE TO THE EQUIPMENT. 3M SHALL NOT BE LIABLE FOR ANY INJURY, LOSS OR DAMAGE DIRECT OR CONSEQUENTIAL ARISING OUT OF THE USE OF OR INABILITY TO USE THE PRODUCT. NO CHANGES IN THE WARRANTY SHALL BE EFFEC- TIVE WITHOUT THE PRIOR APPROVAL IN WRITING OF BOTH PARTIES. THIS WARRANTY AND THE OBLIGATIONS AND LIABILITIES THEREUNDER SHALL REPLACE ALL WARRANTIES OR GUARANTEES EXPRESS OR IMPLIED ARISING BY LAW OR OTHERWISE.

MW–DCD-1

MINNESOTA MINING AND MANUFACTURING COMPANY