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biomation

MODEL K100-D
DIGITAL LOGIC ANALYZER

OPERATING AND SERVICE MANUAL

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GOULD

An Electrical/Electronics Company

OPERATING AND SERVICE MANUAL

MODEL K100-D

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SECTION I

GENERAL INFORMATION

1.1 Certification

Gould Inc. certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory.

1.2 Warranty

All Gould Inc. products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products that prove to be defective during the warranty period. If a unit fails within thirty days of delivery, Gould Inc. will pay all shipping charges relating to the repair of the unit. Units under warranty, but beyond the thirty day period, should be sent to Gould Inc. prepaid and Gould Inc. will return the unit prepaid. Units out of the one year warranty period, the customer will pay all freight charges. IN THE EVENT OF A BREACH OF GOULD INC.'S WARRANTY, GOULD INC. SHALL HAVE THE RIGHT IN ITS DISCRETION EITHER TO REPLACE OR REPAIR THE DEFECTIVE GOODS OR TO REFUND THE PORTION OF THE PURCHASE PRICE APPLICABLE THERETO. THERE SHALL BE NO OTHER REMEDY FOR BREACH OF THE WARRANTY. IN NO EVENT SHALL GOULD INC. BE LIABLE FOR THE COST OF PROCESSING, LOST PROFITS, INJURY TO GOODWILL, OR ANY SPECIAL OR CONSEQUENTIAL DAMAGES. THE FOREGOING WARRANTY IS EXCLUSIVE OF ALL OTHER WARRANTIES, WHETHER EXPRESSED OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

1.3 Description

The Model K100-D Logic Analyzer was designed to provide the utmost in performance and versatility for the digital designer and troubleshooter; i.e., it can be considered to be a true benchmark tool. It serves as both a time domain (data recorded asynchronously), and a data domain analysis tool (data recorded synchronously). The unit accepts up to 16 logic signals through its active input probes, and stores these discriminated signals in its 1024 word memory, at sample rates to 100 MHz. The unit is depicted in Figure 1.1.

The Model K100-D has comprehensive recording and display analysis capabilities that enable the user to perform complex timing and state analysis of his digital systems. The unit has three distinct features that make it a useful tool for logic troubleshooting.

First, the signals from the user's system are input via specially designed hybrid active probes. The input impedance of each probe is 1 MΩ, 5 pF. The probes are individual to allow spanning to physically separated points in the system, and also to provide for convenient connection at the PC board level. Signal conditioning, or threshold detection, and buffering of a particular signal is provided at a point as close as possible to the user's circuitry. The probe tip, with its accessories, allows convenient connection to a system. The probes detect logic spikes or glitches down to 5 ns regardless of clock rate used.

Second, the instrument can clock at rates to 100 MHz, allowing timing measurements on up to 16 signals, with a 10 ns time resolution. A relatively long memory, 1024 words, allows precise timing measurements over longer intervals of time. The performance of the active probes complement this high-speed recording capability.

Third, the instrument uses a microprocessor linked to a front keyboard for instrument control. Comprehensive display prompting is used to make it easy to set up the unit for desired recording and display formats. This gives a greater degree of flexibility

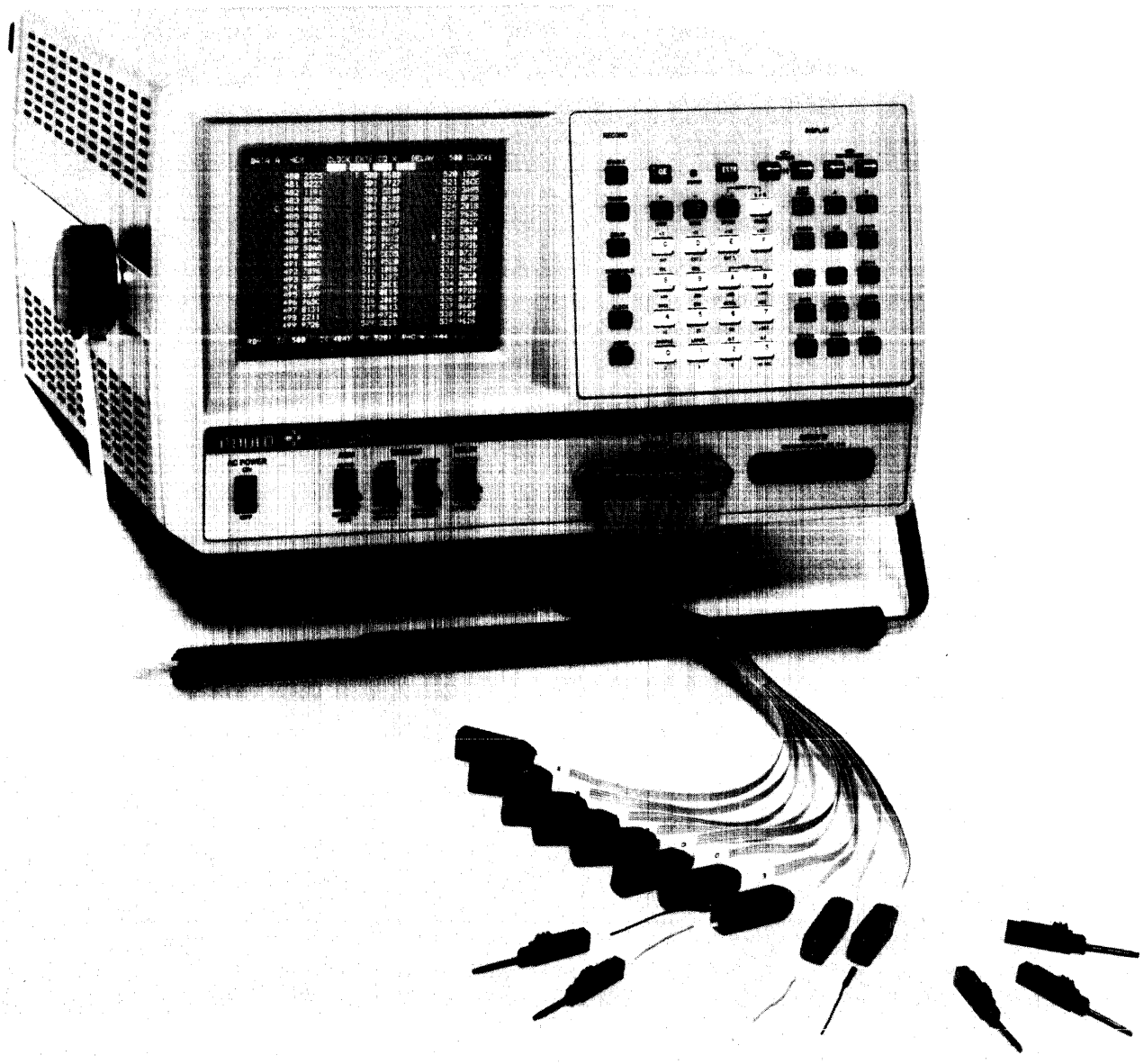


Figure 1.1 The Model K100-D with its high performance active probes.

in recording and display functions than was possible with earlier instruments.

1.4 Specifications

SIGNAL INPUTS

Number. 20, including 16 data, external clock and qualifier, and 2 trigger qualifiers.

Impedance. 1 MΩ, 5 pF, over input range of ±10 V.

Threshold. Each input may be assigned one of four references: TTL (+1.4 V), ECL (-1.3 V), VAR A, VAR B; A & B selectable between -6.4 V and +6.35 V, in 50 mV increments. Thresholds are referenced to probe tip. High or low true logic polarity selectable each channel.

Maximum Voltage. ±50 V continuous, ±100 V transient.

Modes. Each data input selectable Sample or Latch.

SAMPLE. Unit stores the detected logic level present at each active clock transition simultaneously on all inputs. Minimum pulse always detected and stored is one clock period plus 4 ns.

SKEW. Channel to channel, 1 ns typical.

LATCH. Whenever an even number of threshold transitions occur between two successive clock intervals, an input latch stores the state opposite that stored at the previous clock interval on the next clock. The glitch may be stored in one or two memory cells.

MINIMUM DETECTABLE PULSE. 5 ns with threshold overdrive of 25% of total voltage swing, or 250 mV, whichever is greater.

CLOCK

Internal. Selectable from 10 ns (100 MHz) to 50 ms (20 Hz) in a 1-2-5 sequence.

External. Selectable positive or negative edge active, DC-70 MHz rate. Minimum pulse width 5 ns.

SETUP TIME. Data must be present 2 ns before clock active edge.

HOLD TIME. Data must be present 2 ns after active edge.

QUALIFIER. Must go TRUE a minimum of 12 ns before the clock goes TRUE, and go FALSE a minimum of 1 ns after clock goes TRUE; must go FALSE a minimum of 10 ns before clock goes FALSE. See Figure 1.2.

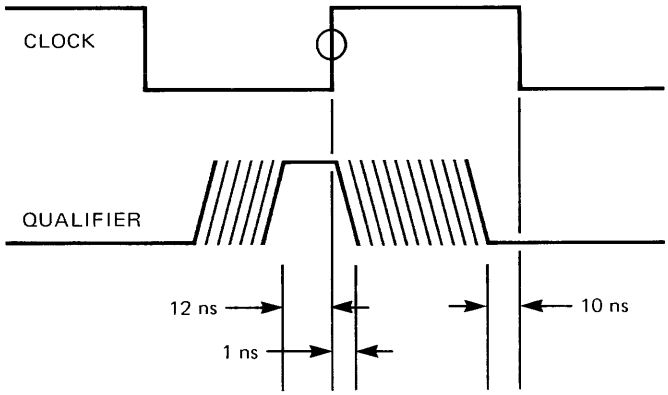


Figure 1.2 K100-D Clock Qualifier.

TRIGGER

Three events control data recording: Arm, Enable and Trigger.

Arm. Selectable Manual (front panel switch), Auto, Auto Stop, Auto Stop with limits.

Enable. Selectable Auto, Manual or Combinational. When Combinational selected, unit will seek a defined word. Once detected, unit will seek the Trigger.

Trigger. Selectable Manual or Combinational. When Combinational selected, unit will seek a defined word. Once detected, unit will execute the trigger delay selected, and stop recording.

Qualifiers. Q1 and Q2 may be applied to

Enable, Trigger, both to each, or one to each.

Pattern Select. Enable and Trigger events may each be specified as an 18-bit word. Unit accepts binary (1, 0, X-don't care), as well as hexadecimal input. Can be selected for a GO TRUE or GO FALSE condition.

Delay. Trigger delay selectable clock intervals or Trigger occurrences (or events) to 65, 530. Delay by clocks is always measured between Trigger event and end of memory. When delaying by events, the nth + 1 event occupies memory location 501.

Filter. Selectable from 1 to 14 clock samples. Enable and Trigger must remain TRUE for the selected number of samples before being recognized.

Trigger Output. Rear panel BNC connector, TTL active high signal when unit detects trigger event. Synchronous with input data.

MEMORY

The K100-D contains three memories: high speed record memory M, storage memory A, and reference memory B.

Size. M, A, and B are each 16 bits wide, 1024 words long.

Use. M accepts new data, and automatically transfers it to A for display. B may be loaded through A and is used as a reference.

Auto Stop. The unit Arms itself and acquires new data in A, which is compared with the contents of B.

Whenever conditions are met, any further recording is prevented. This allows comparison between the contents of A and B. Conditions may be A=B or A≠B.

Comparison may be made over entire 1024 words, or may be limited to the data that lies between the positions of Cursor and Reference, inclusive. Also, only those channels displayed participate in the comparison.

Search. Via Status display, the unit accepts a 16-bit word for which it will search in memory A and/or B. All occurrences are marked by an asterisk. First and last occurrence, and total number of occurrences, are tabulated in Data display.

DISPLAY

Status, Timing, and Data domain displays are via built-in raster scan CRT. User control over order in which channels are displayed.

Status. Permits keyboard selection of recording and display parameters. Each parameter field (reverse video entry) is randomly addressable.

Timing. 16 channel format. Horizontal expansion X5, X10, X20. Vertical expansion X2, X4, via deleting channels. Cursor and Reference permit direct time measurements when using internal clock. Binary readout of data at Cursor or Reference position. Trigger event, if in memory, is marked.

Data. Selectable binary, hexadecimal, octal, or Special display. Decoding depends on user selection of channel order. In Special display, channel grouping permits decoding of data in binary, hexadecimal, octal, or ASCII, or any combination.

Video Output. BNC rear panel connector provides composite video output,2.2V pp into 75 Ω.

MISCELLANEOUS

Size. 21.8 cm (8.6 in) high; 44.6 cm (17.5 in) wide (with bail); 54.5 cm (18.9 in) deep (with bail).

Weight. 19.5 kg (43 lbs), including probes.

Power. 100, 120, 220 or 240 V RMS, ±10%; 400 W.

Temperature Range. 0-50°C, operating.

Warranty. All Gould/Biomation products are warranted against defects in materials and workmanship for one year from date of delivery.

Accessories. Each unit is supplied with a set of input probes (20 inputs) with probe leads and spring hook tips, power cord, and one Operating and Service Manual. Probes are available in 1.2 m (4 ft) or 1.8 m (6 ft) length.

SECTION II

INSTALLATION

2.1 Introduction

This section contains information on unpacking, inspection, repacking, storage, and installation of the Model K100-D.

2.2 Unpacking and Inspection

Inspect instrument for shipping damage as soon as it is unpacked. Check for broken knobs and connectors; inspect cabinet and panel surfaces for dents and scratches. If the instrument is damaged in any way or fails to operate properly, notify the carrier immediately. For assistance of any kind, including help with instruments under warranty, contact your local Gould Inc., Biomation Division, representative or Gould Inc., Biomation Division, in Santa Clara, California, U.S.A.

2.3 Storage and Shipment

To protect valuable electronic equipment during storage or shipment, always use the best packaging methods available. Contract packaging companies in many cities can provide dependable custom packaging on short notice.

2.4 Power Connection

The K100-D may be used on a wide range of power line voltages at frequencies of 50 or 60 Hz nominal. The rear panel contains a fuse holder and a pair of slide switches for selection of nominal power line voltages. Table 2.1 lists these voltages, switch positions, and fuse selection required for that power line voltage. The selected switch positions are referred to as left and right when viewed facing the rear panel.

Table 2.1 Line Voltage/Fuse Selection. Range shown is for 50-60 Hz line frequency.

Range (+10%)	Selector Switch Positions	Fuse-Amp (Slow Blow 3AG)
100	Both in	5
120	Left in, right out	5
220	Left out, right in	2.5
240	Left out, right out	2.5

Figure 2.1 illustrates the power input grouping (voltage change, fuse, and input connector).

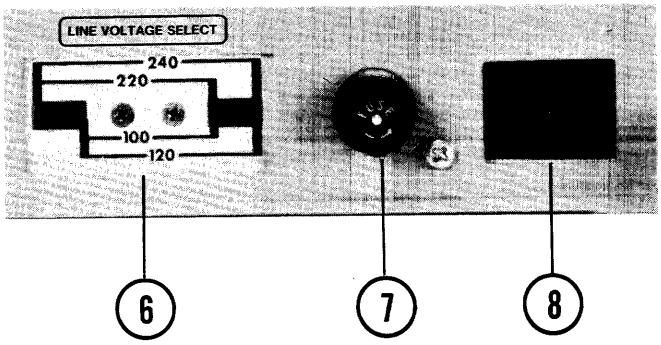


Figure 2.1. Power input grouping. Position the switches (6) as noted in Table 2.1, using the proper fuse.

In addition to selecting the proper line voltage, you must also place a jumper on the MPU printed circuit board, as shown in Figure 2.2, if you operate the unit on 50 Hz line frequency. This changes the refresh rate of the raster scan display to 50 Hz. Operation at 50 Hz may require minor adjustment of R2, the horizontal oscillator frequency control. See Section V Calibration.

2.5 Preparation for Use

The Model K100-D is entirely self contained with a built-in display and integral probe assemblies. All that is required is to connect the instrument to the line power and plug the probe assemblies into the front panel. The unit automatically senses whether it has

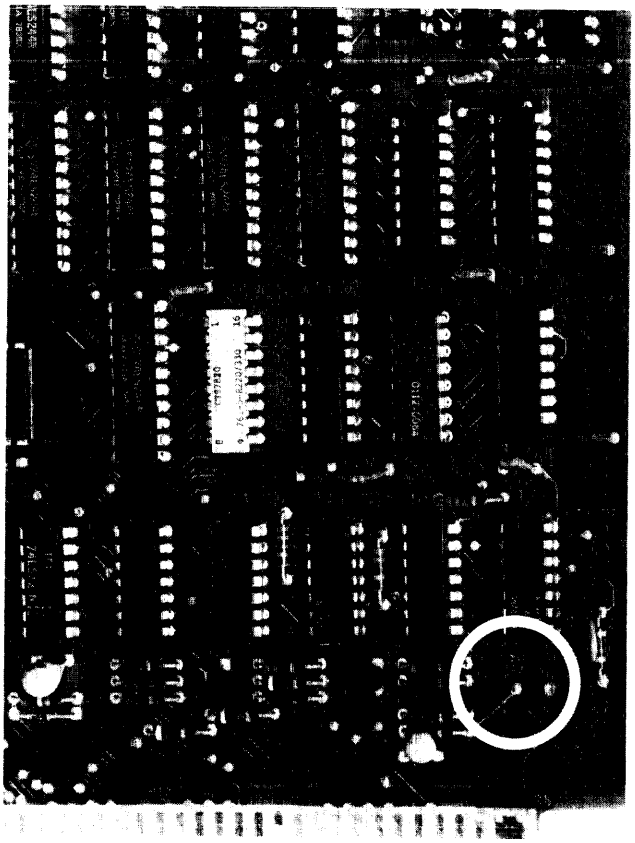


Figure 2.2. To operate the unit on 50 Hz power line frequency, remove the MPU board and install a jumper as shown.

the 16-channel probe assembly or the optional Model K100-D/32 Input Adapter. The status display mode thus displayed is a reflection of the respective input configuration.

When the K100-D is first turned on, it self-programs, allowing you to connect your probes and collect data from your system. Once the data has been collected, you may easily modify the data collection or display to suit your requirements. This operation enhances the self-teaching ability of the instrument, so you can quickly learn how to operate it. For details, refer to Section III Operation.

2.6 Initial Warm-up

Although the Model K100-D is a solid-state instrument, a brief warm-up period of approximately 10 minutes is required for the internal circuitry to reach thermal stability.

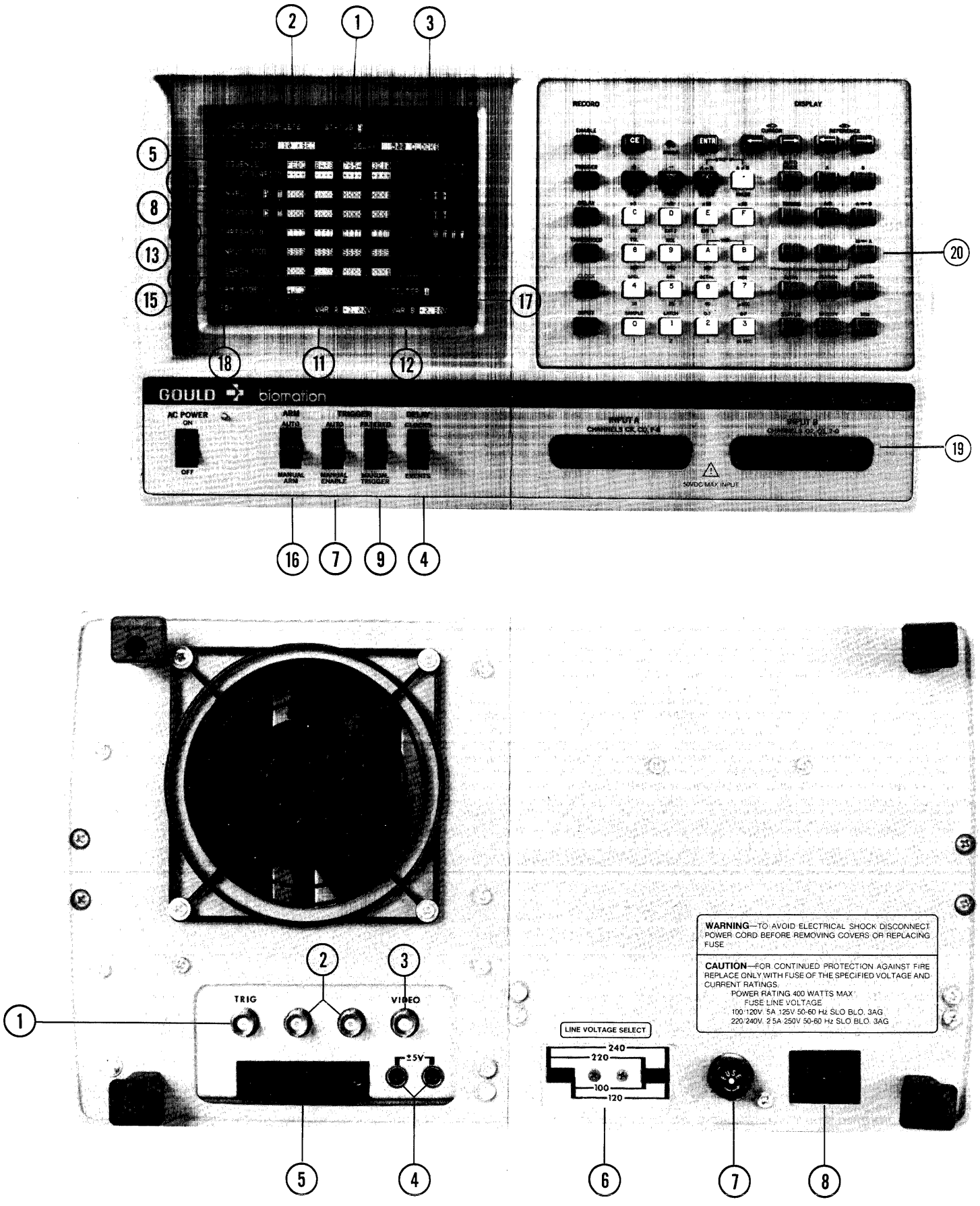


Figure 3.1 Front and rear panels of the K100-D.

SECTION III

OPERATION

3.1 Introduction

This section explains the use and function of the front panel controls and inputs, as well as the rear panel outputs. It also offers you a step-by-step procedure for operating the unit.

3.2 Front Panel Controls and Inputs

Refer to Figure 3.1 while reviewing this section.

The Model K100-D uses a keyboard entry system and interactive display for control of recording and display parameters. The arrangement of this control subsystem was designed to help you learn quickly and easily the effect of various keys, and the proper use of the features available in the instrument. It does this through the use of the Status display mode, shown in Figure 3.1.

When you first power up the K100-D, it goes through a detailed self-diagnostic test, wherein it checks its keyboard and memories. A detailed explanation of the test and its error indications are found in Section VI Maintenance. If the instrument indicates any errors in the power up self test, the source of the error may be diagnosed down to the IC package level using the diagnostic routine. The unit also loads part of its own program into display memory. This allows you to practice specifying display parameters without having to record data.

Once self test is complete, the instrument sets itself into a default condition, as shown in the Status display in Figure 3.1.

Two default parameters can be user specified. There is a DIP switch on the Record Control board; you may cause the power up threshold condition to be either TTL or ECL. In addition, you may select Internal Clock or External Clock Rising Edge Active. See Figure 3.2.

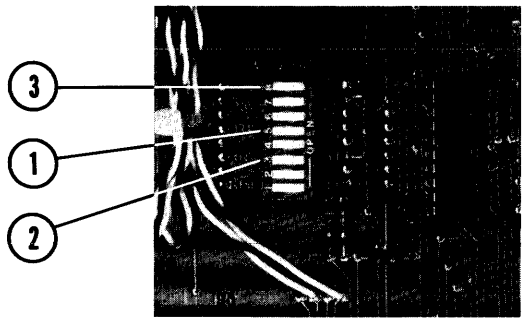


Figure 3.2. On the Record Control PCB (center board in unit), you can preprogram default conditions for threshold (1) and record clock (2). You can also lock out trigger holdoff (3) by turning switch 8 on. See also item (18) regarding status byte CK?

PARAMETER FIELDS

Each reverse video (bright box) entry in the Status mode denotes a "parameter field." Any one of these parameter fields may be randomly addressed and modified. Use the column of black keys on the left edge of the display to access any one of these parameter fields. In addition to the column of black keys, the blue keys labeled SEQ (Sequence) and SEARCH are used in the same fashion to access those respective parameter fields. There are also four momentary toggle switches on the lower front panel that access various parameter fields.

The operation of all keys and switches is covered below.

(1) STATUS W, A, B

STATUS W is the Status display mode shown on the CRT when any parameter field has been addressed or changed. This denotes that you are intending to make a subsequent measurement with different parameters from those used for the last measurement. Once a parameter field has been changed, and a

new measurement (or recording) is made, STATUS W becomes STATUS A.

STATUS A indicates the parameter fields that were used to record and display information that is stored in Memory A. STATUS A display cannot be changed before a measurement has been made.

STATUS B refers to the data stored in Memory B. It is a mnemonic for the data stored, and cannot be changed except by changing the data stored in Memory B. This is done by loading new data into A and transferring to B.

STATUS A or B displays may be called up on the CRT while in the Status mode by pressing the blue keys A or B. STATUS W may be called up by opening any one of the parameter fields (any black button in the left column) and pressing the blue key ENTR.

(2) CLOCK

Open this parameter field by pressing the CLOCK key. The label on this key is colored red. All white keys with red labels beneath the key pertain to this parameter field. You may enter any internal clock interval from 10 ns to 50 ms, in a 1, 2, 5 sequence. Any other entry will cause the ERROR LED to come on when the ENTR key is pressed.

When you key in EXT_/‾ or EXT‾_ the unit will then allow you to select the sense of the clock qualifier input in this same parameter field. You may select a binary 1, 0 or X (don't care). Use the three black keys so labeled for entry of the clock qualifier.

If you have selected an external clock, and wish to return to the internal clock period previously selected, merely open the CLOCK field and press the INT key. The unit will revert to the previously programmed internal clock period.

CLOCK QUALIFIER EXPANSION

You may desire to qualify the external clock with more than one bit. The Model 10-TC Probe Pod allows you to expand the qualifier input by as many as 10 bits. Power for the Pod is obtained from the rear panel of the K100-D. For specifc information on this accessory, contact the factory or your local Gould/Biomation representative.

(3) DELAY, (4) DELAY CLOCKS/EVENTS

The K100-D always operates in the Pretrigger Record mode. When you select a trigger delay by clocks, the number of clock periods selected lies between the trigger occurrence and the end of the memory. The default condition is 500 clock periods. Thus, when the instrument detects the trigger event, it will wait 500 more clock periods and then stop recording. Thus, in memory you will have 500 memory cells loaded with prior trigger information, and 500 cells loaded with post-trigger information.

The K100-D has a memory that is 1024 words long. For convenience in setting the unit up, there is a built-in trigger delay of 23 clock periods. Thus, with the trigger delay set to 0, the trigger event will occupy memory location 1000, rather than 1023. See also Figure 3.3.

The DELAY parameter field is addressed by pressing the black left column key marked DELAY.

You may select trigger delay in terms of trigger events or occurrences. Selection of delay by clocks or event is via switch 4, DELAY CLOCKS/EVENTS. Enter the desired decimal number, and then select delay by clocks or events.

When you select delay by events, the unit will count trigger occurrences and place the nth + 1 trigger occurrence at the center of the memory at location 501. For instance, if you select a delay of 10 events, the unit will place the 11th trigger event at memory location 501.

Trigger delay by events is a helpful mode when you are troubleshooting software in a system. It enables you to capture data on the nth occurrence of a software loop.

The delay field operates only on the Trigger event, and not on the Enable event.

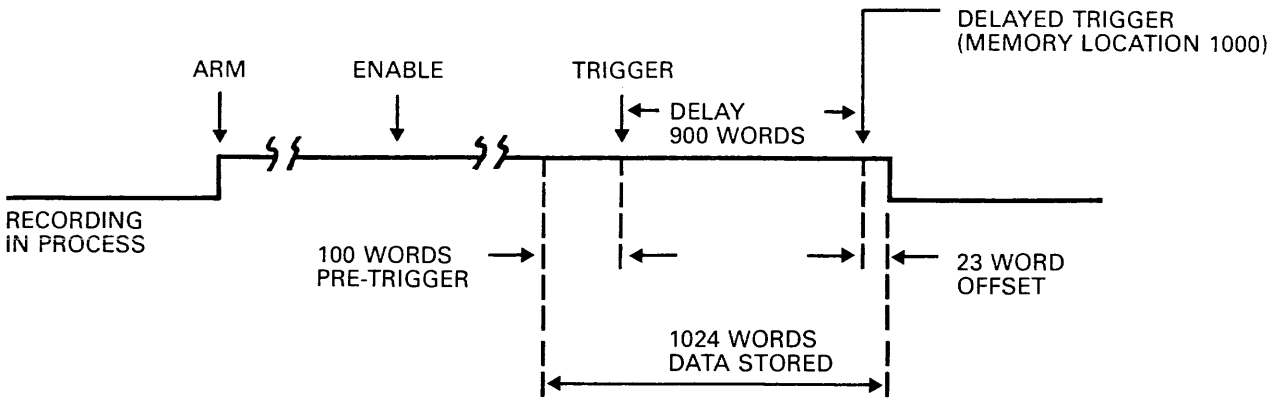


Figure 3.3. Three events, in sequence, are required to complete a recording. The Trigger actually controls the memory contents. The Enable is a qualifying event to allow the instrument to seek the trigger. The Arm event not only begins the recording, but also acts as a precursor of the Enable event. The combination of Enable and Trigger event allow "nested" triggering. For setup convenience, the unit has a trigger offset, or built-in delay, of 23 words. In this example, the trigger delay is 900 words.

(5) SEQUENCE/POLARITY

This parameter field operates on the display of recorded information and does not affect the recording.

The SEQUENCE portion of the parameter field allows you to rearrange all 16 channels in any desired order. The one restriction in this parameter field is that no channel may be entered more than once. If you do attempt to enter a channel more than once, and press the ENTR key, the ERROR LED will come on, and the underline cursor will move to the second entry of that channel. This allows you to recover easily from an entry error. You can delete the second entry of that particular channel by pressing the SPACE key and then ENTR. If there are several multiple entries, the underline cursor will point them out so that you may remove them.

The Sequence field permits you to format the data in a manner that makes the most sense to your analysis approach. In addition to single keystroke selection of hex, octal, or binary displays when in the Data domain, you can combine data decoding.

The SPCL key causes the unit to observe the channel grouping you have selected as shown in Figure 3.4. Here, the channels have been grouped, with spaces between groupings, to tell the unit how to decode the data. Channels F and E are binary, DCB are octal, A987 are hex, and 6543210 are ASCII.

The full ASCII character set is decoded, including upper and lower case (denoted by brackets) letters, numbers, and all control characters. Those entries in the ASCII string that are not decoded (displayed as seven binary bits) are the characters that are not universally defined.

In the Special Data domain, you can arrange the channels in any desired order, and in any combination of groups.

You may also use the SEQUENCE field to display less than the total number of channels. Placement of the period, or decimal point, anywhere in the SEQUENCE row will delete from display all channels to the right of the period. The double entry rule also

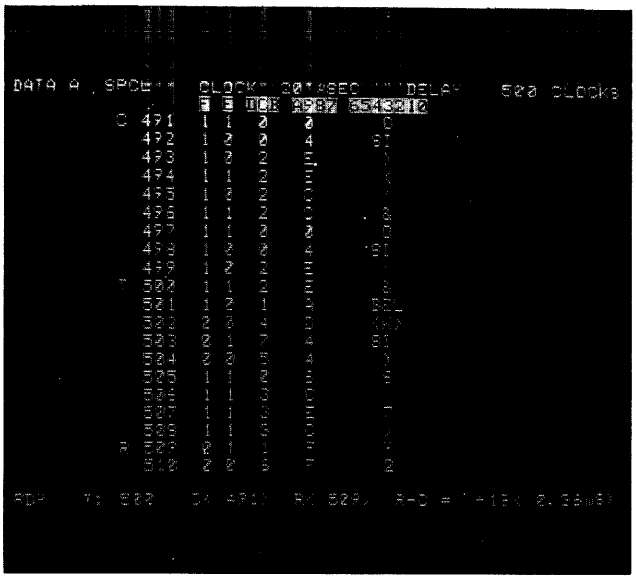


Figure 3.4. Special display mode, where you can format the data decoding in any channel order and any channel grouping to get binary, octal, hex, and/or ASCII.

applies to the period or decimal point.

TRUNCATED DISPLAY

The position of the decimal point controls what is actually displayed on the CRT. Thus, if you enter

FEDC BA98. 7654 3210

the K100-D will display only channels F through 8, but trigger from all 16 inputs.

If you enter

FEDC BA98.

where channels 7 through 0 are deleted using the SPACE key, the K100-D will display, and trigger from, only channels F through 8.

As an example, press the blue key SEQ and, using the Cursor or Reference position keys, place the underline one position to the right of Channel C. Key in a period and press ENTR. The ERROR LED will come on. Note that the underline cursor now positions itself to the second entry of the period. Press SPACE and then ENTR. The Status display will be refreshed and show only four channels.

Press the blue key labeled TIMING. Also press the white key labeled X20. Your display should now look like Figure 3.5.

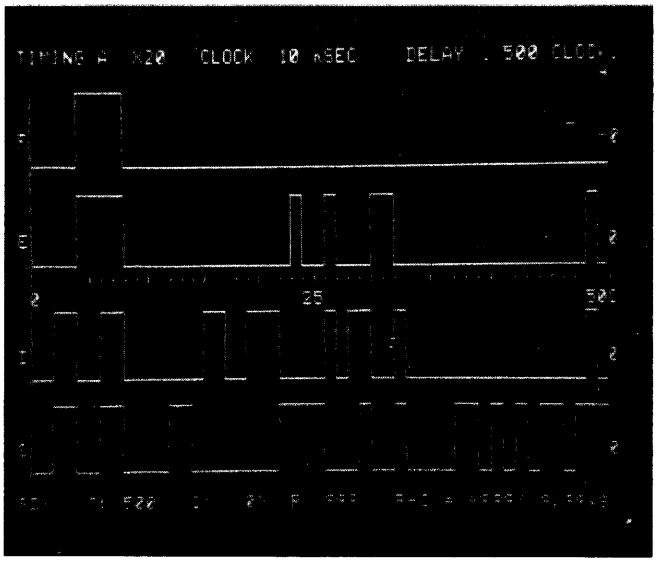


Figure 3.5. Just four channels are displayed, giving an automatic vertical expansion of 4. Times 20 horizontal expansion is also selected.

Notice that only four channels are now displayed, F through C. Also notice that a vertical expansion by a factor of 4 has occurred. This vertical expansion is automatic when four or less channels are displayed. A vertical expansion of X2 occurs whenever 5 to 8 channels are displayed. Also, since you selected a horizontal expansion factor of 20, the data displayed is now only 50 memory cells and gives a very easily examined timing format.

Press X1 and then STATUS. Next press SEQ and place the cursor at the position of the period. Press SPACE and ENTR.

Press TIMING. Your display should now look like Figure 3.6.

Here we are displaying all 16 channels of information and 50 words of memory.

Press STATUS. The POLARITY portion of the parameter field allows you to select for display, on a per channel basis, either positive or negative convention polarity. This

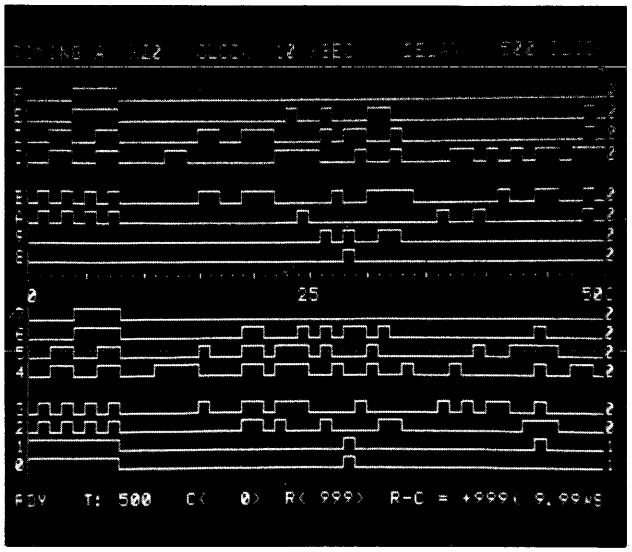


Figure 3.6. Same as Figure 3.5, except that all 16 channels are displayed.

allows you to rearrange the data domain format to allow for any inverted signals in your system. You can enter plus or minus signs by using the black keys labeled +/-.

(6) ENABLE, (7) TRIGGER AUTO/ MANUAL ENABLE

The Enable parameter field allows you to define a 16-bit word, plus two qualifier bits. Once the unit is Armed, it must find the Enable word before it can look for the Trigger word.

The default condition for the Enable word is automatic, as denoted by the A in parentheses. This means that the K100-D bypasses the Enable event and immediately looks for the Trigger.

There are two other conditions for the Enable event. They are manual (M) and combinational (C). These other two conditions are also shown within the parentheses. To define a manual Enable, press down switch 7, and the M will appear in the parentheses. Note that the unit will not seek a defined Enable word, but will always expect to see a manual Enable, initiated by switch 7.

The act of defining an Enable word changes the letter in parentheses to a C, denoting combinational Enable. This is done by opening the enable parameter field with the enable KEY. You can then key in, using either the three binary keys (black keys labeled 1, 0, X), or key in a hexadecimal word. When you key in a hex word, the unit decodes each hex character (16 white keys) and places four binary bits in the parameter field for each hex character entered.

If you define a combinational Enable for a subsequent measurement, the Enable word selected may not be found by the instrument once you Arm it. In that case, you may press down on switch 7 to manually Enable the unit, and complete the measurement. For the next measurement, the unit will be in the manual Enable mode, and you will have to press switch 7 again. To select a combinational Enable without disturbing the Enable word previously entered, you must reopen the Enable parameter field and enter that Enable word already there. In other words, press ENABLE, then ENTR.

To the left of the Enable word parameter field is a reverse video T. This denotes true or false Enable. When you have selected true Enable, the instrument will seek the Enable word. When it finds a condition where the input signals match the pattern defined, it will have detected the Enable event.

It can also select combinational false Enable. In this mode, the unit will seek the defined Enable event. It will continue to monitor this event until any one of the bits changes states. At that point, it will recognize the Enable event.

To select Enable true or false, open the Enable parameter field by pressing the key ENABLE. The underline cursor will locate itself to the entry for the left most channel; in this case, Channel F. Then use the Cursor or Reference left arrow key to move the underline cursor beneath the T in the field. Then use white key FALSE to change the T to F. To select T, again position underline cursor as before, and press FALSE again.

The qualifiers Q1 and Q2 at the right end of the Enable and Trigger parameter fields can be independently set for both Enable and Trigger Events. When you have entered the LSB for the enable word, in this case Channel 0, the underline cursor will step to the Q1 position. You can then select the states for

Q1 and Q2 by using the three binary keys.

QUALIFIER EXPANSION

You may wish to Enable or Trigger from a word wider than 18 bits. You can expand Q1 and Q2, each by a factor of 10, by using the Model 10-TC Probe Pod. Power for the Pod is obtained from the rear panel of the K100-D. For specific information on this accessory, contact the factory of your local Gould/Biomation representative.

TRUNCATED DISPLAY

As discussed under item 5, SEQUENCE/POLARITY, the position of the decimal point controls what is actually displayed on the CRT. Thus, if you enter

FEDC BA98. 7654 3210

the K100-D will display only channels F through 8, but trigger from all 16 inputs.

If you enter

FEDC BA98.

where channels 7 through 0 are deleted using the SPACE key, the K100-D will display, and trigger from, only channels F through 8.

(8) TRIGGER, (9) TRIGGER FILTERED/ MANUAL TRIGGER

All the comments that apply to the Enable parameter field also apply to the Trigger field, with the exception that there is no automatic Trigger mode available, just combinational and manual. As before, the letter in parentheses denotes which mode has been selected or used for a given measurement.

DATA THRUPUT RATES

The data thruput rate, or maximum rate of accepting trigger events and trapping data, depends on the display mode used. Using Auto arm, the following nominal rates apply, assuming a clock interval of 20 ns:

Timing diagram	1 cycle per 2 s.
Data list	1.5 cycle per s.
Status	12 cycles per s.

(10) THRESHOLD, (11) VAR A, (12) VAR B

This parameter field allows you to independently select a threshold reference level for each channel. You can assign one of four different threshold voltages to any one channel. The black THRESHOLD key opens this field. Notice on the keyboard that the row of four white keys to the right of the THRESHOLD key are those keys used to assign the thresholds. You can select from a preset TTL (+1.4 V), preset ECL (-1.3 V), and two variable thresholds, A and B, that you can specify through the keyboard.

All 16 input channels, plus the qualifier inputs and the external clock and its qualifier may be independently assigned from this list of four different threshold levels.

To specify the variables A and B, you open these parameter fields by pressing the blue SPECIFY key, and then the white VAR A or VAR B key. You can enter a threshold voltage from the keyboard using keys 0 through 9, subject to two restrictions.

1. Voltage entered must lie between -6.4 V and +6.35 V.

2. Voltage can only be specified in 0.05 V increments.

Any entry condition that violates the above rules will cause the ERROR LED to come on.

(13) INPUT MODE

You can select Sample or Latch input modes independently for each channel. This parameter field is addressed via the black key INPUT. Notice, as with the Threshold parameter field, the four keys associated with the Input mode are in the same row with the Input key.

There are two ways of programming the

inputs. First, you may go through the parameter field and assign Sample and Latch input modes on a per channel basis by pressing SAMPLE or LATCH keys.

If you wish to assign Sample and Latch input modes on a group basis, you may do so by pressing the 0-7 key and SAMPLE or LATCH keys. This will program channels 0-7 to whatever Input mode you select. The same holds true for channels 8 through F. The K100-D will seek out these channels, no matter where they appear in sequence, and assign them Sample or Latch input modes.

The ability to assign Sample or Latch Input mode on a per channel basis gives you an extra measure of flexibility. For instance, you may wish to ignore any asynchronous glitches (those noise spikes that are not synchronous with a Sample Clock Edge), except on one or two channels. This per channel assignment gives that flexibility.

Refer to Figure 3.7. In the Sample mode, the unit will ignore threshold transitions between active clock edges. This mode finds greatest use when recording in synchronous logic systems. Synchronous logic makes decisions at active system clock edges and is immune to logic changes that occur between these clock edges.

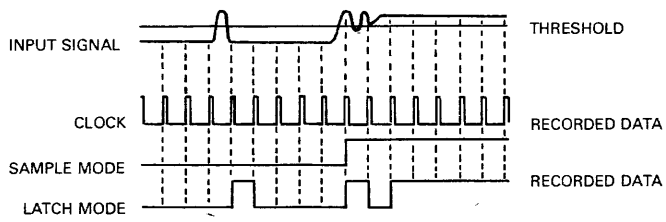


Figure 3.7. Sample and Latch Input modes, and an illustration of how each mode affects the data recorded in memory.

Asynchronous logic is not clocked, and responds to virtually any threshold transition within its speed range even if it is noise. Knowing that narrow noise spikes exist in an asynchronous logic system is of great value.

The Latch mode detects and flags in the analyzer's memory any threshold transitions that occur between the clock edges. The K100-D can detect glitches or noise spikes as narrow as 5 ns, with a voltage overdrive of 25% of total voltage swing or 250 mV, whichever is greater, even though the shortest clock period is 10 ns.

The sensitivity of the Latch mode is depicted in Figure 3.8. Note that the specification is not stated in terms of absolute voltage levels, but rather a percentage of voltage swing. This is important in those logic systems, namely ECL, where, as the clocking rate of the logic increases, the total voltage swing on either side of the threshold decreases. Thus, the glitch capture capability is in reality only related to percentage of voltage overdrive rather than a finite voltage swing.

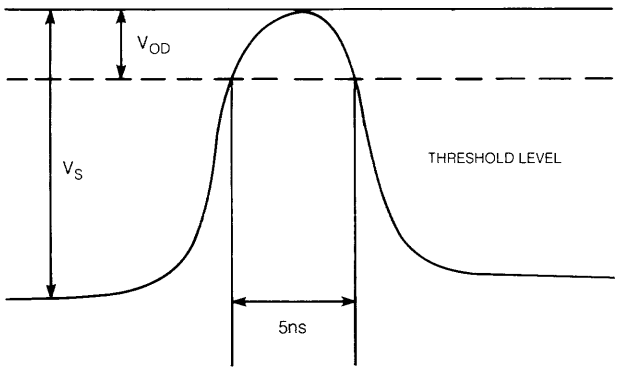


Figure 3.8. A graphical illustration of the Latch mode specification, which is related to percent voltage overdrive rather than a finite overdrive. VOD is 25% of VS. The same is true for negative-going glitches.

Noise spikes between clock edges are flagged in memory as pulses represented as being one clock interval wide, opposite in state to the previously clocked state. Figure 3.6 illustrates the treatment of an input signal, with both the Sample and Latch modes, and what effect these input modes have on the actual recorded information.

The Latch mode indicates the presence of noise spikes, or glitches, and their time occurrence relative to the other recorded information. The period of the noise spike is not indicated by the Latch mode flag; the measurement of the glitch is limited to the time value of one memory cell.

Even though you cannot measure the actual width of the glitch, its presence is recorded, and this gives you very definite information for diagnosing a problem in your system.

(14) SEARCH

This parameter field operates on the Data domain display. When in Status display mode, open this parameter field by using the blue SEARCH key. This allows you to specify, in binary or hexadecimal, a word that you wish to find in the Data domain display. The word need not be known to exist in the memory. The analyzer will find that word for you if it exists.

Using the data automatically stored in memory upon power up, let's use this mode to search for a word. In the Status display, open the Search parameter field by pressing the SEARCH key. Then key in hexadecimal 1010, and press the ENTR key.

Press the blue DATA key and the blue SEARCH key. Your display will look like Figure 3.9.

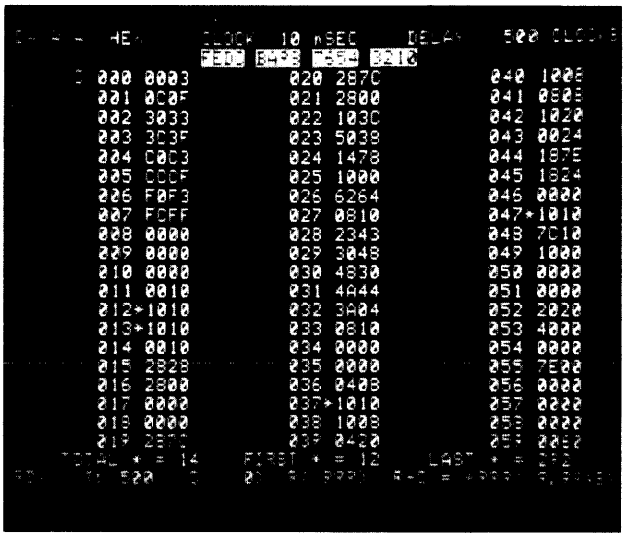


Figure 3.9. Here the unit has been programmed to search for the hex word 1010. It found this word 14 times; first occurrence at memory location 12, and last one at 292. This information is read out at the bottom of the screen. Each occurrence is marked by an asterisk.

Note that there are 14 occasions where the hex words 1010 occurred. These occurrences are marked by asterisks, and the total number of occurrences is tallied along with the first and last occurrences of that word. If your display does not look like Figure 3.9, go back and execute the above routine.

To look at the last occurrence of 1010, for instance, you can specify Cursor position as follows without scrolling through the memory. Press SPECIFY and either Cursor arrow key. At the CRT bottom, the Cursor parameter field will be in reverse video. Key in 292 and press ENTR. The Cursor will reposition itself to memory location 292, the last time 1010 occurred. The Reference position can also be specified in this fashion.

The Search mode allows you to spotlight a particular address in a loop, for instance, so that you may be able to visualize in the data domain the structure of that loop. Notice that you need not specify a state for every channel; for instance, if you wish to find those occasions in memory when the first four channels assume a particular combination of states, you may key in the desired states for the first four channels only, and leave the other channels in "don't care" positions. Then the instrument will search for those occasions where the first four channels occupied the desired states. This gives you the flexibility of finding in memory only those states that you wish to locate.

(15) ARM MODE

You can select either Auto Arm or Manual Arm with switch 16. In Manual Arm mode, the instrument makes a measurement after you have manually armed it with switch 16. It completely executes the measurement and returns to a ready for arm state, as denoted by entry 18 RDY. If you push up on switch 16, the instrument then automatically arms itself upon completion of each measurement. Because of internal housekeeping, the maximum rate at which the instrument can arm itself, and detect Enable and Trigger events, is on the order of 10 times per second.

Usually, you use the Manual Arm mode when you wish to directly control the measurement process. Use of the Auto Arm mode

is generally in those cases where you wish to observe continuous updates of the operation of your circuit. To avoid possible errors in a recording, always return the instrument to Manual Arm, RDY state, before changing any record parameters. If the instrument is in some other state, this can be accomplished by pressing switch 16 down a second time.

The Arm function also controls the Compare mode of the instrument. This is a mode in which you can store in a reference memory a sequence of events from your system. This may be, for instance, a correct sequence of events against which you wish to compare an incorrect sequence of events. Specifically, this could be a situation where you have a system that randomly malfunctions. By the nature of the malfunction, or symptoms of it, you can usually narrow down on a certain portion of the system program within which the malfunction occurs. This series of program steps can be recorded and stored in the Reference memory, B. The instrument can then be put into a mode where it will continually monitor that flow of program executions, make a measurement each time, and compare that captured data with the reference. Once it finds a difference between the two memories, it will halt on that occurrence and save the incorrect sequence of program steps. The instrument can do this in the automatic and unattended mode; therefore, you can allow it to monitor your system for any length of time and be sure that the malfunctioning sequence will be captured and displayed.

The manner in which the instrument does this is via the Compare mode. Figure 3.10 is a block diagram of the memory structure of the K100-D. The memory M receives the signal inputs at real time rates; M is the memory that operates at 100 MHz. Once the memory has been filled with data, this data is then automatically transferred to the A memory, and then will be displayed on the CRT.

In addition, you can manually transfer using the A→B key, the contents of A into memory B. By doing so, you have created in B a reference memory of up to 1024 program steps, against which the instrument will automatically compare the contents of A. Manual comparison between two subsequent measurements can also be compared.

The steps to follow for the use of this feature are as follows.

The use of the Auto Stop Compare mode depends upon measurements made with respect to some system clock (synchronous recording) and some specific trigger event. If the comparison is made with respect to data stored using the internal clock of the K100-D (asynchronous recording), a valid comparison cannot be made because of the asynchronous nature of the measurement; i.e., the two compare recordings can differ by one clock period, thus making comparisons invalid.

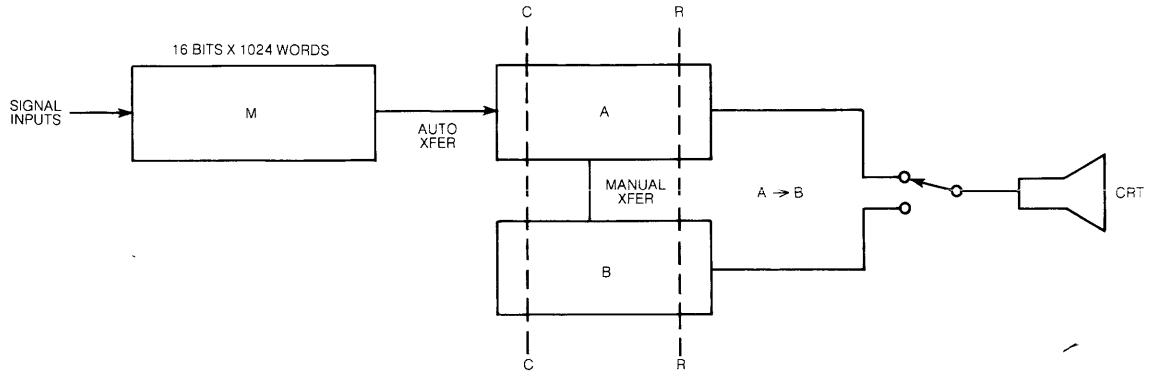


Figure 3.10. Record (M) and display/compare (A and B) memory structure inside the K100-D.

1. Select from your system operation a sequence of events that you will use as a reference, and record this sequence in the instrument. Use manual Arm mode, rather than Auto, at this point.

2. Transfer the contents of the A memory into memory B by using the blue key A→B.

3. Call up Auto Stop mode by using the blue key AUTO STOP. The Arm mode parameter field will change from MANUAL to AUTO.

4. Select the condition for comparison, either A=B (black key) or A≠B (white key). Arm mode field will now read AUTO STOP, A=B or A≠B.

You have control of the interval over which the comparison will be made, in addition to the width of the word compared. You can place the Cursor and Reference anywhere within the 1024 word memory to specify a sequence of memory locations for comparison. For instance, in Figure 3.8 if you invoke the limits on the comparison, the actual comparison interval between the two memories would be memory locations 491 through 509 inclusive.

To control the width of the word to be compared, use the decimal point as explained under item 5, SEQUENCE/POLARITY. Thus, if you enter

FEDC BA98. 7654 3210

the K100-D will display and compare only channels F through 8 in A and B memories, but will trigger from all 16 channels.

If you enter

FEDC BA98.

where channels 7 through 0 are deleted by using the SPACE key, these deleted channels will not be displayed, nor be compared, nor contribute to the combinational trigger word.

To tell the K100-D to observe the limits imposed by the Cursor and Reference positions in the Status display mode, after specifying Auto Stop, A=B or A≠B, press the blue key (LIMITS). The display will now read AUTO STOP <A=B> .

5. Without changing any recording parameter fields, press switch 16 up. This initiates the sequence of making a measurement and then comparing that measurement with the stored reference. When the unit is in the Auto Stop mode, it will not update the display memory until it finds a block of data that meets the selected condition. At that point, the A memory will be updated with the just trapped and compared data. This allows the unit to detect triggers at rates up to about 8 per second.

6. The Status byte in the lower left corner, entry 18, will be blinking through its routine. When the instrument display is a steady RDY indication, it means that the selected condition has been met. The unit is now standing by with information in the A memory that compares, or does not compare, with the reference.

To view the two memories, press the blue key DATA and the blue key A/B. Now the instrument will alternately display the information from the A and B memories. By moving the Cursor through the memory, you may view those selected portions.

To initiate another round of comparisons, merely press switch 16 up. This will cause the instrument to go through measurement and compare cycles until the selected condition is met. Before initiating the Auto Stop cycle again, place the instrument back into the Status Display mode so that you can achieve the maximum throughput rate.

AUTO STOP RECORD RATES

When C is set at memory location 0 and R at 999, the Auto Stop cycle takes approximately 120 ms, assuming a record clock period of 10 ns. When C and R are both set to the

same memory location during Compare with limits, the cycle takes approximately 100 ms.

When comparing a full memory, the unit will be unable to respond to each trigger event unless it occurs at an interval greater than 120 ms.

Note that when in the Auto Stop mode, the unit will repeat the cycle until the comparison condition is met (A = B or A ≠ B). It will not update the display until the condition is met.

(17) FILTER

This parameter field is selected by pressing switch 9 up. Any number between 1 and E (14) may be entered in this field. The K100-D will then test any input bit patterns that match the specified Enable and Trigger events. Any bit pattern must match for a minimum of record clock sample periods. For instance, if you enter the number 5, the K100-D will test the Enable and Trigger events to insure that these events are valid for a minimum of 5 clock periods. On the Time or Data displays, notice that the Trigger event is labeled not at the first period that it matches the trigger combination, but after the number of clock periods specified by the trigger filter.

The filter will always reject events when the event time duration T meets the following: $T \leq (F-1)$ (CLK INTERVAL) -3 ns, where F = Filter setting. The Filter will always accept events that meet the following: $T \geq F$ (CLK INTERVAL) +4 ns.

(18) RDY, CK?, EN?, TG?, DLY, BSY

The Status byte is displayed in the lower left-hand corner of the Status, Time and Data Domain displays. Below is a tabulation of the meaning of each one of these bytes, in the order in which they are displayed. Refer to Figure 3.3.

RDY The unit is ready for an Arm event. The only time you will see this displayed is when you are in manual Arm mode. If you have Armed the instrument and wish to get it back into a ready for arm status, press switch 16 down a second time. This will cancel the measurement that you called for. As mentioned earlier, all changes to record parameters should be made from the RDY state to avoid erroneous recordings.

CK? When you are operating the instrument with an external clock from your system, and the clock is very slow or not active in your system (or the clock qualifier bit is in the opposite state of that specified) the instrument will respond by asking for a clock. This will occur only when trigger holdoff is operational.

Trigger holdoff can be locked out. See Figure 3.2.

When you are operating on internal clock, and this message is displayed, it means that the instrument is executing a trigger holdoff and is flushing its memory of any old data that exists. During this time it will not recognize Enable or Trigger events. The clearing of the record memory occurs at the record clock rate, so that if you're operating at clock intervals considerably shorter than 1 ms, you will not see this message.

CK? will only be displayed under the above conditions. It will NOT be seen after the trigger holdoff period if the clock is halted.

EN? The unit is waiting to receive or detect an Enable event. If you have it programmed for a combinational Enable event, it means that the instrument has not yet detected it. If you have it programmed for manual, it is asking you to press down switch 7.

TG? The unit is waiting for a Trigger event. It has not yet detected it or is waiting for you to manually trigger it via switch 9.

DLY The unit is counting down the trigger delay, either in terms of clock periods or trigger events. When delay is no longer displayed, it means that the recording has been completed, and the following message will appear.

BSY The unit has completed the measurement and is now updating its display memory. The unit will not record any information during this period of time.

(19) Input A, Input B

These connectors are labeled so that you can match up the labeled probe assemblies to the proper connector. The only difference between the two probe assemblies supplied is the shrink sleeve label at the end of each probe wire. Otherwise, the probe assemblies are identical.

⚠

The probe assembly inputs are rated 50 VDC maximum.

Figure 3.11 shows a representative probe podlet along with its supplied accessories: one each red and black short flying leads, and two spring loaded hook tips. The BNC adapter shown is an accessory available from the factory. This BNC adapter allows for easy conversion of any probe podlet to a female BNC for convenient connection of the Model 10-TC Probe Pod. This pod may be used for extending the combinational Trigger word (or Enable word) out to the maximum of 36 bits.

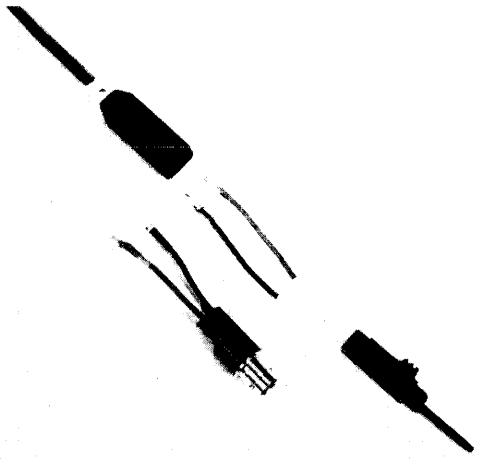


Figure 3.11. Channel F probe podlet. The flying leads and spring loaded hook tip are supplied with the instrument, along with the probe assemblies. The BNC adapter shown is an accessory.

Each 10-TC can detect up to a 10-bit word. By connecting two 10-TCs to Q1 and Q2 respectively, you are then able to AND together the 16 bits of the trigger word with the two qualifier inputs, which gives you a total of 36 bits for a trigger. The trigger output on the 10-TC is via coax cable and a BNC connector. Thus, the adapter shown provides an interface between the trigger qualifier input and the trigger output cable of the 10-TC. In like manner, you can expand the clock qualifier CQ. Thus, you can qualify an external clock with up to 10 bits from your system.

PROBE INPUTS

Each probe assembly consists of 10 podlets; each podlet contains a hybrid active circuit. All 20 podlets are identical electrically. Each podlet provides a 1 MΩ , 5 pF input impedance provided by the buffering amplifier in the hybrid circuit. The hybrid also provides threshold detection, and converts this discriminated signal to a differential ECL signal, which drives the flat ribbon cable back to the instrument. Thus, your system only sees the input circuitry of the podlet, and not the flat ribbon cable.

⚠

Each input has a voltage rating of 50 VDC maximum.

The length of the short flexible leads has been selected for a maximum length that will not degrade the high performance of the instrument. Attaching flexible leads of a length longer than those supplied will cause degradation in performance. However, if you wish to use flexible leads of a length longer than that supplied, you may purchase from the factory a connector kit containing both connectors used on the flexible wire. From this you may fabricate any special wire lead assemblies that you desire for connection to your system.

Notice that the female socket that mates with the spring loaded hook tip kit is designed to mate with a 0.025 inch square post. Even though these female connectors were chosen

for their rugged design, damage may result in forcing them over posts of larger size. The result will be that if you subsequently mate this socket to the hook tip, the integrity of the connection will be lost. This is an Augat receptacle, part number LSG-2BG2-1.

The female connector at the other end of the wire lead is a snap fit into the male pin recessed into the podlet. This means interconnection to your system is a very good compromise between ruggedness and miniaturization. This is an AMP receptacle, part number 60789-3.

Available also from the factory is a repair kit for each individual podlet, in case of physical damage to the active circuitry. For details on any of the above mentioned accessories, please contact us at the factory or your local Biomation representative.

EXTERNAL CLOCK AND CLOCK QUALIFIER INPUTS

The K100-D can accept your system clock at rates between DC and 70 MHz. The minimum clock pulse width shall be 5 ns. The setup time requires that the data be present and settled out 2 ns before the active clock edge. Likewise, the hold time requires that the data must stay settled for 2 ns after the active clock edge.

When you input a qualifier signal on CQ, it must go TRUE a minimum of 12 ns before the clock goes TRUE, and go FALSE a minimum of 1 ns after the clock goes TRUE. Also, the qualifier must go FALSE a minimum of 10 ns before the clock goes FALSE. See Figure 3.12.

These timing requirements are necessary to ensure that no false clocks are generated due to signal edge overlap. The requirements are such as to limit the qualified clock rate to a maximum of approximately 40 MHz.

(20) M→A

During normal K100-D operation, the unit completes a measurement, transfers the

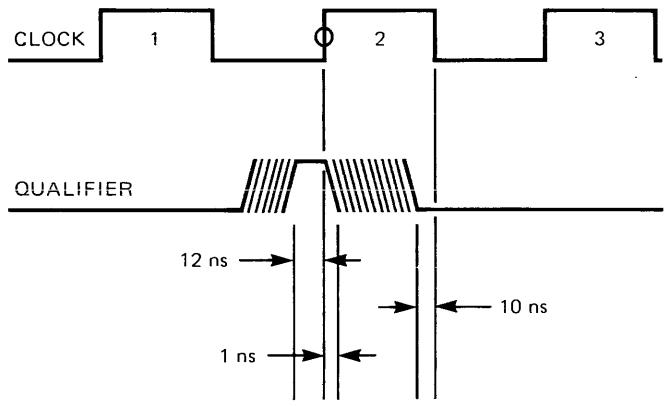


Figure 3.12. To qualify clock pulse 2, the minimum timing requirements for the qualifier are as shown.

data from the record (M) memory to the display memory (A), and puts the data on the CRT. A complete measurement requires that a record clock be present for the duration of the measurement, including Enable, Trigger, and Trigger delay. See Figures 3.3 and 3.10.

In some cases when using an external clock, the clock may cease activity before the measurement has been completed. This may be due to a normal system function or a failure. When this occurs, the data existing in M may still be of interest for analysis.

The M→A key allows you to transfer the contents of M into A for display. You can record a short burst of data, press M→A, and view it. You can record and display a second burst in the same fashion. The second burst will be displayed following the first, provided the total number of clocks received during the two bursts is less than 1024. This preserves all of both bursts in memory.

3.3 Rear Panel Inputs and Outputs

Refer to Figure 3.1 while reviewing this section.

(1) TRIG OUT

This signal is TTL active high. It goes low as soon as the instrument detects the trigger event selected. The signal stays low for the entire period of time that the trigger event is valid. This signal is synchronous with the input data.

ADDENDUM FOR (1) TRIG OUT

This output is useful for synchronizing other instruments, such as a scope or other logic analyzer, with the occurrence of the defined trigger event. Please note the following:

1. TRIG OUT exhibits a nominal delay of 45 ns between input of the trigger word at the probe tips, and output at the rear panel BNC.

2. When the K100-D is in the RDY state (see item 18), TRIG OUT occurs each time the trigger word occurs. During display update, or during comparison in the Auto Stop mode, TRIG OUT does not occur.

(2) SPARE BNC CONNECTORS

(3) VIDEO OUT

This is a composite video output with an amplitude of 1 V peak-to-peak into a 75 Ω load. With this output you can drive a large raster scan CRT display for viewing by several people.

Note that the video output is such that it causes full scan on a video monitor. Since many video monitors overscan by approximately 10%, you will lose the outside edges of the K100-D display unless your monitor can be adjusted to just scan the screen area with no overscan.

(4) ±5 V CONNECTORS

These outputs provide power for two 10-TC probe pods, or for various signal input adapters. Minimum available power is +5 V at 1.1 A, -5.2 V at 0.3 A.

(5) DIGITAL INTERFACE CONNECTOR

This connector is used for digital I/O in the IEEE 488-1975 format, if the instrument is so equipped.

Refer to the appropriate operating manual supplement that describes this digital interface and the I/O software.

(6) LINE VOLTAGE SELECTOR, (7) FUSE

The K100-D may be used on a wide range of power line voltages at frequencies of 50 or 60 Hz nominal. The rear panel contains a fuse holder and a pair of slide switches for selection of nominal power line voltages. Table 3.1 shows these voltages, switch positions, and fuse selection required for that power line voltage. The selected switch positions are referred to as left and right when viewed facing the rear panel.

Table 3.1

Range (+10%)	Selector Switch Positions	Fuse-Amp (Slow Blow 3AG)
100	Both in	5
120	Left in, right out	5
220	Left out, right in	2.5
240	Left out, right out	2.5

Figure 2.2 shows the placement of a jumper on the MPU PC board for 50 Hz operation of the display. You may have to adjust the horizontal oscillator frquency control, R2, for 50 Hz operation. See Section V for display control layout.

(8) POWER INPUT CONNECTOR

Connect the line cord to this connector, using a three-wire grounding type plug for connection to line power.

3.4 Set-up Procedure and Operation

The purpose of this section is to offer the K100-D user several operating examples that he may duplicate in his facility. The examples are designed to increase user understanding and familiarity with the K100-D. The examples highlight recording in the self-programmed mode (default); recording using a 50 ns clock period; recording with 200 words of pretrigger and 800 words of post-trigger

information; and recording with a user-selected event delay of four.

The data source selected for the following examples is a pulse generator that has a manual, single pulse output mode. The high and low levels of the pulse output should be adjusted for TTL compatibility. A "1" = 2.4 V and a "0" = 0.4 V. The width of the pulse should be 1.0 μs. Again the generator should be in the manual, single pulse output mode.

3.4.1 Self-Programmed Recording

The K100-D has a self-programmed mode of operation that was designed to enhance its self-teaching ability. This first recording will be made with all the status parameters programmed exactly as they are immediately after power up. Turn the power off, wait 1 minute and turn the power back on. The K100-D's status display will look exactly like the one shown in Figure 3.1.

Connect the signal generator's output and ground to their corresponding points on probe zero of the K100-D. The status display indicates that this recording will be at the K100-D's maximum recording rate and that half of the unit's memory will be allocated to pretrigger and the other half to post-trigger recording. The Enable and Trigger channel are zero; however, the Enable word has been defeated by being placed in the auto mode. All thresholds have been set at TTL, which is compatible with the signal generator's output. The Arm mode is auto, but becomes manual the first time the K100-D is manually Armed.

Manually Arm the K100-D and the unit begins recording. Note that the record status (lower left corner of the CRT) reads TG?, indicating the trigger word has not been detected. Manually pulse the generator. The record status indicator will read RDY. Press the blue TIMING button in the Display button group. The timing display will be exactly like Figure 3.13.

In this recording it is important to note that the trigger point is exactly in the center of the memory as dictated by the

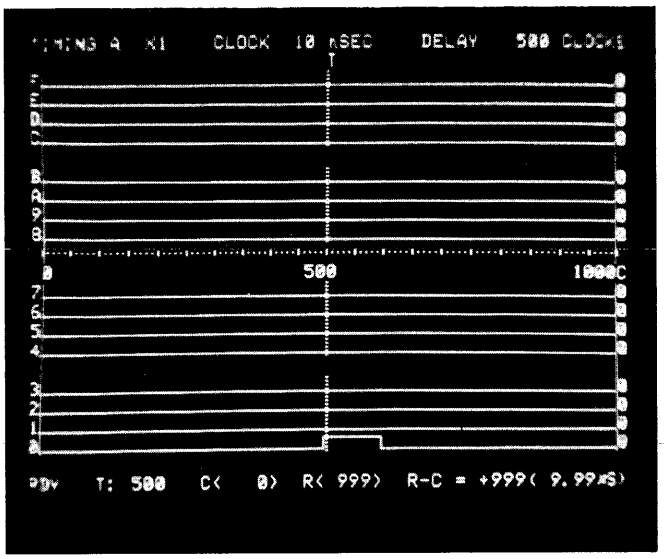


Figure 3.13. A self-programmed recording by the K100-D of a 1 μs pulse.

delay of 500 clocks, and the 1 μs pulse has been sampled 100 times as a result of the high clock rate (100 MHz or 10 ns/sample) of the K100-D.

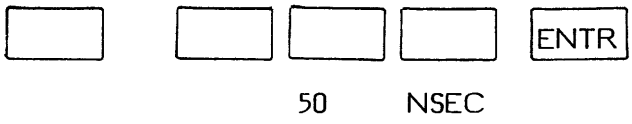
The number of times that the K100-D has sampled the pulse can be determined by moving the C Cursor to the rising edge of the pulse and the reference cursor to the right edge of the pulse. The word difference and time difference between the two cursors is found at the lower right corner of the display, R-C. The number in front of the parenthesis represents the number of memory cells the 1 μs pulse occupies. The number inside the parenthesis is the period of the pulse. These numbers should be +100 and 1.0 μs, respectively, contingent upon how accurately the period of the generator pulse was set.

Please recall that all logic analyzers are sampling devices and this was an asynchronous recording. That is, the logic analyzer's sampling clock has no fixed phase relationship to the pulse output. If this example recording is repeated several times, a ± 1 word variation will be noted in the word difference indicator. The time difference indicator will also reflect this variation. These variations are inherent in asynchronous recordings.

3.4.2 A User Programmed Recording Using a 50 ns Clock

To program the K100-D's clock for the next recording, the following keystrokes are necessary.

STATUS CLOCK



50 NSEC

The new status, STATUS W, will look exactly like Figure 3.14.

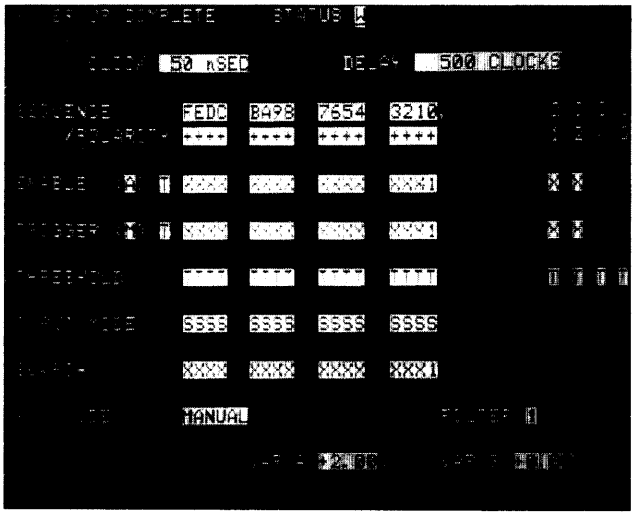


Figure 3.14. Status W reflects the fact that the clock period has been changed to 50 ns.

Manually arm the K100-D; the record status will read TQ? Manually pulse the generator. The record status indicator will read RDY. Depress the blue TIMING button. Your display will be a duplicate of Figure 3.15. Note the left and right cursors in this figure reflect the suggested pulse measurement of the previous example.

Note that the pulse period appears shorter even though the pulse is the same period. The changing of the clock sample period has increased the amount of time recorded and displayed on the CRT by a factor of 5. This dwarfs the 1 µs pulse. Using the K100-D's cursors, horizontal expansion and word difference/time difference

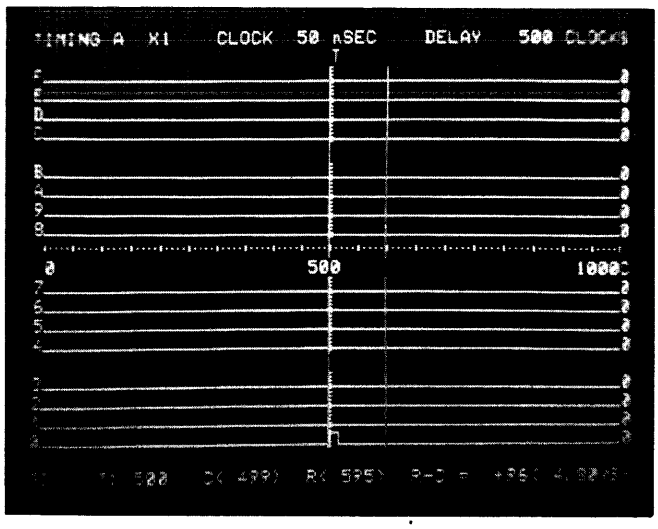


Figure 3.15. A 1 µs pulse recorded using a 50 ns clock period.

indicators, verify that the pulse's period is 1 µs. Remember that when operating in a horizontal expansion of X5, X10, or X20, the data to the right of the C cursor is expanded. Figure 3.16 measures the 1 µs pulse using a X20 horizontal expansion.

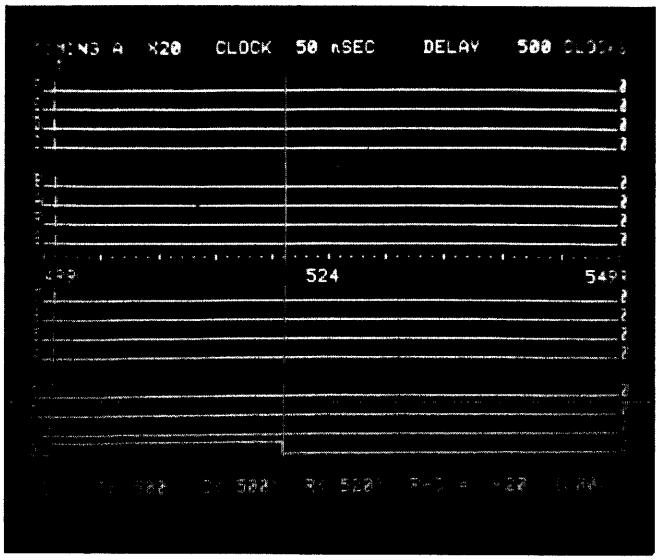


Figure 3.16. This 1 µs pulse is being measured using both cursors and a horizontal expansion of X20.

3.4.3 A User Programmed Recording With 200 Words of Pretrigger and 800 Words of Post-Trigger Data

To make a recording with the memory allocations indicated in the title, the following

keystrokes are necessary.

STATUS DELAY

[ ] [ ] [8] [0] [0] [ENTR]

Arm the K100-D and manually pulse the generator. After pressing the TIMING button the display should look exactly like Figure 3.17 when viewed with a X1 horizontal expansion.

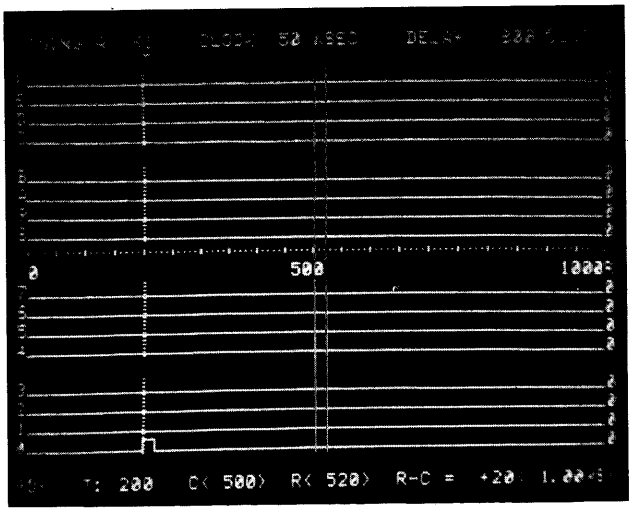


Figure 3.17. This figure demonstrates a recording where 200 words of Pretrigger and 800 words of post-trigger information have been saved.

Note that Delay positions the K100-D's 1024 word recording relative to the Trigger. In the first two examples, the Delay was set for 500 words resulting in half of memory being allocated to pretrigger and the other half to post-trigger recording. This last example has changed the memory allocation to 20% pretrigger and 80% post trigger.

This information may be viewed in the data domain by pressing the DATA button, then the BIN button. This will give you a Binary display of the recorded information. To view channel zero changing from a logic "0" to "1", address the C cursor to memory position 199 as follows.

SPECIFY LEFT CURSOR

[ ] [ ] ↓ [1] [9] [9] [ENTR]

Moving the cursor has allowed the user to view channel 0 changing to a logic "1" at K100-D memory cell 200.

Figure 3.18 illustrates the resultant CRT display. Other decode formats may be used by depressing the desired decode base buttons to the left of the DATA button.

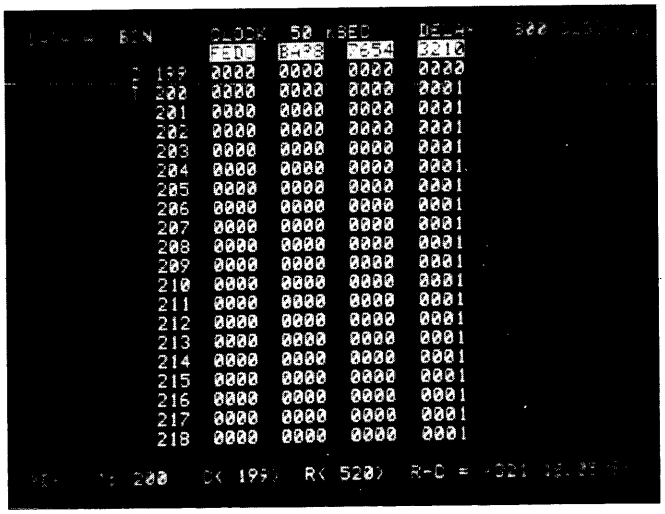


Figure 3.18 A BINARY decode of the data recorded at the trigger point.

3.4.4 A User Programmable Recording with an Event Delay of Four

To program the K100-D for a four event delay recording, the following changes to the status must be made. Make these changes with the following keystrokes. Please pay special attention to the DELAY switch manipulations; this will change the K100-D from Clock to Event delay.

STATUS DELAY DELAY

[ ] Clocks ↓ [ ] [3]
Events

[ENTR]

The K100-D is now programmed for a event delay recording of 4. Recall that the K100-D's formula for event delay is N (user selectable) +1. The K100-D adds 1 event of static delay in addition to the user-selected amount, giving an event delay of four.

Manually ARM the K100-D and manually pulse the signal generator four times. The K100-D will record the data about the fourth occurrence of the "0" to "1" trigger on channel 0. The exact data recording allocation about the fourth trigger is:

500 words of pretrigger information, and

523 words of post-trigger information including the trigger word.

The fourth trigger will be in memory cell 501. This can be verified by pressing the DATA button and moving the C cursor to the 500 memory cell. See Figure 3.19.

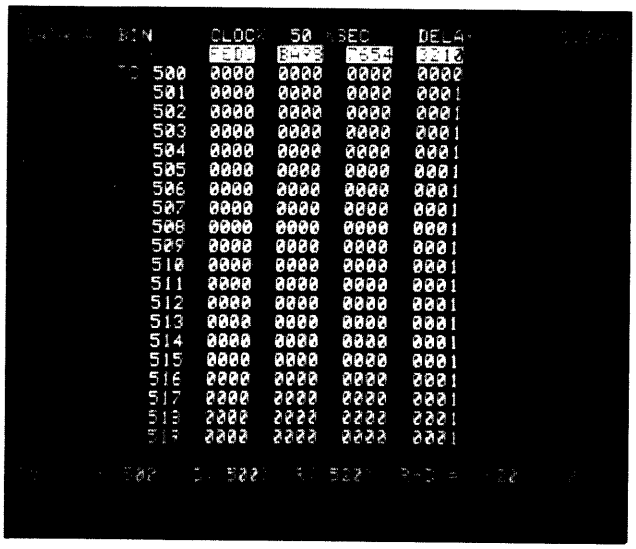


Figure 3.19. This Event delay recording of four allows the user to view 500 words of pretrigger and 523 words of post-trigger information.

User-generated variations on the examples given will further your understanding of the K100-D.

SECTION IV

PRINCIPLES OF OPERATION

4.1 Introduction

This section is divided into two parts. The first part gives a block diagram description of the instrument, and the second part gives a detailed treatment of the theory of circuit operations.

4.2 Basic General Description

Figure 4.1 is a block diagram of the Model K100-D. The blocks are arranged in their approximate physical locations as viewed from the top.

Each block in Figure 4.1 will be described briefly to indicate the functions performed. Then, each block will be described in greater detail in subsequent sections.

4.2.1 MPU PWB

6800 microprocessor.

ROM program storage (up to 24K bytes).

RAM for processor use (32K bytes).

Crystal-controlled processor clock generation and dynamic RAM timing generation.

CRT controller using "split-phase memory access" and "dot-mapped" display.

Strappable-50 Hz or 60 Hz CRT frame rate.

Automatically refreshes dynamic RAM.

Keyboard scanning interrupt (50 Hz or 60 Hz).

Provides separate signals for VIDEO, HORIZ.SYNC, and VERT.SYNC.

Provides COMPOSITE VIDEO for external use.

I/O device address decoding on MPU board. (Allows simple I/O device decoder)
Memory mapped I/O.

Buffers Address Bus and Data Bus (Bi-Directional) for system use.

MPU self diagnostics.

4.2.2 Front End

Differential Line Receivers for all 20 input probes.

Clock selection (INT/EXT) and distribution.
Up to 100-MHZ clock rate; provides Clock to Record Control Logic.
Input sampling circuitry (sample/latch mode).
Sixteen data inputs and two qualifiers.

Combination Detector Logic
Sixteen data and Two qualifiers { Trigger* / Enable* / Scope Sync*
"1", "0", or "X" selection.

*Passes these signals to Record Control Logic.

Completely controlled by the MPU.
Clock selection.
Sample/latch control.
Combination selections.
High-speed memory diagnostic.
Diagnostic logic to allow MPU data input to high-speed memory.

Differential line drivers for data to high speed memory.

4.2.3 High-Speed Memory

100-MHZ recording rate.

1024 words x 16 bits/word.

Partitioned into two identical boards, where each provides 1024 words x 8 bits/word.

Differential line receivers for data from Front End.

Data is transferred to the MPU for display processing.

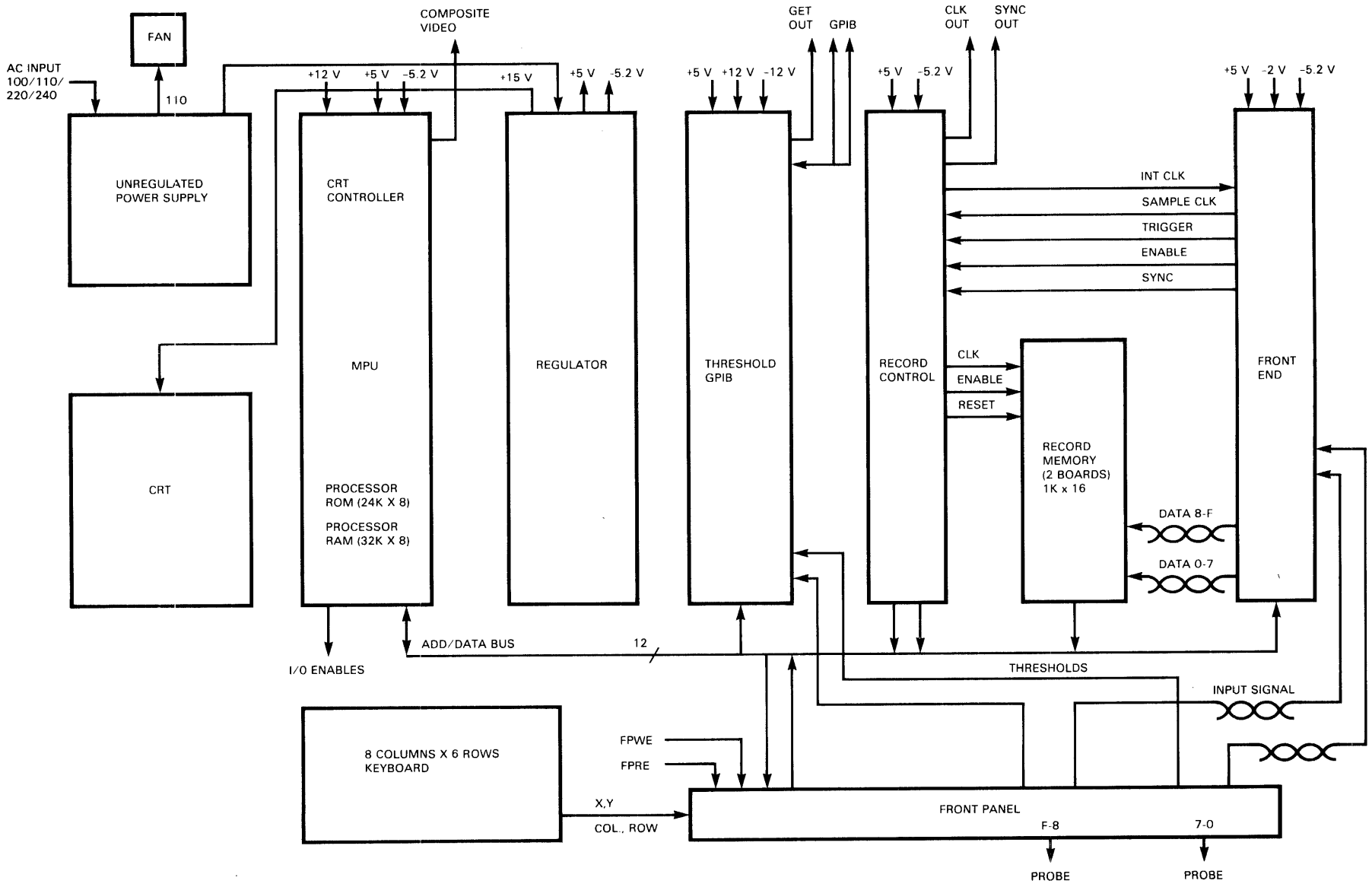


Figure 4.1 Block Diagram of K100-D

4.2.4 Record Control Logic

Completely controlled by MPU.

Time Base generates 10 ns to 50 ms sample rates in 1, 2, 5 sequence; sends to Front End for clock selection and distribution.

Record cycles are always initiated by the MPU and may be terminated by the MPU.

Provides "Trigger-Hold-Off" logic.

Provides Transition Detection Logic and Digital Filtering Logic for both Enable and Trigger signals from the Front End board.

Trigger Delay counter determines the "END OF RECORD" as specified by the MPU. May be N clocks after trigger or may be 500 clocks after the Nth Trigger event.

Provides clock and control signals to the High-Speed Memory boards (2).

Provides "RECORD CONTROL STATUS" information to the MPU.

Switches allow user selection of power-up initialization conditions for threshold selection TTL/ECL (on all inputs), clock selection INT/EXT $\int$, and trigger hold-off ON/OFF.

4.2.5 Threshold/GPIB

Completely controlled by MPU as memory mapped I/O.

GPIB circuitry was never utilized on this board (refer to 0112-1040).

Generates threshold levels-

TTL +1.4 nominal *
ECL -1.3 nominal *

*both are internally adjustable from -2.0 V to +2.0 V.

VAR A **
VAR B **

**MPU programmed D/A converters that provide outputs from -6.40 V to +6.35 V in 0.05 V steps.

Selects any one of the four threshold levels to be provided to each of the twenty input probes.

4.2.6 CRT Display

7 in. CRT (Diagonal measure).

Viewing area (3/8 in. x 5.0 in.).

Raster scan type display.

Requires +15 VDC at 1 A.

TTL inputs for Video, Horiz.Sync, and Vertical Sync.

4.2.7 Front Panel and Keyboard

Interfaces to the MPU address (3 LSBs only) and Data Bus.

Completely controlled by MPU.
Scanning is done by the MPU with memory mapped I/O.

(Scan rate is 60 Hz or 50 Hz).

Forty-seven keys on keyboard plus eight momentary switches on the front panel.

Two LEDs {"Power on" / "Error"} under MPU control.

Connectors for the input probes provide separation of (power, ground, thresholds) and (input signals) and connectors to route them to their destination.

Circuitry for detection of special input adapter probes. (E.g., K100-D/32, 32-channel adapter.)

4.2.8 Probes

Unique hybrid design gets active circuitry close to the input signal source (3 in. normally). Reduces loading effects.

Hybrid contains--

FET input buffer (allows 1 MΩ input impedance).

Threshold Detector (±10 V range).

ECL differential line driver.

Signal ground isolation from power ground.

Removable input wires allow flexibility.

4.2.9 Unregulated Supply

Provides for input line voltage selections of 100 V, 120 V, 220 V, 240 V nominal ±10%.

Provides 120 V ±10% for the fan.

Has fuse and RFI filter unit.

Provides four unregulated DC voltages.

+7 V min./+10 V max. for +5 V reg.
-7 V min./-10V max. for -5.2 V and -2.0 V reg.
+17 V min./+25 V max. for +15 V and +12 V reg.
-17 V min./-25 V max. for -12 V reg.

4.2.10 Regulator

Voltage reference (early boards)

+5 V reg.
-5.2 V reg.
-2.0 V

Overvoltage protection.

Current limit circuit (+5 and -5.2).

+15, +12, -12 V three terminal regulators.

4.3 Detailed Description

4.3.1 MPU and Address Decoding (Refer to Figure 4.2A)

The MPU board is a complete microcomputer. It includes the MPU (6800), 32K bytes of dynamic RAM (Random Access Memory), 24K bytes of ROM (Read Only Memory), the CRT display controller, Input/Output address decoding, keyboard scan interrupt logic, and timing generation for the MPU and the CRT controller.

The MPU is a standard 6800 and is operated at a 1-MHZ clock rate. The 16 address lines are buffered by 74LS244s (at locations B11 and D13) and are terminated by 220/330 Ω thevinin terminations (at locations D14 and C11). The eight data lines are buffered by 74LS244s (at locations E9 and E10) and are terminated by 220/330 Ω thevinin terminations (at location D5).

The addresses are decoded into 16K byte pages and separated for Read or write by a 74LS138 (at location E8). The pages are used as shown in Table 4.1.

Table 4.1

Page	Hex Addresses	
0	0-3FFF	RAM (used by MPU and CRT)
1	4000-7FFF	RAM (used by MPU only)
2	8000-BFFF	I/O and ROM
3	C000-FFFF	ROM only

This address decoder is enabled by the signals VMA (Valid Memory Address) and Ø2 (phase two) to ensure that the decoder outputs are always valid and glitch free. The page 0 and 1 write outputs of this decoder directly drive the WE (write enable) lines of the RAMs and the read outputs enable the buffers that read the data from the RAMs to the DATA Bus. The page 2 read output is gated with address A13 so that the first half of this page (i.e., when A13 is low) enables the I/O address decoders and the second half of this page (A13 high) enables the address decoder for the first four ROMs (ROM 0,1,2,3). The page 3 read output enables the address decoder for the other eight ROMs (ROM 4 through ROM B).

The ROM address decoder consists of two 74LS244s (at locations B10 and D8), and it decodes an enable signal for each of the 13 ROMs. The ROM address lines and the ROM data output lines are buffered to reduce loading on the bus and to increase the output drive capability of the ROMs.

The I/O address decoders provide a Read Enable (RE) and a Write Enable (WE) signal for each I/O device. This simplifies the interface circuitry required on each I/O device. This decoder provides signals listed in Table 4.2.

Table 4.2

Hex Address	Signal Name	Description
8000-83FF	RRE1	Ram Read Enable 1 (used for CH 0-7 high speed RAM)

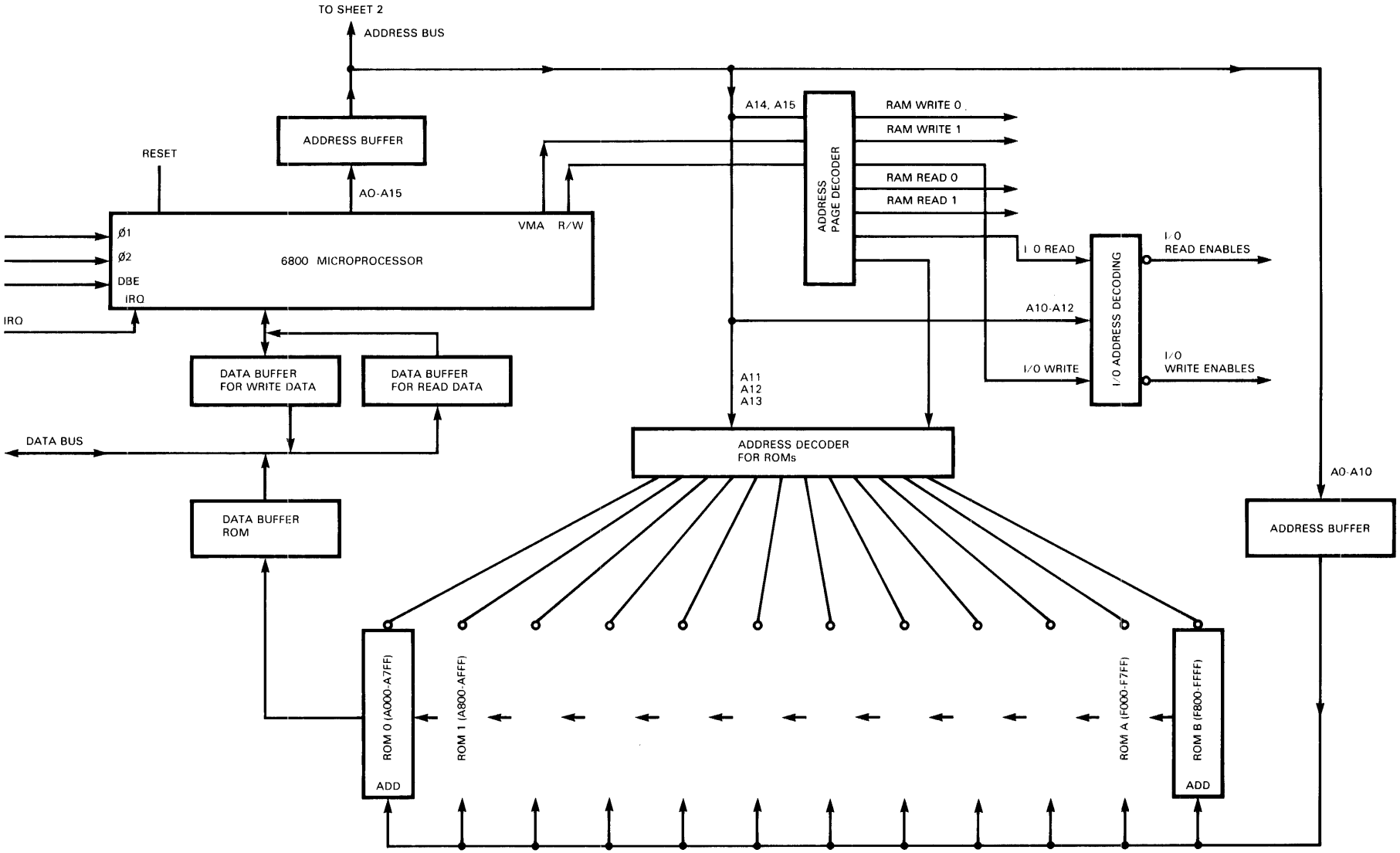


Figure 4.2A Block Diagram of MPU Board

Hex Address	Signal Name	Description
	RWE1	Ram Write Enable 1 (not used)
8400-	RRE2	Ram Read Enable 2 (used for CH 8-F high speed RAM)
	RWE2	Ram Write Enable 2 (not used)
8800-	CRE	Control Read Enable (reads status of record control)
	CWE	Control Write Enable (control words for record control board)
8C00-	FERE	(not used)
	FEWE	Front End Write Enable (trigger/enable/clock select/sample)
9000-	GPRE	GPIB Read Enable*
	GPWE	GPIB Write Enable* *not used.
9400-	FPRE	Front Panel Read Enable (keyboard scanning)
	FPWE	Front Panel Write Enable (error lite)
9800-	-	not used
	-	not used
9C00-9FFF	-	not used
	-	not used

Each I/O device is decoded as a 1K byte page even though no more than 16 bytes are used by any I/O device. This is done to make the decoding simpler. The read enable signals are enabled by the Ø2 clock and they are used by the I/O devices to enable 74LS244 buffers that place the data onto the DATA BUS.

The Write Enable signals are enabled by a special clock CP2P, which clocks 50 ns before the end of Ø2. This allows for prop. delay in the Write Enable decoder and in the I/O devices. The rising edge of these signals are used to transfer the data from the DATA BUS to holding registers in the I/O devices.

4.3.2 RAM (Refer to Figure 4.2B)

The dynamic RAM uses sixteen 16K x 1-bit dynamic RAM ICs of the 4116 type. Locations B1 through B8 are addressed as page 0 (add 0-3FFF) and locations C1 through C8 are addressed as page 1 (addresses 4000-7FFF). The dynamic RAMs are run with a 500 ns READ/WRITE cycle. The RAM is organized as a two port split-phase memory system that allows transparent DMA access for the CRT controller. The MPU and the CRT controller are synchronized in such a way that the RAM performs two complete Read/Write cycles every 1 µs. The first cycle occurs during Ø1 and is used by the CRT controller to read the display data. The second cycle occurs during Ø2 and may be used by the MPU to either Read data (from the RAM to the MPU) or Write data (from MPU to RAM).

Refer to Figure 4.2C for a detailed timing diagram of the RAM operation, the MPU clock generation, and the CRT data transfer.

The RAM operation is as follows:

1. Arbitrarily define T=0 at the trailing edge of Ø2 at T=0. The CRT row address (bits 0-6) is gated to the RAM address pins and RAS is already high.
2. At T=50 ns, CAS is brought high completing the previous cycle.
3. At T=100 ns, RAS is brought low; transferring the row address into the RAM chips.
4. At T=150 ns, the CRT row address is removed and the CRT column address (bits 7-13) is gated to the RAM.
5. At T=200 ns, CAS is brought low; transferring the column address into the RAM chips.
6. At T=400 ns, RAS is brought high and the CRT column address is removed.
7. At T=500 ns, the RAM output data is transferred into the CRT data shift register (location D7). Also, at T=450 ns, the MPU row address (A0-AG) is gated to the RAM inputs for the next RAM cycle.

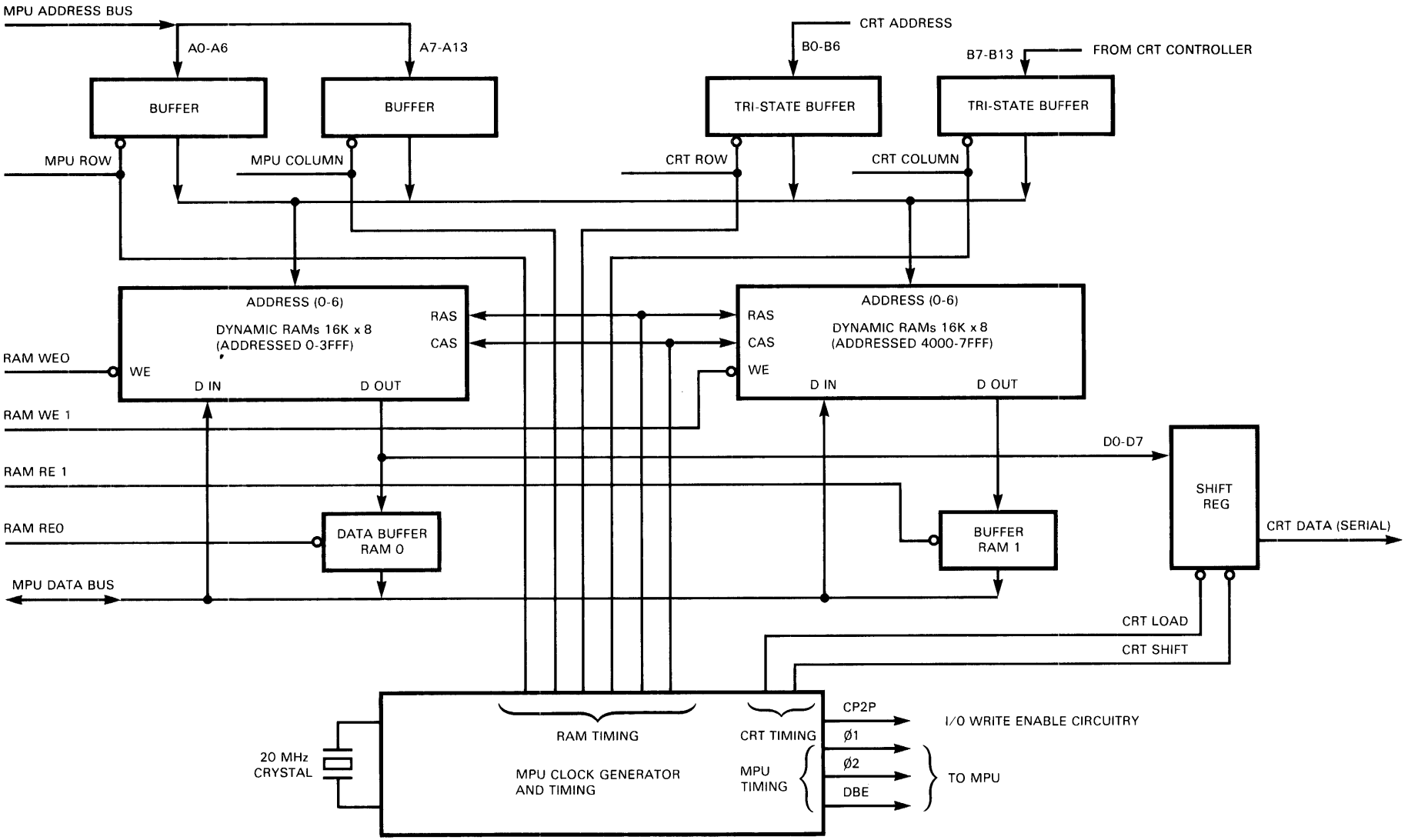


Figure 4.2B Block Diagram of RAM

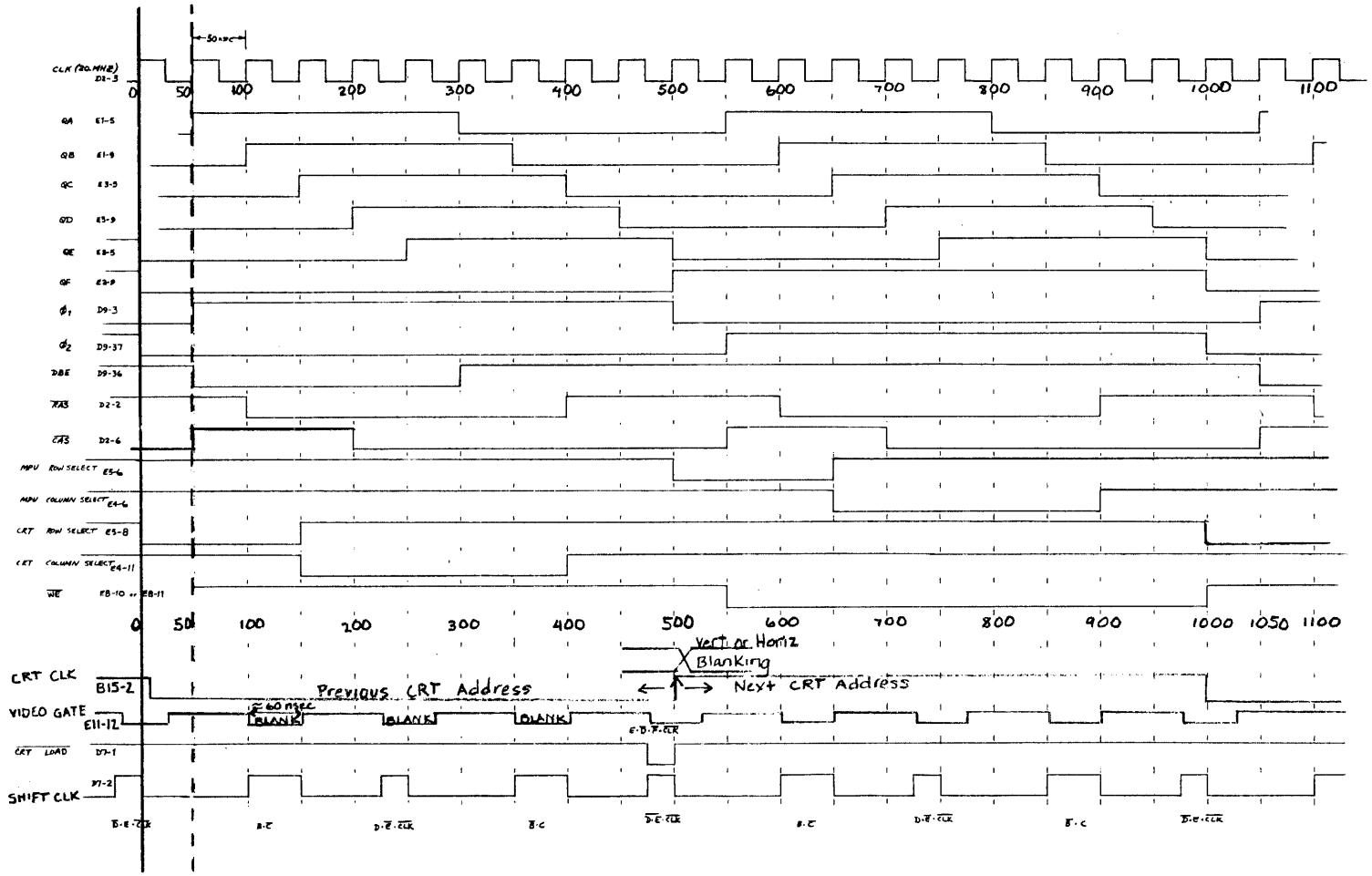


Figure 4.2C Timing Diagram of RAM Operation

8. At T=550 ns, CAS is brought high completing the first RAM cycle; also, if the MPU is doing a write cycle, the WE line will be brought low.
9. At T=600 ns, RAS is brought low; transferring the MPU row address into the RAM chips.
10. At T=650 ns, the MPU row address is removed and the MPU column address is gated to the RAM inputs.
11. At T=700 ns, CAS is brought low; transferring the MPU column address into the RAM chips.
12. At T=900 ns, RAS is brought high.
13. At T=1000 ns, the RAM data is transferred to the MPU if the MPU is doing a read cycle. Or, at T=1000 ns, WE is brought high if the MPU is doing a write cycle.
14. At T=1050 ns, CAS is brought high completing the second RAM cycle. Also, at T=1000 ns, the CRT row address is gated to the RAM inputs for the next RAM cycle.

The RAM is automatically refreshed for the row addressed by each cycle. And, because the CRT controller increments its address every 1 μs, all of the row addresses will be accessed approximately every 128 μs.

4.3.3 MPU Clock Generation

The MPU clock generation makes both Ø1 and Ø2 450 ns wide and provides 50 ns between them on both edges. To meet the 6800 specified logic levels for Ø1 and Ø2, a special driver circuit is made by paralleling six CMOS inverters for each clock phase (locations C9 and C10).

4.3.4 CRT Data Transfer

The CRT data transfer cycle operates as follows:

1. The trailing edge of Ø1 is used to clock everything in the CRT controller except for the data shift register (the signal is called CRT CLK).
2. The RAM data is loaded into the shift register (location D7) 25 ns before the trailing edge of Ø1. At this time data bit 7 from the RAM is presented at the output of the shift register.
3. The signal SHIFT CLK is generated by a 74S65 (location F3) to provide a clock edge every 125 ns. This clock shifts the data in the shift register eight times for each data byte from the RAM. Presenting the data bits in sequence 7/6/5/4/3/2/1/0.
4. A video gating pulse is generated by a 74LS123 (location E11) and blanks the video for appoximately 50 ns immediately following each SHIFT CLK. This prevents display of erroneous data during the propagation time of the ICs and it also creates the video "DOT" for each data point on the CRT.
5. The CRT video is the combination of the serial RAM data from the shift register and the three blanking signals (video gate, horizontal blanking, and vertical blanking).

4.3.5 CRT Controller

The CRT controller is shown in the block diagram of Figure 4.2D and in the schematic in Section VII, Figure 7.11 (sheet 3). The desired CRT Display pattern is computed by the MPU and stored in the RAM as a complete "DOT MAP"; i.e., every "dot" location of the CRT is represented by a bit in the RAM ("1"=white, "0"=black). A typical procedure for the MPU is:

1. The CRT display addresses are all set to zero (blanking the CRT).
2. The MPU converts each displayed character into a pattern of "1s" and "0s" and stores them in the proper locations in RAM.
3. The CRT controller continuously cycles through the RAM and transfers the information to the CRT. Each RAM byte is read from RAM and converted into a string of eight "DOTs" on the CRT.

The CRT controller generates a standard "RASTER SCAN" display format with data being presented as a series of horizontally scanned lines. Each horizontal line is presented starting at the left side and proceeding to the right side. The first horizontal line displayed is at the top and the last is at the bottom. Sync and blanking signals are generated per the standard.

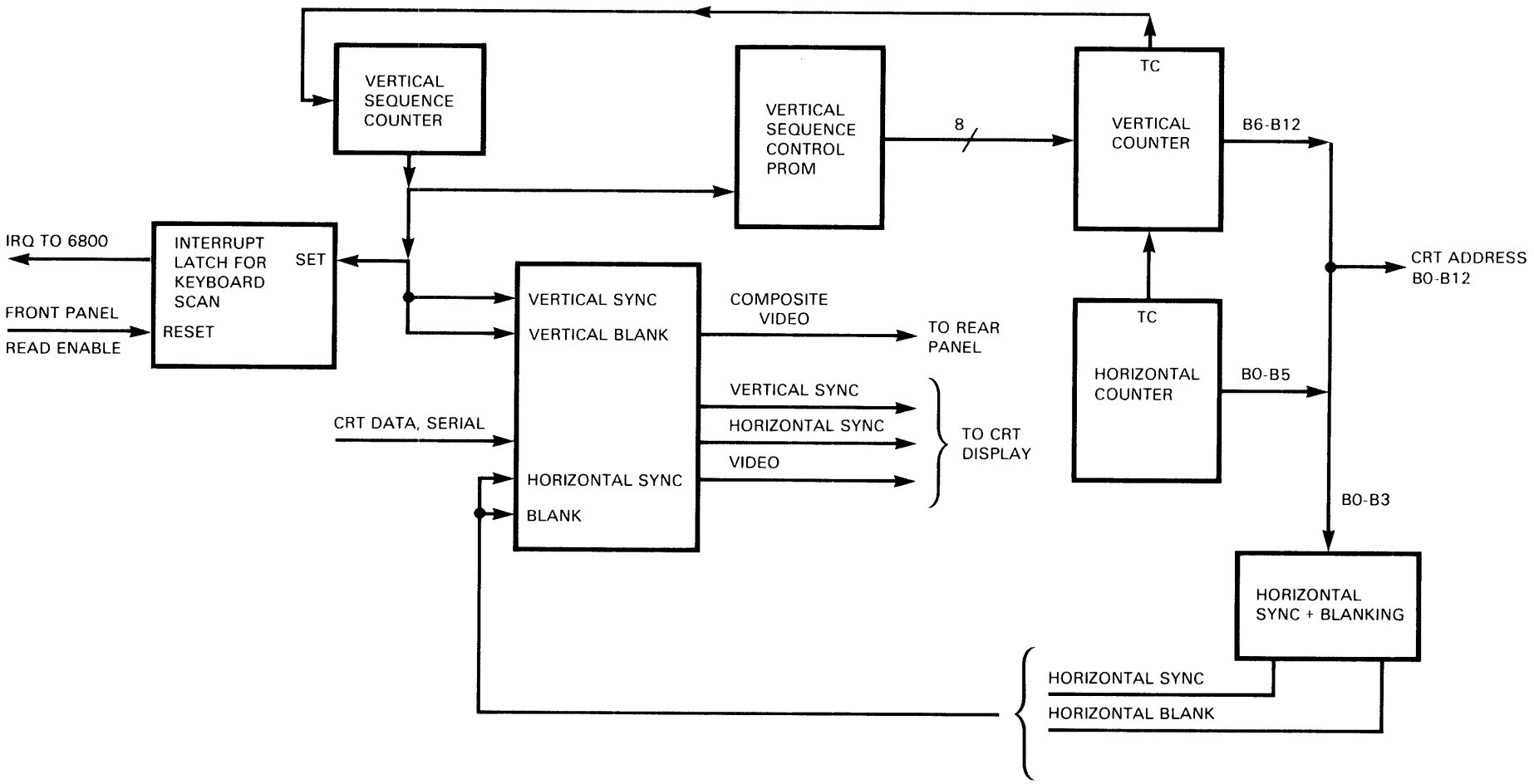


Figure 4.2D Block Diagram of CRT Controller

4.3.5.1 Horizontal (Refer to Figure 4.3A)

Each horizontal scan line is 64 μs and presents 52 μs of video with 12 μs blanked and a 5 μs sync pulse during the blank time. This horizontal sequence is generated by the circuitry as follows.

1. The 74LS161s (locations B14 and B15) run continuously and count from 0-63 repeatedly. Note that only 6 bits are used and that the two used bits are always set to "1s." The outputs of this 6-bit counter are referred to as the Horizontal Address.
2. The horizontal blanking pulse is generated by the 74LS112 (location B17) and goes true (i.e., blanked) at address 0 and false (unblanked) at address 12. Thus addresses 0 through 11 are blanked and addresses 12-63 are unblanked. Note that the data from the RAM is delayed by one clock when it is strobed into the data shift register. Thus the actual displayed data is from address 11 through address 62.
3. The horizontal sync pulse is generated by the 74LS112s (locations B17 and B18) and the 74LS11 (location B16) and goes true for addresses 1 through 5.
4. The horizontal scan is not affected by the position of the 50 Hz/60 Hz jumper.

4.3.5.2 Vertical (Refer to Figure 4.3B)

The vertical address is generated by two 74LS161s (locations C16 and C17) forming an 8-bit binary counter. This counter is controlled by the PROM (location D16) and the vertical sequence counter (74LS161 at location D15). The vertical sequence is generated as follows.

For 60 Hz operation,

1. assume the sequence counter is at zero (D15). The PROM will be addressed to 24 and its output should be 10_{hex} (refer to the table on sheet 3 of Figure 7.11).
2. when the vertical address counter reaches TC, then at the next line (TC from the horizontal address) the vertical address counter will be present to "10"$_{(hex)}$ and the vertical sequence counter will advance to 1. This begins the vertical unblanked display (which will last for 240 lines).
3. The vertical address counter will then continue to increment at the beginning of each horizontal line until it reaches TC (FF_{hex}). At the beginning of the next line, the vertical address counter will be preset to "FD" hex and the vertical sequence counter will advance to 2. This begins the blanked portion of the vertical sequence.
4. The sequence counter will remain at 2 for three lines (192 μs) and then advance to 3. This will initiate vertical sync and preset the address counter to "FD" again. Vertical sync will remain true for 3 lines (192 μs) until the counter again reaches TC ("FF").
5. the secquence counter will advance to 0 and the vertical address counter will be preset to "F1" hex. This state provides a vertical retrace delay of 15 lines (960 μs).
6. The process returns to step 1 above.

For 50 Hz operation:

The PROM values are changed so as to change the length of time spent in the sequence state as shown in Table 4.3.

Table 4.3

State	60 Hz	50 Hz	
0	15 lines	40 lines	Delay from sync to scan.
1	240 lines	240 lines	Scan (i.e., display).
2	3 lines	28 lines	Delay from scan to sync.
3	3 lines	3 lines	Sync pulse.

Note that the scan (display) and the vertical sync remain the same and the extra time is divided equally between the two delays. This keeps the display centered vertically.

The PROM values are determined by taking the desired length of the next state and subtracting it from 256 and converting the answer to hex.

PROM = (256 - length)

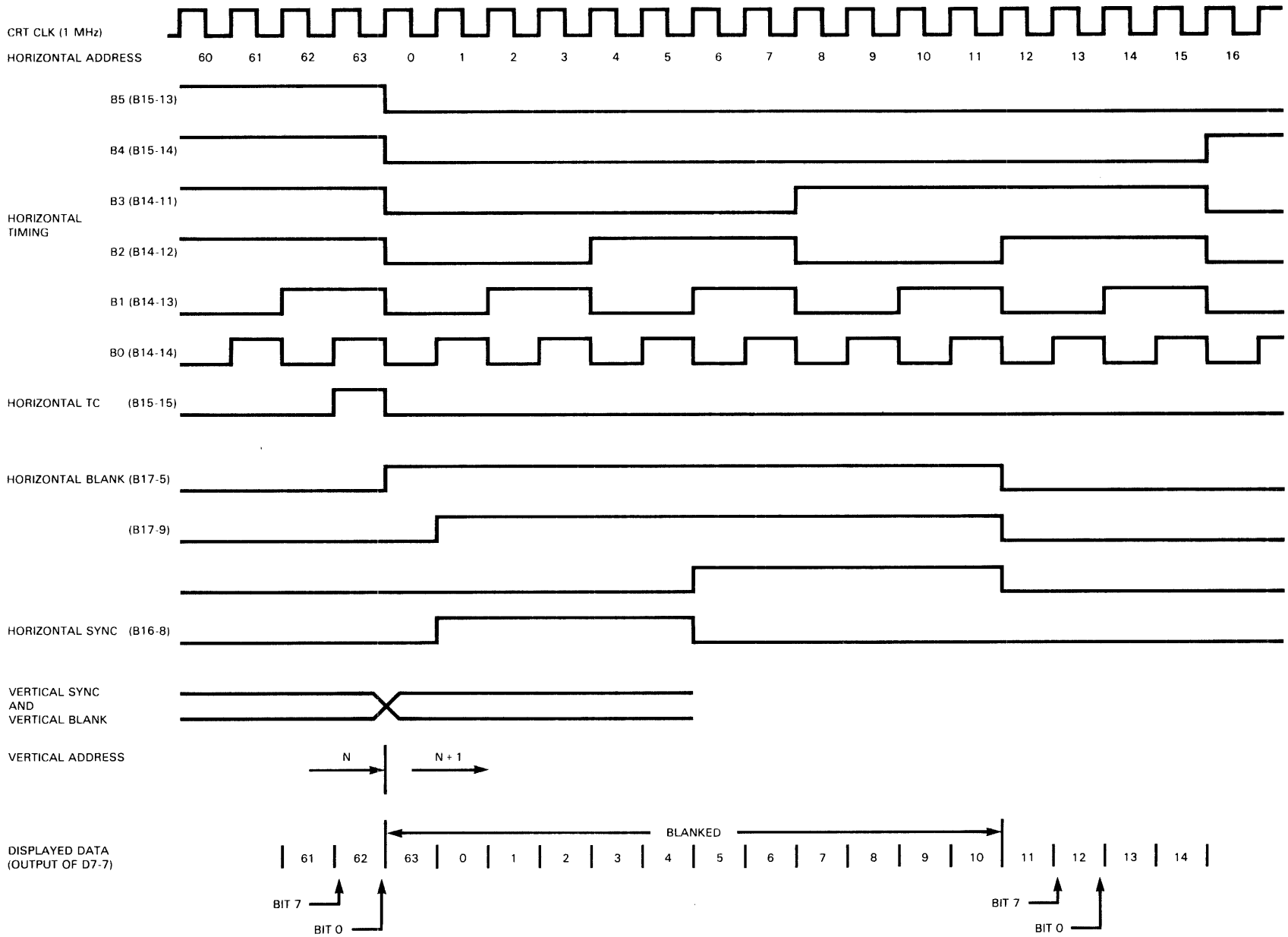
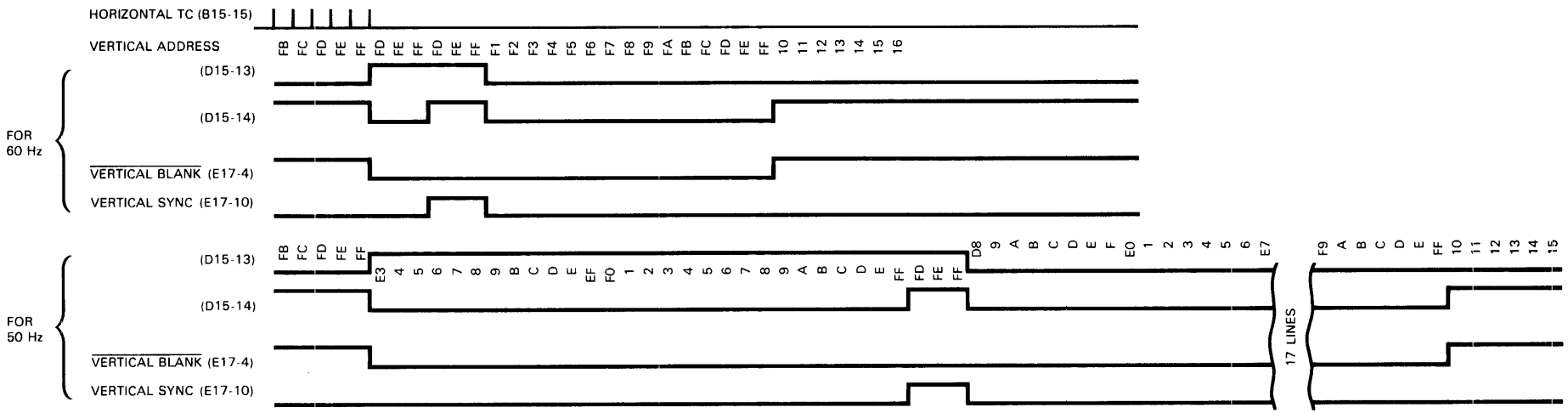


Figure 4.3A CRT Horizontal Timing



FOR 60 Hz

64 μs PER HORIZONTAL LINE

21 LINES BLANKED:
- 3 LINES DELAY
- 3 LINES VERTICAL SYNC
- 15 LINES DELAY

240 LINES DISPLAYED

261 LINES TOTAL

× 64 μs

16,704 μs ⟶ 59.74 Hz

FOR 50 Hz

71 LINES BLANKED:
- 28 LINES DELAY
- 3 LINES VERTICAL SYNC
- 40 LINES DELAY

240 LINES DISPLAYED

311 LINES TOTAL

× 64 μs

19,904 μs ⟶ 50.24 Hz

Figure 4.3B CRT Vertical Timing

For example:

PROM (state 0)=(256-length of state 1)
=(256-240)
=(16)
=10 hex

The correct PROM values are shown in Table 4.4

Table 4.4

State	Prom Addr. (dec.)	Prom Data (hex)	Delay # of lines	
0*	16 (20)	10	240	
1*	17 (21)	E4	28	
2*	18 (22)	FD	3	total 311 lines
3*	19 (23)	D8	40	
0**	24 (28)	10	240	
1**	25 (29)	FD	3	
2**	26 (30)	FD	3	total 261 lines
3**	27 (31)	F1	15	

* 50 Hz
** 60 Hz

Note that the values are repeated twice for each state. This is because the third output of the vertical sequence counter is connected to the PROM address input to allow for the possibility of generating an "interlaced" raster scan display. If interlaced scan were desired, then pin 14 of the PROM (location D16) would be jumpered to ground and another set of values would be programmed into the first 16 locations of the PROM. The interlaced scan technique was evaluated for the K100-D and was found to have an undesirable flutter effect. Therefore, the first half of the PROM is left unprogrammed and the third bit of the counter is not used.

Note that the PROM table given on sheet 3 of Figure 7.11 may be in error. The specification drawing for the PROM (P/N 0112-0064) gives the correct values.

4.3.5.3 CRT RAM Addressing (Refer to Figure 4.3C)

The CRT address that is presented to the RAM is formed by combining the horizontal address and the vertical address as shown in Table 4.5.

Table 4.5

RAM address	13	12	11	10	9	8	7	6	5	4	3	2	1 0
6-bit horizontal address									5	4	3	2	1 0
8-bit vertical address	13	12	11	10	9	8	7	6					
RAM row address								6	5	4	3	2	1 0
RAM column address	13	12	11	10	9	8	7						

The RAM address may be calculated from the vertical address and the horizontal address by the following formula.

RAM address (decimal)=Horiz.Add +
(Vertical Add x 64)

or

RAM address (hex)=Horiz.Add(hex) +
(Vertical Add (hex) x 40 (hex))

The first displayed dot of each horizontal line is bit 7 of Horiz. Add 11 and the last displayed dot is bit 0 of Horiz. Add 62.

The first displayed line is Vertical Add=16 (or 10 hex) and the last line is Vertical Add = 255 (or FF hex)

Thus the first dot of a raster is

RAM add (first dot)=B_{hex}+ (10_{hex} x 40_{hex})=40B(hex) bit 7

RAM add (last dot)=$3E_{hex}$+(FF_{hex} x 40_{hex})=3FFE(hex) bit 0

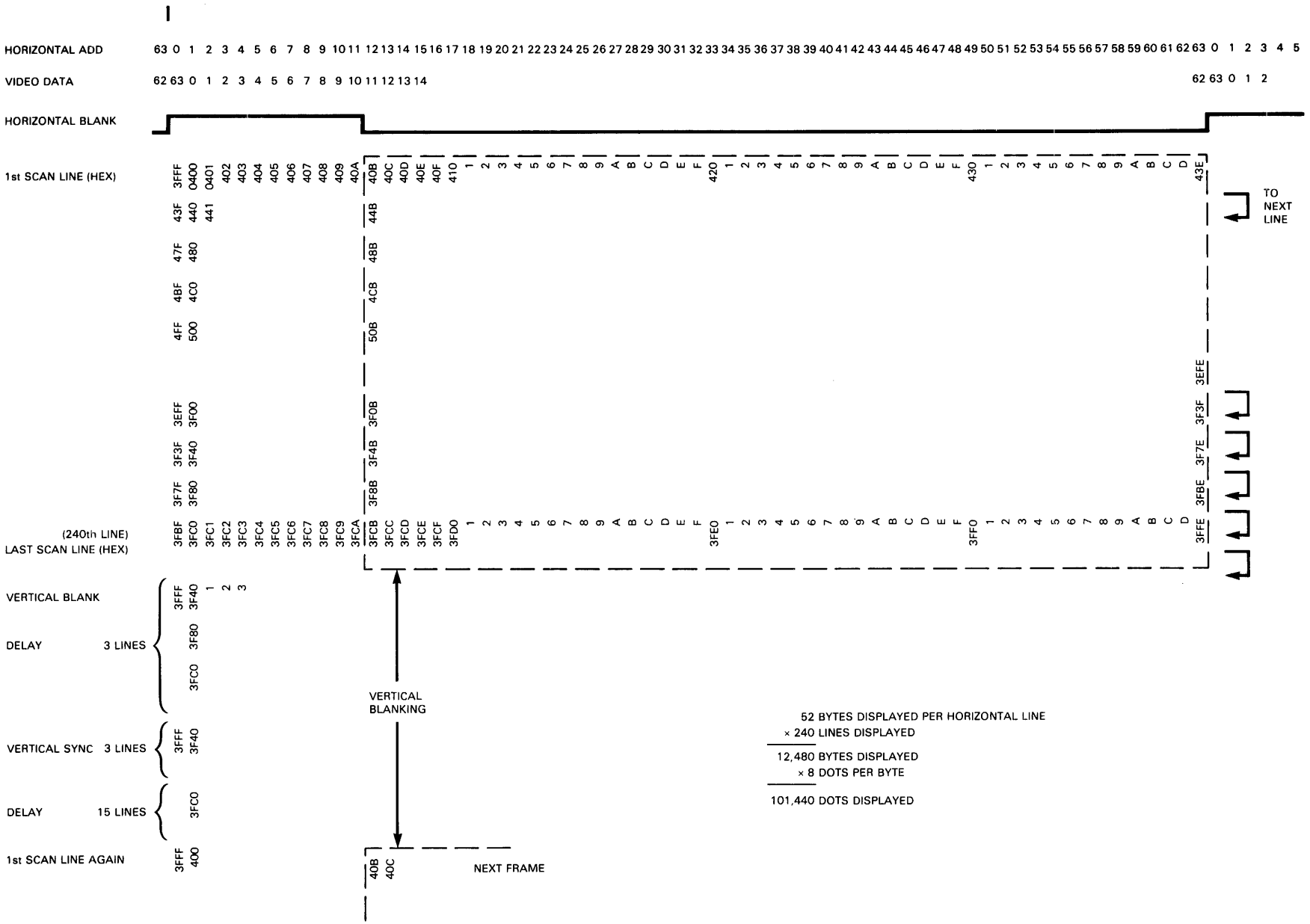


Figure 4.3C CRT RAM Addressing

4.4 Front End

The Front-End board provides the input probe line receivers, input sampling, combination detectors, and clock selection. Figure 4.4 is a block diagram of the Front-End board.

4.4.1 Input Probe Line Receivers

The input probes (discussed in detail later) provide a differential ECL signal. These signals are received on the Front-End board by differential line receivers (10216 type). There are 20 input signals; 16 data, two trigger qualifiers, one clock qualifier, and one external clock.

4.4.2 Input Sampling

The input sampling circuit (for channel 0 only) is shown in Figure 4.5. Note that all termination resistors are omitted. This circuit can operate in either "sample" or "latch" mode as controlled by the MPU.

For "Sample" mode, the signal from 5B-4 (CH 0 Sample mode) is HI and this forces 1C-3 and 1C-2 low and enables the 10130 (1E) such that the output (1E-2) follows the input (1E-7). The 10231 (1H) then samples the input data each time it is clocked.

For "Latch" mode, the signal from 5B-4 is LOW and this allows the 10130 to operate as a latch. The D input (1E-7) of the 10130 no longer has any effect on the output. The outputs now are determined by the signals at the direct set (1E-5) and the direct reset (1E-4) input as follows:

1. Assume 1E-2 and 1H-2 are HI to start.

2. The input 1C-5 is high and 1C-3 is held low. Thus, no signal can be applied to 1E-5 as long as 1H-2 is HI.

3. The input 1C-9 is low, allowing any low input signal to reset the latch (by placing a high on the direct reset (1E-4)).

4. The latch remains in this state regardless of any other activity on the input signal (thus it is referred to as "latched").

5. At the next clock the 10231 goes to a low (on 1H-2) and

6. the latch is enabled to respond to a high input signal only.

7. If, at any time, the input signal goes high, signal 1A-14 goes low and 1C-3 goes high and sets the latch to a high for the next clock.

4.4.3 Combination Detectors

There are three combination detectors; asynchronous trigger, synchronous trigger, and enable. Both the asynchronous and the synchronous trigger detectors are controlled by the same selection register from the MPU. The asynchronous trigger detector monitors the data at the output of the latch (10130) before it has been sampled by the 10231. This detector provides an output signal whenever the specified combination is true. The delay from signal input to trigger output is the delay of the probes and the gates only and is not affected by the K100-D sample clock. This delay is typically 40-50 ns.

The combination detector circuit is shown in Figure 4.6. The circuit is shown for the synchronous trigger detector only and channels 0, 1, 2, and 3 only. Note that the data has been sampled by the K100-D clock before being presented to the combination detector. Each channel has two select lines from the MPU and they are active low. Select HI is low if that channel was specified to be a high by the operator and select LO is low if low was specified. If "X" (don't care) was specified, then both select HI and select LO are high. The terms HI and LO correspond to "1" and "0" when positive logic polarity is specified by the operator. If negative logic polarity is used, then HI corresponds to "0" and LO corresponds to "1." Each gate in the detector circuit is drawn as an "AND" gate and is programmed by the MPU to respond to a condition that would cause the trigger to be false (i.e., <u>not trigger</u>). For example, if CH 0 select HI is active (low) <u>and</u> the CH 0 data is low, then the output (1J-3) is forced high (indicating <u>not</u>

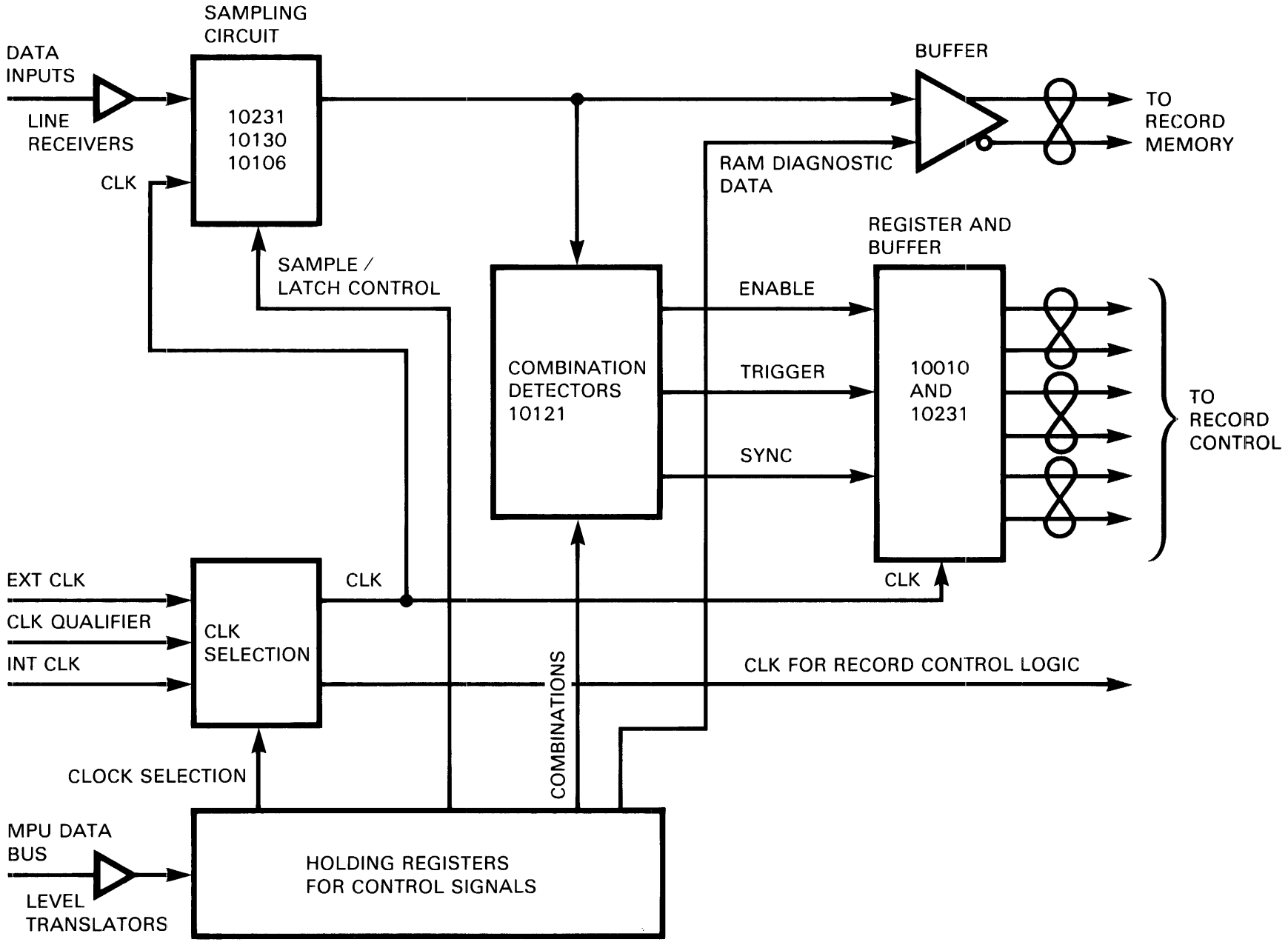


Figure 4.4 Block Diagram of Front-End Board

(PIN NUMBERS AND REFERENCE DESIGNATIONS ARE
SHOWN FOR CHANNEL O)

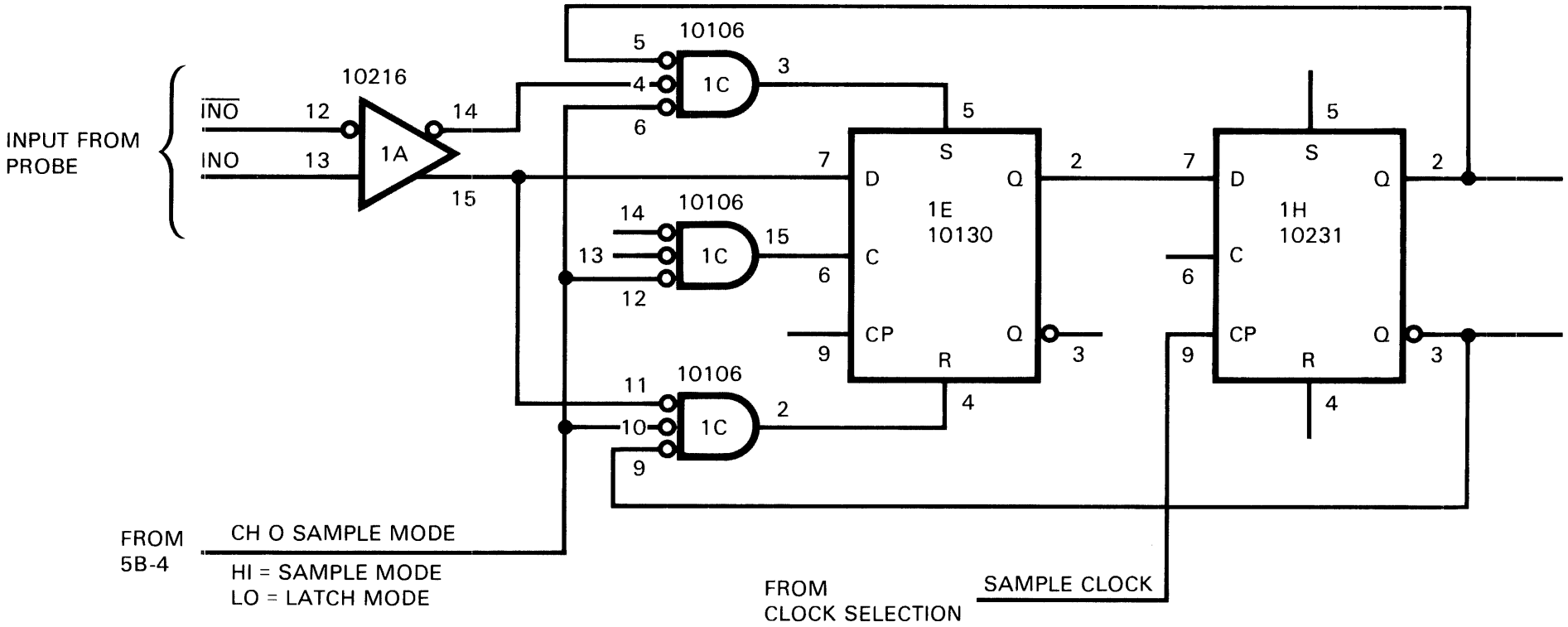


Figure 4.5 Input Sampling Circuit

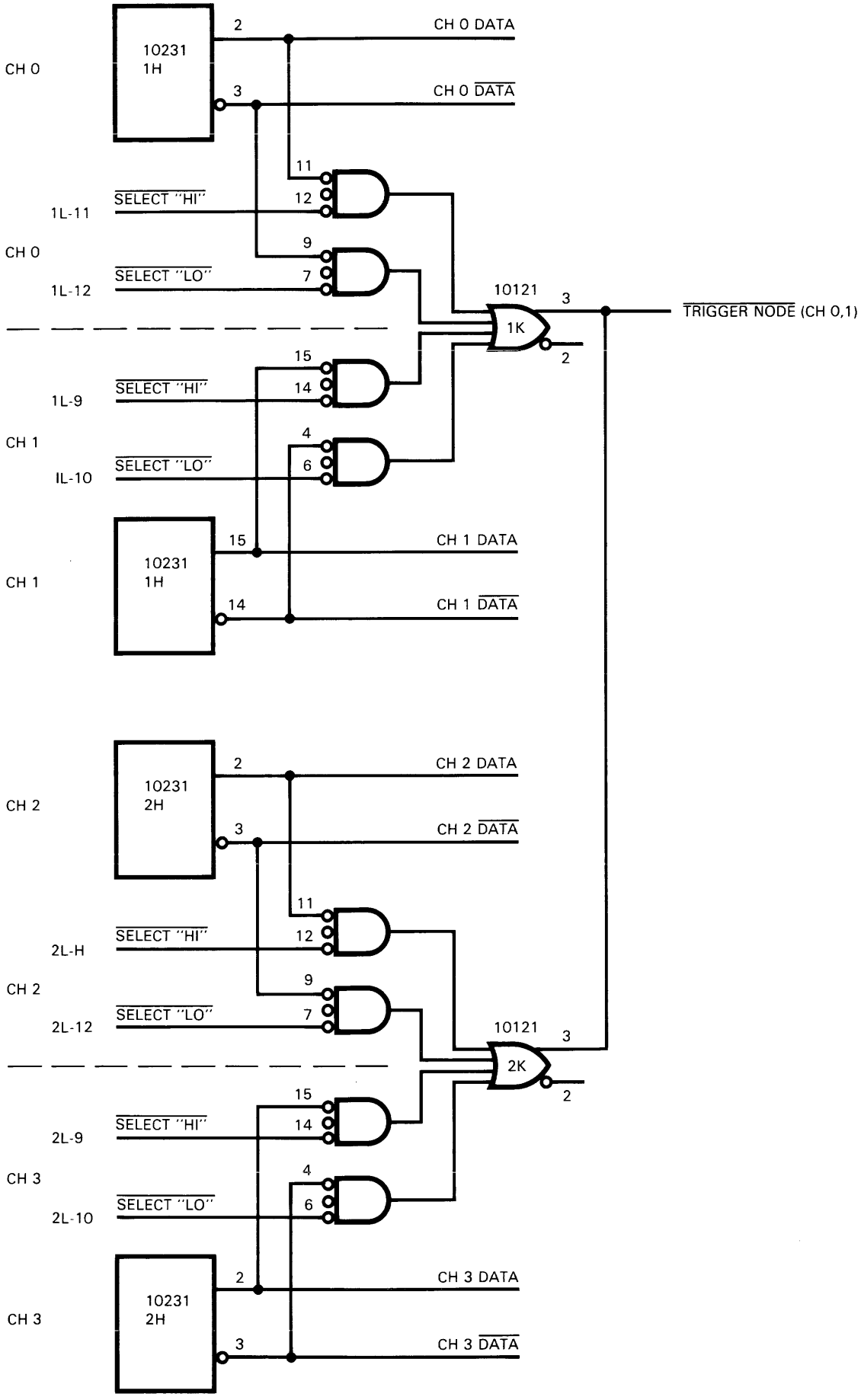


Figure 4.6 Combination Detector Circuit

trigger detected). To have the trigger detected (1J-3 low), the CH 0 data must be high.

Each 10121 in the detector handles two data channels. There are a total of nine 10121's for each combination detector (eight for the 16 data channels and one for the two qualifiers). To get the complete trigger for all 18 inputs, the outputs (pin 3) of all nine 10121's must be logically OR'ED together. Figure 4.7 shows how this is done.

To achieve operation at 100 MHz clock rate, the trigger node must be broken into several smaller nodes. This keeps the capacitive loading down and also reduces the problem of glitches that can be generated in a large "wired-OR." The trigger node is broken into four partial nodes (Ta, Tb, Tc, and Td). The propagation delay up to this point is typically about 9-10 ns. This is the propagation delay of the sampling 10231 (location 1H) and the 10121 (1K) and the extra delay caused by the extra heavy loading on both. The register at location 7K (10010 or 10016) serves two purposes; it resynchronizes the nodes with the clock and it buffers the nodes so that they can be "wired-OR'ED." The clock to this register is delayed by approximately 2 ns (18 in. of twisted pair) to allow the required set-up time (1 ns minimum). The flip-flop (10231 at location 6H) also serves two purposes; it provides differential drive for sending the signal to the Record Control board and it resynchronizes the signal to the clock with minimum propagation delay. The extra 2 ns of delay caused by delaying the clock to the register adds to the propagation delay of the register such that the total propagation delay (as seen by 6H) is approximately 6-8 ns. Because the 10231 at 6H does not have its clock delayed, the effect of delaying the clock to the 7K register does not affect the propagation delay of the signal being transmitted to the Record Control board.

4.4.4 Enable

The Enable combination detector works the same as the Trigger.

The asynchronous trigger detector circuit is the same as Figure 4.6 except that the data is taken from the outputs of the latch (10130) instead of from the sampling flip-flop (10231). This means that the data has not been clocked by the sample clock. Also, because the asynchronous trigger is not clocked, the trigger node is formed by a simple "WIRED-OR" of all nine 10121s and then buffered by a 10117 (6E) for transmission to the Record Control board.

The sampled data is buffered by 10117s and driven on twisted pairs to the Record Memory boards. The 10117s also provide a means for the MPU to turn off the sampled data and substitute diagnostic data instead.

4.4.5 Clock Selection

Clock selection and distribution is done by four 10211s (locations 7C, 7E, 7H, and 7J). Figure 4.8 shows half of the circuit; refer to the schematic for the other half. The four gates (in each half of the circuit) form a "Wired-OR." This allows for the selection of one of three clock sources; Internal, External positive edge, or External negative edge. The fourth gate is used for the clock qualifier. Each gate has three identical outputs. Thus a total of six clock circuits are formed that allow each clock circuit to drive two or three inputs. The MPU controls the selection of one of the three clock sources and the clock qualifier is enabled by the hardware whenever external clock is selected. Figure 4.8 shows an "OR" gate that enables the qualifier circuit. This "OR" gate is made by a "wire-OR" of two unused 10216 gates (10A and 9A) followed by a third unused 10216 (11A) that inverts. These 10216 are converted from differential line receivers to one-input buffers by connecting one of their inputs to a bias voltage source (-1.3 V), which is supplied by pin 11 of each 10216.

4.4.6 Control Signals

The control signals for the Front-End board are transferred from the MPU to holding registers on the Front-End board. Because all of the logic on the Front-End board is ECL, the holding registers are operated between ground and -5.2 V. To communicate with the MPU (which is TTL), the MPU data bus and address lines (3) are translated by

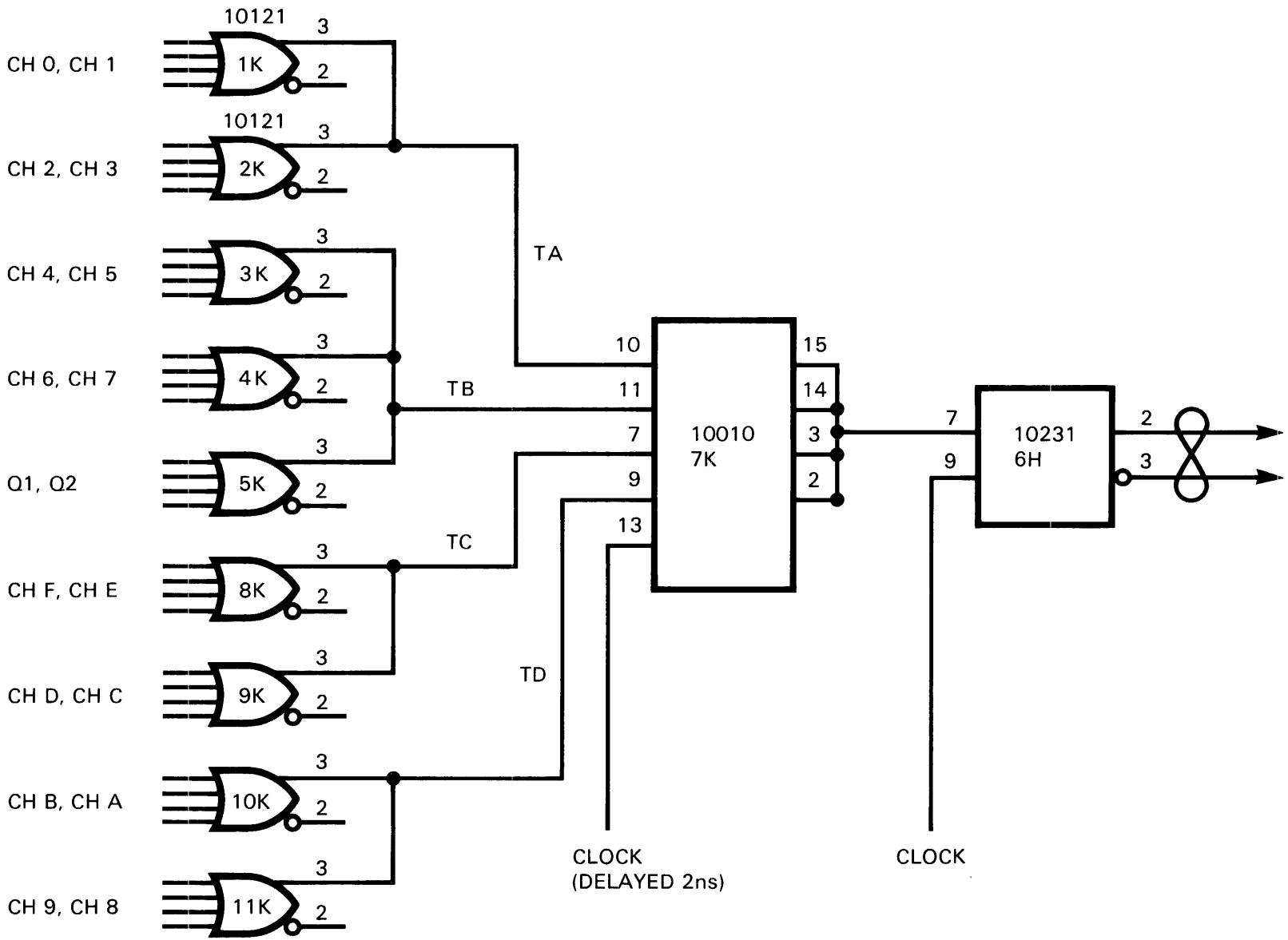


Figure 4.7 Trigger Node Formation

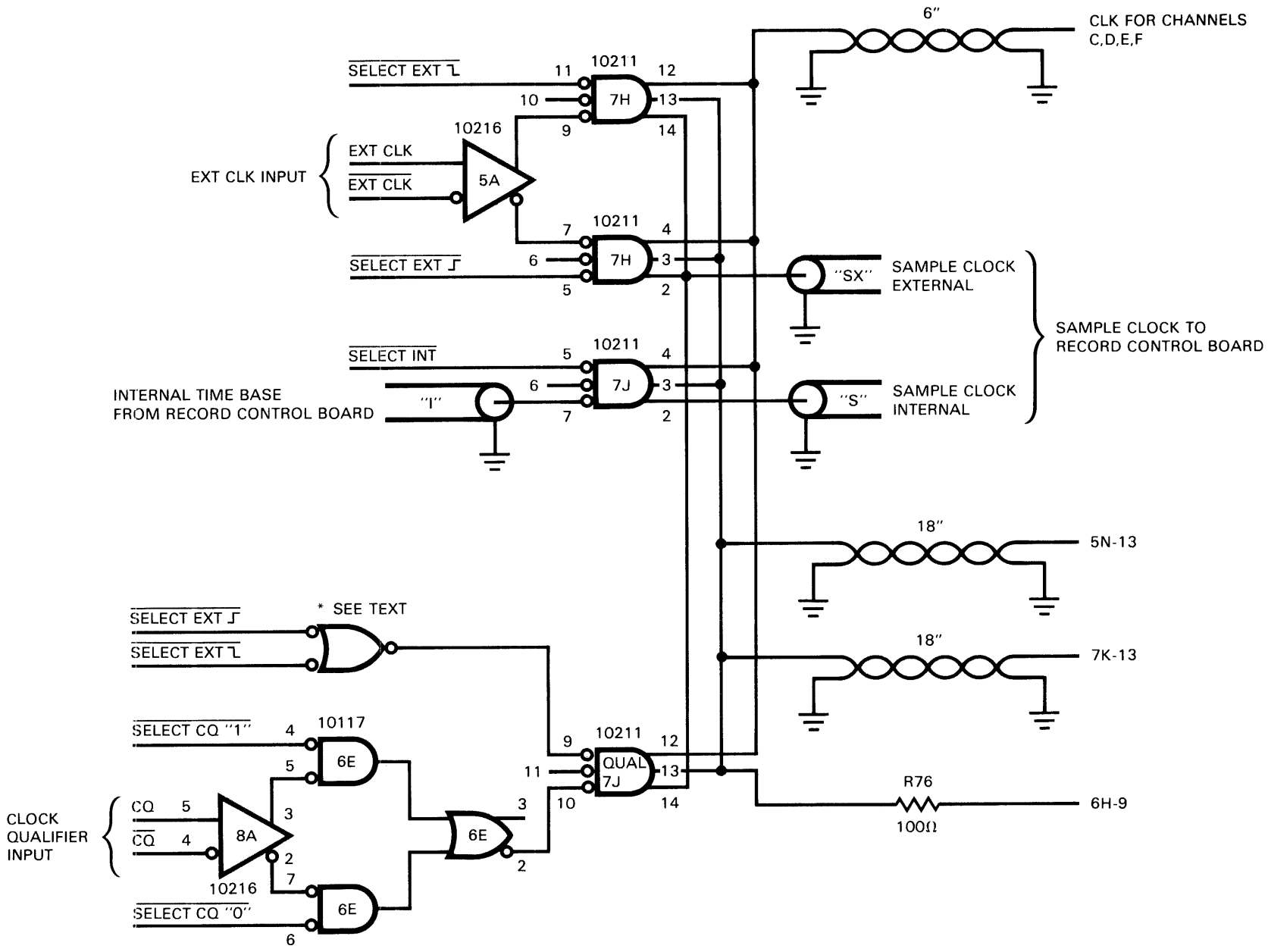


Figure 4.8 Clock Selection and Distribution

the circuit shown in Figure 4.9. This circuit also inverts the signals. The signals that are translated are:

DB0-DB7 data bus (eight lines)
A0-A3 address (four last significant bits)
$\overline{\text{FEWE}}$ write enable pulse (decoded by the MPU board)
$\overline{\text{MRST}}$ master reset (used at power-on only)

The holding registers are 8-bit addressable latches (4724). This reduces the amount of decoding needed on the Front-End board and also reduces the number of traces that must be run to each register. This type of register also offers the advantage of getting 8 bits of storage into a 16-pin IC (for example, an 8-bit parallel load register would require a 20-pin IC). Because the 4724 is CMOS, it can directly drive the ECL inputs. Note that, because the address lines are inverted, the 4724 output 07 is addressed by the MPU as address 0 and output 06 is address 1, etc.

4.5 Record Control

The Record Control board contains the time base for generating the internal clock, the enable and trigger filter/edge detector, the trigger hold-off counter, the trigger delay counter, and the record control flip-flops.

4.5.1 Time Base

The crystal-controlled oscillator circuit provides a stable and accurate 100 MHz signal. The crystal (Y1) is designed to operate at the fifth overtone. Inductor L1 and capacitors C10, C11 and C46 form a resonant "tank" circuit at 100 MHz and guarantee that the crystal does not oscillate on any other overtone. Resistors R10, R11, and R82 establish a bias point for the transistor. Resistors R9 and R48 establish the quiescent DC operating voltage on the collector of Q15. Inductor L2 acts as a high impedance at 100 MHz and increases the circuit gain so that it can oscillate. Adjustment of the pot (R48) shifts the average value of the 100 MHz signal on the collector of Q15 and this adjusts the symmetry of the clock signal (output from 17B-2).

The 100 MHz clock is divided by a series of counters to provide 10 MHz, 1 MHz, 100 kHz, 10 kHz, 1 kHz, and 100 Hz signals. The counters for 10 MHz and 1 MHz are 10138s (locations 16C and 15C respectively) and are connected as bi-quinary counters so that they provide 50% duty cycle signals. The duty cycle of these clocks is not critical. The 1 MHz clock output from $\overline{\text{15C-15}}$ is buffered by Q16 to provide a larger signal to allow the use of CMOS counters for the next four decades.

The 10164 at location 17C is programmed by the MPU and selects one of the six decade clocks. This selected decade clock (output on 17C-15) clocks the counter 18C and generates a divide-by-two clock and a divide-by-five clock. The MPU then programs the 10102 at location 18B to select one of these three clocks to be used as the internal clock. Gate 17B-13 then buffers this clock and drives the coax to the Front-End board clock selection circuitry.

4.5.2 MPU Data Bus

The MPU data, address, and control lines are translated from TTL (+5 V) to CMOS (-5 V) by transistors Q1 through Q14. This allows the use of less expensive low-power Schottky circuitry for decoding and latching the MPU control information. The 74LS138 at location 8D decodes the six addresses used by the Record Control board and provides the clock signals to the six 74LS273 registers that latch the information. To ensure that the "high" logic level output by the 74LS273s is high enough to meet the input requirement of the ECL, each output is connected to a pull-up resistor to ground. Outputs that drive more than one ECL input are connected to more than one resistor.

4.5.3 Filter/Edge Detector Circuit

The Filter/Edge Detector circuit is shown in Figure 4.10.

The enable circuit operates in the following way:

1. Assume that the enable condition is false(this is determined on the Front-End board) and that the MPU has selected "enable true."

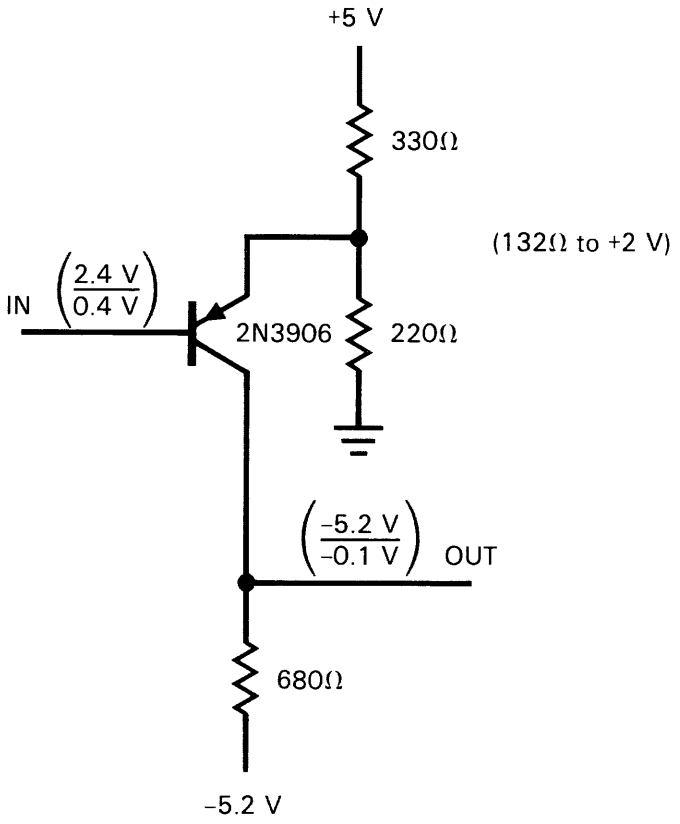


Figure 4.9 Level Translator for MPU Bus

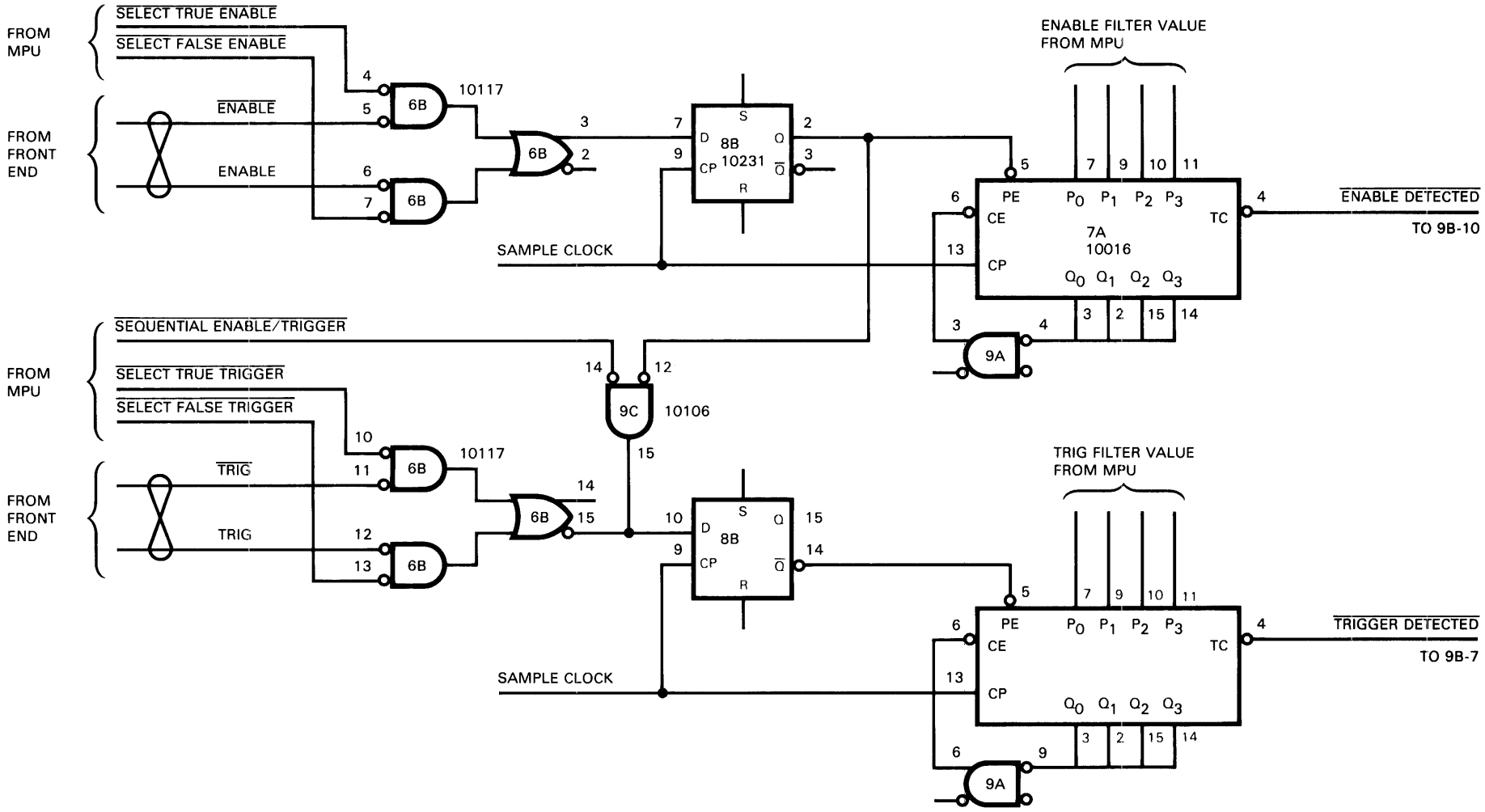


Figure 4.10 Block Diagram of Filter/Edge Detector

2. The signal "Enable" from the Front-End board is high at 6B-5 and the signal "select enable true" is low at 6B-4; therefore, 6B-3 outputs a low.
3. The flip-flop (10231 at location 8B) is clocked by the sample clock to resynchronize the signal to the clock. This has no logical effect; it is solely for the purpose of removing the effect of the delays.
4. Thus the output of the 10231 (pin 8B-2) is also a low and this is applied to the $\overline{PE}$ input of the 10016 (pin 7A-5). The 10016 is thus preset to the number that was loaded into the register (location 7C) by the MPU.
5. Assume a filter of 1 was selected. Then the MPU loads the number 14 into the register and at this time the 10016 is preset to 14. Since the 10016 is a binary counter, its TC output is false at this time (i.e., high at pin 7A-4).
6. When the enable condition becomes true, the signal "Enable" goes low and this is clocked through the 10231 and puts a low on 7A-5. If the "Enable" condition remains true, then on the next clock the 10016 is allowed to count from 14 to 15. This causes the TC output to go low.
7. On the next clock the record control flip-flop is clocked to the enabled state and the 10016 is clocked to count zero. Thus the $\overline{TC}$ output returns to high.
8. When the count of zero is reached, the outputs of the 10016 (goes to a low) and the gate 9A pulls the $\overline{CE}$ pin high and the counter stops at count zero.
9. When the enable condition is no longer true, the counter again presets to count 14.
10. If the enable was only true for one sample, the counter would have counted from 14 to 15 and then back to 14.

4.5.4 Filter Values Other Than 1

For filter values other than one, the circuit operates as follows:

1. Assume a filter value of 5. The MPU subtracts the filter value from 15 (15-5=10) and stores the number 10 in the register.
2. Thus, whenever the enable is false, the counter is preset to 10. For the counter to get to the count 15, the enable signal must go true for at least five consecutive clocks. If the signal goes false before the counter reaches 15, it resets back to 10.
3. See Figure 4.11 for some examples of the filter operation.

4.5.5 Trigger Filter/Edge Detector

The Filter/Edge Detector for the Trigger operates exactly the same as the Enable with the following exceptions:

1. The output of the 10117 is taken from pin 15 instead of pin 14. This inverts the signal at this point. The signal is then reinverted by using the $\overline{Q}$ output of the 10231 (pin 8B-14).
2. The net result of inverting this signal twice is that the circuit operates exactly the same except that the signal from 6B-15 may now be "Wire-Or'ed" with the signal from the 10106 (pin 9C-15).
3. In normal 16-channel operation, this gate (9C-15) is disabled by the MPU and the trigger circuit operates exactly the same as the enable circuit.
4. In 32-channel operation (when the K100-D/32 is plugged into the K100), the MPU enables this gate by putting a low on pin 9C-14. This mode may be called Sequential Enable/Trigger because it requires that the trigger must be true on the next clock immediately following the enable true.
5. This is accomplished by "or-ing" the output of 8B-2 (enable) with the input to 8B-10 (trigger). Thus, for the trigger circuit to receive a trigger, enable must have been true for the previous clock.
6. In this mode the filter values are always set for one and the enable and trigger conditions are always true for only one clock period. The enable is used for the "address" information and the trigger is used for the "data" information.

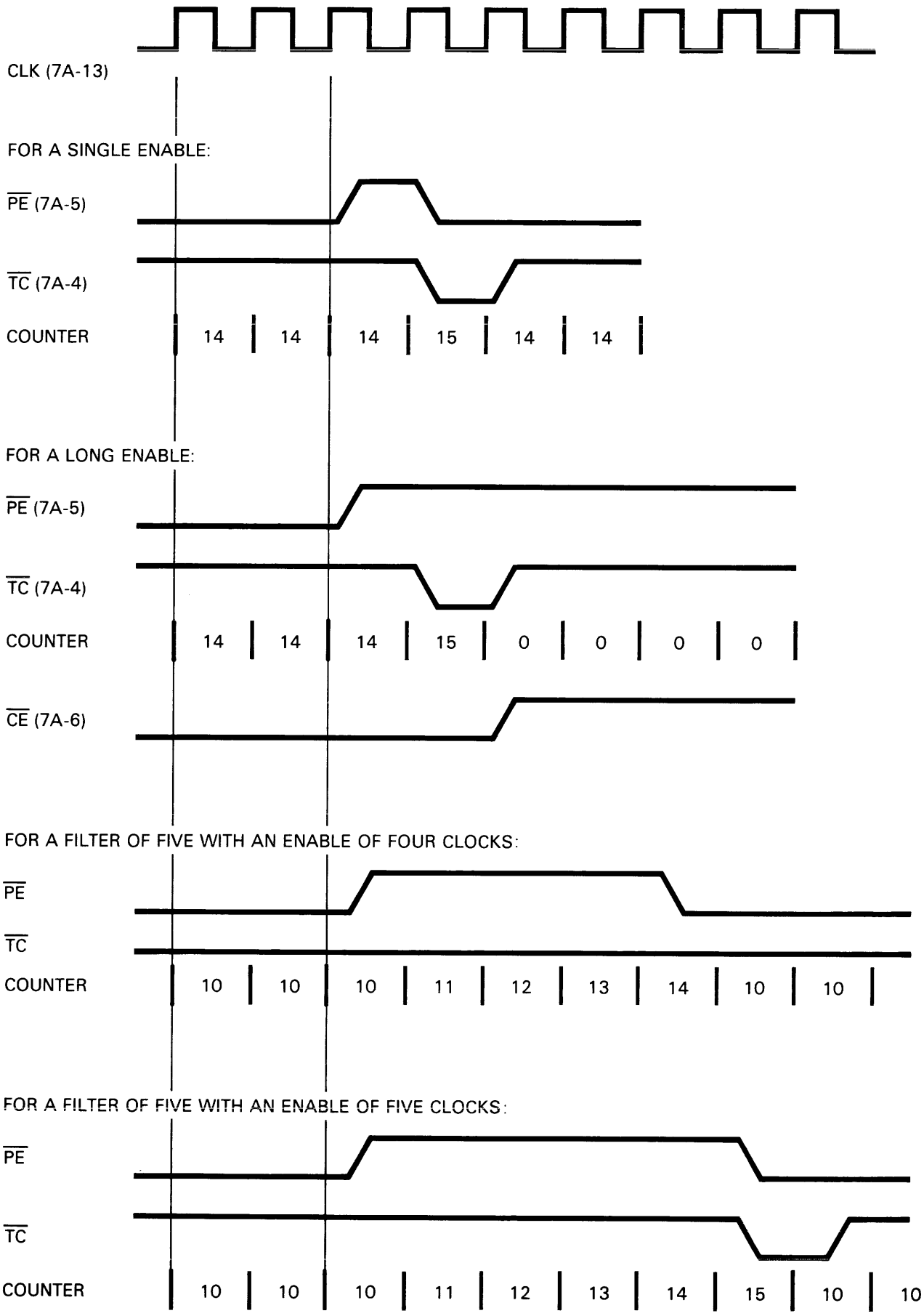


Figure 4.11 Filter Operation Examples

4.5.6 Trigger Hold-Off Counter

The Trigger Hold-Off Counter is controlled by the Record Control Logic and its purpose is to inhibit (or hold-off) the acceptance of the enable event until the memory has been filled with new data. This prevents the display of any "old" data.

Operation is as follows:

1. When a recording is initiated by the MPU, the hold-off counter is reset to zero and the counter is enabled to count (a low applied to 13D-6 and 13D-11).
2. The two flip-flops (at location 13D) form a 2-bit binary counter and their output (13D-14) clocks the 8-bit counter formed by two 10016's (locations 11D and 11C).
3. Note that 11D and 11C are ripple clocked by the 10231. This is acceptable here because the exact number of hold-off clocks are not critical. The only requirement is that there be at least 1,000 clocks in the hold-off time.
4. The $\overline{TC}$ output of this counter is formed by the 10102 at location 18B. When the output of 18B-9 goes low, the control flip-flop (at location 10B-3) changes state to indicate the end of the hold-off period and the enable circuitry is allowed to begin operation. The output of this flip-flop also disables the hold-off counter by placing a high on 13D-6 and 13D-11.
5. The trigger hold-off may be defeated by a switch at location 7E. If this switch is in the open position, then 12E-11 is allowed to go low and the output 12E-7 goes low and puts a low on the $\overline{PE}$ inputs of the 10016s. This causes the 10016s to go to TC as soon as they get a clock. The hold-off is thus reduced to one clock.

4.5.7 Trigger Delay Counter

The Trigger Delay Counter is controlled by the Record Control Logic and its purpose is to determine the end of the record cycle. The end of the record cycle is specified as a certain number of clock cycles after the detection of the trigger event. In the "EVENTS DELAYED" mode of operation this counter serves two functions; it counts the "events" delay and then it counts the number of clocks to the end of the record cycle.

4.5.7.1 Operation in "CLOCK DELAYED" Mode

1. The trigger delay counter is held preset to the value that the MPU has loaded into registers 2C and 3C (74LS273s) by the control logic until the enable condition is detected and the "ENABLED" flip-flop set (i.e., 9B-14 goes high). This puts the PE inputs to the 10016s high and allows them to be controlled by the $\overline{CE}$ inputs.
2. The counter does not begin counting until the trigger condition is detected and the "TRIGGERED" flip-flop is set (i.e., 9B-3 goes high). The signal 9B-2 goes low which turns off the outputs of the 10210 (location 4C) and allows the $\overline{CE}$ inputs of the counters (locations 2A, 2B, 3A, and 3B) to be controlled by the gate 4A. The $\overline{CE}$ input of the first counter goes low whenever 9B-2 is low. The $\overline{CE}$ input of the second 10016 goes low only when 9B-2 is low and the TC output of 2A is low. The $\overline{CE}$ input of the third 10016 goes low when 9B-2 is low and both $\overline{TC}$ of 2A and 2B are low. Similarly, the $\overline{CE}$ of the fourth 10016 requires the $\overline{TC}$ of all three 10016s preceding it to be low. Note that the TC output of each 10016 is low whenever the count of that 10016 is at 15 and does not include the $\overline{CE}$ input.
3. When the counter reaches top count on all four counters, then on the next clock it counts to all zeros. When this happens the $\overline{TC}$ output of the last counter (pin 3B-4) goes from low to high and clocks the flip-flop 12B-15 from high to low. This flip-flop is called "DELAY INHIBIT" and it indicates that the counter has completed the amount of delay that the MPU programmed it for.
4. The counter continues counting for 16 more clocks at which time the "16" output of the counter (pin 2B-3) goes high and the 10121 at location 5B outputs a low (pin 5B-3), indicating the end of the record cycle.

5. Thus the counter counts the number specified by the register (as a two's complement number) plus 16 more counts. These extra 16 counts plus the extra clocks that were required to pass the trigger condition through the front-end (two clocks), the filter/edge detector (two clocks), the "ENABLED" flip-flop (one clock) and the flip-flop that stops the recording, result in the actual end of the recording being 22 clocks beyond the actual desired place. This number was chosen to allow for the fact that the record memory actually is 1024 samples long and the user specified end of record point is defined as the 1000th sample. The number loaded by the MPU into the counter is actually the one's complement (inverted) of "the number entered by the operator plus one." For example, for a delay of zero the counter is preset to FFFE (hex) and for a delay of 10 the counter is preset to FFF4 (hex).

4.5.7.2 Operation in "EVENT DELAYED" Mode

1. In this mode, the counter serves two different functions. First it counts the specified number of trigger events after the "TRIGGERED" flip-flop is set and then it counts 516 clocks after the last trigger event. The reason for the number 516 is that it positions the last trigger event at the 500th sample. Note that 516 is exactly 500 more than the 16 that was used in "CLOCK DELAYED" mode.
2. In this mode, the MPU puts a low on the signal "EVENTS" and puts a high on the signal "CLOCKS." This enables the 10106 gate (location 9C) to control the $\overline{CE}$ inputs to the counter. The counter is then allowed to count only if "ENABLE" is set and the trigger detector output says the trigger is detected. Since the "trigger detected" output is only true for one clock period (because it is edge detected), the counter can only count once each time the trigger is detected. The flip-flop (location 10B-14) delays the trigger detected signal by one clock so that the counter counts the trigger event, which causes the "ENABLED" flip-flop to be set. Note that the signal out of 10B-14 goes through two gates before it gets to the $\overline{CE}$ inputs of the counters. This is too much propagation delay for operation at 100 MHz clock rate; therefore, this mode of operation is specified for a maximum clock rate of 50 MHz.
3. When the specified number of trigger events have been counted, the "DELAY INHIBIT" flip-flop is clocked and a high is applied to input 9C-5. This enables the counter to count on every clock. This also enables the end of record detector (the 10121 at 5B) to start looking for count 516 (the combination of the 512 bit (3A-2) and the 4 bit (2A-15)). When count 516 is reached, 5B-3 goes low and the record cycle is stopped on the next clock.

4.5.8 Record Control Flip-Flops

The record control flip-flops are shown in Figure 4.12 and their functions are described as follows:

1. All five are set to a one at the beginning of each record cycle.
2. Hold-off prevents the acceptance of any enable condition until after the hold-off condition is satisfied. Normally the hold-off condition is 1020 clocks (see Section 4.5.6).
3. Enabled (not enabled) prevents the acceptance of any trigger condition until after the enable condition is detected. The enable condition may be a specified combination (see Section 4.5.3) or it may be a manual enable or auto enable. For a manual enable the MPU puts a low pulse on 12D-11, which sets the Enabled flip-flop. For auto enable, the MPU puts 12D-11 low continuously and as soon as the hold-off flip-flop is set the enabled flip-flop is set.
4. $\overline{\text{Triggered}}$ (not triggered) prevents the delay counter from starting until the trigger condition is met (see Section 4.5.7).
5. Delay Inhibit prevents the end of record logic from decoding end of record until the counter reaches TC. It is also used to switch from counting trigger events to counting clocks in the "EVENTS DELAYED" mode (see Section 4.5.7).

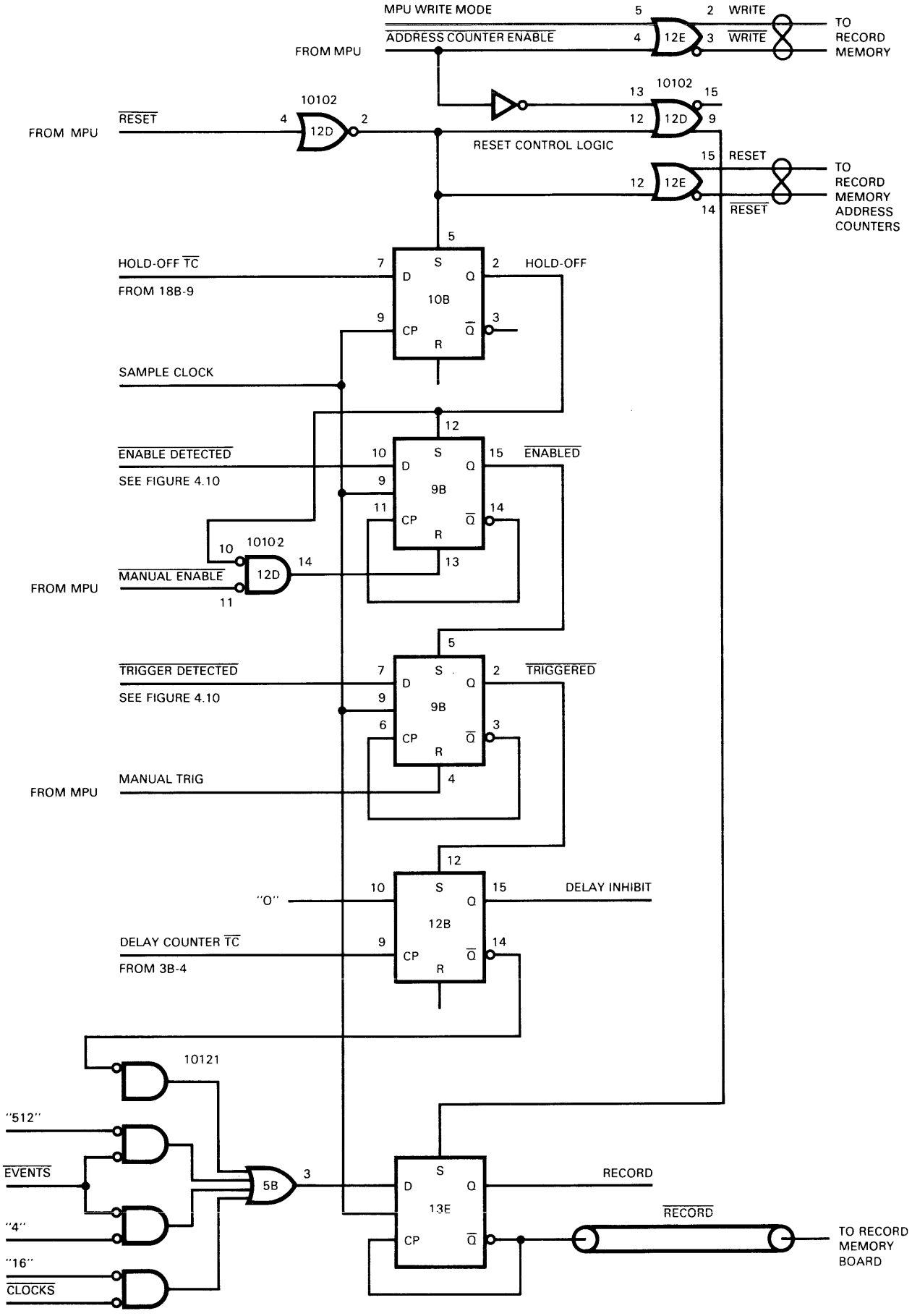


Figure 4.12 Block Diagram of Record Control Flip-Flops

6. RECORD enables the clock for the record memory. This flip-flop stops the record memory system when the trigger delay counter decodes the end of record condition (see Section 4.5.7). After the recording is complete, the MPU resets the record flip-flop to enable the memory address counters so that the MPU can read the data from the record memory (see Section 4.5.10).

4.5.9 The record control flip-flops are translated from ECL to TTL by the 10124s at 9D and 10D and are read by the MPU (using 74LS244 at 9E) so that the MPU may determine the record control status. The record status indicator displayed in the lower left-hand corner of the CRT is a direct indication of the state of these flip-flops. The status displays are:

1. CK? means that HOLD-OFF is still set.
2. EN? means that HOLD-OFF is satisfied and "not enabled" is still set.
3. TG? means that both Hold-off and "not enabled" are satisfied (i.e., reset) and "not triggered" is still set.
4. DLY means that CK?, EN?, and TG? are satisfied and the record flip-flop is still set.
5. BSY means that the record cycle is completed and the MPU is processing the data. All five of the record flip-flops must have been satisfied (reset) to reach this point. Note, however, that the MPU sets RECORD true again to read the data from the Record Memory.
6. RDY means that no recording is in process and the MPU has processed the data from any previous recording. If either Man Arm or Auto Arm is pressed by the operator at this time, the MPU begins a new record cycle.

4.5.10 Clock distribution for the Record Control board is shown in Figure 4.13. The primary purpose of the clock distribution is to buffer the clock to reduce the loading effects. On early boards (designated by -10) the sample clock came from the Front-End board on a single coax (called "S") and was connected to the three inputs of the 10210s. These 10210s then provide nine buffered outputs. In this design the "S" clock signal is quite heavily loaded - four outputs "wire-or'ed" at the Front-End board and three inputs on the Record Control board. The -20 design reduced the loading by splitting the signal into two coaxes and using the 10210s to "or" them together. The "S" coax carries the clock only if INT is selected and the "SX" coax carries it if EXT is selected. Thus the loading for the INT clock is reduced from four outputs to one output at the Front-End board. This removes about 10-15 pF of load and gives a much better waveform.

The outputs are distributed in such a way that each output drives no more than two inputs and the length of the trace is kept to less than 2 inches after the coax. The coaxes also allow for some adjustment of the delays by changing the lengths.

The clock outputs for the Record Memory boards are wire-or'ed to allow the use of the signal "RRE1" to clock the memory address counters when the MPU is reading the data from the Record Memory. The MPU terminates the recording process as follows:

1. The MPU detects that the recording is completed - the RECORD flip-flop is cleared.
2. The MPU deselects all clock sources - i.e., no clock is selected and both "S" and "SX" go to low. (This is done by loading the clock selection register on the Front-End board.)
3. The MPU sets the signal "MPU Clock Source" to a low. This enables the signal "RRE1" to be the clock to the Record Memory board. At this time, "RRE1" is high and the clock remains low.
4. The MPU sets the signal "Address Counter Enable" high (see Figure 4.12), forcing the RECORD flip-flop to be set. This puts RECORD low, enabling the Record Memory to respond to the clock signal "C1" or "C2". This signal also forces the signal "WRITE" to a low and this disables the write enable circuitry on the Record Memory board. Thus the

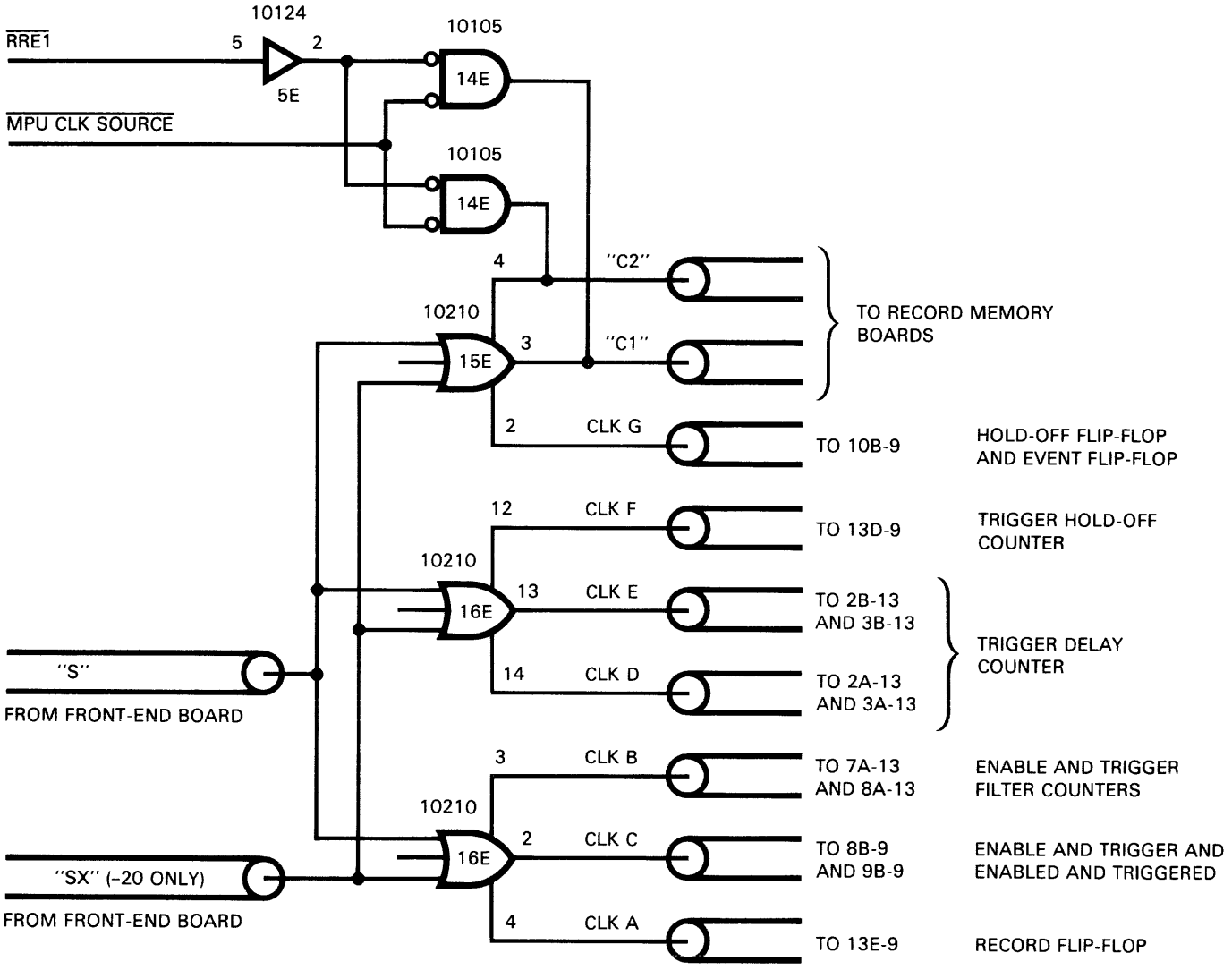


Figure 4.13 Block Diagram of Clock Distribution on Record Control Board

system is now ready to read data from the Record Memory to the MPU.

5. The MPU now executes a read from the memory board for channels 0-7. This is decoded by the MPU logic and generates a 500 ns negative pulse on "RRE1". The clocks "C1" and "C2" go high for 500 ns. The memory address counters are increments when "C1" goes high. The data from the Record Memory board is gated onto the MPU data bus by the RRE1 pulse and the MPU reads the data near the end of the pulse. Thus the address is incremented before the data is read by the MPU. Note that both memory boards are incremented by the RRE1 signal.
6. The MPU now executes a read from the memory board for channels 8-F. This generates a similar pulse on "RRE2" and reads that data into the MPU. This has no effect on the clock signals and does not increment the address counters.
7. The MPU repeats steps 5 and 6 above a total of 1024 times to read all of the data. Note that at this time the Record Memory address counters return to exactly the same address that they were at when the recording was completed.
8. The MPU loads the Front-End board to select the sample clock to the original source (either INT, EXT ∫ or EXT ⅂). At this time the selected clock is applied to all circuits, including the memory's because the signal "RRE1" is high. The signal "WRITE" is still held low.
9. The MPU sets "MPU Clock Source" high and "Address Counter Enable" low. This allows the "WRITE" signal to go high as long as the RECORD flip-flop stays set and the data in the Record Memory board may be destroyed. This data is no longer needed by the MPU because the MPU has stored it all in the MPU RAM on the MPU board.
10. If, at any time, the operator pushes the "M→A" button, the MPU performs the above sequence starting at step 2. Note that when step 9 is executed the K100 resumes the recording process at the same state that it was in when the M→A cycle was started. This is why the RRE1 signal is not allowed to clock any of the other logic. During the execution of step 8 one extra clock may be generated when the clock is reselected. Also note that the last sample of data that was recorded in the Front-End board 10231's was not transferred to the Record Memory board and will thus not be transferred to the MPU.

4.5.11 Power-up MPU diagnostics also utilize this control logic for using RRE1 as the clock source for the Record Memory. In this mode the clocks are deselected and the "Address Counter Enable" signal is asserted. In addition, the signal "MPU Write Mode" is also asserted, enabling the record memory write enable circuitry. Thus each time the MPU executes a read on RRE1, the data from the Front-End board is written into the Record Memory board. When the MPU has written all 1024 addresses, it then turns off the write enable circuitry by setting "MPU write mode" false. Then the MPU can read the data and see if it is correct.

4.6 Record Memory

The Record Memory provides the primary means of storing data as it is recorded. The Record Memory can operate at up to a 100 MHz clock rate in the Record mode and the data may be read by the MPU at the data bus rate (1 MHz). The Record Memory system is divided into two identical boards because it does not fit on a single board. Each board provides eight channels of memory and all of the required address counters, write enable circuits, and other control logic. Each board receives its data signals from the Front-End board and its clock and control signals from the Record Control board. The MPU communicates to the Record Memory boards through the Mother board. The Mother board wiring dictates the function of each board; connectors J3/J4 (closest to the Front-End board) are wired for channel 8-F memory and connectors J13/J14 are wired for channel 0-7 memory. The Memory boards may be interchanged without affecting operation as long as the data cables from the Front-End board are connected to the correct Memory board (channels 8-F to the first memory and channels 0-7 to the second memory from the Front-End board). The clock and record control signals are identical for both Memory boards and may be interchanged.

4.6.1 A block diagram of the Record Memory board is shown in Figure 4.14. The basic memory element used on this Memory board is a 256 x 1 TTL RAM of the 82S117

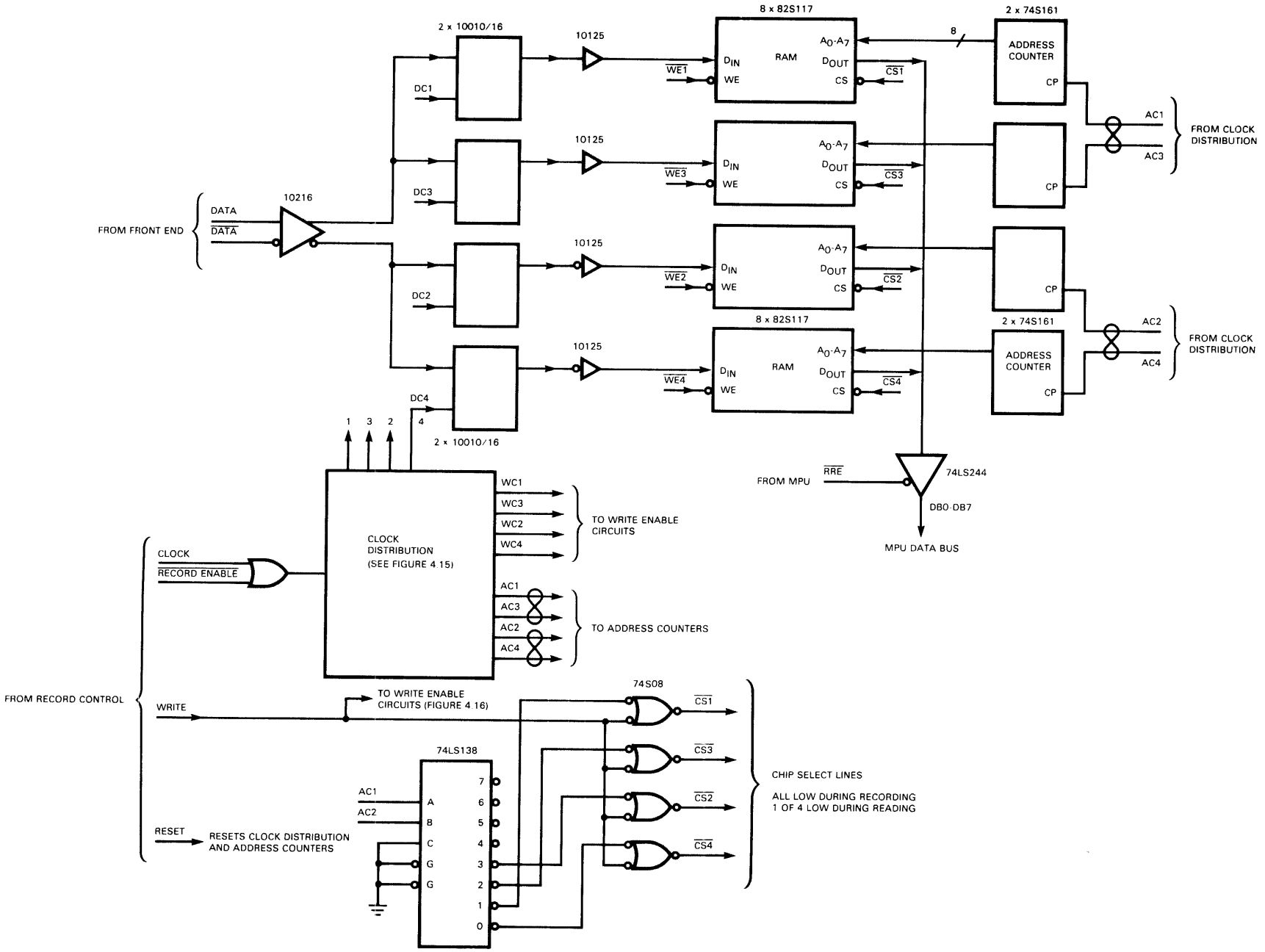


Figure 4.14 Block Diagram of Record Memory Board

type. These memory ICs are operated in a four-way multiplexed system. There are four identical memories for each data channel and the data is sequentially stored into each of these four memories. In this way each memory receives every fourth data bit and the memory system operates at four times the rate of each memory. Thus for a 100 MHz memory system, each memory is required to operate at 25 MHz. This multiplexed system is implemented by the clock distribution circuit that generates a four phase clock. Each phase of this clock drives one of the four memory banks. Each memory bank has an 8-bit holding register for the input data, an 8-bit address counter, a write enable pulse generator, and eight RAMs. All of these elements of the memory bank are activated by the positive edge of the clock for that bank. The four memory banks are referred to as Phase 1, Phase 2, Phase 3, and Phase 4 and they operate in time sequence 1, 2, 3, 4. Thus a typical sequence of operation is as follows. (Refer to Figure 4.15.)

1. Assume that the clock distribution flip-flops are both reset. This gives DC1 and DC2 low and DC3 and DC4 high.
2. On the next clock, DC1 (pin 4C-2) goes high. This clocks the data into the holding registers for phase 1 (locations 3A and 4A).
3. The level translator circuit provides a clock AC1 to the address counters (18A and 19A) and increments the address to the RAMs for phase 1.
4. The write enable generator for phase 1 is clocked by WC1 (which is the same as DC1 clock) and generates a write enable pulse about 20 ns after the positive edge of DC1 with a pulse width of about 20 ns.
5. On the next clock, DC2 (pin 4C-15) goes high. This clocks the data, address, and write enable generator for phase 2.
6. On the next clock, DC3 (pin 4C-3) goes high. This clocks phase 3.
7. On the next clock, DC4 goes high. This clocks phase 4. At this point both flip-flops have returned to the initial state (reset) and the above cycle repeats.
8. Note that when DC3 goes high, DC1 goes low and vice versa. Because all of the circuits are clocked by the positive edge, the exact time when each clock goes low does not affect the operation. However, it is quite helpful to generate phase 1 and 3 (also 2 and 4) as complementary signals. This allows the use of twisted pairs for transmission instead of coax and it also allows the use of the differential level translators Q1, 2, 3, 4, which are much faster than 10125s.

4.6.2 Figure 4.17 shows the typical timing of the memory system signals.

4.6.3 Figure 4.16 shows the write enable generator circuit (for phase 1 only). This circuit is enabled to operate only if the signal WRITE MODE is high. This signal comes from the Record Control board and is directly controlled by the MPU. If Write Mode is high, then when the clock goes high (WC1) the first flip-flop (11C-2) goes high. The Q output (11C-3) is pulled low by the resistor R13 with the capacitor C17 determining the time required to reach the threshold level of the 10195 (10C-12). When the threshold is reached, the output of the 10195 (10C-15) goes high and resets the 10231 (forcing 11C-2 low and 11C-3 high). This also charges C17 back up to a high. The resistor R11 (30 Ω) limits the charging current to C17 and reduces any tendency for ringing on the positive edge of 4C-3. When 4C-2 goes low, the output 10C-13 goes high and clocks the second 10231 (forcing 11C-15 high and 11C-14 low). The RC time constant of R12 and C16 then determines the time delay until the output 10C-14 goes high and resets the 10231 (11C-15 low and 11C-14 high). Note that the next WC1 clock may be received before the second flip-flop has completed its cycle.

4.6.4 The signal RESET is generated by the MPU at the beginning of every record cycle and resets all four memory address counters and the two clock distribution flip-flops. The data holding registers are <u>not</u> reset. This reset signal is <u>not</u> necessary for normal operation of the Record Memory board. However, it allows the power-up diagnostic to determine which RAM is being addressed during the diagnostic.

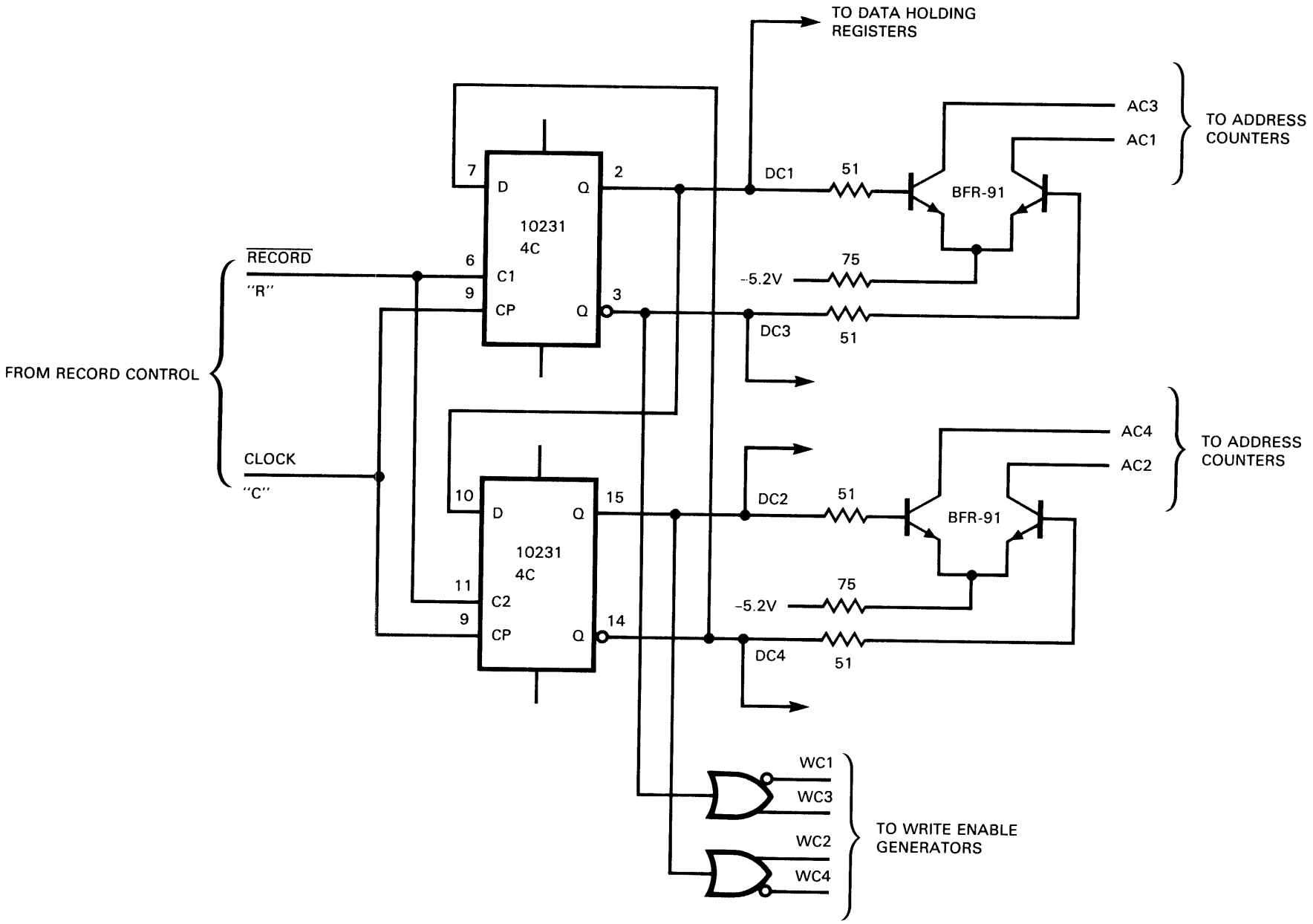


Figure 4.15 Block Diagram of Record Memory--Mulitplexing Scheme and Clock Distribution

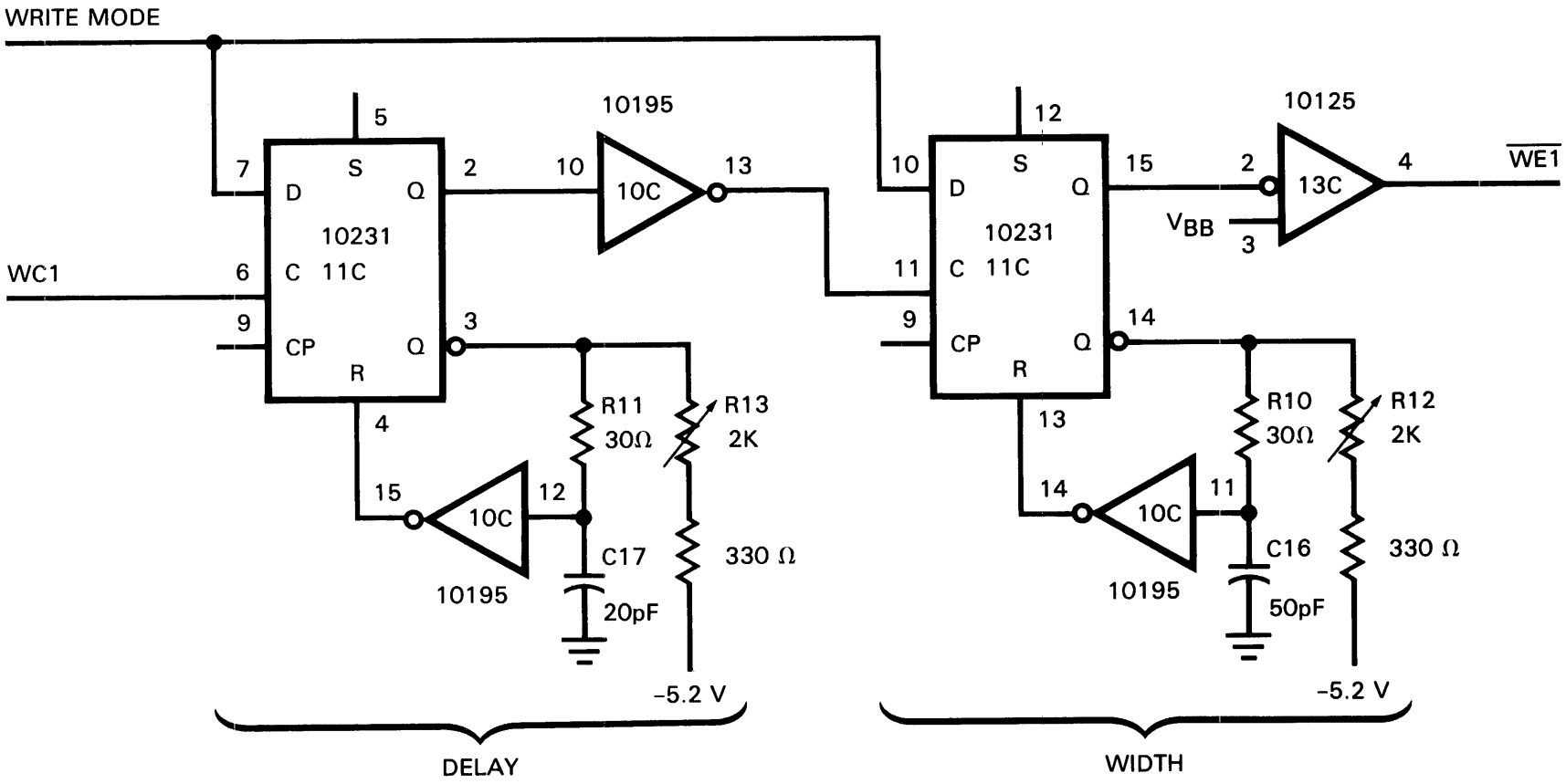


Figure 4.16 Block Diagram of Record Memory--Write Enable Circuit

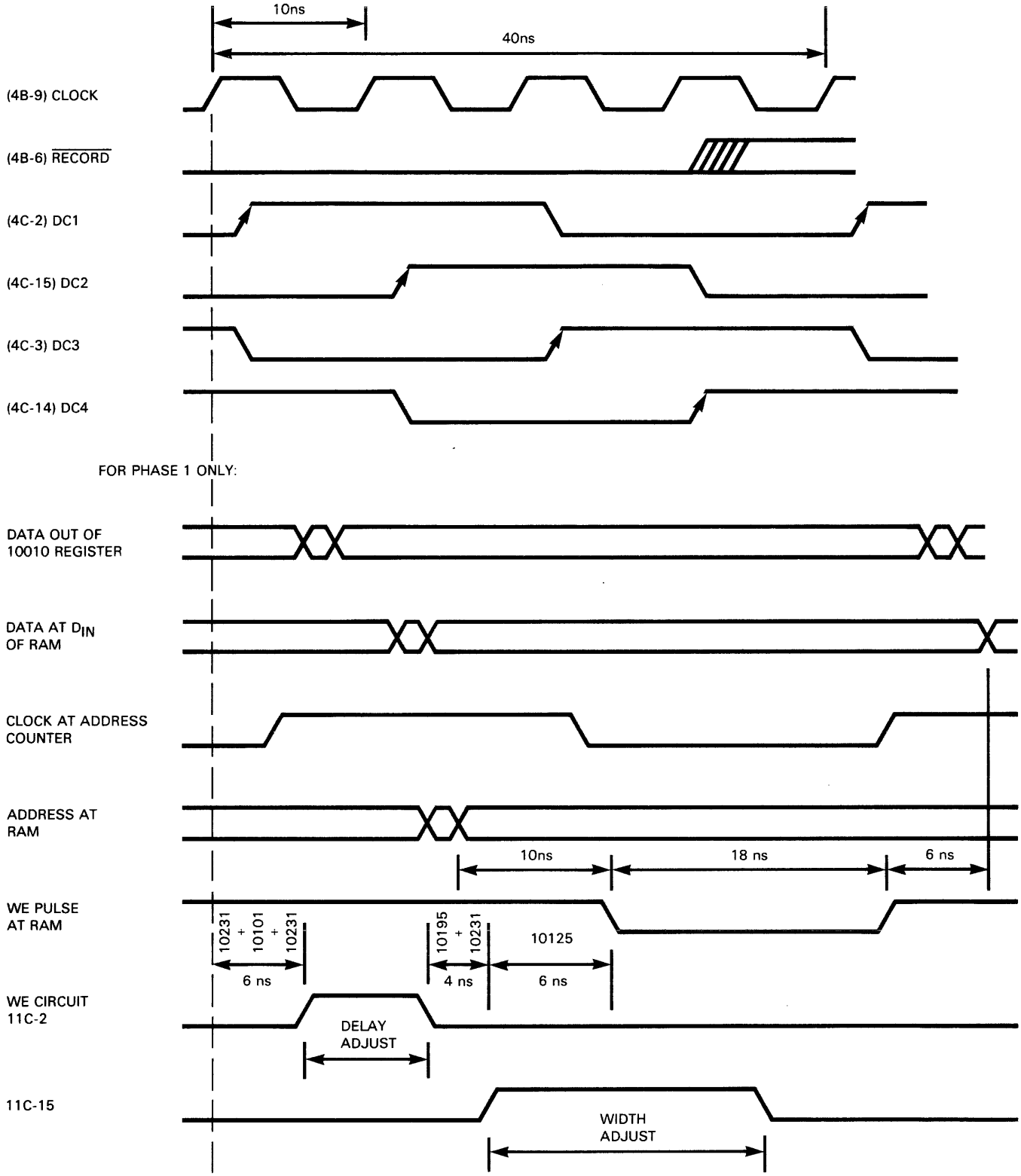


Figure 4.17 Record Memory Timing

4.7 Threshold

The Threshold board has holding registers for the MPU control information, two 8-bit D/A converters, twenty-four input analog switches and twenty op amp buffers.

4.7.1 The MPU data bus is buffered into the Threshold board by the 74LS244 at location 7E whenever the MPU is doing a WRITE operation. The three lowest address lines (A0-A2) are decoded by the 74LS138 (location 8D) and provide the clock signals for the 74LS273 holding registers. The Threshold board is addressed by the MPU as if it were part of the Record Control board. Address "880X" hex is decoded by the MPU board and sent to both the Record Control and the Threshold (called $\overline{CWE}$). The A3 bit is then used to determine which board responds. The Record Control responds if A3 is low and the Threshold responds if A3 is high. This is done by connecting A3 to the G1 input of the 74LS138 (8D-6) and connecting $\overline{CWE}$ to the $\overline{G2}$ inputs (8D-4 and 8D-5). The holding registers are as shown in Table 4.1

Table 4.1

Location	MPU Address	Description
7C	8808	DAC A All zeros= -6.4V
7B	8809	DAC B All ones= +6.35 V Effective Threshold
6C	880A	ch E,F,CQ,CK Threshold Selection
7D	880B	ch A,B,C,D Threshold Selection
6D	880C	ch 8,9,Q1,Q2 Threshold Selection
6A	880D	ch 4,5,6,7 Threshold Selection
6B	880E	ch 0,1,2,3 Threshold Selection
None	880F	not used

4.7.2 The Threshold DAC (Digital-to-Analog Converter) circuit is shown in Figure 4.18. Only the circuitry for DAC A is shown. The DAC B circuit is similar. The 1408 is a multiplying-type DAC. The output current is equal to the reference current (IREF into pin 13) times the number applied to the digital input. The digital input is interpreted as a binary fraction (i.e., the MSB is 1/2, the next MSB is 1/4, etc.). Some examples are shown in Table 4.2.

Table 4.2

Inputs $D_7D_6D_5D_4$ $D_3D_2D_1D_0$	Multiplier	DAC Output pin 9B-1
0 0 0 0 0 0 0 0	0	3.20 V
1 0 0 0 0 0 0 0	0.5	0 V
0 1 0 0 0 0 0 0	0.25	-1.60 V
1 1 1 1 1 1 1 1	0.996	+3.175 V

The output of the DAC is converted from a current to a voltage by the op amp (9B-1) and the feedback resistor (3.16K). The op amp maintains the voltage on the inverting input (pin 2) at 0 V. Thus the output voltage goes to that value that makes the current flowing in the feedback resistor equal to the sum of any other currents from the input pin. The 4.53K resistor and the 1K pot are adjusted to give one-half of the DAC current (approximately 1 mA). This is called I_{OFFSET} and causes the output voltage to be offset by one-half of the full-scale value. Thus the output goes from -3.20 V to +3.175 V. This voltage is multiplied by two by the output buffer. See Figure 4.19.

4.7.3 The reference voltages (+VREF and -VREF) are generated by the zener diode (IN751A) and the op amp (9C) and provide stable operation that is insensitive to changes in any of the supply voltages. The first op amp provides a current source for the zener (approximately 20 mA). The second op amp is a unity gain inverter and provides the positive reference voltage.

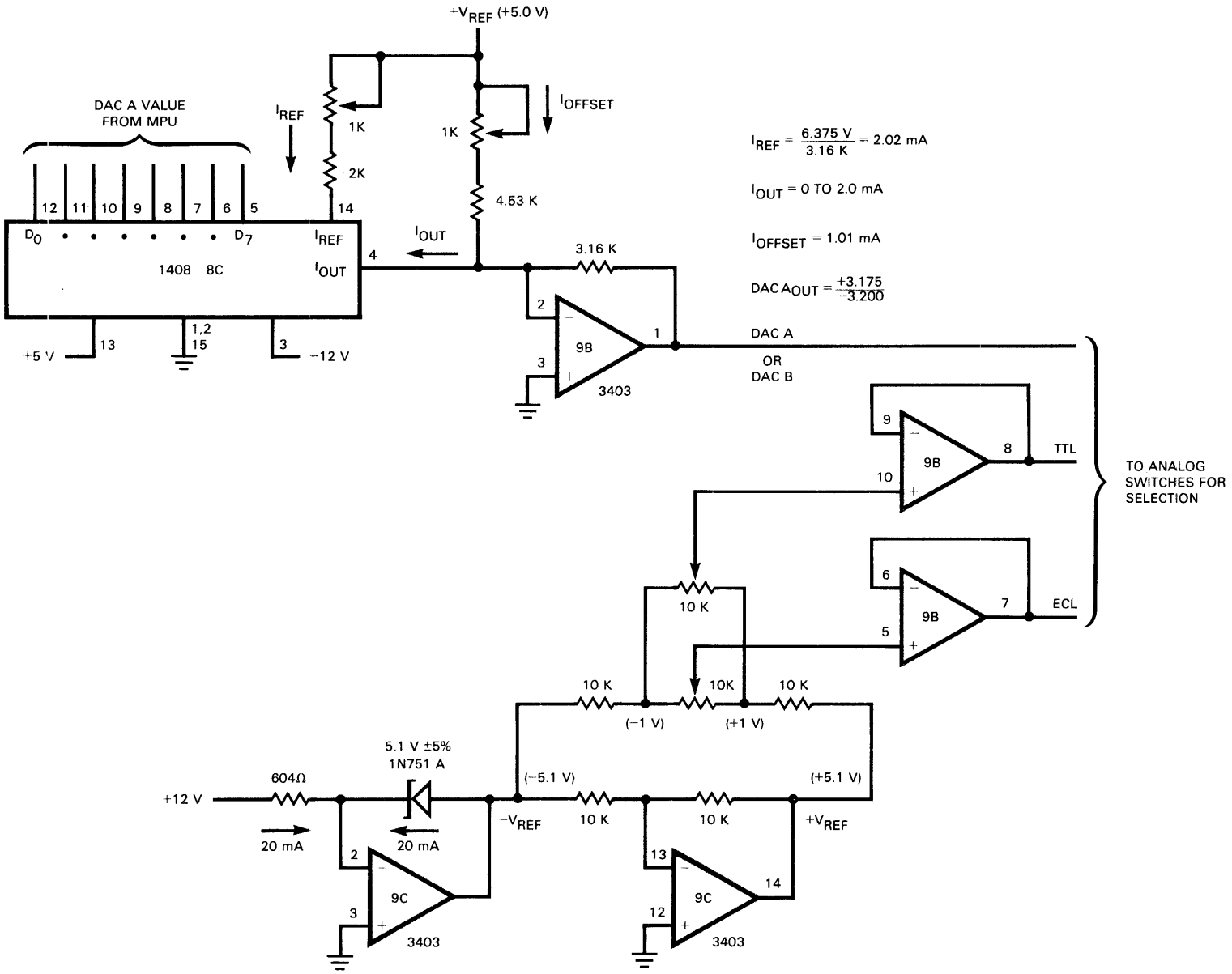
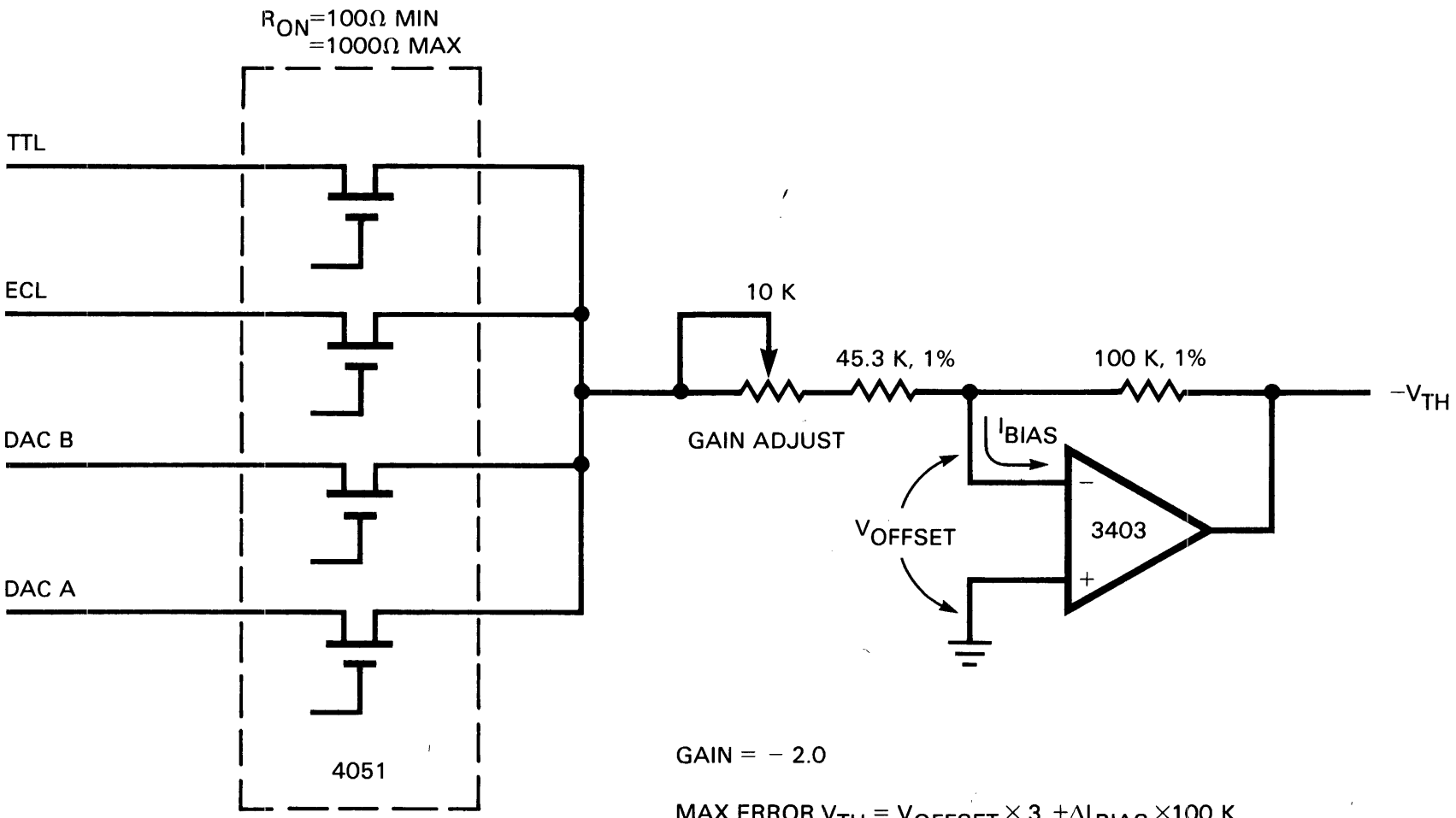


Figure 4.18 Threshold DAC Circuit



GAIN = − 2.0

MAX ERROR $V_{TH} = V_{OFFSET} \times 3 + \Delta I_{BIAS} \times 100\ K$

$= \pm 30\ mV + \left(\frac{+30\ mV}{-10\ mV}\right)$

$V_{OFFSET} = \pm 10\ mV$

$I_{BIAS} = 200\ nA \begin{pmatrix} +300 \\ -100 \end{pmatrix}$

Figure 4.19 Threshold Selection and Output Buffer

4.7.4 The TTL and ECL thresholds are generated by a resistor divider between +VREF and -VREF. The 10K resistors limit the range of adjustments to ±1.0 V (±2.0 V at the probes) and improve the settability. The op amp (9B) buffers both TTL and ECL thresholds to allow them to drive all 20 of the analog switches.

4.7.5 The analog switches are CMOS 4051s and are operated from +5 V and -5.2 V supplies. This requires that the analog signals input to the 4051s be kept to less than ±5 V, which is the reason for the output buffers having a gain of 2. Thus the maximum analog signal required at the 4051s is ±3.2 V to give an output range of ±6.4 V. There are twenty 4051 switches (one for each probe) and each switch is controlled by two signals from the MPU (stored in the 74LS273 registers).

4.7.6 The circuit shown on the schematic and identified with asterisks (*) was intended for future use as an IEEE 488 (GPIB) interface. It has never been implemented on this board. A new board was designed for GPIB operation.

4.8 Front Panel and Keyboard

Refer to the Front Panel schematic and the Keyboard schematic in Section VII. The Keyboard is arranged as an X-Y matrix. There are eight columns (vertical) and six rows (horizontal). When a key is pushed it makes a connection between the column and row that are connected to that key. For example, pushing the "ENABLE" button connects column X_0 to row Y_0. The row lines are each pulled up to +5 V by a 10K resistor and connected to the 74LS244 input (U5), which allows the MPU to read the level of each row. The column lines are driven by the 74LS138 (U4). U4 is connected to the MPU address lines (A0, A1, and A2) such that the line X_0 is driven low when the address is 0, and line X_1 is low when the address is 1, etc. The address lines are buffered by U3 (74LS04) to ensure an adequate voltage level to drive U1, U2, and U6, which are CMOS.

4.8.1 U1 is an 8-bit addressable latch (4724) and is used to control the two LEDs (ERROR and POWER-ON). The signal $\overline{FPWE}$ clocks data from the MPU data bus (bit 7) into the bit, which is addressed by A_0-A_2. Address 7 writes D7 into the Q_0 bit and controls the "power-on" LED. A high on Q_0 turns the LED off and a low turns the LED on. Address 5 writes D7 into the Q_2 bit and controls the "Error" LED. The resistors R1 and R2 set the LED current at 10 mA.

4.8.2 The switches on the Front Panel (not the keyboard) are read into the MPU by the eight-input multiplexer (U2) and are buffered onto the data bus D1 by U5 (74LS244). The circuitry of U7 (NE521) is used to detect when the 32-channel adapter is connected to the K100-D. Resistors R7 and R8 set the noninverting inputs of U7 to -2.6 V. R5 and R6 connect the inverting inputs of U7 to the clock qualifier input lines. These lines are terminated on the Front-End board by 51 resistors to -2.0 V. The outputs of U7 are thus LO if the CQ lines are higher than -2.6 and are HI if they are lower than -2.6. If nothing is connected, both lines are at -2.0 V and both U7 outputs are LO. If the probes are connected, the lines are ECL logic levels (-0.8 and -1.3 V) and both U7 outputs are LO. If the 32-channel adapter is connected, resistor R13 in the adapter is connected from the CQ line to -5.2 V and pulls it to -3.0 V. This causes output U7-9 to go high (U7-4 is LO). The eight-input multiplexer (U6) reads the outputs of U7, and U5 buffers them onto the data bus.

4.8.3 The input A and B connectors (J20 and J21) are mounted on the Front Panel circuit board. The signal lines from each input connector are connected to a 20-pin connector (J22 and J23) that goes to the Front-End board. The threshold lines, the power (-5.2) and the ground lines are connected to a 14-pin connector (J18 and J19) that goes to the Threshold board via the Mother board.

4.9 Probes

Figure 4.20 shows the probe circuit. The probe circuit compares the input signal to the threshold level and outputs a differential ECL logic signal.

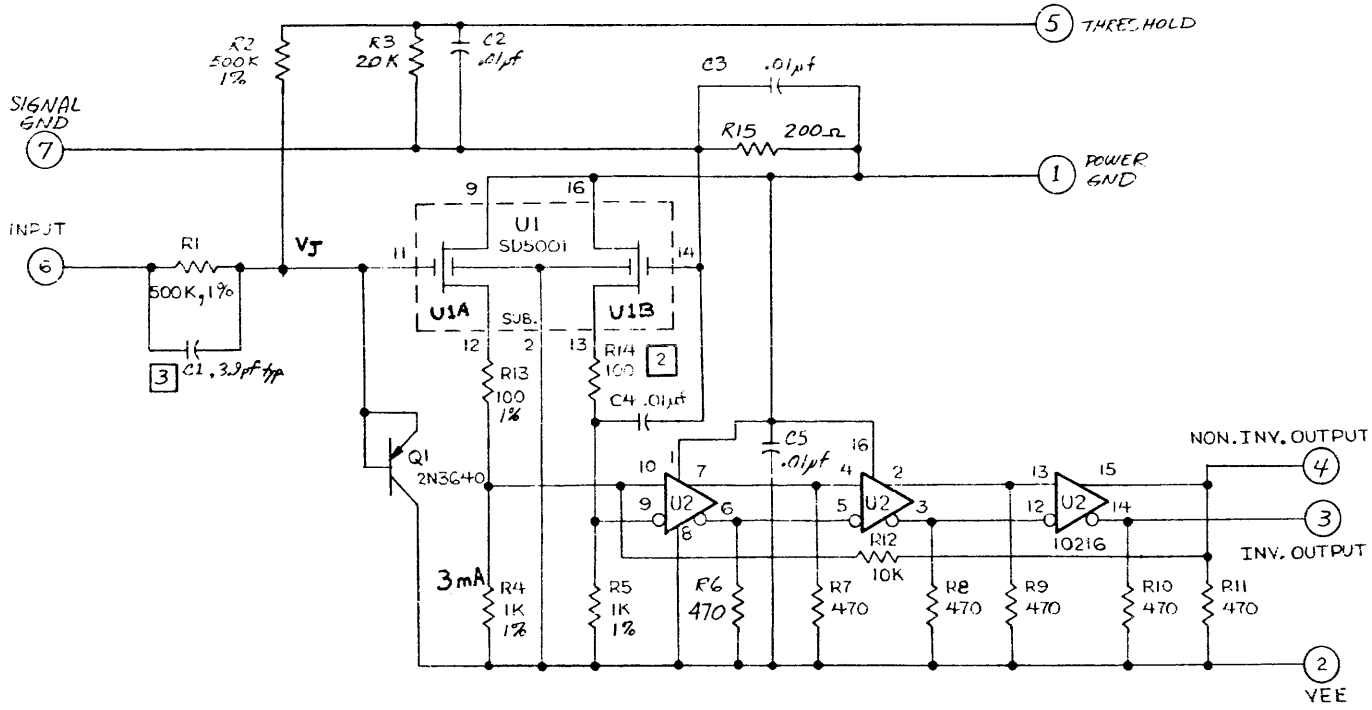


Figure 4.20. Probe Circuit

4.9.1 Resistor R1 (500K) is connected to the input and resistor R2 is connected to the threshold voltage. The voltage at the junction of R1 and R2 is equal to zero when the input voltage is exactly opposite of the threshold voltage (e.g., +1.4 V and -1.4 V):

$$V_J=\tfrac{1}{2}(V_{IN} + V_{TH}).$$

4.9.2 Transistor Q1 protects the gate of U1 from large voltages. The base-collector junction breaks down if V_J is greater than 20 V, and it also conducts if V_J is less than -6 V.

4.9.3 Capacitor C1 compensates for the capacitance from the junction (V_J) to ground. C1 was determined to provide a small amount of overshoot (5-20%).

4.9.4 Transistor U1A operates as a source follower and provides a very high input impedance for V_J. The output of U1A (pin 12) is about 2-3 V lower than the input. Transistor U1B provides a reference voltage that is the same as the gate to the source voltage of U1A. Resistor R13 drops about 300 mV and resistor R14 is adjusted so that, if V_J=0, the voltages at U2-9 and U2-10 are equal. This compensates for the offset voltage of U1A and U1B. The maximum voltage that U1A can output is about -0.6 V at U2-10.

4.9.5 U2 is a 10216 ECL differential line driver and operates in this circuit as a differential amplifier. All three stages are connected to increase the gain. Each stage has a differential gain of about 5 (125 gain for three stages). Thus an input voltage of 8 mV is sufficient to change the output from balanced (both at -1.3 V) to full output (one output at -0.8 and the other at -1.8). To change the outputs from H1 to L0 would require about 16 mV of input change.

4.9.6 Resistor R12 provides positive feedback and introduces hysteresis. The amount of hysteresis is:

$$V_{HYS}=\frac{1 \text{ volt}}{10 \text{ K}} \times 200\ \Omega = 20 \text{ mV}$$

4.9.7 Resistor R15 connects the input ground to the power ground. This protects the input ground lead in case it is connected to a voltage other than ground. The maximum voltage that may be applied without damaging the probe is ±5 V. This resistor also allows the voltage drop in the probe cable (about 50 MV) ground wire to be eliminated and reduces the flow of ground current in the event that the K100 ground is not at the same potential as the system that the probe is connected to. Any ground potential difference changes the effective threshold of the probe. Operation of the probe without

connecting the ground lead introduces about a 50-mV threshold shift (negative).

4.10 Regulator

Refer to the regulator schematic in Section VII.

4.10.1 The Regulator board receives unregulated DC power and provides regulated DC power at the following voltages and currents:

+5 V	up to 15 A
-5.2 V	up to 15 A
+15 V	up to 1 A
+12 V	up to 1 A
-12 V	up to 1 A
- 2 V	up to 3 A

4.10.2 Standard three-terminal regulators are used for +15 V (U3), +12 V U2, and -12 V (U1). R46 and R47 are bleeder resistors for discharging the capacitors when power is off. C14, C15, C17, and C18 are filter caps to ensure stability of the regulators. C12, C13, C16, C21, C19, and C20 also ensure stability and reduce the AC output impedance. Each output has an LED to indicate power-on. R42, R43, and R44 set the LED current at 10 mA.

4.10.3 Regulator boards ETCH D and earlier have a reference voltage circuit that is used by both the +5 V and the -5.2 V regulator. The reference voltage circuit provides a stable +1.2 V reference. The op amp U7C outputs a constant current (26 mA) to the diode CR3 (pin 1). The voltage at pin 1 of CR3 is typically 0.8 V. The resistor R52 provides most of the current necessary and the op amp sources or sinks a small amount of current so as to regulate the current to the diode. The second op amp (U7D) outputs the reference voltage (+1.2 V):

$$V_{ref} = (V_2 - V_1) \times 3 + V_2 = 4V_2 - 3V_1$$

$$= (0.8 - 0.6) \times 3 + 0.6$$

$$= 1.2 \text{ V}$$

The current in the second diode is about 10 mA. The temperature coefficient of the first diode is greater than the second diode because it has 2.5 times the current. The result is that the temperature coefficient of the reference voltage is much less.

4.10.4 Regulator boards ETCH E and later use the output of the -12 V regulator as the reference for the +5 and -5.2 regulators.

4.10.5 The +5 output voltage is regulated by op amp U7B. The output voltage is sensed by R32, R30, and R37 and the op amp compares this to the reference voltage. If the output voltage is low, the op amp output (U7-7) increases. This causes Q4 to conduct more current from the base of Q3 and Q3 supplies more current to the output, which raises the output voltage. The output current is sensed by a 0.01 Ω resistor (actually a PC trace with 0.01 Ω resistance). Resistors R25, R33, R34, R35 form a balanced bridge and R24 unbalances it. If the voltage drop across the 0.01 Ω resistor exceeds the voltage across R24 (about 150 mV), then U7-3 is higher than U7-2 and the output U7-1 goes positive until CR4 starts to conduct. This raises the voltage at U7-6 and causes the drive to Q3 to be reduced so that the output current cannot increase. The voltage drop across R24 is equal to the voltage drop across the 0.01 Ω resistor. Note that the voltage drop across R24 is proportional to the output voltage. This causes the maximum output current to decrease as the output voltage decreases (called foldback current limit) and reduces the power dissipated in the pass transistor (Q3) during current limits such as output shorts. Resistor R36 alters the current limit value so that it does not decrease all the way to zero.

4.10.6 The short circuit current limit can be determined in the following manner:

1. Vout 0

2. $V(\text{at U7-2}) = \frac{8 \text{ V} \times 150}{100K} = 12 \text{ mV}$

150 Ω is R25 in parallel with R33

3. V(at U7-3) = 12 mV + Voffset of U7

4. $I \text{ Limit} = \frac{V(U73)}{200} \times \frac{804 + R_{24}}{0.01} \cong 5A$

if $R_{24} = 25\ \Omega$ and Voffset=0

Note that if Voffset is more than 12 mV positive, the current limit is zero and this could cause start-up problems. And if Voffset is equal to 10 mV negative, the current limit is 9 A.

4.10.7 The maximum current when the output is +5 V is:

$$I_L \text{ (at 5 V)} = \frac{5 \text{ volts}}{R34+R35} \times \frac{R_{24}}{0.01} + I_{S.C.}$$

$$= (0.62 \text{ A}/\Omega) R_{24} + 5 \text{ A}$$

$$\text{for } R_{24} = 25$$

$$I_L \text{ (at 5 V)} = 20 \text{ A}$$

4.10.8 The -5.2 V circuit operates basically the same as the +5 V circuit.

4.10.9 The transistor Q7 provides a -2.0 V output. Resistors R48 and R49 put the base of Q7 at about -3.5 V. The base to the emitter voltage of Q7 is about 1.5 V and the output (emitter of Q7) is -2.0 V. Short circuit protection is provided by the -5.2 V regulator circuit.

4.11 CRT Display

The CRT display receives three signals from the MPU board (Horizontal Sync, Vertical Sync, and Video) and +15 V power (1 amp max.). Figure 4.21 is a block diagram of the CRT display.

4.11.1 The horizontal processor (U1) generates and synchronizes the horizontal scanning by controlling the horizontal output transistor Q2. The flyback transformer serves two purposes; it provides the energy required to return rapidly the scan to the left side and it serves as a DC-to-DC converter for generating the operating voltages for the CRT. The voltages are:

1.	+10 kV	Anode Voltage
2.	+200 V	Focus Voltage (grid 2 and 3)
3.	+38 V	Video (on cathode)
4.	-40 V	Brightness Control (on grid 1)

The horizontal output transistor also serves two purposes; it provides energy to the flyback transformer and it draws current from the horizontal deflection coil to generate the scan from left to right. The horizontal processor synchronizes the horizontal scan so that the "flyback" begins at the same time that the HORIZ. SYNC pulse begins. The MPU board generates the SYNC pulse such that it begins (goes low) 1 µs after the end of the video for each horizontal line and 11 µs before the beginning of the video for the next line. The synchronization may be adjusted by R10 (HORIZ. PHASE) over about a 2-µs range to compensate for component variations. The inductors L1 and L2 allow adjustment of HORIZ. LINEARITY and HORIZ. WIDTH respectively.

4.11.2 The vertical processor (U2) generates and synchronizes the vertical scanning. The vertical processor drives the vertical deflection coil directly and senses the current by measuring the voltage drop across the 1 Ω resistor (R44) in series. U2 contains an oscillator that is synchronized to the VERT. SYNC input pulse, an adjustable constant current source ramp generator, an emitter follower buffer and a power amplifier to drive the deflection coil. The vertical processor circuitry allows adjustment of VERT. HOLD (R36), VERT. HEIGHT (R37), and VERT. LINEARITY (R40).

4.11.3 The VIDEO INPUT signal (+2 V = WHITE, 0 V = BLACK) is amplified and inverted by transistor Q3 and controls the beam current in the CRT (V1). The voltage levels are typically +38 V for black (no beam current) and +20 V for white. The voltage applied to grid #1 is adjusted by R23 (BRIGHTNESS) to compensate for variations in the CRTs. The amplitude of the video signal applied to the cathode may be adjusted by R24. The adjustment procedure for R23 and R24 is covered in the calibration section.

4.11.4 Refer to the schematic (0113-0006) in Section VII for the following more detailed description. Components that are part of the integrated circuits U1 and U2 are denoted by an asterisk following their designators (e.g., Q5*).

4.11.5 Horizontal processor (U1) contains an oscillator, an output buffer, and a phase detector. The oscillator is formed by transistors Q5*, 6*, 7*, 8*, 9*, and 10*. Assume a starting point with C3 discharged (i.e., 0 V across C3). Q5*, 6*, 7*, and 10* are off and Q8 is on. Q9 is a constant current source for the pair Q7 and Q8 and does not change.

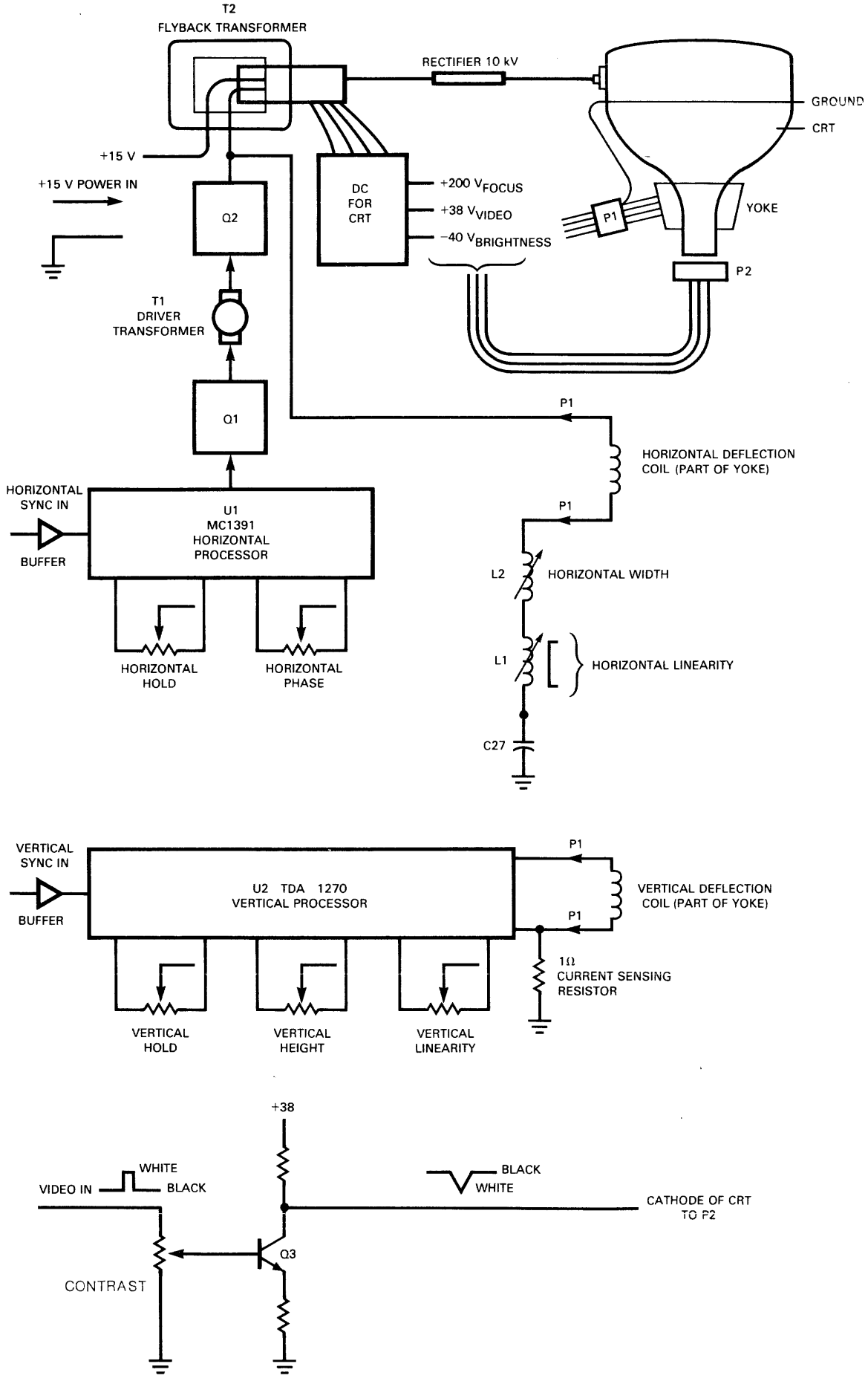


Figure 4.21 CRT Block Diagram

Because Q5* is off, the voltage on C3 is allowed to raise as C3 is charged by the current from R2 and R3. R8* and R10* set the base of Q8* at about 5 V. Thus, when C3 reaches 5 V, Q7* begins to conduct and the voltage dropped across R6* turns on Q6*, which turns on Q5* and Q10*. Q10* and R9* pull the voltage at the base of Q8* down to 2.2 V. This causes Q8* to be turned off completely (and Q7* completely on) until the voltage on C3 drops down to 2.2 V. The voltage on C3 is discharged by Q5* and R4* (430 Ω). This takes about 3 μs. When C3 reaches 2.2 V, Q7*, 6*, 5*, and 10* all turn off, Q8* turns on, and C3 is allowed to begin charging up again. The rate at which C3 charges is determined primarily by R2 and R3 and is typically about 61 μs. The complete period is 64 μs for both charging and discharging (15,625 Hz). Transistor Q4* is an emitter follower buffer and Q3* gives an output signal (Q1* on) whenever C3 is above the voltage level set by R6 and R7 (typically 3.6 V). Typically Q1* is on for 40 μs and off for 24 μs. The resistor R5 can change the frequency of the oscillator by about 2% and is used to synchronize the oscillator to exactly the same frequency as the HORIZ. SYNC input. The voltage applied to R5 is controlled by the phase detector part of U1. C2, C1, and R4 form a low-pass filter and smooth out the voltage. The phase detector compares the leading edge of the HORIZ. SYNC pulse to the leading edge of the flyback voltage and increases or decreases the voltage applied to R5 so as to keep them in synchronization. R10 allows about 2 μs of adjustment by delaying the flyback signal before it gets to the phase detector input (U1-4). When properly synchronized, the signal at U1-4 crosses the V_{REF} level (2 V) exactly in the middle of the phase detector window (established by the HORIZ. SYNC signal applied to U1-3). C28 differentiates the SYNC signal and makes the "window" about 1 or 2 μs wide beginning when the SYNC input goes low. Refer to the waveforms on the schematic (0113-0006), sheet 1. The phase detector operates only during this "window" (when U1-3 is below +1.25 V). When U1-3 is above +1.25 V, Q12* is on and Q17* is off and the phase detector has no current.

4.11.6 Transistor Q1 buffers the output of the horizontal processor (U1-1) and drives the horizontal output transistor (Q2). The transformer T1 provides a negative base drive to Q2 to ensure good turn-off characteristics when Q1 is on (24 μs ± 2 μs). When Q2 turns off, the stored energy in T1 causes the transformer to kickback until the equivalent current is drawn by the base of Q2. The current, when Q1 is on, is about 210 mA (a 1-V drop across R12). Because of the 6.7:1 turn ratio of T1, the base current when Q1 is off is about 1.4 A. During the 40 μs when Q1 is off, this current gradually decreases. When Q1 is on, the current increases again for the next cycle.

4.11.7 Horizontal Output Transistor (Q2).

At the moment just before Q2 turns off, Q2 is drawing current from the flyback transformer (-3 A typical) and from the horizontal deflection coil (-3 A typical). When Q2 turns off, both the flyback and the deflection coil kickback and raise the collector voltage to about 150 V. This very rapidly increases the deflection current to +3 A (rapidly deflecting the CRT beam to the left side of the CRT). The flyback transformer then rings negative and the catch-diode CR1 clamps the Q2 collector to about 0 V. The clamp diode now supplies the deflection current until the deflection current reaches zero. At that time, Q2 (which has already been turned on) begins supplying the deflection current and also starts charging up the flyback transformer. The single turn winding on T1 provides a small voltage to minimize the negative voltage on the collector of Q2 while CR1 is conducting. This negative voltage causes a slight nonlinearity in the horizontal deflection. The single turn winding may be increased to 2 or 3 turns if it is necessary to reduce this nonlinearity.

4.11.8 Horizontal deflection is proportional to the current in the deflection coil and the distance traveled by the electrons. When the beam is deflected, the distance traveled by the electrons increases because the face of the CRT is almost flat. This changes the amount of current required to deflect the beam. To compensate for this and to have a uniform motion of the beam from left to right, the deflection current is changed more slowly when the beam is at either side than when it is in the center. (Once again refer to the waveform on the schematic.) This is implemented by the capacitor C27 (called an

"S" cap because it creates an "S" shaped current waveform). The value of C27 is chosen to give enough voltage change to compensate correctly for the change in deflection sensitivity. A larger value of C27 causes faster deflection at the edges and a smaller value of C27 causes slower deflection at the edges. The variable inductor L2 increases or decreases the deflection current without changing the shape of the waveform and is used to adjust the width of the scan. The inductor L1 can be adjusted to saturate near the end of the waveform. When L1 saturates, the total inductance decreases and the rate of change of current increases. This changes the rate of deflection at the right side of the CRT without affecting the left side. Sometimes a small correction is needed at the left side of the screen, and resistor R52 and capacitor C29 slow down the scan slightly there. Normally R52 and C29 are not needed.

4.11.9 The vertical processor (U2) is synchronized to the VERT. SYNC input. When the VERT. SYNC input goes low, a negative pulse is applied to U2-3 (by C19) and the capacitor C20 is discharged. The ramp generator is also discharged (U2-12) goes to zero and U2-1 goes to zero). The oscillator is adjusted to a slightly lower frequency than the vertical sync pulses. Thus the sync pulse always discharges the oscillator just before it reaches the threshold of Q3*, and the oscillator runs at the sync input frequency. The ramp generator output (U2-12) supplies a constant current of about 20 µA (determined by R37 and R38), and the network of R39, C20, C21, R40, and R41 generates the ramp waveform as shown on the schematic. This curved waveform, when added together with the waveform generated by C23, controls the deflection current waveform. These signals are added together by R42, R45 and R46. The waveform at U2-4 shows the operation as follows:

1. Just before the sync pulse is received, the deflection current is about -0.25 A (flowing into U2-4).
2. The leading edge of the sync pulse resets the ramp and the amplifier stops drawing current.
3. The deflection coil kicksback until it forward biases the catch dioded from U2-4 to +15.
4. The deflection current rapidly decreases to zero.
5. The amplifier turns on saturated and provides a +15-V output until the deflection current reaches the desired level (+0.25 A).
6. At this time, U2-4 drops to the voltage required to maintain the desired current.
7. The voltage across C26 is approximately 8 V and the voltage dropped by the 0.25 A flowing through the deflection coil (6 Ω) and the current sense resistor R44 (1 Ω) is about 1.75 V.
8. The voltage at &2-4 is maintained at about 0.35 V below the sum of C26 and the drop across the series resistance. This causes the desired decrease of deflection current of about 0.033 A/ms. The voltage at U2-4 is about 10 V (8 + 2) at the beginning and about 6 V (8 - 2) at the end of the vertical scan.

4.11.10 R48 and C25 provide a low impedance load for the amplifier at high frequencies to ensure stability of the amplifier and do not otherwise affect the shape of the deflection waveform. R47 and C24 are also used only to compensate the amplifier to ensure stability.

SECTION V

CALIBRATION PROCEDURES

5.1 Recalibration of Internal Circuits

The following calibration procedures are intended to be used in recalibrating the internal circuits of the Model K100-D. The entire circuitry was calibrated before shipment and should not require any recalibration for at least six months or 1000 hours of operation. Refer to the schematics and assembly drawings in Section VII for additional help in locating devices referenced in this procedure. The raster scan display used in the K100-D has many adjustments that can be verified during power up "STATUS" mode.

5.2 Required Test Equipment

The test equipment listed in Table 5.1 are required to calibrate the K100-D.

Table 5.1 Test Equipment

Equipment	Manufacturer	Model No.
Digital Voltmeter	Dana	4200
Oscilloscope	Tektronix	485
Pulse Generator	Tektronix	PG502

5.3 Calibration of Raster Scan Display

5.3.1 Front Panel Controls

To check the front panel function and software control, select AC input to 120 VAC, connect AC power input, and turn the K100-D ON.

1. The "POWER ON" LED and the "ERROR" LED should both come on.
2. The "ERROR" LED should go out after 12 to 13 s.
3. Within one minute the CRT should show the Status mode.
4. "POWER UP COMPLETE" should be in the upper left corner of the screen. This is the only time this label appears.
5. If a fault is detected in power up, "ERROR IN POWER UP" should appear in the upper left corner of the screen.
6. Check the screen in Figure 5.1 for the proper power-up format.
7. Check all modes for proper format and operation.
8. Verify the quality of the display by checking for a linear display, a stable horizontal sync, good intensity (brown out), and characters centered in the display field and CRT.
9. With "POWER UP COMPLETE," the diagnostic routine has performed the following checks.
   - All keys and switches on the front panel are checked for a "not pressed" condition.
   - All 32,768 bytes of processor RAM are checked by writing and reading data to and from every bit.

- All 24,576 bytes of processor ROM are checked.

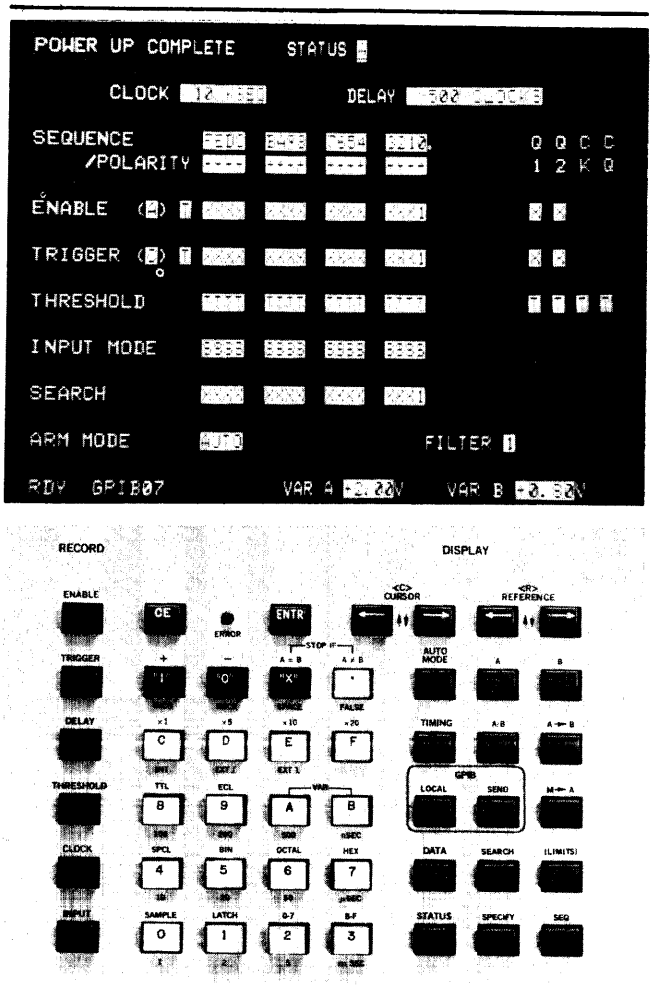


Figure 5.1 Status Display and Keyboard

- All 1024 words of high-speed record memory are checked.

10. Remove the top cover of the K100-D by taking out six screws. The display board will be accessible.

NOTE: If an error has occurred, an error indication will be given. Go to the Maintenance section of the manual for a full explanation.

The display was fully calibrated prior to shipment on an alignment fixture. Any adjustment will be minor unless total failure has occurred. Calibration of the display is as follows.

Power up the K100-D. Status mode is shown. Verify the full display on the screen. Obtain the desirable display as follows (see Figures 5.1, 5.2 and 5.3):

- Adjust L2 for WIDTH.
- Adjust R14 for FOCUS.
- Adjust R23 for BRIGHTNESS.
- Adjust R37 for HEIGHT.

Adjust R37 (height) so that full Status mode display is shown 0.250 in. from top and bottom of screen (see Figure 5.2).

Adjust L2 (width) so that full status mode display is horizontally about 0.100 in. from the edges of the bezel (see Figure 5.2).

Adjust R14 and R23 to obtain a clear display.

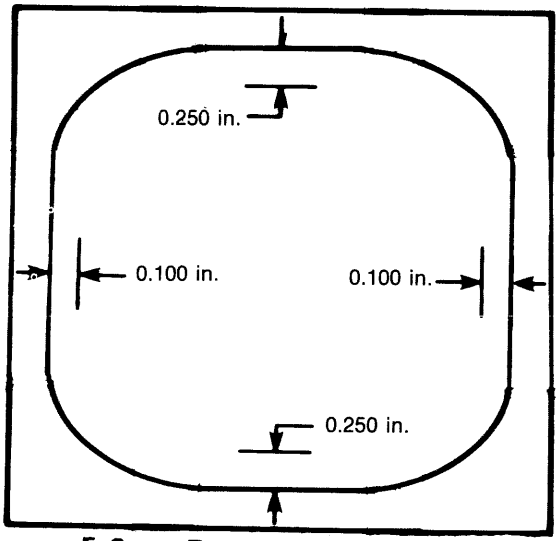


Figure 5.2 Position of Status Mode Display

If total alignment is required, consult the Biomation Division factory for information.

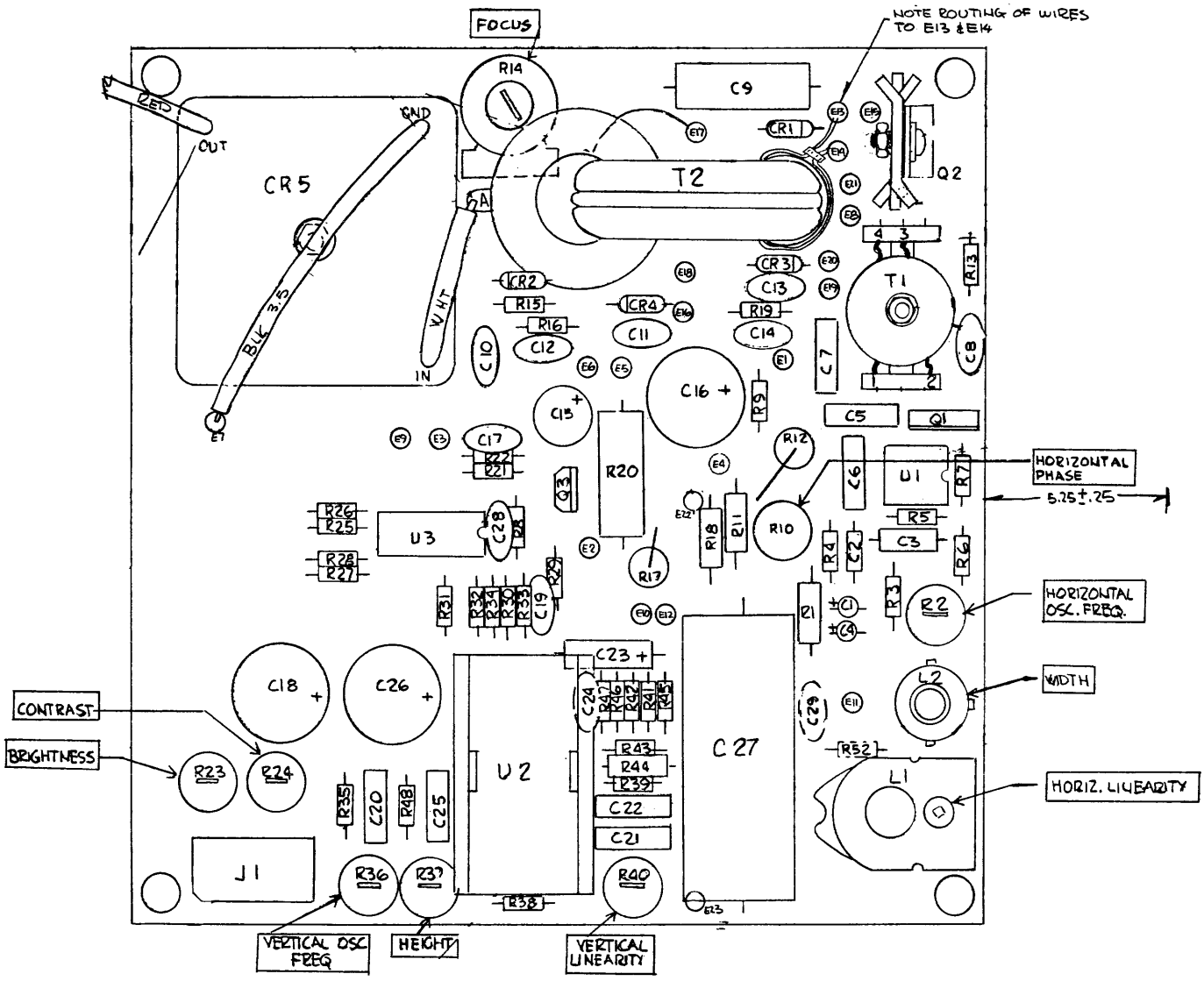


Figure 5.3 Data Display Assembly

5.4 Power Supply Adjustments

> - CAUTION -
>
> **First select proper AC voltage on slide switches on the rear panel.**

Allow the unit to warm up for 10 to 15 minutes. After warm up, turn the power off and put the regulator board on the extender.

> - CAUTION -
>
> **Do not remove the regulator board immediately. After AC power has been turned off, allow 15 to 20 s for filter caps to discharge.**

Turn power on.

> - CAUTION -
>
> **Do not leave the regulator on the extender for more than 20 minutes.**

Adjust R30 for +5 V ±0.01 V at J10-4.

Adjust R2 for -5.2 V ±0.01 V at J9-3.

Check +12 V for +12 V ±0.6 V at J10-8.

Check +15 V for +15 V ±0.75 V at J10-11.

Check -2 V for -2 V ±0.06 V at J9-11.

Check for -12 V ±0.6 V at J10-9.

Turn power off and return the regulator board to its chassis position.

5.5 Threshold Adjustments

Place threshold board on the extender. Turn the K100 on and allow 2 to 3 minutes for power supplies to stabilize. See Figures 5.4 and 5.5.

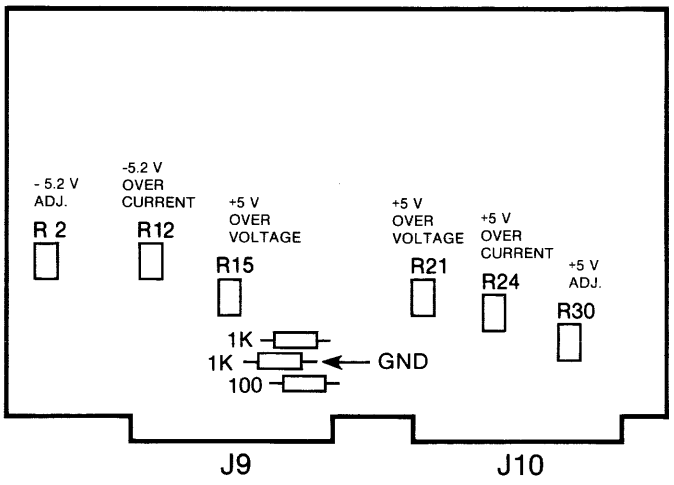


Figure 5.4 Regulator Board

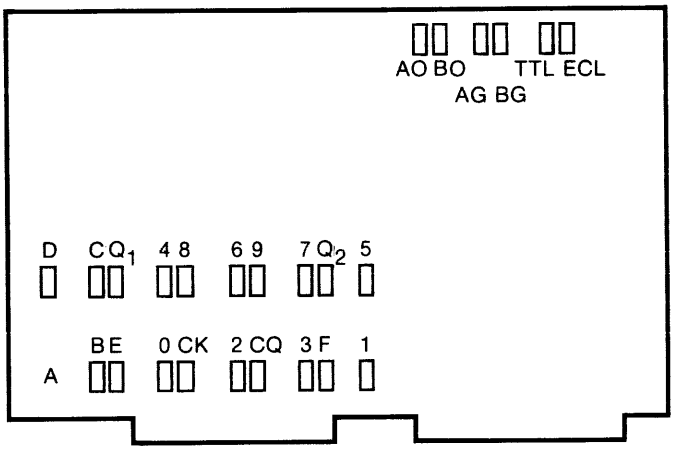


Figure 5.5 Threshold Board

Monitor IC 1E pin 1 with DVM. Perform the following tests while monitoring the test point.

KEYSTROKE [THRESHOLD] [VAR A] STEP 1
[VAR A] STEP 2
[VAR B] STEP 3
[VAR B] STEP 4

(20 times) [ENTER]

SPECIFY [VAR A] [-] STEP 1 [6] [.] [3] [5]
[VAR A] [+] STEP 2
[VAR B] [-] STEP 3
[VAR B] [+] STEP 4

[ENTER] [AUTO ARM]

1. Use "VAR A," "VAR A," and "-" for set up. Test point should read +6.35 ±50 mV. Adjust AO to obtain proper value.

2. Use "VAR A," "VAR A," and "+" for set up. Test point should read -6.35 ±50 mV. Adjust AG to obtain proper value.

3. Use "VAR B," "VAR B," and "-" for set up. Test point should read +6.35 ±50 mV. Adjust BO to obtain proper value.

4. Use "VAR B," "VAR B," and "+" for set up. Test point should read -6.35 ±50 mV. Adjust BG to obtain proper value.

KEYSTROKE [THRESHOLD] [TTL]

(20 times) [ENTER] [AUTO ARM]

1. Test point should read -1.40 ±50 mV. Readjust TTL to obtain proper value.

KEYSTROKE [THRESHOLD] [ECL]

(20 times) [ENTER] [AUTO ARM]

1. Test point should read +1.30 ±50 mV. Readjust ECL to obtain proper value.

Monitor all threshold outputs: THO-THCQ (20 each) for all the above tests. See Figure 5.6.

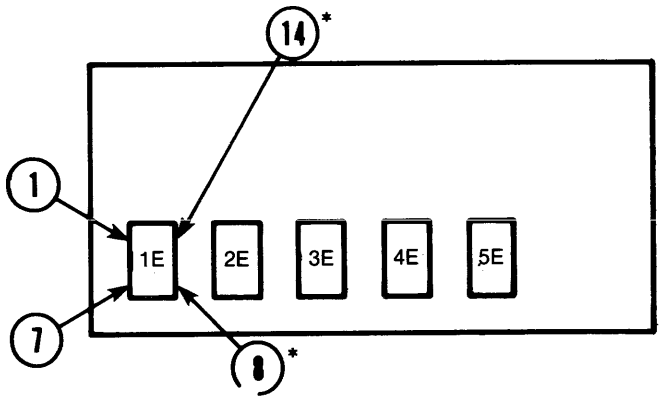


Figure 5.6

*NOTE: Some units have two ICs in each IC location, labeled A and B. Pins 1 and 7 are the outputs.

This procedure adjusts the threshold to its proper values, but if failure occurs contact the Customer Service Department at the factory, Phone (408) 988-6800, TWX 910-338-0509, for the Summation Alignment technique.

5.6 Record Memory Adjustments

Remove the "0-7" memory board (see Figure 5.10) and put on an extender. Turn the power on. Tests are performed using power up status mode.

Using input B, put a 1 MHz TTL square wave into channels 0-7.

1. If there is an error in power up, keystroke [CE].

2. Keystroke [AUTO ARM]. A flickering "BSY" should be displayed in the lower left corner of the screen. Keystroke [TIMING]. The timing mode should be displayed with some kind of data on channel 0-7.

3. Monitor test point IC 9A pin 12 ($\overline{WE}$) with Channel A of scope. With Channel B monitor test point IC 9A pin 1 (ADDR). Synchronize scope to Channel A.

NOTE: Superimpose the two patterns so as to create a common TTL threshold (+1.4 VDC).

a. Adjust D1 (R13) for 10 ns between the last address edge and falling edge of the $\overline{WE}$ (see Figure 5.7).

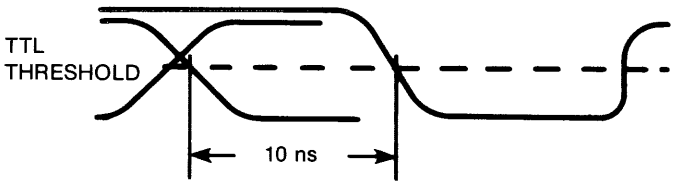


Figure 5.7

b. Adjust W1 (R14) for 10 ns between the $\overline{WE}$ rising edge and the first address edge. (See Figure 5.8).

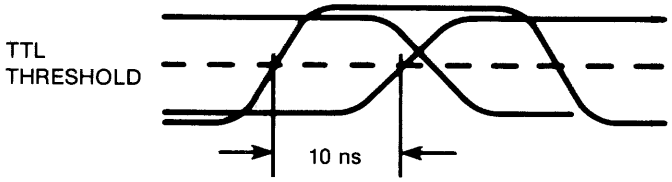


Figure 5.8

4. Repeat procedure for Ø2, Ø3, and Ø4. See Figure 5.9 and Table 5.2.

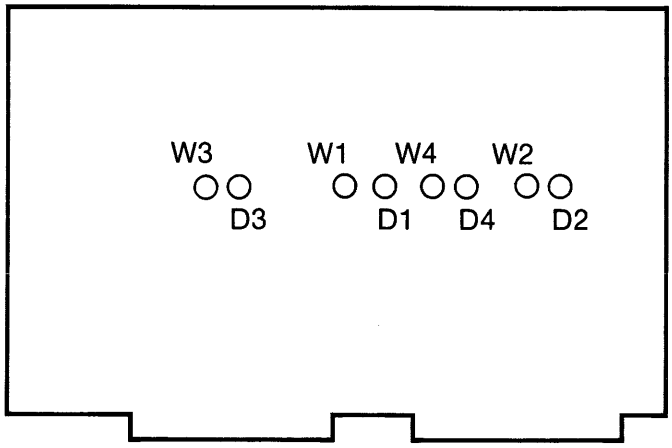


Figure 5.9 Adjustments

Table 5.2

	Testpoint	Adjust
Ø2	9D12	W2 (R20)
	9D1	D2 (R21)
Ø3	9B12	W3 (R6)
	9B1	D3 (R7)
Ø4	9E12	W4 (R14)
	9E1	D4 (R15)

5. Turn power off and return "0-7" memory to its chassis position. Repeat the process for "8-F" memory (see Figure 5.10). Use an input.

6. Turn unit off and replace "8-F" memory to its chassis position.

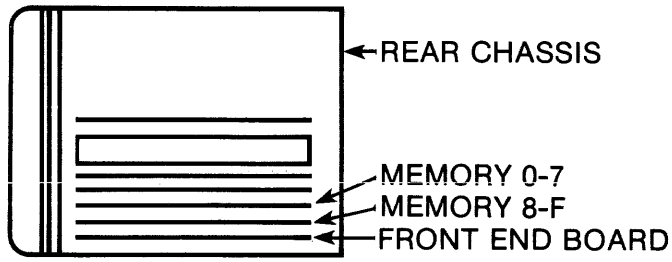


Figure 5.10 8-F Memory Location

5.7 Special Precautions

There is an adjustment on the record control board for a 100 MC oscillator. This adjustment was set at the factory using a special alignment technique. Do not change the setting unless failure occurs! Consult the factory for the alignment procedure. This adjustment is critical to the operation of the K100-D.

This completes the calibration of the Model K100-D Logic Analyzer.

SECTION VI

MAINTENANCE

6.1 Introduction

This section covers the K100-D self-diagnostic routine within the instrument. The diagnostic routine checks the microprocessor ROMs and RAMs. Repair of other boards can be performed with the aid of the technical description or additional information from the factory.

The drawings in Section VII have been included to aid service personnel who wish to troubleshoot to the component level. Additional assistance in a particular problem can be obtained by contacting the Customer Service Department at the factory: Phone (408) 988-6800, TWX 910-338-0509.

In summary, there are two methods of service available:

1. Return the entire unit to the factory or service center for repair.

2. Troubleshoot the problem to the component level with the aid of the Technical Description and schematics or with the aid of factory personnel.

6.2 Diagnostic Routine and Indications

The K100-D diagnostic routine performs the following checks everytime the power is turned on.

1. All keys and switches on the front panel, except AC POWER, are checked for a "not pressed" condition. If any key or switch is pressed or shorted, an error indication is given.

2. All 32,768 bytes of microprocessor RAM are checked by writing and reading data to and from every bit. If any failure is detected, an error indication is given.

3. All 24,576 bytes of microprocessor ROM are checked. A parity byte is generated for each ROM when the ROM is "burnt." The parity value is generated again by the diagnostic routine and compared to the original parity byte. If there is a difference, an error indication is given.

4. All 1024 words of high-speed record memory are checked by writing and reading data to and from every bit. If any failure is detected, an error indication is given.

If no errors are discovered by the diagnostic routine, the following occurs:

1. As soon as the AC POWER switch is turned on, the ERROR light at the top of the keyboard will light. The CRT will display a random pattern. (If the K100-D is "cold" when power is turned on, nothing will be displayed until the CRT warms up. This usually takes longer than it takes to execute the diagnostic routine. In this case, steps 1 through 5 will not be seen on the CRT.)

2. The CRT will have an all bright display.

3. The CRT will be erased (i.e., the screen will be dark).

4. The CRT will display alternating black and white vertical lines.

5. The vertical lines will shift slightly. By the end of this step, about 4 s will have gone by since the power was turned on.

6. After about 13 s from power on, the ERROR light will go off and STATUS display will appear on the CRT. The message "POWER UP COMPLETE" will be in the upper left corner of the screen.

If an error has occurred, an error indication will be given. The following is a list of the error indications that can occur and the associated error description.

ERROR INDICATION	ERROR DESCRIPTION
The ERROR light is still on at least 20 s after power is turned on. It is not blinking.	The microprocessor has failed to reset and/or cannot run properly. No operation of the K100-D is possible.
The ERROR light starts to blink as soon as power is turned on. Pressing only the black "X" key for at least 1 s does not stop the blinking.	One or more keys or switches are pressed or shorted. The key or switch must be released or the short must be cleared before any further operation of the K100-D is possible. NOTE: The operator of the K100-D may check to see that a particular key or switch makes contact by doing the following procedure. 1. Turn the power off. 2. Press the key or switch. (If a switch under the CRT is being checked, it should be held either up or down.) 3. Without releasing the key or switch, turn the power on. The ERROR light should immediately start to blink and should continue to blink as long as the key or switch is pressed. 4. As soon as the key or switch is released, the ERROR light should return to a steady on state. The remaining diagnostics will run and if everything else is okay, normal operation will begin.
The ERROR light starts to blink within 6 s after power is on. Pressing only the black "X" key for at least 1 s turns the ERROR light off for as long as the key is pressed.	An error has been detected in either ROM or RAM of the microprocessor. To determine which part of ROM or RAM has the error, do the following. 1. Press the black "1" and the black "0" keys down **one key at a time.** Hold the key pressed for at least 1 s. Do not press any other key or switch. One of these keys will turn the ERROR light off for as long as the key is pressed. The other key will have no effect on the ERROR light. If the "1" key turns the ERROR light off, the error is in ROM. If the "0" key turns the ERROR light off, the error is in RAM.

ERROR INDICATION

ERROR DESCRIPTION

2. Press the white keys **one key at a time.** Hold the key pressed for at least 1 s. Do not press any other key or switch. One of these keys will turn the ERROR light off for as long as the key is pressed. The other keys will have no effect on the ERROR light. Note the number or letter of the key that turns the ERROR light off. If the error is a ROM error, do steps 3 and 5. If the error is a RAM error, do steps 4 and 5.

3. Find the ROM on the microprocessor PC board that has the same number or letter as noted in step 2. (The number or letter will be on the PC board immediately above the ROM.) That will be the ROM in error.

4. The table below gives the relationship between the number or letter of the key that turns off the ERROR light and the code for the defective RAM.

Key	RAM Code
0	B1
1	B2
2	B3
3	B4
4	B5
5	B6
6	B7
7	B8
8	C1
9	C2
A	C3
B	C4
C	C5
D	C6
E	C7
F	C8

NOTE: The C8 RAM is the first RAM tested. If it appears to be in error, it is likely that the problem is really somewhere else (e.g., a short in the address lines or chip select lines.) A check should be made for these other possible problems before replacing the RAM chip.

ERROR INDICATION

The ERROR light starts to blink 6 to 13 s after power on. A display similar to Figure 6.1 appears on the CRT.

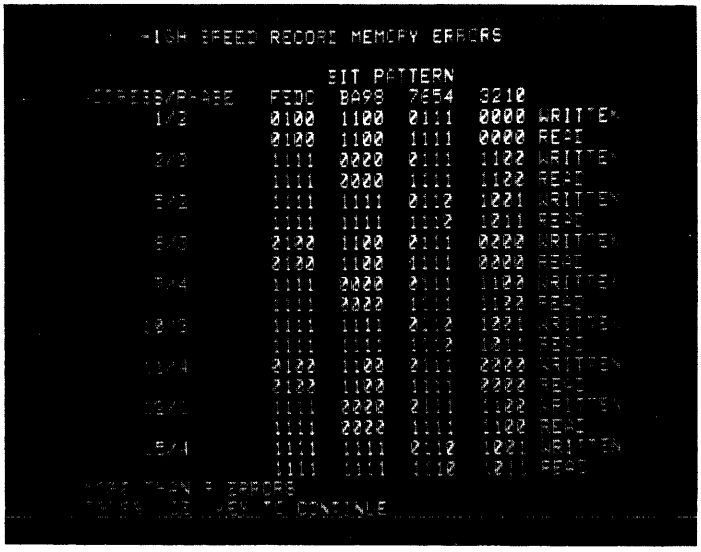


Figure 6.1

ERROR DESCRIPTION

The RAM code gives the PC board the row letter (either B or C) and the column number (1-8.) The row letters and column numbers are printed on the PC board, not on the chip.

5. The operator may attempt to bypass errors in microprocessor ROM or RAM by pressing the CE key for at least 1 s. If the CE key is pressed, the K100-D will skip the remaining diagnostics and go to the STATUS display. The message "ERROR IN POWER UP" will be in the upper left corner of the screen.

   Note that the K100-D may not function properly if an error is bypassed in this way.

An error has been detected in high-speed record memory. The display on the CRT gives the following information.

1. ADDRESS - The address within high-speed record memory (0 through 1023) where the error was detected.

2. PHASE - The phase within high-speed record memory (1 through 4) where the error was detected.

3. BIT PATTERN WRITTEN - The bit pattern that was written to high-speed record memory. Each bit corresponds to a particular channel (0 through 9 and A through F). The channel ID appears as a column heading on the display.

4. BIT PATTERN READ - The bit pattern that was read back from high-speed record memory.

Any difference between what was written and what was read is an error. Up to nine addresses with one or more bit errors will be displayed on the CRT. Usually, when a particular chip is bad, all addresses will have the same phase number and all addresses will have the same channel bit wrong. Refer to the record memory board schematic to locate the bad chip. If more than one phase is wrong or more than one channel bit is wrong, the error is usually a shorted trace or other PC board error. Other kinds of errors can cause these same indications.

ERROR INDICATION	ERROR DESCRIPTION
	The operator may attempt to bypass errors in high-speed record memory by pressing the CE key for at least 1 s. The K100-D will go to the STATUS display. The message "ERROR IN POWER UP" will be in the upper left corner of the screen. Note that the K100-D may not function properly if an error is bypassed in this way.

6.2.1 Failure Chart

The following setup shows how to read the failure chart. Refer to Figure 6.1.

HIGH SPEED RECORD MEMORY ERROR BIT PATTERN

Address/Phase → FEDC BA98 765433210
└ (Channel Designation)

1/2 → 0100 1100 0111 0000 Written
└ (Data going into memory)
→ 0100 1100 1111 0000 Read
└ (Data read out of memory)

2/3 1111 0000 0111 1100 Written

1111 0000 1111 1100 Read

(Phase of sample clock failed)

(Location in memory addressing)

NOTE: Upon reading this chart, notice Channel Designation 7 has 0 written and 1 read out of memory. This shows data is incorrect at Memory Address 1, Sample Clock phase 2.

Phase location on PCB:

Phase Ø1 Row A
Phase Ø2 Row D
Phase Ø3 Row B
Phase Ø4 Row F

Channel Location on PCB:

CHANNEL B	INPUT A	COLUMN on PCB
0	8	9
1	9	10
2	A	11
4	B	12
5	D	14
6	E	15
7	F	16

Locate the channel where the failure to read back what was written in occurred. Determine the phase of failure and its location in memory. Verify the inputs on the failed memory I.C. See Table 6.1.

NOTE: The Memory boards, when viewed from front of machine, can be identified as follows:

Channel 0-7: Third from right side.
Channel 8-F: Second from right side.

Table 6.1 Identification of Failed Record Memory IC Package Related to Input Channel and Clock Pulse.

Channel / Phase	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
1	9A	10A	11A	12A	13A	14A	15A	16A
3	9B	10B	11B	12B	13B	14B	15B	16B
2	9D	10D	11D	12D	13D	14D	15D	16D
4	9E	10E	11E	12E	13E	14E	15E	16E

6.3 Required Test Equipment

The following test equipment will be required to conduct the diagnostic procedure.

1. Two pulse generators capable of <1 ns rise and fall times. A minimum pulse width of 2 ns of output adjustable from -5 to +5 V into 50Ω with single pulse capability.

2. An oscilloscope: two channel DC to 200 MHz input bandwidth. Horizontal resolution to 1 ns.

3. A frequency counter, range 1 to 100 MHz (minimum).

6.4 Diagnostic and Troubleshooting Procedures

DIAGNOSTIC PROCEDURE

6.4.1 Equipment Set-Up

Connect the K100-D to AC power cord. Turn on the K100 and allow a few minutes for "POWER UP COMPLETE" status mode:

NOTE: The "POWER UP COMPLETE" status mode should appear in the upper left-hand corner of the display. If failure occurs, verify step 6.2, diagnostic.

Connect Input A and Input B probe sets to K100-D inputs.

Display should be as in Figure 6.2.

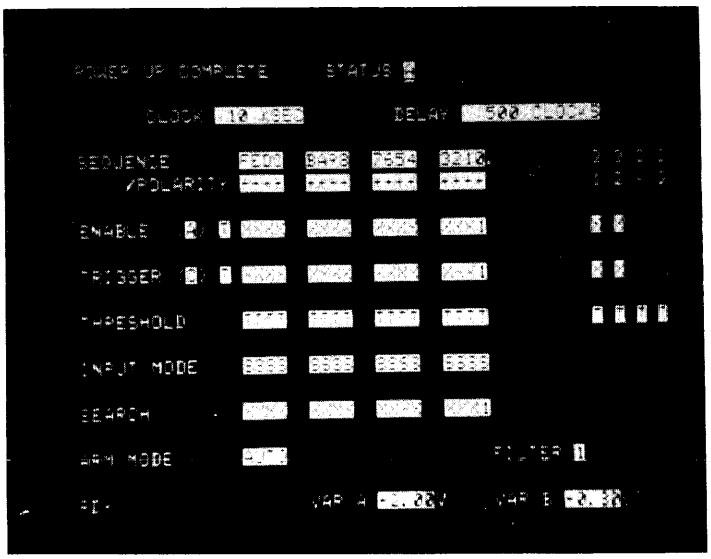


Figure 6.2

NOTE: **The Power Up Status mode condition can be selected so that all channels start in TTL or ECL Threshold. The Clock can be started in INT or EXT ∫ via the customer selection switches on the Record Control board. The switches are factory set so that all channels power up in TTL Thresholds and Internal Clock.**

Depress Manual Enable, Arm, Enable and Trigger. Verify that lower left-hand corner of the display changes. RDY→EN?→TRIG?→BSY→RDY .

Depress [TIMING] , verify sixteen traces on screen. Data should be all logic Low levels.

Depress [STATUS] , [THRESHOLD] , [ECL] , 16 times [ENTR]. Manual Arm .

Depress [M→A] , [TIMING] . Verify that there are sixteen traces on the screen. Data should be all logic High levels. Depress [STATUS] , [THRESHOLD] , [TTL] , 16 times [ENTR] Auto Arm.

6.4.2 Combinational Trigger

Set an external pulse generator for 1 MHz square wave at +3 V level (0 VDC baseline). Input to Channel 0.

Depress Auto Arm, Auto Enable, [STATUS], [TRIGGER] , Auto Arm. Verify that lower left-hand corner of the display changes RDY→BSY rapidly. Depress [TIMING] . Verify data on screen. Trigger point to show up on rising edge of data in the center of screen.

Depress [STATUS] , [ENABLE] , ["X"] , 14 times, ["1"] , ["X"] , [ENTR] .

Depress [TRIGGER] , ["X"] , 14 times, ["1"] , ["X"] , [ENTR] , Auto Arm.

Move input to channel 1. Verify display RDY→BSY rapidly changes.

Repeat for all channels 2-F. Change TRIGGER and ENABLE to "1" on channel under test. Return channel not under test to "X". Verify results.

Perform same test starting with channel 0, but change TRIGGER BIT to "0." Verify results.

Input external generator to channel 0 with all ENABLES set to "X." Set channel 0 TRIGGER to "1," all other channels to "X." Depress AUTO ENABLE and AUTO ARM. Verify RDY→ BSY.

Set external generator to 1 MHz at ECL levels (-0.8 V to -2.0 V).

Depress [STATUS] , [THRESHOLD] , [ECL] , 16 times. [TRIGGER] , [F] , 4 times [ENTR]. Input to channel 0.

Depress AUTO ARM, [TIMING] , verify data on display. Remove input from channel 0.

Repeat test for all channels (1-F).

6.4.3 Threshold Checks

Depress [STATUS] [SPECIFY] , [A] , [-], [4] , [.] , [0] , [0] , [ENTR] , [THRESHOLD] [A] 16 times [ENTR] .

Set external generator for 1 MHz square wave at -5 V level (0 VDC baseline). Input to channel 0. Depress [TIMING] and verify data on screen.

Repeat tests for channels 1-F.

Depress [STATUS] [SPECIFY] [A] , [+] , [4] [.] [0] [0] [ENTR] .

Depress [TRIGGER] [0] (white), 4 times.

Set external generator for 1 MHz square wave at +5 V level (0 VDC baseline). Input to channel 0. [TIMING] , verify data on screen.

Repeat tests for channels 1-F. Repeat tests using [B] in place of [A] and verify results.

6.4.4 Internal Clock

Depress [STATUS] , [THRESHOLD] [TTL] 16 times [ENTR], Auto Arm.

Set external generator to rates in Table 6.2. Verify [TIMING] diagram. Specify clock as in Table 6.2. Rearm (Auto Arm) is necessary after clock change.

Data may be input to any channel. The combinational trigger for channel used may be "1" or "0"; set all unused channels to "X."

Table 6.2

Data Rate	Clock Rate	Display Cycles
10 µs (square wave)	10 ns	1
	20 ns	2
	50 ns	5
	100 ns	10
100 µs (square wave)	200 ns	2
	500 ns	5
	1 µs	10
1 ms (square wave)	2 µs	2
	5 µs	5
	10 µs	10
10 ms (square wave)	20 µs	2
	50 µs	5
	100 µs	10
100 ms (square wave)	200 µs	2
	500 µs	5
	1 ms	10
1 s (square wave)	2 ms	2
	5 ms	5
	10 ms	10
10 s (square wave)	20 ms	2
	50 ms	5

Return all settings as in Figure 6.2.

[ENABLE] , Auto Arm, TRIGGER FILTERED

[3] [ENTR] , Auto Arm. Set external generator to +3 V (15 ns pulse width and 100 ns (Period) with 0 VDC baseline. Input to channel 0. Verify EN? Increase pulse to 20 ns. Verify that unit triggers. Perform values as in Table 6.3.

Table 6.3

F = 4	PW = 30 ns (triggers unit)
F = 5	PW = 40 ns (triggers unit)

6.4.5 Filter Tests

Depress Auto Enable. With F=5, reduce pulse width to less than 37 ns. TG? should appear.

6.4.6 Delay Insertion Tests

Return all settings as shown in Figure 6.2. Set external generator to 1 μs pulse, with single pulse capability. The signal should be at a +3 V level (0-VDC baseline).

Depress AUTO ENABLE. [STATUS] [DELAY] [8] [0] [0] [ENTR]. Arm the K100-D and manually pulse the generator. TIMING. Display should show pulse at 200 (TRIGGER-T).

Depress [STATUS] [DELAY] [4] [0] [0] [ENTR]. Arm the K100-D and manually pulse the generator. [TIMING]. Display should show pulse at 600 (TRIGGER-T).

Depress [STATUS] [DELAY] [2] [0] [0] [ENTR]. Arm the K100-D and manually pulse generator. [TIMING]. Display should show pulse at 800 (TRIGGER-T).

Depress [STATUS] [DELAY] [1] [0] [0] [ENTR]. Arm the K100-D and manually pulse generator. TIMING. Display should show pulse at 900 (TRIGGER-T).

Return all settings as shown in Figure 6.2. Pulse generator should be set for 1 μs.

Depress [CLOCK] [20] [ns] [ENTR]. EVENTS DELAY [DELAY] [4] [ENTR] AUTO ARM. [TIMING].

Pulse generator five times. Verify that the edge (positive going) is at the center of the screen.

[SPECIFY] [DELAY] [8] [ENTR] AUTO ARM.

Pulse the generator nine times. Verify that the edge (positive going) is at the center of the screen.

NOTE: 100 MHz operation is not specified in EVENTS DELAY.

6.4.7 Display Functions

Power down K100, then turn on. Allow five minutes for warm up.

Depress [TIMING]. Verify data as in Figure 6.3.

Depress [X5]. Verify data as in Figure 6.4.

Depress [X10]. Verify data as in Figure 6.5.

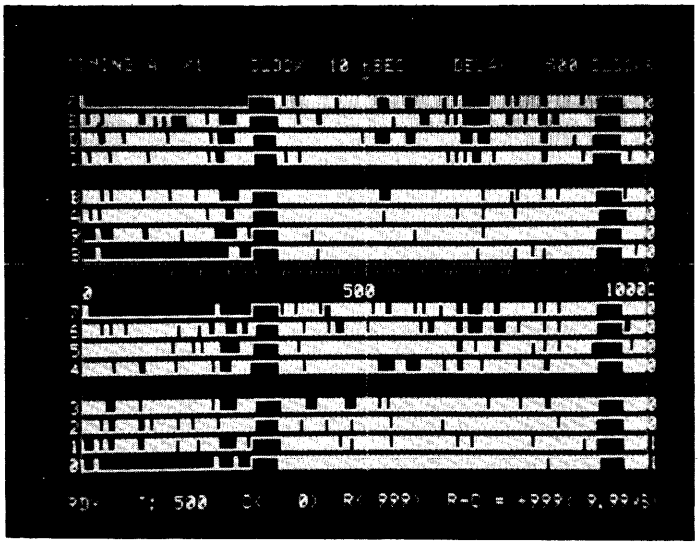


Figure 6.3

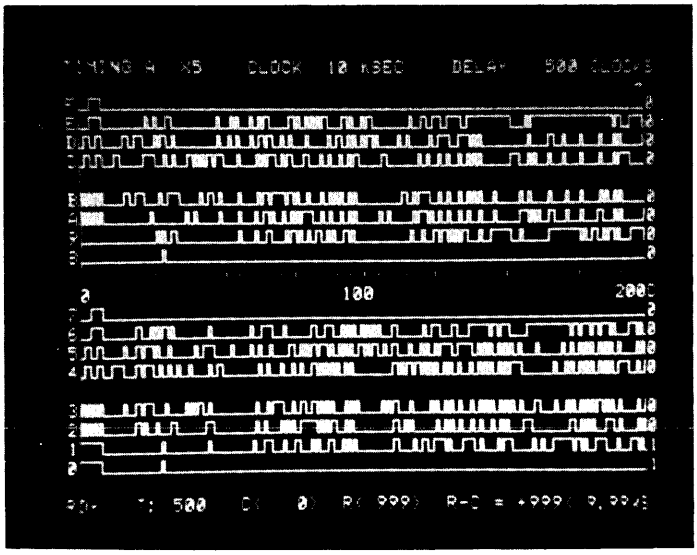


Figure 6.4

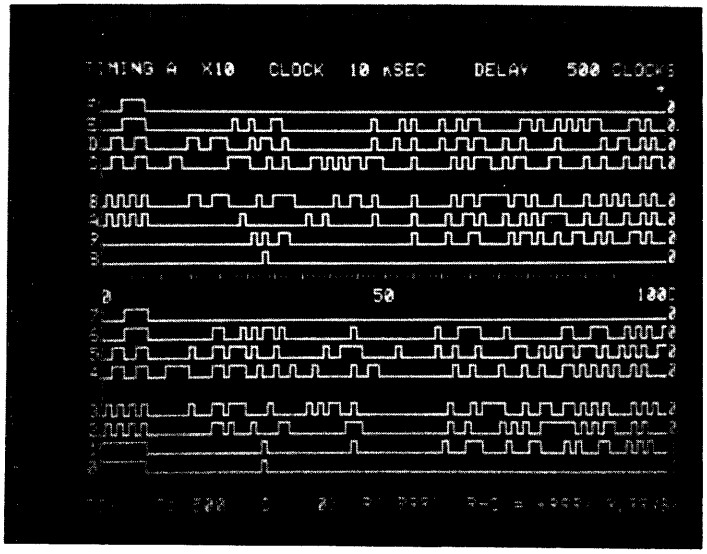


Figure 6.5

Depress X20 . Verify data as in Figure 6.6.

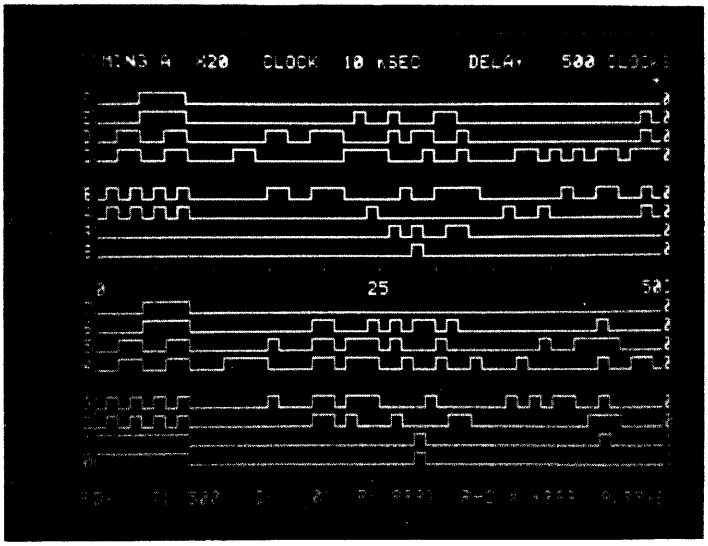


Figure 6.6

Depress [SPECIFY] [←] CURSOR [5] [0] [0] [ENTR] . Verify that the vertical line at the left-hand edge of the display is "T."

Depress [SPECIFY] [→] REFERENCE [5] [2] [4] [ENTR] . Verify that vertical line at center of screen is "524."

Observe the characters at the bottom of the display. They should read as follows:

RDY T:500 C ⟨500⟩ R ⟨524⟩ R-C = +24 (0.24 μs).

Depress [SPECIFY] [→] REFERENCE [5] [1] [0] [ENTR] . Verify that the vertical line moves left to "510."

Observe the characters at the bottom of the display. They should read as follows:

RDY T:500 C ⟨500⟩ R ⟨510⟩ R-C = +10 (0.10 μs).

Depress [DATA] [BIN] . Verify that the display is as in Figure 6.7

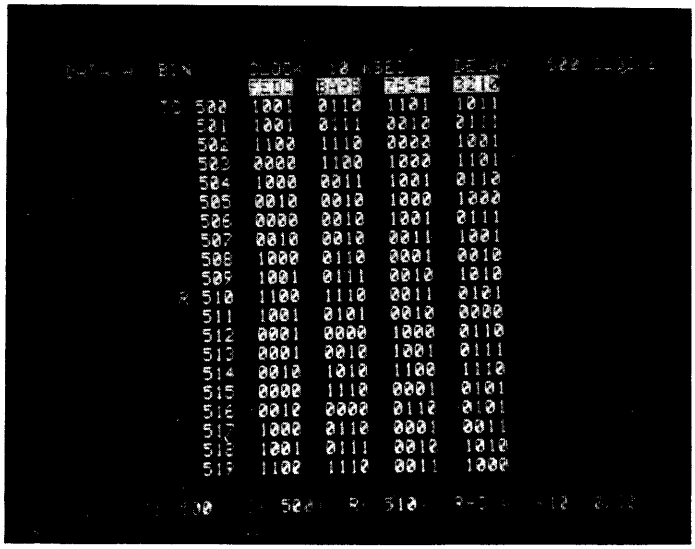


Figure 6.7

Depress [OCTAL] . Verify that the display is as in Figure 6.8.

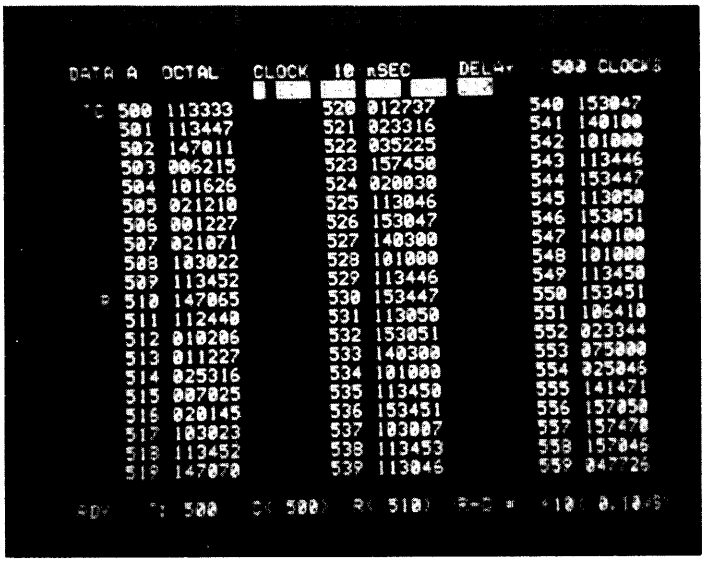


Figure 6.8

Depress [HEX] . Verify that the data on display is as in Figure 6.9.

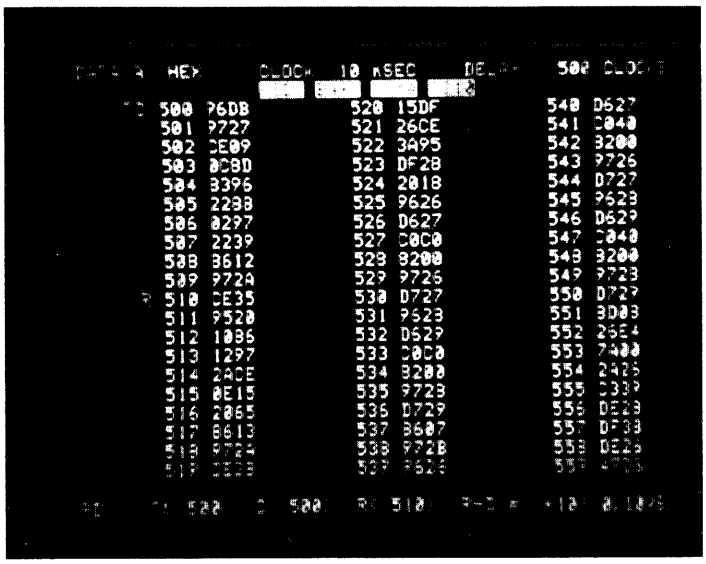


Figure 6.9

Depress [A] . No change of data.

Depress [A→B] . [M→A] . Verify data is all Logic Low levels.

Depress [B] . Verify that the data on display is as in Figure 6.9.

Depress [A/B] . Verify that the data alternates between all Logic Low levels and Figure 6.9.

Power down K100, then power up. Allow a few minutes for warm up. (This allows A to be inputted with data.)

Depress [DATA] [SPCL] . Verify that the display is as in Figure 6.10.

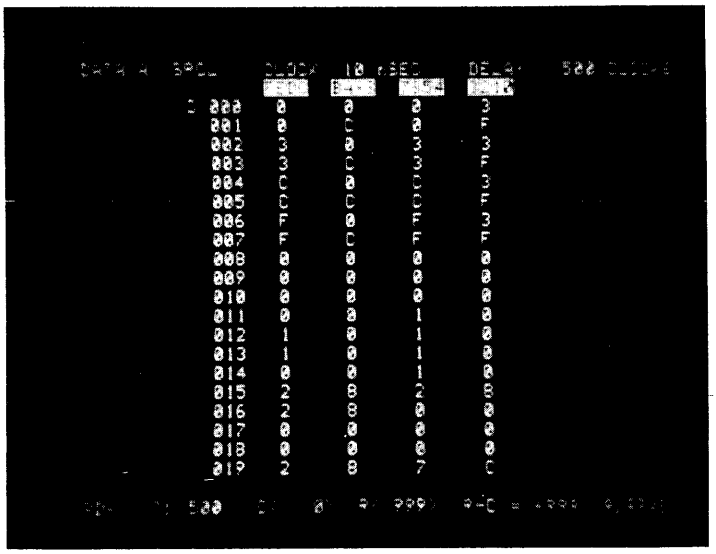


Figure 6.10

Depress [SEARCH] . Verify that the display is as in Figure 6.11.

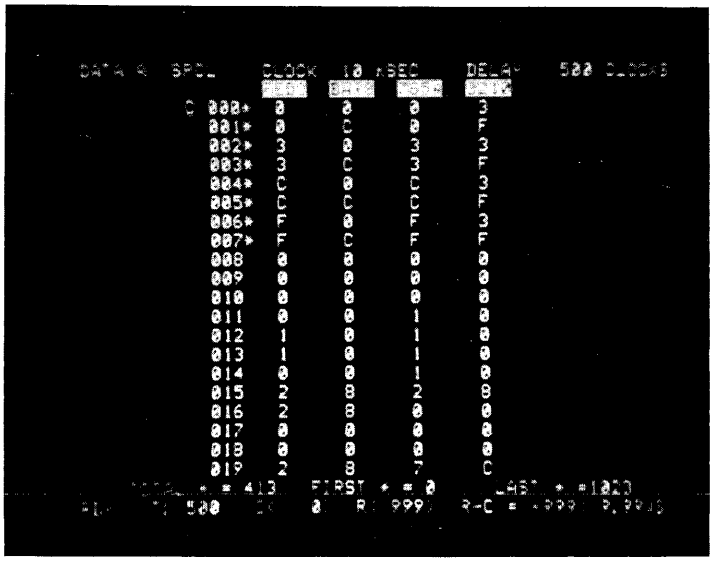


Figure 6.11

Depress [→] CURSOR down. Display should update (addresses change). Single step [→] CURSOR; verify single increments of Address. Return cursor to Address OOOO* by depressing [←] cursor.

Depress [SPECIFY] [SEQ] [SPACE] 8 times. [ENTR] [HEX]. Verify that the display is as in Figure 6.12.

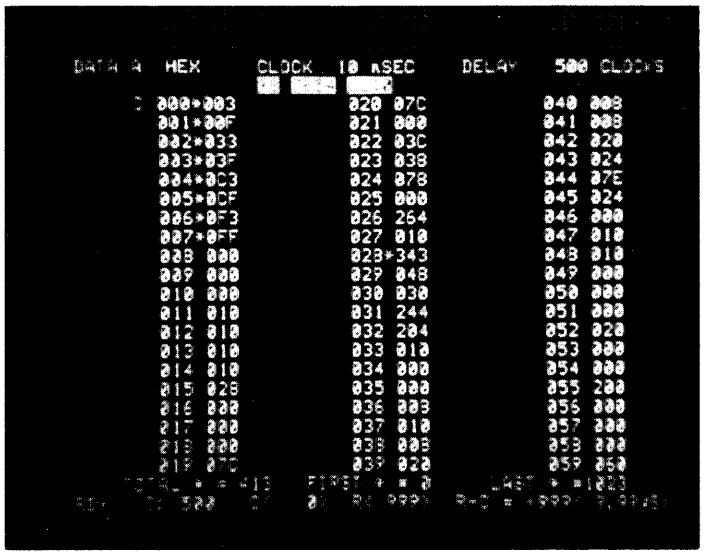


Figure 6.12

Depress [SPECIFY] [SEQ] [SPACE] 8 times. [7] [SPACE] [6] [SPACE] [5] [SPACE] [4] [SPACE] [3] [2] [1] [0] [SPACE] 2 times, [ENTR] , Auto Arm. Verify display as in Figure 6.13.

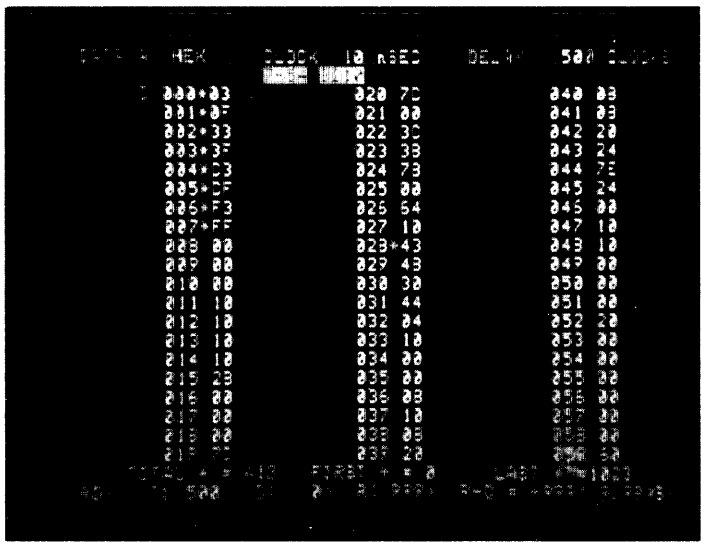


Figure 6.13

Depress [TIMING] . Verify that the display is as in Figure 6.14.

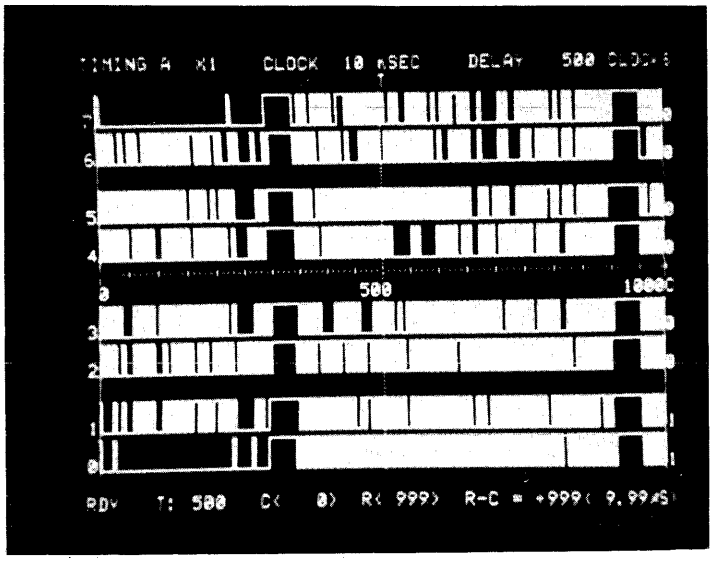


Figure 6.14

Depress [SPECIFY] [SEQ] [SPACE] enough to place (-) under 3. [ENTR] . Verify display as in Figure 6.15.

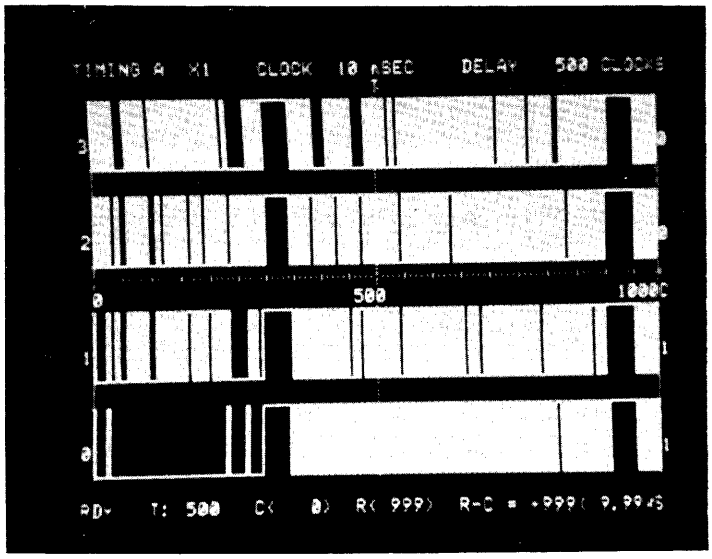


Figure 6.15

6.4.8 Auto Compare Operation

Set external generator for 10 MHz square wave at +3 V level (0 VDC baseline). Input to channel 0.

Return settings as in Figure 6.2. Auto Arm. [TIMING] [X20] [SPECIFY] [←] CURSOR [5] [0] [0] [ENTR] [SPECIFY] [→] REFERENCE [5] [0] [3] [ENTR] . Verify the data and that

the vertical lines move.

Depress [A→B] [AUTO MODE] [A ≠ B] [LIMITS] [ENTR] Auto Arm. Verify that the lower left-hand corner rapidly changes RDY→BSY.

Depress [⟶] REFERENCE . Verify that the display stops and that RDY is shown. Depress [A/B]. Verify that the data alternates between old versus new.

Depress [A], [AUTO MODE] , Auto Arm. The display data and the vertical lines move.

6.4.9 Input Performance

Return settings as in Figure 6.2.

Depress [INPUT] [0-7] [LATCH] [ENTR] [INPUT] [8-F] [LATCH] [ENTR] [TRIGGER] [0] white 4 times [ENTR] . [TIMING] [X5] Auto Arm. Input data as in Figure 6.16.

Verify individual channel performance.

PERIOD = 100 ns
PULSE WIDTH = 6 ns at V_{TH}

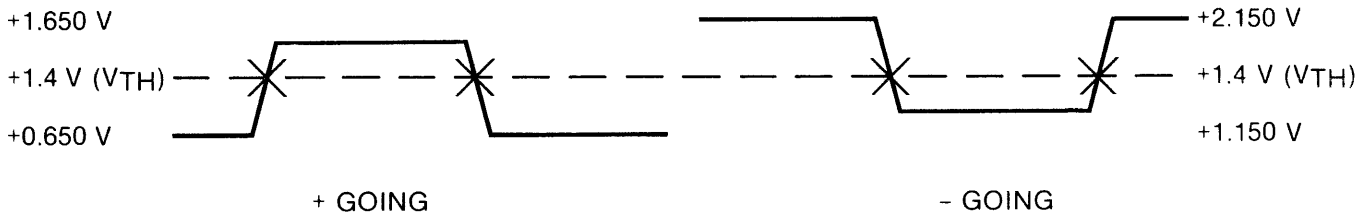


Figure 6.16

Verify no data dropouts. Allow to run a few minutes.

Depress [STATUS] [SPECIFY] [TRIGGER] [F] 4 times [ENTR] [SPECIFY] [THRESHOLD] [ECL] 16 times. [ENTR] [TIMING] [X5].

Auto Arm. Input data as in Figure 6.17. Verify individual channel performance.

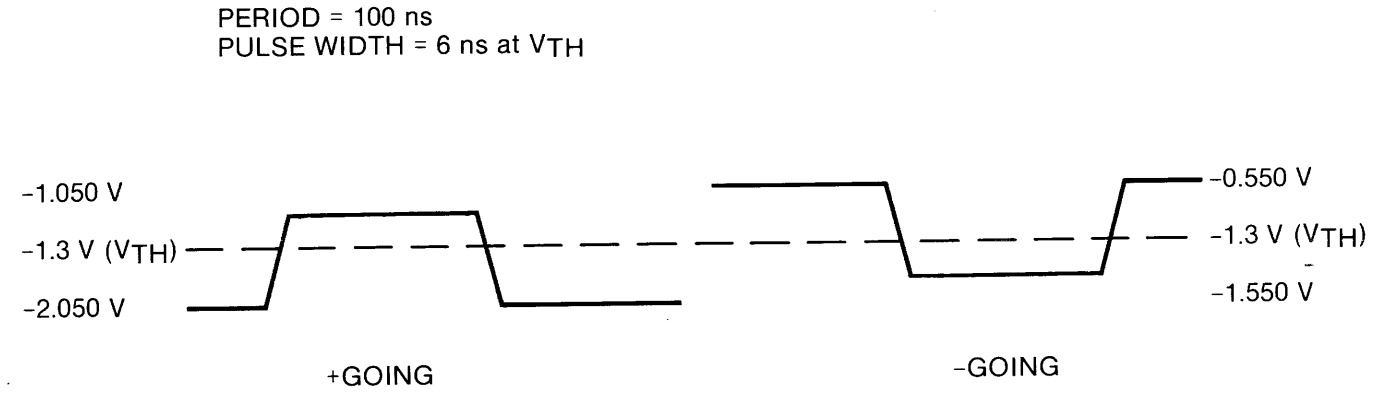


Figure 6.17

Verify no data dropouts. Allow to run a few minutes.

6.4.10 Qualifier Tests

Return settings as in Figure 6.2.
SPECIFY | TRIGGER | "X" 16 times | "0" 2 times | ENTR | .

Set external generator for 10 ns at +2 V level (pulse width at +1.4 V), 0 V baseline, 100 ns period.

Input to Q1, Auto Arm. Verify that unit runs. Move to Q2. Verify results.

Set external generator for 10 ns at -0.8 V level (pulse width at -1.3 V), -2 V baseline, 100 ns period.

Depress | TRIGGER | "X" | 16 times | "1" | 2 times | ENTR | . | THRESHOLD | | TTL | 16 times | ECL | 2 times | ENTR |.

Input to Q1, Auto Arm. Verify that unit runs. Move to Q2. Verify results.

Return unit settings as in Figure 6.2.

Set external generator #1 for 100 kHz square wave at TTL levels. Set external generator #2 for 50 MHz square wave at TTL levels.

Input generator #1 to channel 0, and generator #2 to CK. Auto Arm. | TIMING |

Verify that data runs. | SPECIFY | | CLOCK | | EXT∫ | | ENTR | . Verify that data runs (no breakup). | SPECIFY | | CLOCK | | EXT⤵ | | ENTR | , no breakup. Place CQ on a +5 V level source. Depress CLOCK | EXT∫ | | "0" | | ENTR |. Auto Arm. Display stops. Remove +5 V. Source, unit runs.

THIS ENDS THE DIAGNOSTIC PROCEDURE FOR THE MODEL K100-D.

SECTION VII

SCHEMATICS AND ASSEMBLY DRAWINGS

7.1 Introduction

This section contains the schematics and assembly drawings for the Model K100-D. Parts lists are also included for user convenience.

7.2 List of Drawings

7.3 Parts Lists

The materials in the following lists are subject to change without Gould Inc.'s prior notification. For list verification, contact the Customer Service Department at the factory: Phone (408) 988-6800, TWX 910-338-0509.

7.3.1 List of Parts Lists

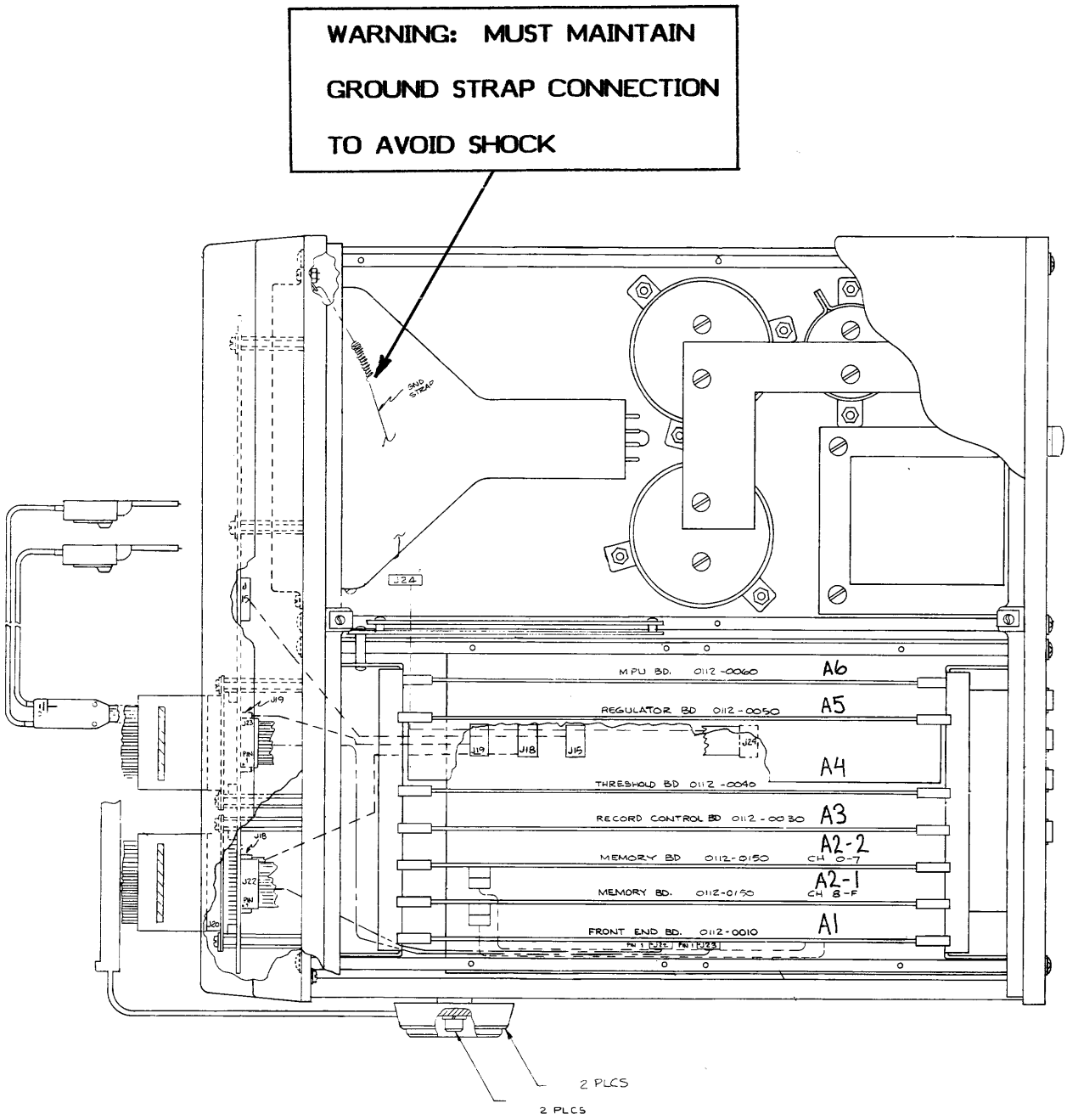


Figure 7.1 Top Assembly, 0112-0003

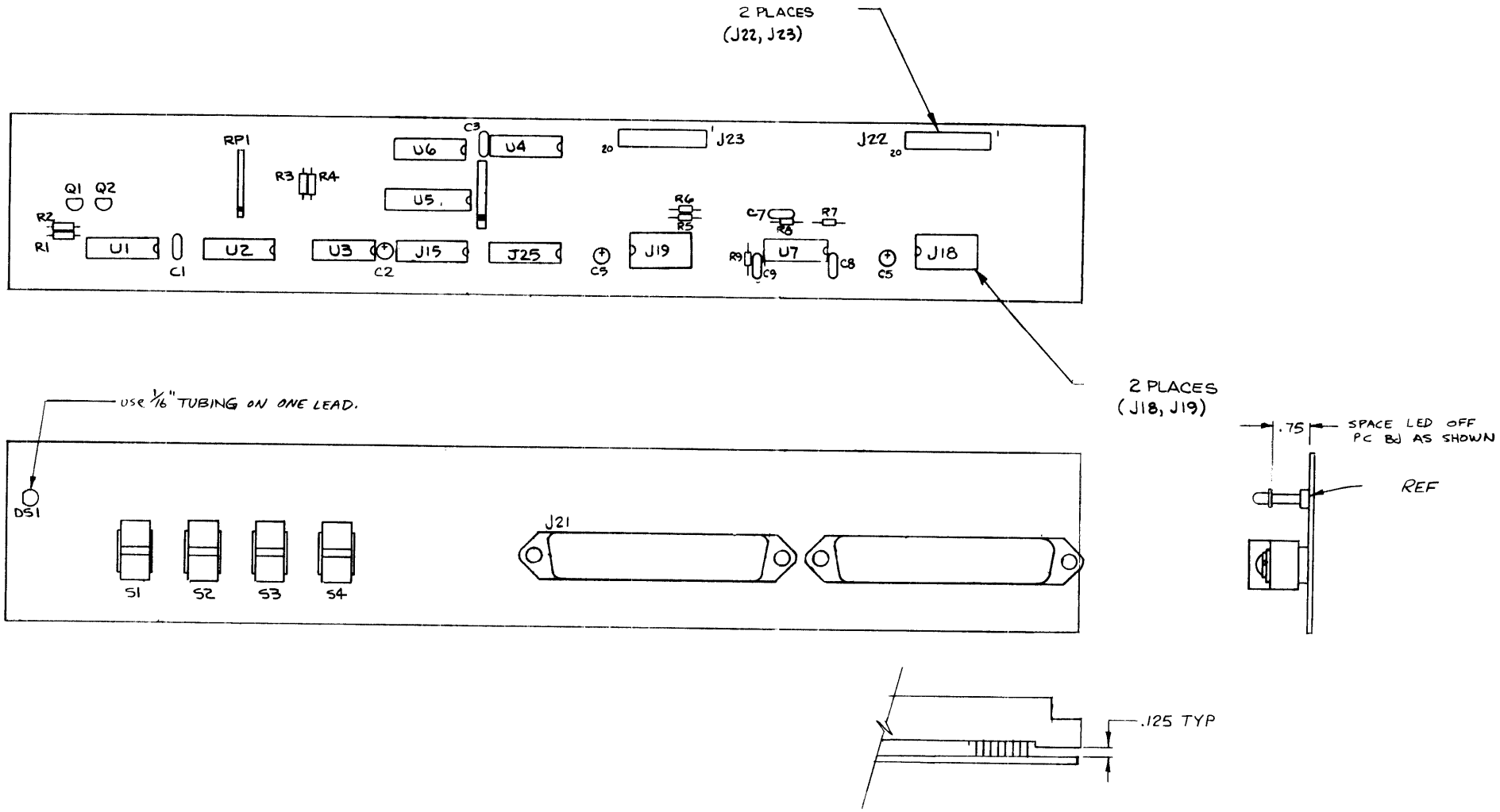


Figure 7.2 Front Panel PWB Assembly, 0112-0115

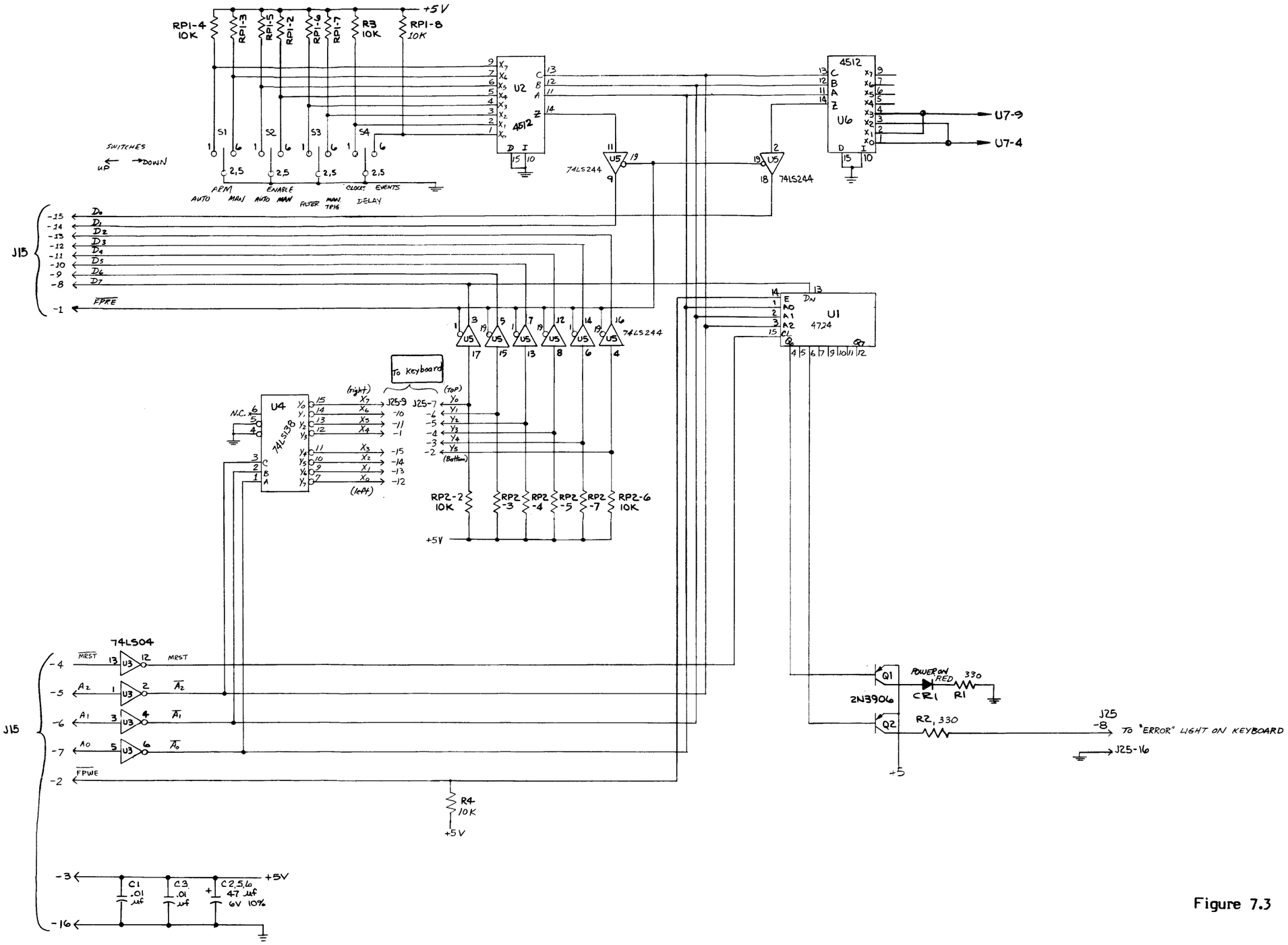


Figure 7.3 Front Panel Schematic, 0112-0116

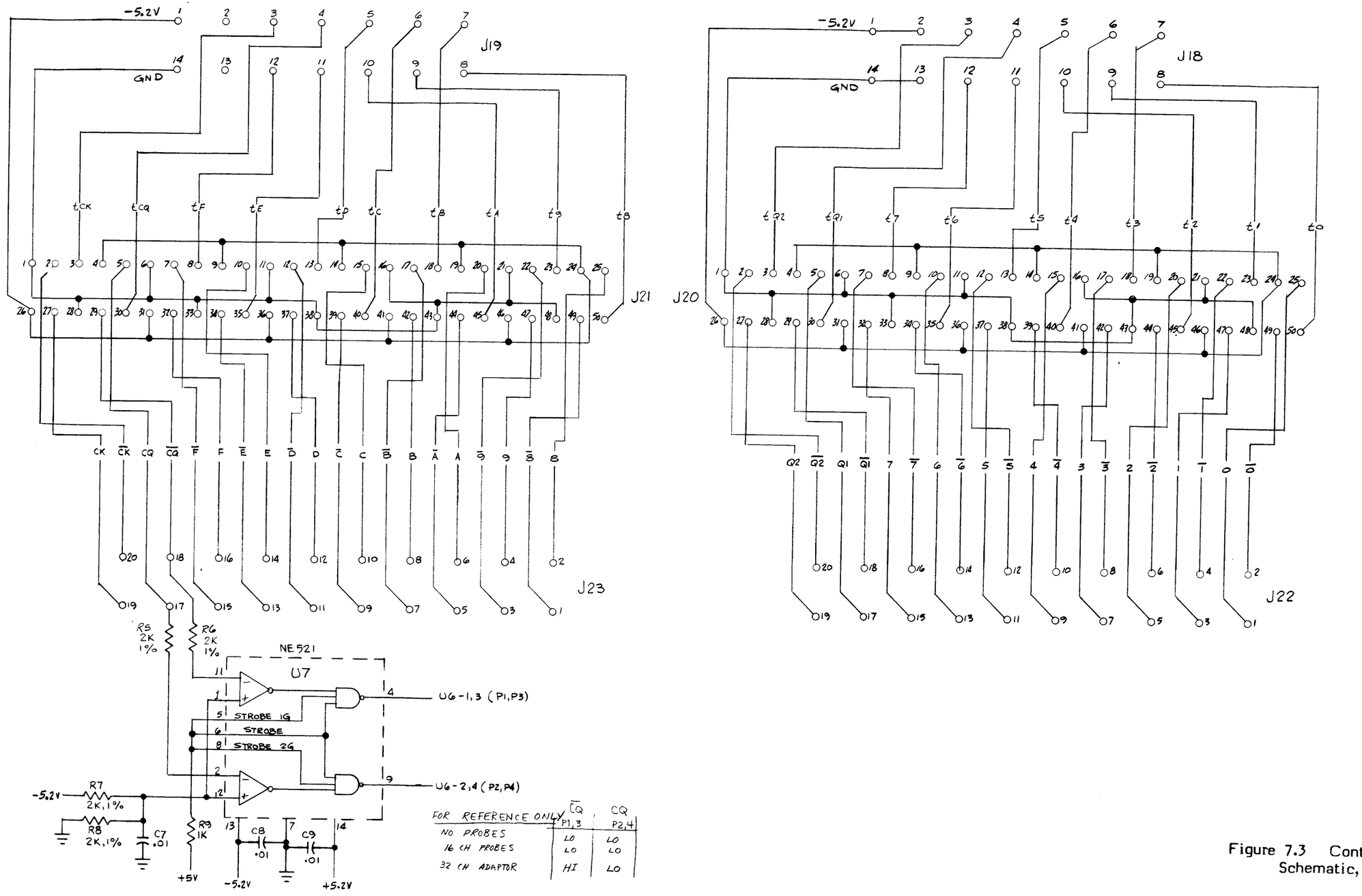


Figure 7.3 Continued. Front Panel Schematic, 0112-0116

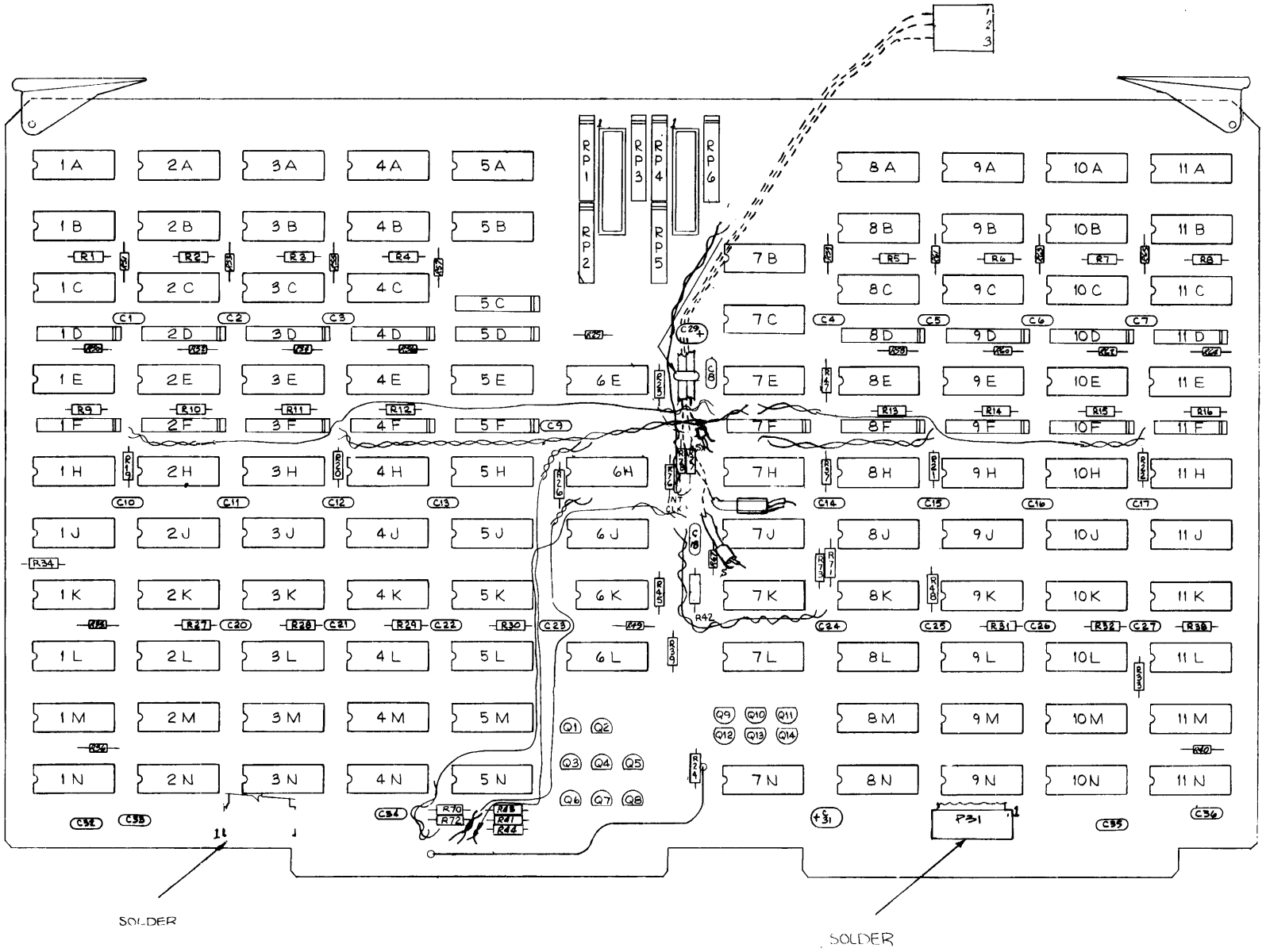


Figure 7.4 Front End PWB Assembly, 0112-0010

DATA LATCH

SOURCE	DESTINATION
J22-1	1A-13
-2	1A-12
-3	1A-10
-4	1A-9
-5	2A-13
-6	2A-12
-7	2A-10
-8	2A-9
-9	3A-13
-10	3A-12
-11	3A-10
-12	3A-9
-13	4A-13
-14	4A-12
-15	4A-10
J22-16	4A-9
J23-1	11A-9
-2	11A-10
-3	11A-12
-4	11A-13
-5	10A-9
-6	10A-10
-7	10A-12
-8	10A-13
-9	9A-9
-10	9A-10
-11	9A-12
-12	9A-13
-13	8A-9
-14	8A-10
-15	8A-12
J23-16	8A-13

RP3 51Ω 10216 — d,1,3,5,7, B,A,C,E — IN1 — IN1 — RP1 51Ω — 1A — 1D-2 330Ω — R1-R8 — -5.2V — CH 1 SAMPLE MODE

RP3 51Ω 10216 — d,0,2,4,6, 9,B,D,F — IN0 — IN0 — RP1 51Ω — 1A — 1D-3 330Ω — 1D-4 330Ω — -5.2V — CH 0 SAMPLE MODE

1D-5 — 330Ω — -5.2V — 1B 10106 — 1E 10130 — 1H 10231 — 1F-6 330 — -5.2

1F-5 330Ω -5.2 — 1F-2 330 — -5.2V — 1C 10106 — 1E 10130 — 1H 10231 — R9 330 — -5.2V

1F-7 — 1F-4 — 1F-8 — 1F-3 — -5.2V — 330Ω

ASYN. TRIGGER — 1J 10121 — R23 82Ω — -5.2V

TRIGGER — 1K 10121

TRIGGER ENABLE — 1M 10121 — -5.2V — SELECT INPUT DATA — SELECT CPU DATA

CH 1,3,5,7,8 A,C,E — CH 0,2,4,6,9 B,D,F — 1N 10117 — 30Ω DATA N — DATA N — d, 1,3,5,7, 8,A,C,E — DATA N — DATA N — d, 0,2,4,6, 9,B,D,F

CHANNEL DATA

SIGNAL	DESTINATION	SOURCE
DATA 0	P30-16	1N-15
DATA 0̄	-1	1N-14
DATA 1	-15	1N-2
DATA 1̄	-2	1N-3
DATA 2	-14	2N-15
2̄	-3	2N-14
3	-13	2N-2
3̄	-4	2N-3
4	-12	3N-15
4̄	-5	3N-14
5	-11	3N-2
5̄	-6	3N-3
6	-10	4N-15
6̄	-7	4N-14
7	-9	4N-2
7̄	P30-8	4N-3
8	P31-16	11N-2
8̄	-1	11N-3
9	-15	11N-15
9̄	-2	11N-14
A	-14	10N-2
Ā	-3	10N-3
B	-13	10N-15
B̄	-4	10N-14
C	-12	9N-2
C̄	-5	9N-3
D	-11	9N-15
D̄	-6	9N-14
E	-10	8N-2
Ē	-7	8N-3
F	-9	8N-15
DATA F̄	-8	8N-14

QUALIFIER

SH2 — 1 — R19 82Ω — CH 0,1,2,3 — 3 — R21 82Ω — CH C,D,E,F — 4 — R22 82Ω — CH 8,9,A,B — 2 — R20 82Ω — CH 4,5,6,7,Q1,Q2

SYNC — 10117 — PI-15 — 6E — PI-S — -5.2V — R25 2K

R34 51Ω

RP2-2 51Ω — J22-18 Q1 — 10216 — 5A — J22-17 Q1 — RP2-3 51Ω — 5D-3 330Ω -5.2V

RP2-4 51Ω — J22-20 Q2 — 10216 — 5A — J22-19 Q2 — RP2-5 51Ω — 5D-4 330Ω -5.2V

5E — 10130 — 5H — 10231 — 330Ω 5F-7 TYP — 5F-4 — 5F-8 — 5F-3 — 5.2V

ASYN. TRIGGER — 5J 10121

TRIGGER — 5K 10121

TRIGGER ENABLE — 5M 10121

R36 330 — -5.2V

R42 10K

5D-7 — 5F-2 — 5F-5 — 5F-6 — 330Ω (TYP) — 5.2V

P1-11 P1-M -2V — C29 47/6

SH2 — 8 — R72 240Ω — R70 360Ω — -5.2V — 9 — R73 240 — R71 360Ω — -5.2V

TRIGGER

TRIG. — 6H 10231 — TRIGGER — P1-13 — P1-P — 6 — R67 330Ω — -5.2V

7K — 10010 OR 10016 — TO 1K3, 2K3 — TO 3K3, 4K3 — TO 11K3, 10K3 — TO 9K3, 8K3

R35 330Ω — -5.2V — R44 10K

5N — 10010 OR 10016 TRIG. EN — TO 1M3, 2M3 — TO 3M3, 4M3 — TO 11M3, 10M3 — TO 9M3, 8M3

330Ω (3PLCS) — -5.2V — R76 (SH2)

330Ω (3PLCS) — -5.2V — P1-14 — P1-R — 5

P1-1 — P1-A — P1-2 — P1-B — -5.2V — C30 47/6

P2-1 — P2-A — P2-2 — P2-B — +5V — C31 47/6

P1-27 — P1-28 — P1-AE — P1-AF — P2-27 — P2-28 — P2-AE — P2-AF — GND

CPU DATA — CH.2 2N-10 — CH.3 2N-6 — CH.4 3N-10 — CH.5 3N-6 — CH.6 4N-10 — CH.7 4N-6 — 6L 4724 — 5B 4724

CH.8 11N-6 — CH.9 11N-10 — CH.A 10N-6 — CH.B 10N-10 — CH.C 9N-6 — CH.D 9N-10 — CH.E 8N-6 — CH.F 8N-10 — 7L 4724 — 7B 4724

5L 4724 — 6J 4724

CH.0 — CH.1 — CH.2 — CH.3 — CH.4 — CH.5 — CH.6 — CH.7 — CH.8 — CH.9 — CH.A — CH.B — CH.C — CH.D — CH.E — CH.F

SELECT SAMPLE MODE — CH.0 to 1C-6,10,12 — CH.1 to 1B-6,10,12 — CH.2 to 2C-6,10,12 — CH.3 to 2B-6,10,12 — CH.4 to 3C-6,10,12 — CH.5 to 3B-6,10,12 — CH.6 to 4C-6,10,12 — CH.7 to 4B-6,10,12 — CH.8 to 11B-6,10,12 — CH.9 to 11C-6,10,12 — CH.A to 10B-6,10,12 — CH.B to 10C-6,10,12 — CH.C to 9B-6,10,12 — CH.D to 9C-6,10,12 — CH.E to 8B-6,10,12 — CH.F to 8C-6,10,12

SH2 — select CQ="1" 6E-4 — select TQ=0 6E-6 — select INT CLK TJ-5 — select EXT CLK — select EXT CLK — select INPUT DATA — select CPU DATA

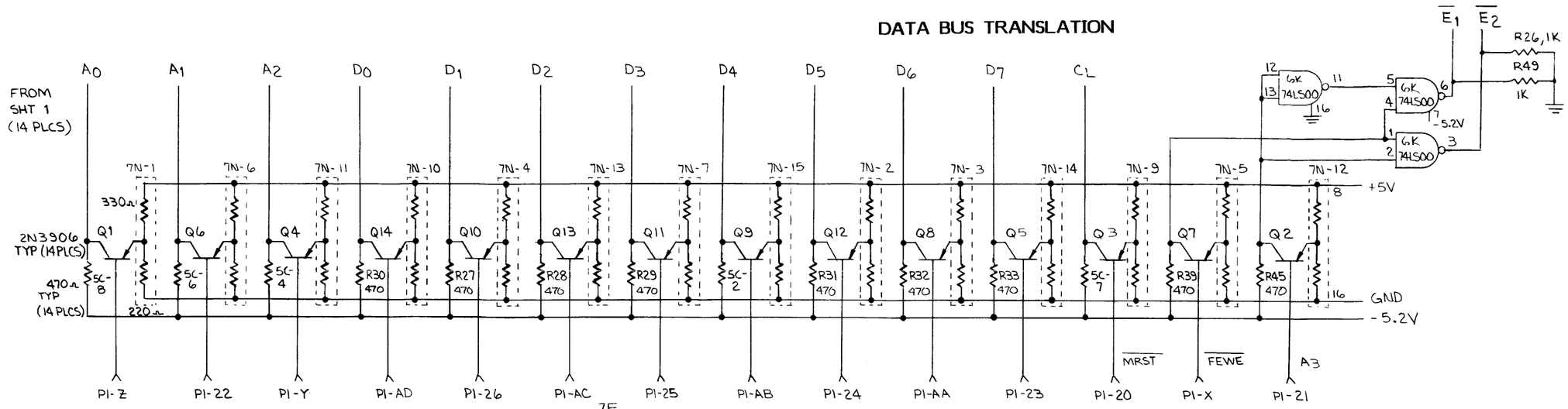
A0 A1 A2 — D0 D1 D2 D3 D4 D5 D6 D7 — E1 E2 — CL

NOTES:

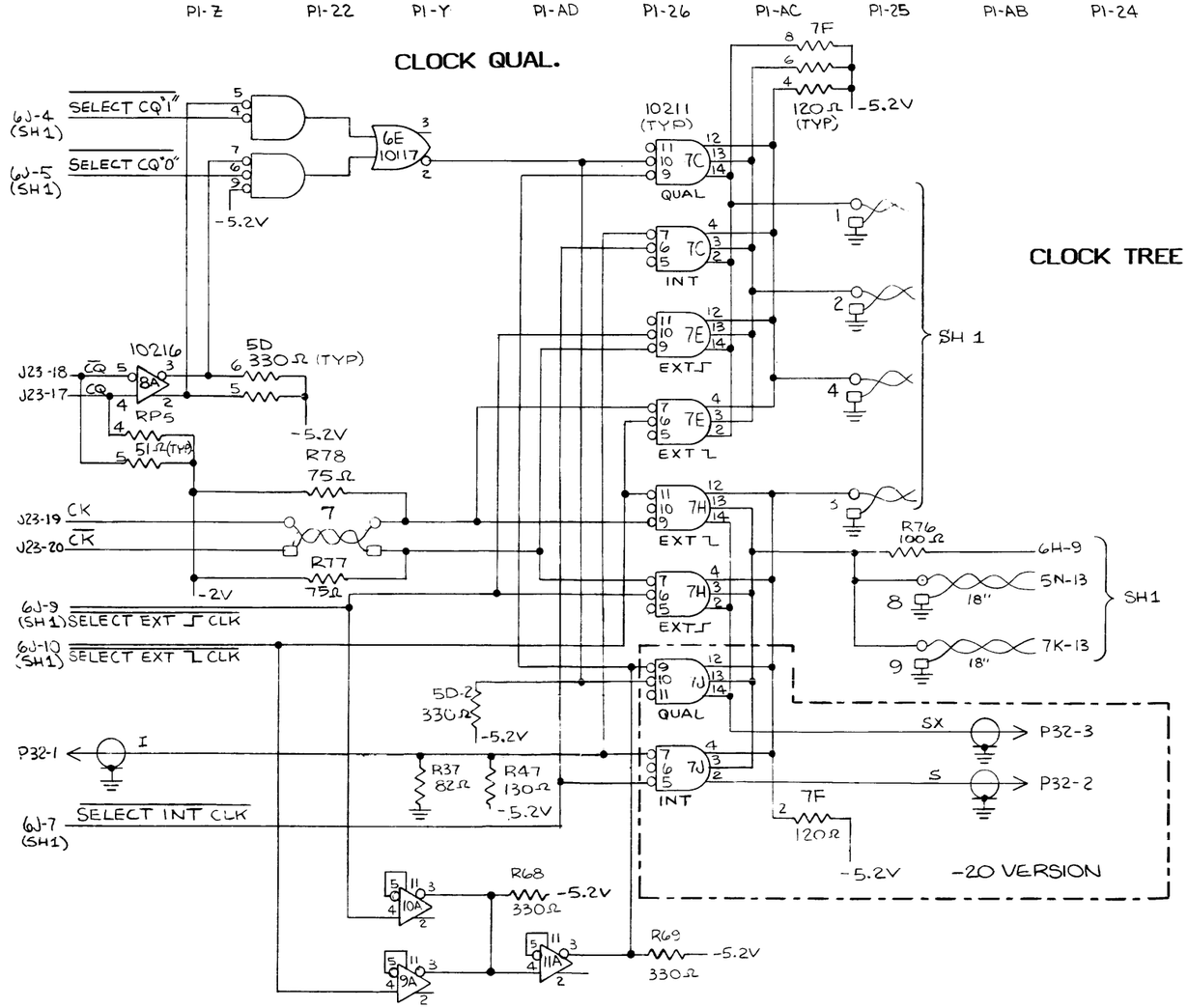
1. ALL CIRCUITRY ABOVE DOTTED LINE IS REPEATED 8 TIMES

Figure 7.5 Front End Schematic, 0112-0011

DATA BUS TRANSLATION



CLOCK QUAL.



CLOCK TREE

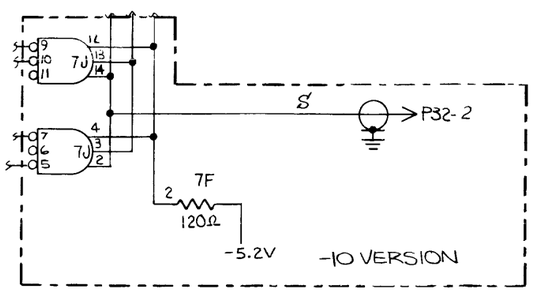
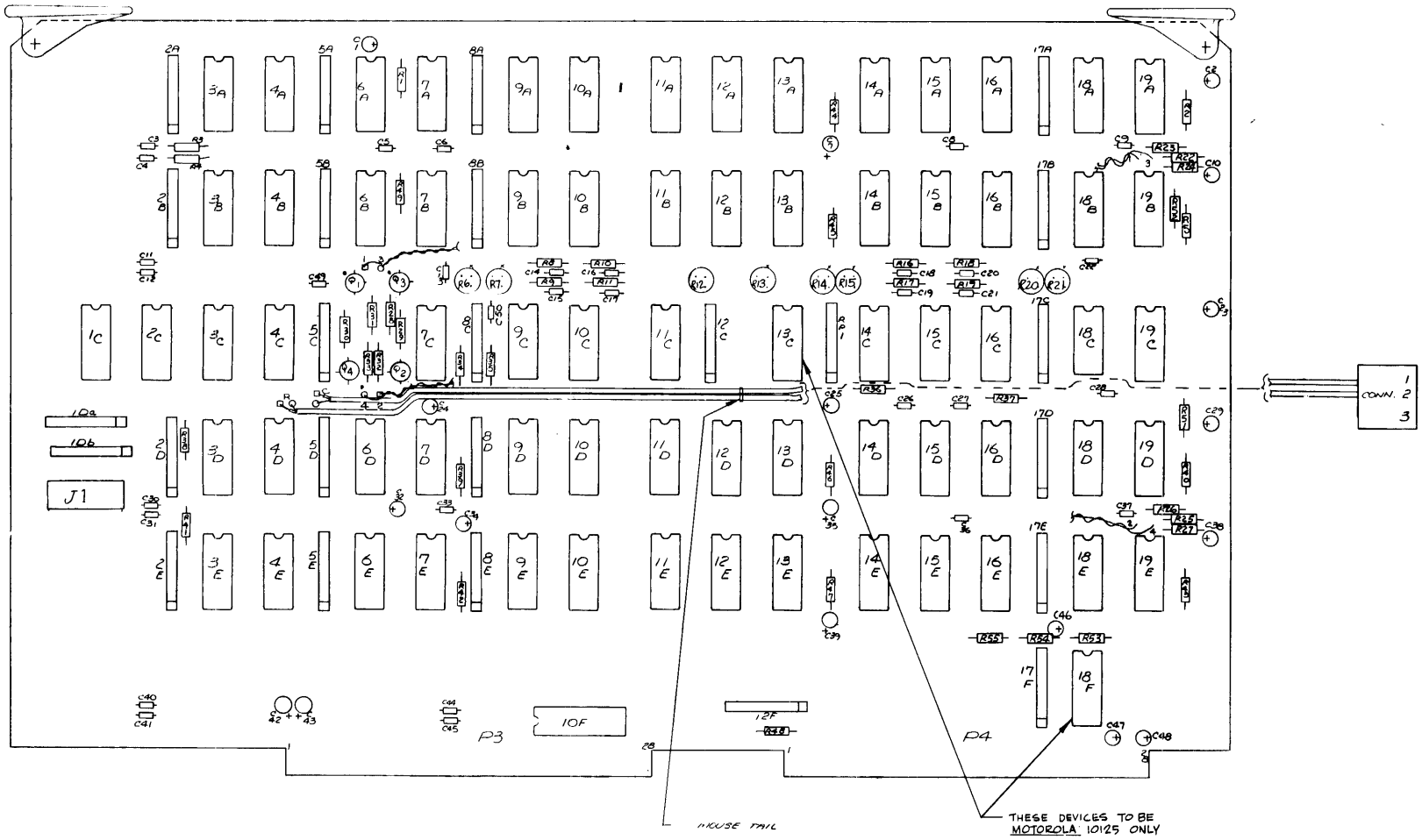


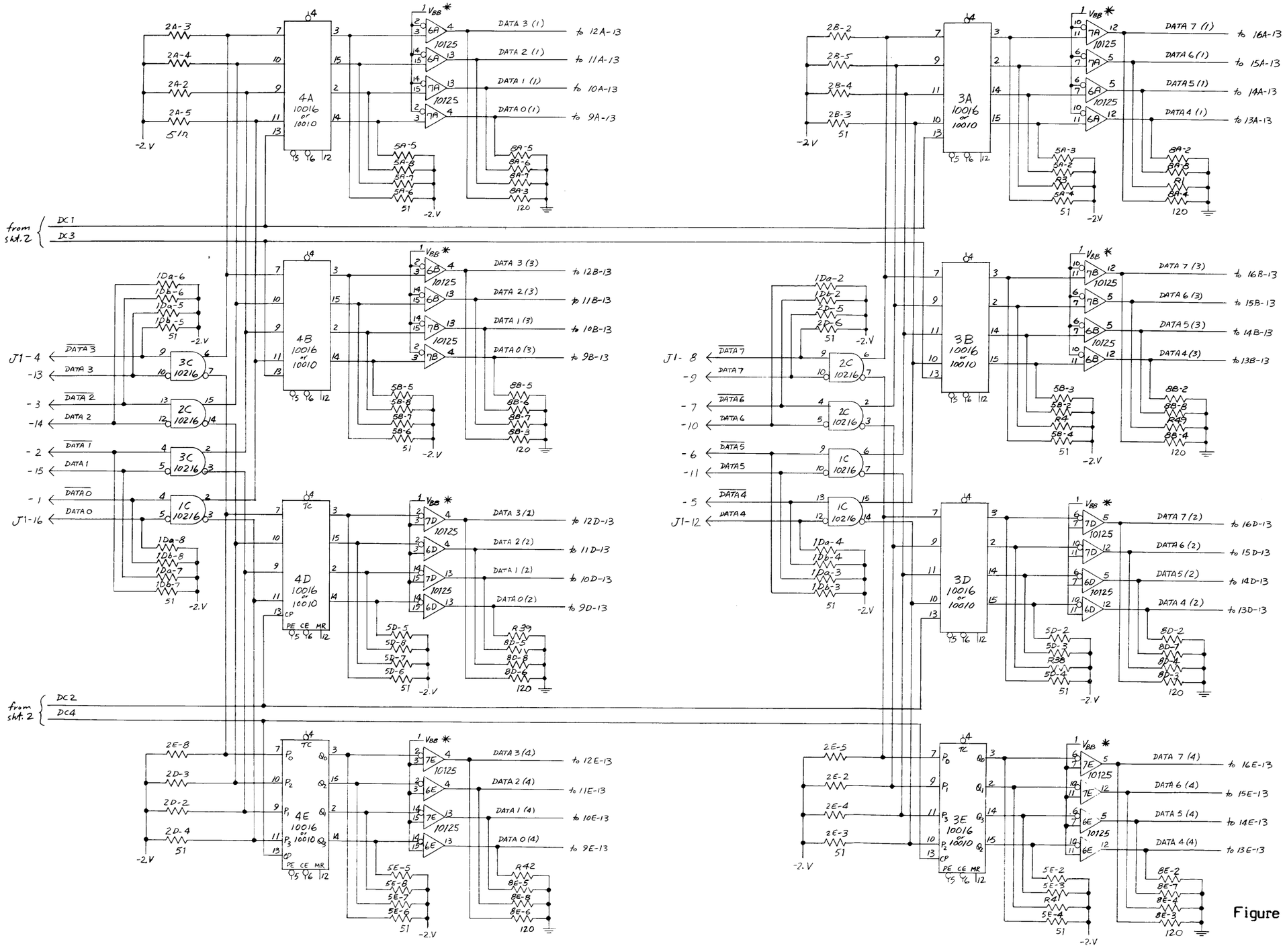
Figure 7.5 Continued. Front End Schematic, 0112-0011



NOTES:

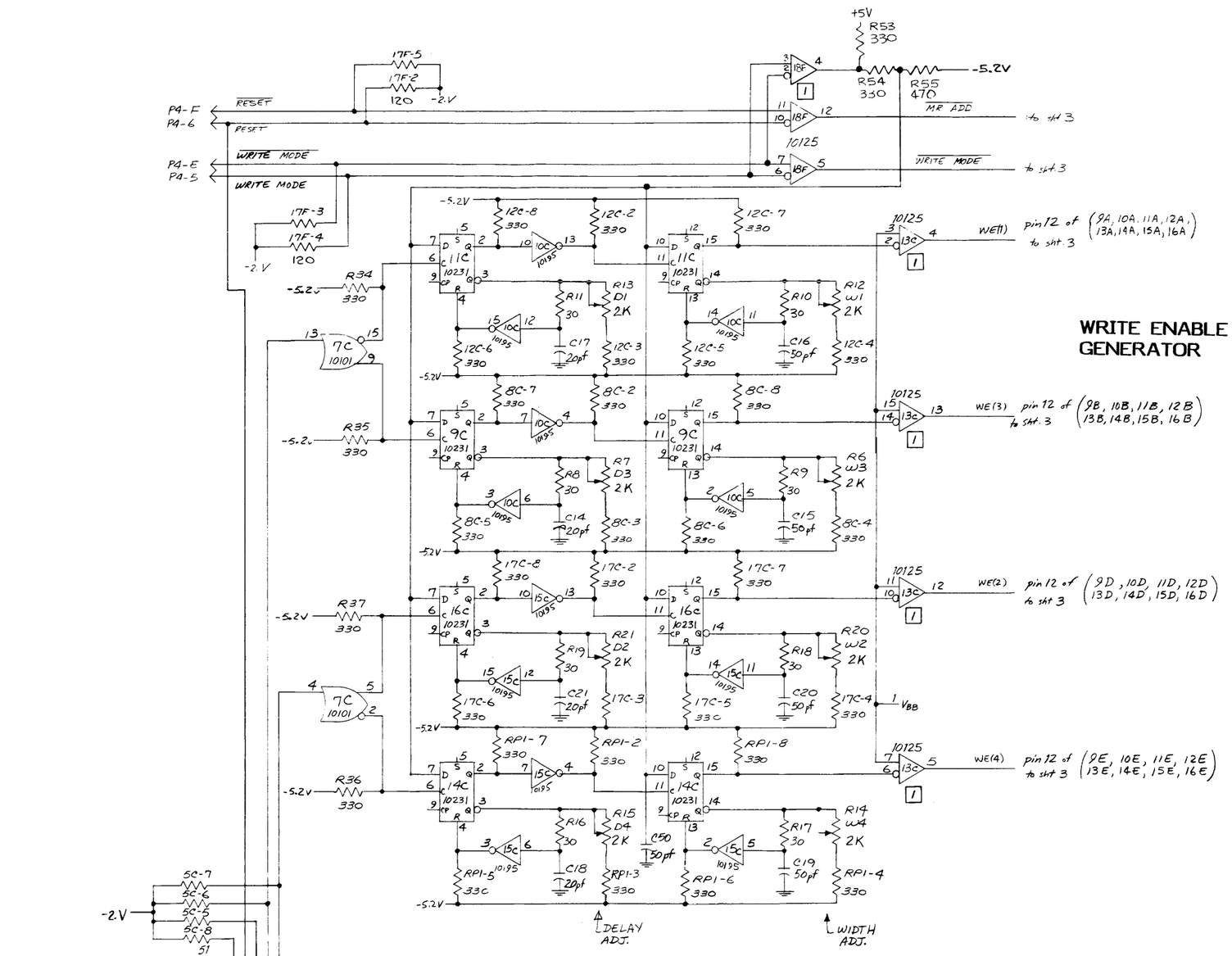
1. TRANSISTORS Q1-Q4 MUST HAVE THE PLATING REMOVED FROM THE MOUNTING HOLES (4 PLACES). THE "DOT" IDENTIFIES THE COLLECTOR (BUMP).
2. THE TWISTED PAIRS MUST CONNECT 1 TO 1, 3 TO 3, 2 TO 2, 4 TO 4
3. THE POTS (ITEM 30) SHOULD MOUNT IN THE 3 HOLES INDICATED, THE FOURTH HOLE (TOWARD TOP OF PWB) IS NOT USED

Figure 7.6 Record Memory Assembly, 0112-0150



* VBB IS CONNECTED TO PIN 1 OF EACH 10125 I.C.

Figure 7.7 Record Memory Schematic, 0112-0151



1 13C & 18F 10125 DEVICE TO BE MOTOROLA ONLY.
2. ALL RESISTANCE VALUES ARE IN OHMS, ¼W, 5%.

Figure 7.7 Continued. Record Memory Schematic, 0112-0151

MEMORY (1K)

ADDRESS CTRS.

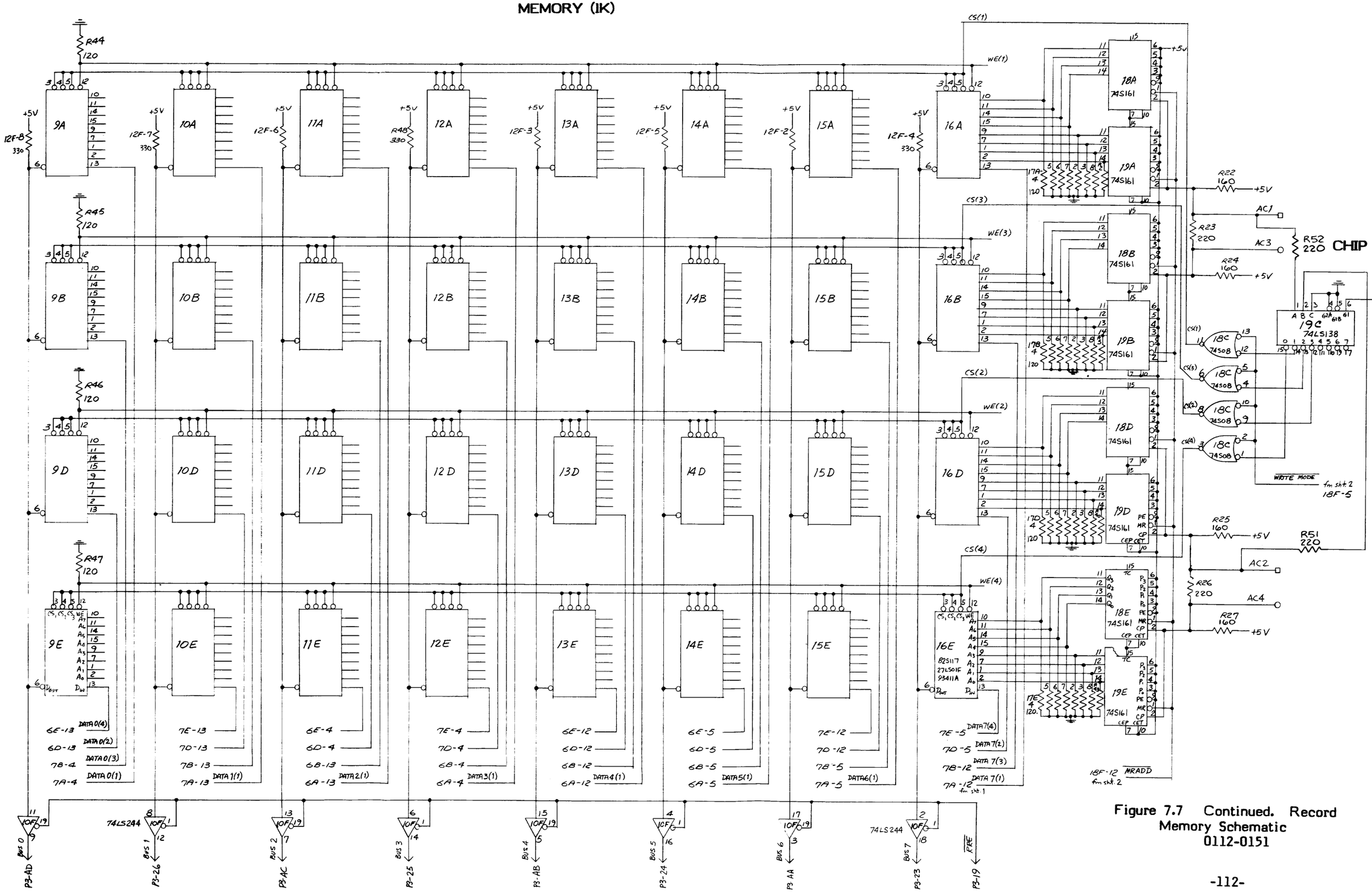


Figure 7.7 Continued. Record Memory Schematic 0112-0151

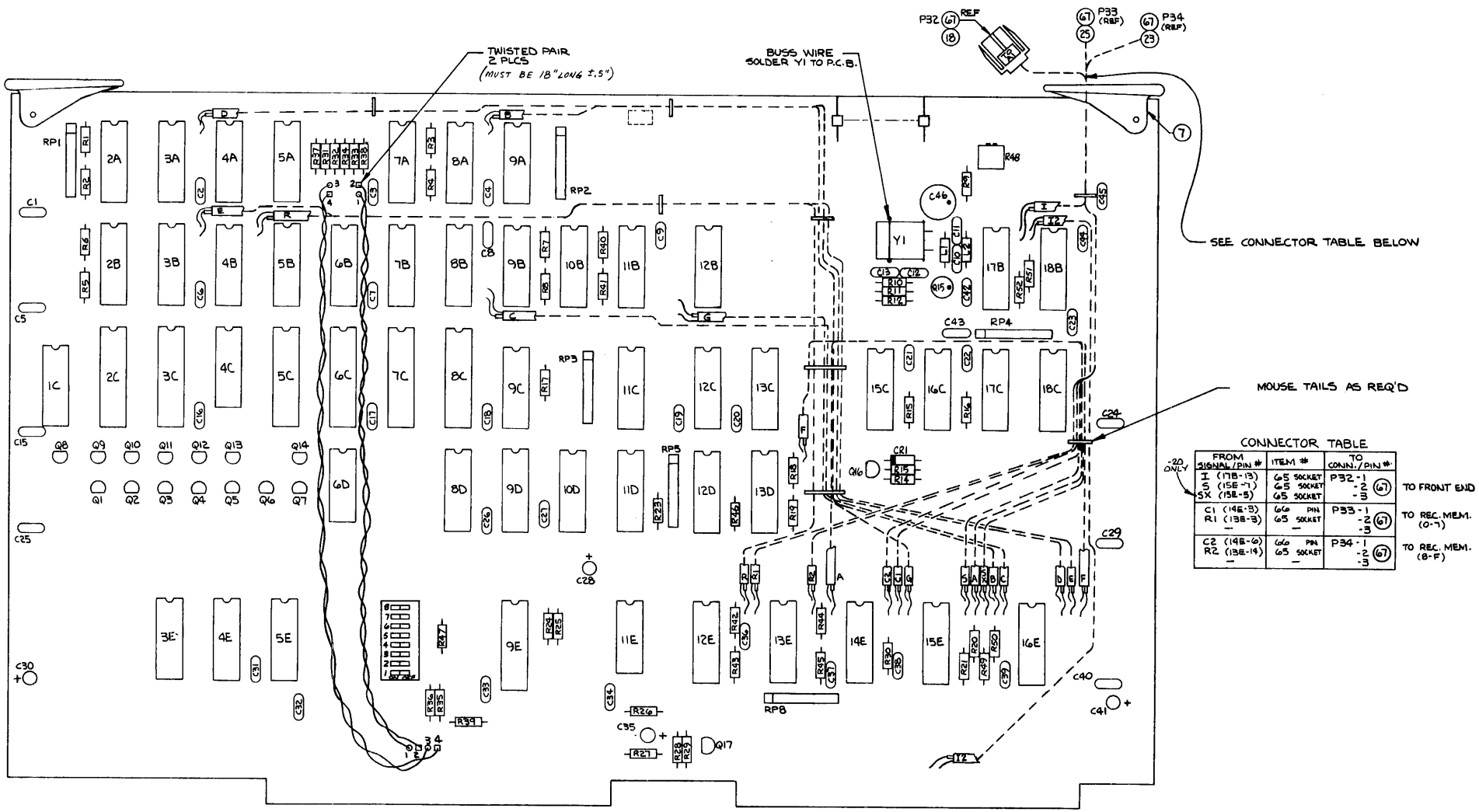
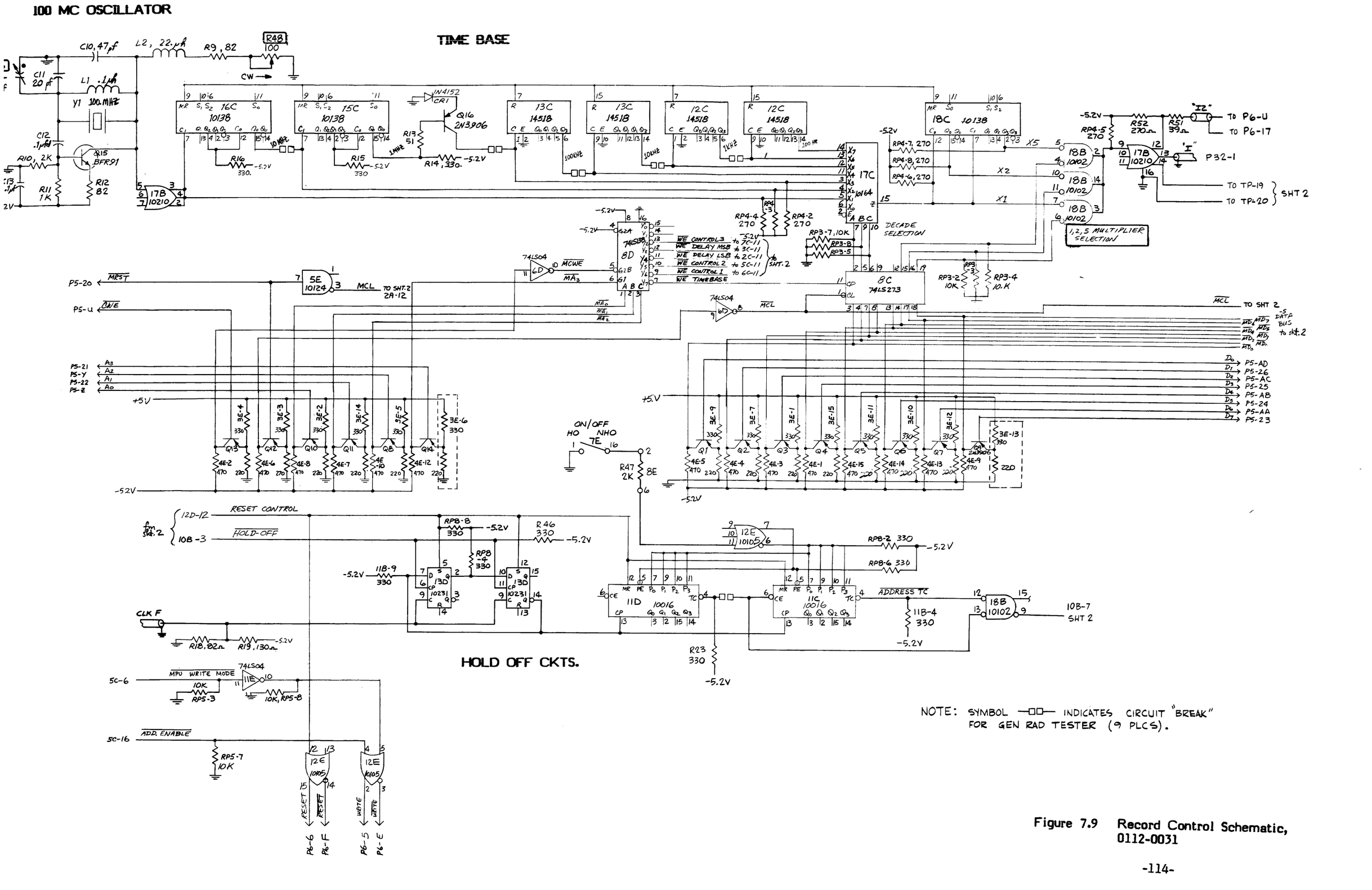


Figure 7.8 Record Control Assembly, 0112-0030



NOTE: SYMBOL —□□— INDICATES CIRCUIT "BREAK" FOR GEN RAD TESTER (9 PLCS).

Figure 7.9 Record Control Schematic, 0112-0031

Figure 7.9 Continued. Record Control Schematic, 0112-0031

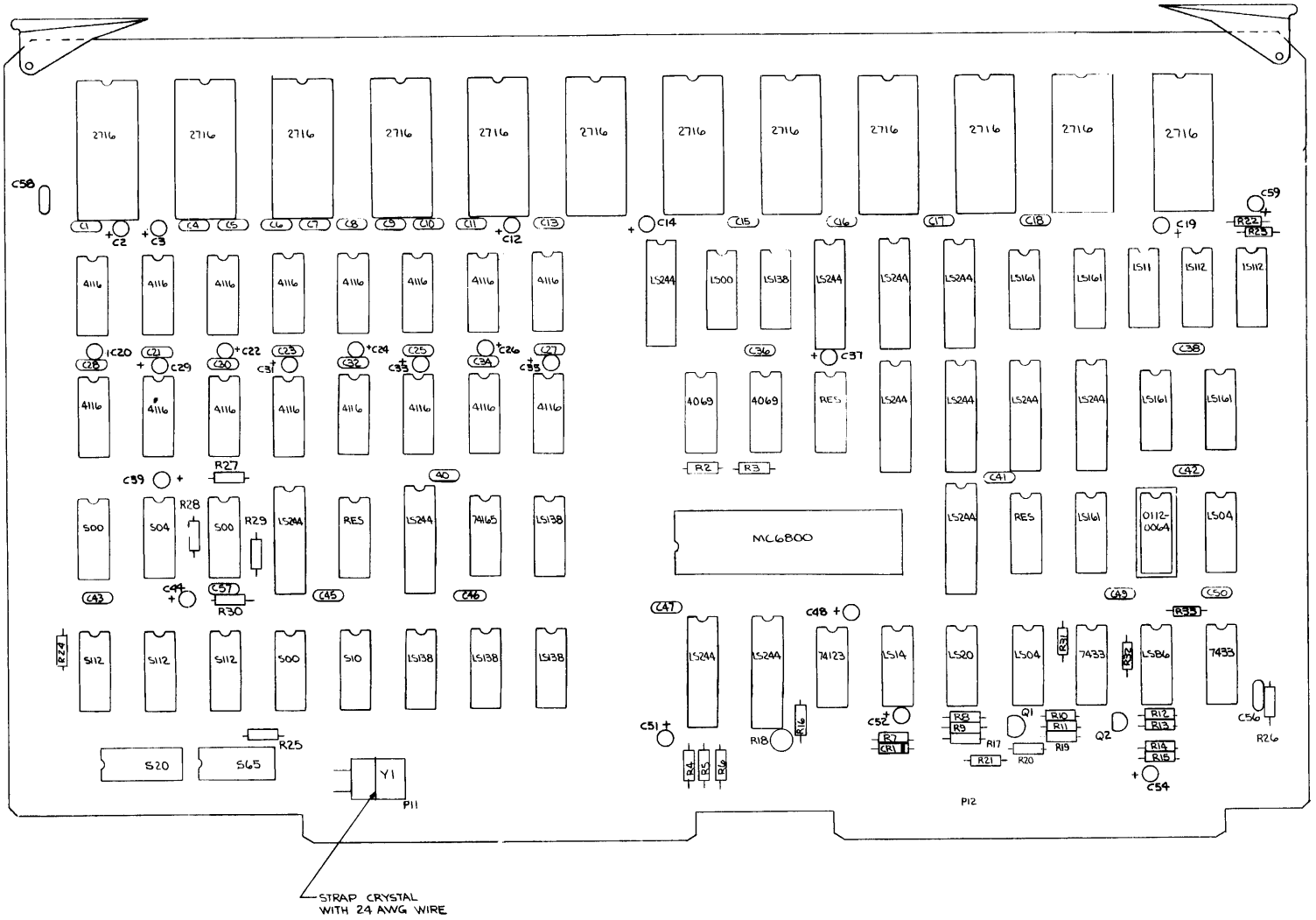


Figure 7.10 MPU Board Assembly,
0112-0060

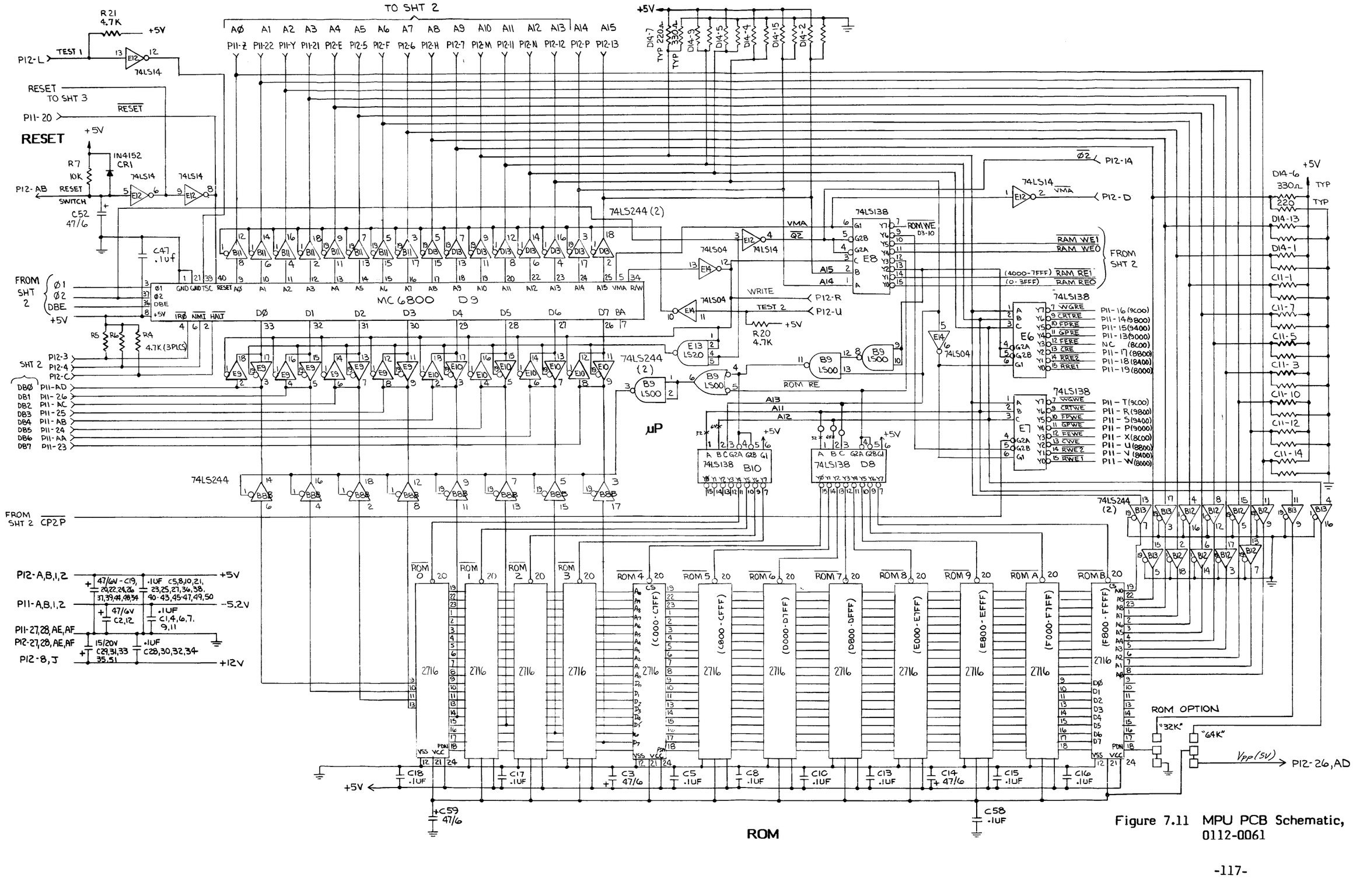


Figure 7.11 MPU PCB Schematic, 0112-0061

FROM SHT 1

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13

MPUCE

MPURE

74LS244 (2)

C11-4 TYP

220Ω

330Ω

C11-6 C11-9 C11-15

C11-13 330Ω 220Ω

C11-11 330Ω 220Ω

C11-2 330Ω 220Ω

P12 A,B,1,2 +5V

P11 A,B,1,2 -5.2V

P12 B,J +12V

P11 27,28 AE, AF GND

P12 27,28 AE, AF

Y1 20 MHZ

R29 410Ω

R30 470Ω

D3 S00

C57 200 pf

R27, 3K -5.2V

R28, 5.1K -5.2V

4116 B1 B2 B3 B4 B5 B6 B7 B8 C1 C2 C3 C4 C5 C6 C7 C8

A0 A1 A2 A3 A4 A5 WE CAS RAS A6 DIN DOUT

FROM CRT CONTROLLER SHT 3

B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13

CRTRE

CRTCE

74LS244 (2)

RAM

CRT CONTROLLER

D7 74165

CRT DATA TO SHT. 3

SHIFT/LOAD

SHIFT CLK

TO SHT 3 (E11-10)

RAM RE1 TO SHT 1

RAM REO TO SHT 1

74LS244 (2)

DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7

TO SHT 1

RES PK D5(8) 330Ω 220Ω D5-9 D5-13 D5-1 D5-11 D5-3 D5-5 D5-7

GND +5V

D5-14 RAM WE1 TO SHT 1

D5-12 RAM WEO TO SHT 1

D5-2 D5-6 DBE TO SHT 1

MPURE CRTRE MPUCE CRTCE

S04 S00 S10 S112

RAS CAS

R24 4.7K

20 MHZ CLK

CRT CLK TO SHT 3.

CP2P TO SHT 1

CP1

F4069 "FAIRCHILD ONLY"

Ø1 TO SHT 1

Ø2 TO SHT 1

R2 470Ω R3 470Ω

E2-7 E2-5 E3-7 E1-9 E3-6 E1-7 E3-5 E2-1 E3-9 E2-6 E3-7 E2-5

F2 S20 F3 74S65 R25 470

TIMING GENERATOR

Figure 7.11 Continued. MPU PCB Schematic, 0112-0061

VIDEO GENERATOR

JUMPER FOR 50HZ CRT OPERATION

R15 330Ω

R14 330Ω

+5V

D15 74LS161 — P3 P2 P1 P0 CEP CET CP MR TC Q0 Q1 Q2 Q3

D16 82S123 — A4 A3 A2 A1 A0 OE O7 O6 O5 O4 O3 O2 O1 O0 — 0112-0064

C17 74LS161 — B13 B12 B11 B10

C16 74LS161 — B9 B8 B7 B6

B15 74LS161 — B5 B4 B3 B2 B1 B0

B14 74LS161

TO SHT 2

D17 74LS04

R26 470

C56 .002 mfd

E17 7433

IRQ — to sht 1. D2-4

from sht 1 E6-10 — FDRE

E16 74LS86

R33 680

R32 680

R31 680

VERT. SYNC

R10 680

Q2 2N3904

R13 510

COMPOSITE VIDEO — P12-Z

P12-22

R11 470

R12 82Ω

E14 LS04

D14-10 220

D14-11 220

330

VERT. SYNC — P12-Y

P12-21

HORIZ. SYNC — P12-X

P12-20

VIDEO HI=WHT LO=BLK

R9 180

R8 270Ω

R17 15Ω

R19 75Ω

Q1 2N3906

P12-W

P12-19

E13 74LS20

CRT DATA FROM SHT 2

RESET FROM SHT 1

CRT CLK (E2-7)

R22 220

R23 330

B17 LS112

B18 LS112

B16 74LS11

COUNT 11

COUNT 5

Horiz. Sync.

R16 4.7K

R18 10K

E11 74123

FROM D7-2 SHIFT CLK

Video Gate

DATA HEX	ADDRESS	DELAY COUNTS-DEC			NON-INTERLACE	50 HZ
10	16	240				
FD	17	3				
FD	18	3				
D8	19	40				
10	20	240				
FD	21	3				
FD	22	3				
D8	23	40				
10	24	240	0	SCAN		
FD	25	3	1	B DELAY		
FD	26	3	2	SYNC		
F1	27	15	3	A DELAY		
10	28	240	4	SCAN		
FD	29	3	5	B DELAY		
FD	30	3	6	SYNC		
F1	31	15	7	A DELAY		

NON-INTERLACE — 60 HZ

Figure 7.11 Continued. MPU PCB Schematic, 0112-0061

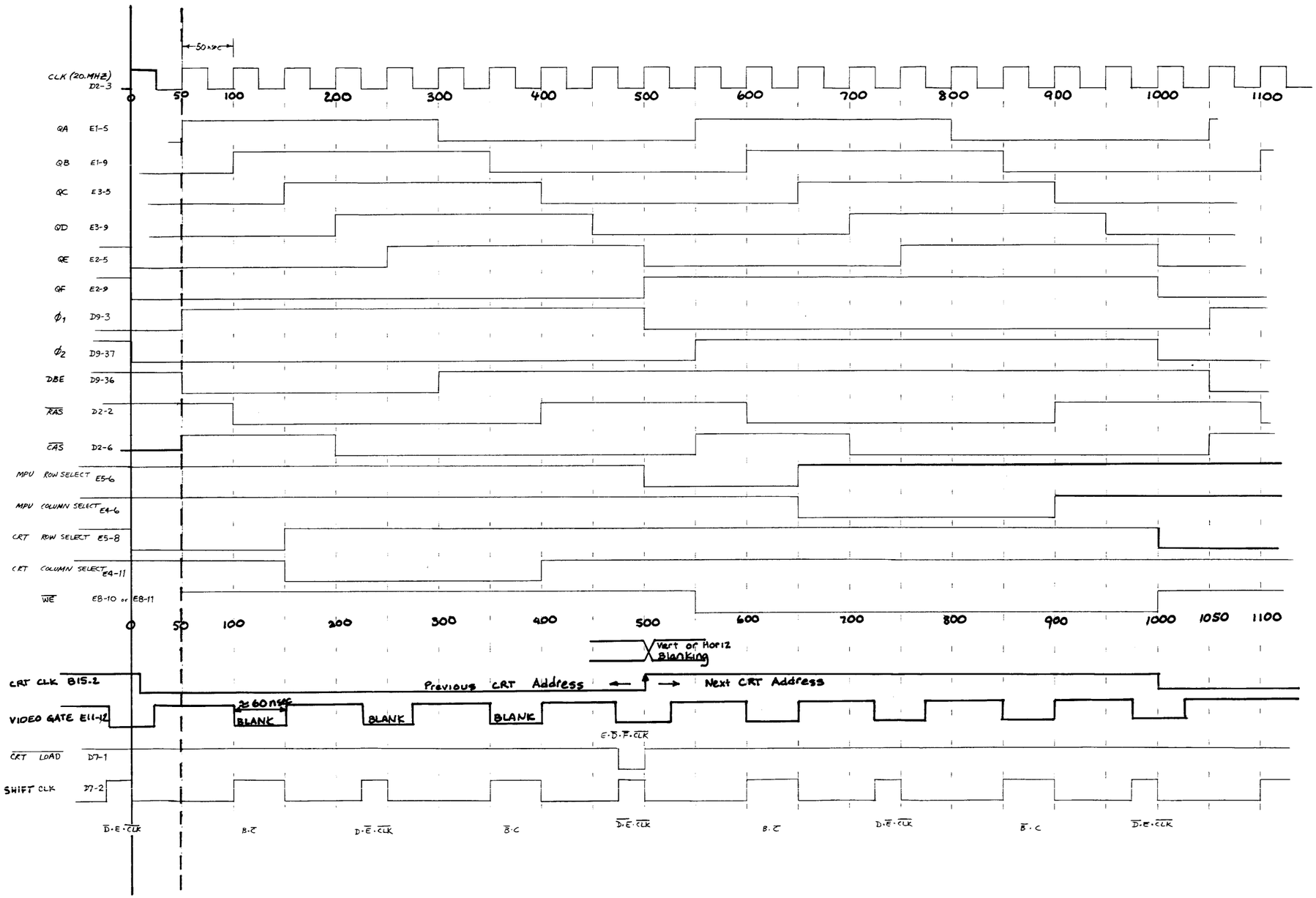
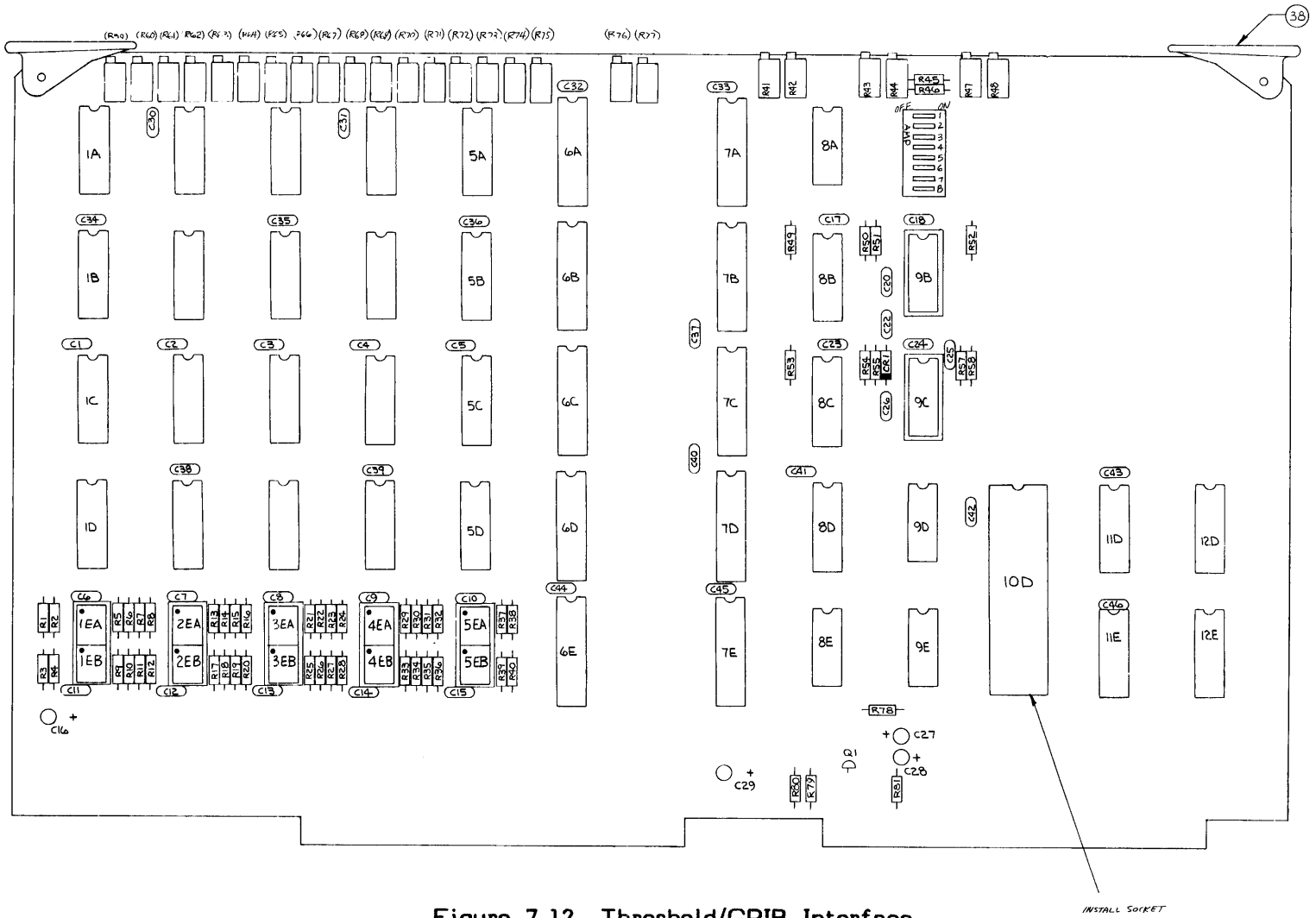


Figure 7.11 Continued. MPU PCB Schematic, 0112-0061



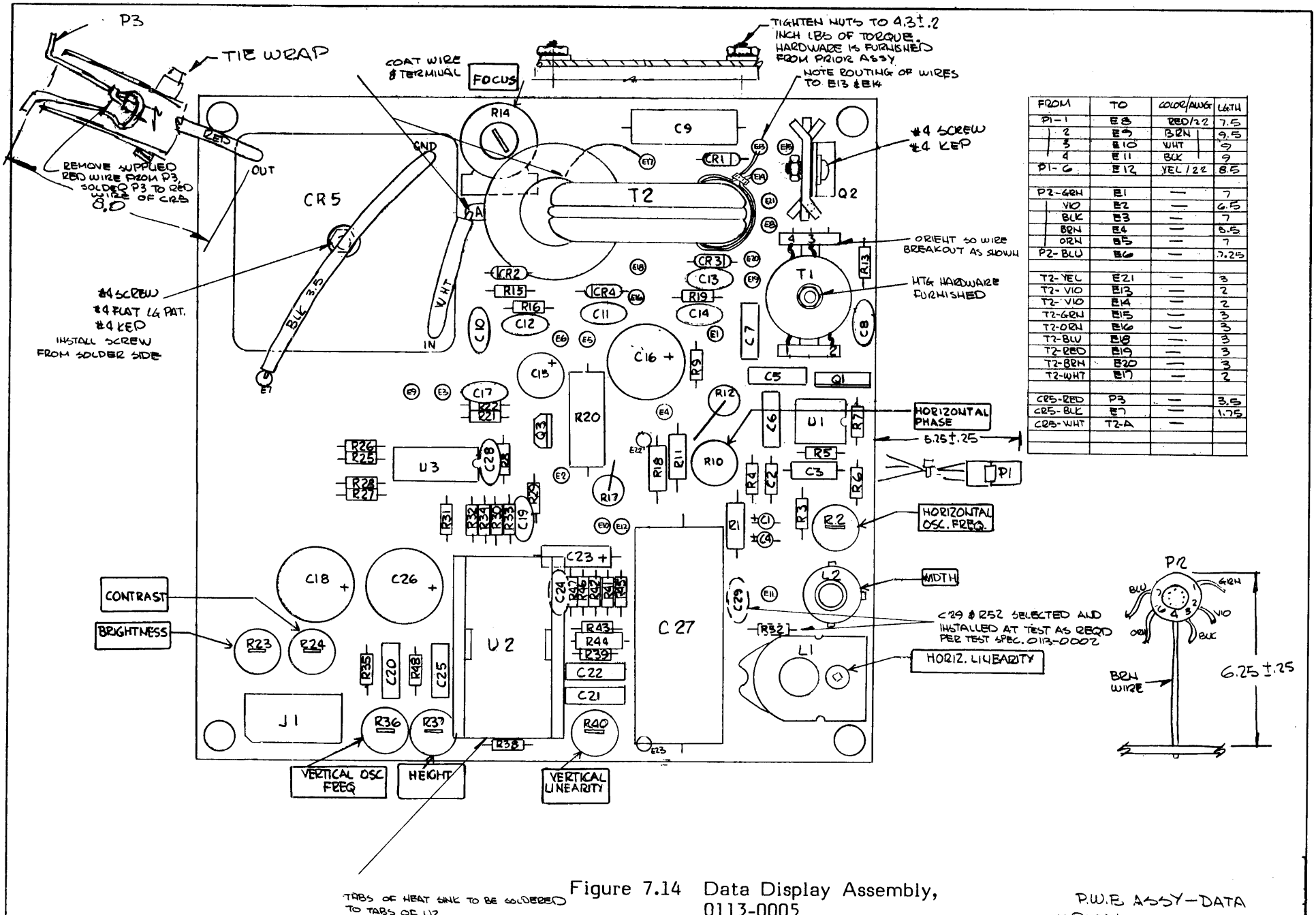
NOTES: UNLESS OTHERWISE SPECIFIED,
1. -20 ASSY IS SHOWN. FOR -10 ASSY, SEE L/M 0112-0040.

Figure 7.12 Threshold/GPIB Interface Assembly, 0112-0040

TO PROBES

NOTE: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTORS ARE IN OHMS. 1/8W ±1%.
2. * COMPONENTS USED ON -20 ASSY ONLY.

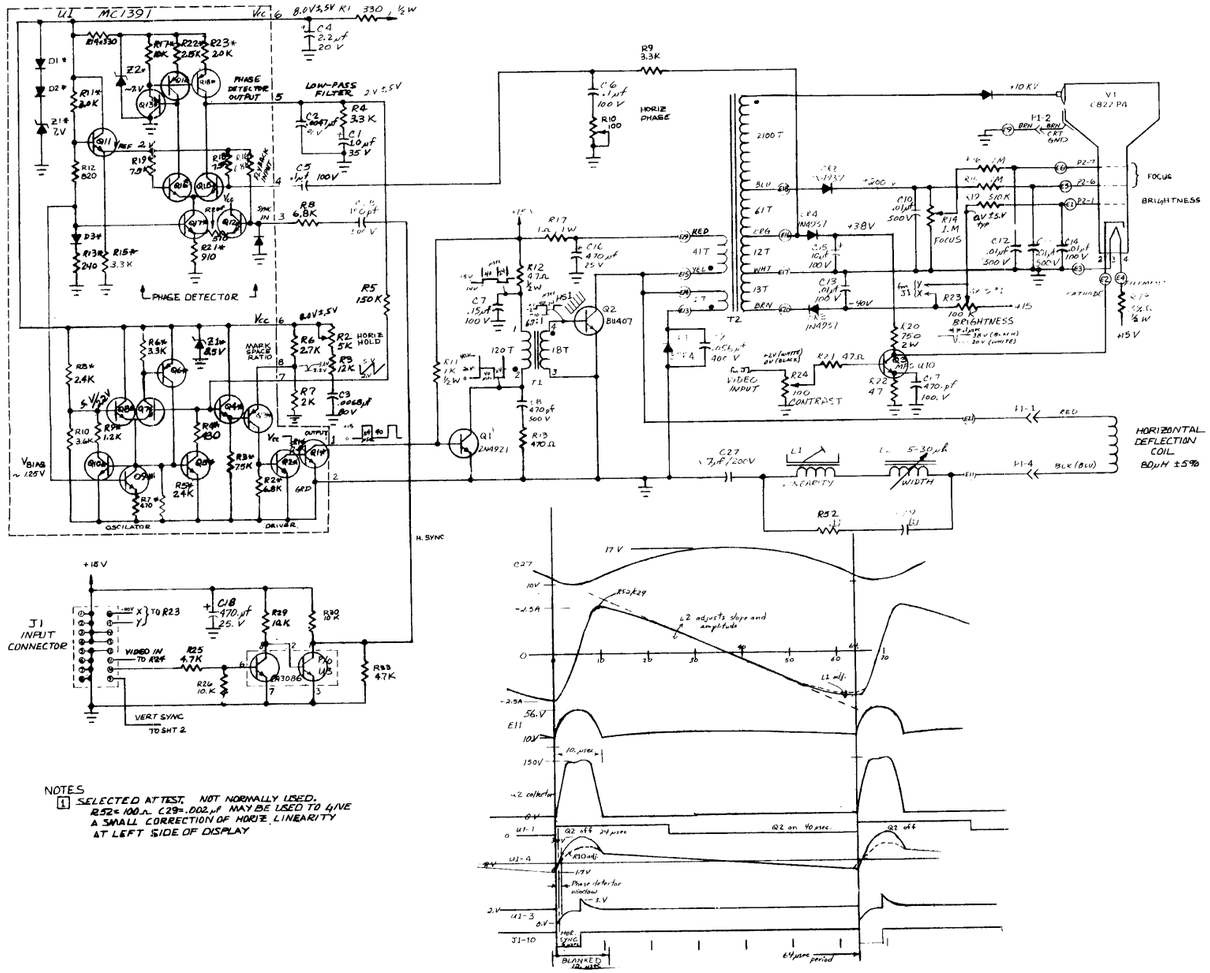
Figure 7.13 Threshold/GPIB Interface Schematic, 0112-0041



FROM	TO	COLOR/AWG	LGTH
P1-1	E8	RED/22	7.5
2	E9	BRN	9.5
3	E10	WHT	9
4	E11	BLK	9
P1-6	E12	YEL/22	8.5
P2-GRN	E1	—	7
VIO	E2	—	6.5
BLK	E3	—	7
BRN	E4	—	8.5
ORN	E5	—	7
P2-BLU	E6	—	7.25
T2-YEL	E21	—	3
T2-VIO	E13	—	2
T2-VIO	E14	—	2
T2-GRN	E15	—	3
T2-ORN	E16	—	3
T2-BLU	E18	—	3
T2-RED	E19	—	3
T2-BRN	E20	—	3
T2-WHT	E17	—	2
CR5-RED	P3	—	3.5
CR5-BLK	E7	—	1.75
CR5-WHT	T2-A	—	

Figure 7.14 Data Display Assembly, 0113-0005

P.W.B ASSY-DATA ISPLAY



NOTES
1. SELECTED AT TEST. NOT NORMALLY USED. R52 = 100 Ω, C28 = .002 μF MAY BE USED TO GIVE A SMALL CORRECTION OF HORIZ. LINEARITY AT LEFT SIDE OF DISPLAY

Figure 7.15 Data Display PWB Schematic, 0113-0006

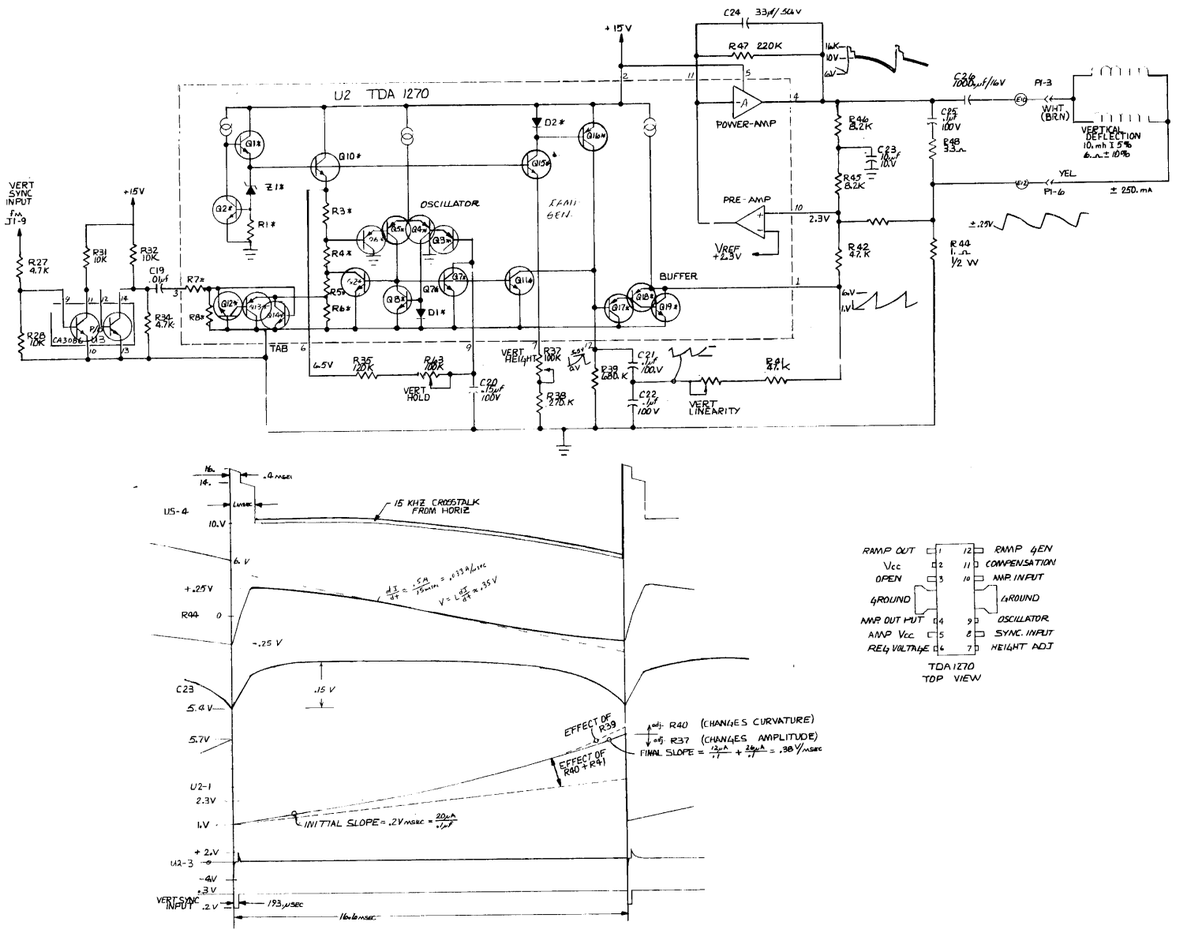
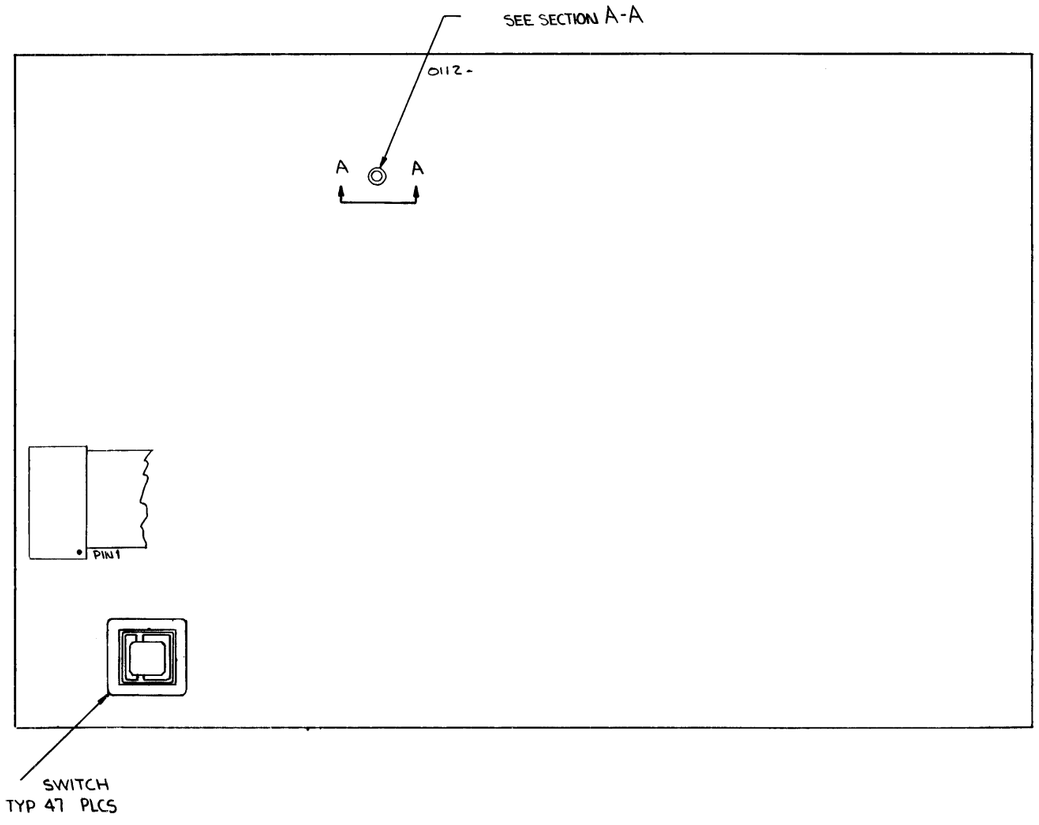
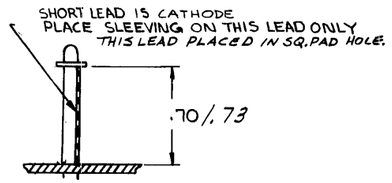


Figure 7.15 Continued. Data Display PWB Schematic, 0113-0006





SECTION A-A
L.E.D. MOUNTING VIEW

Figure 7.16 Keyboard Assembly, 0112-0120

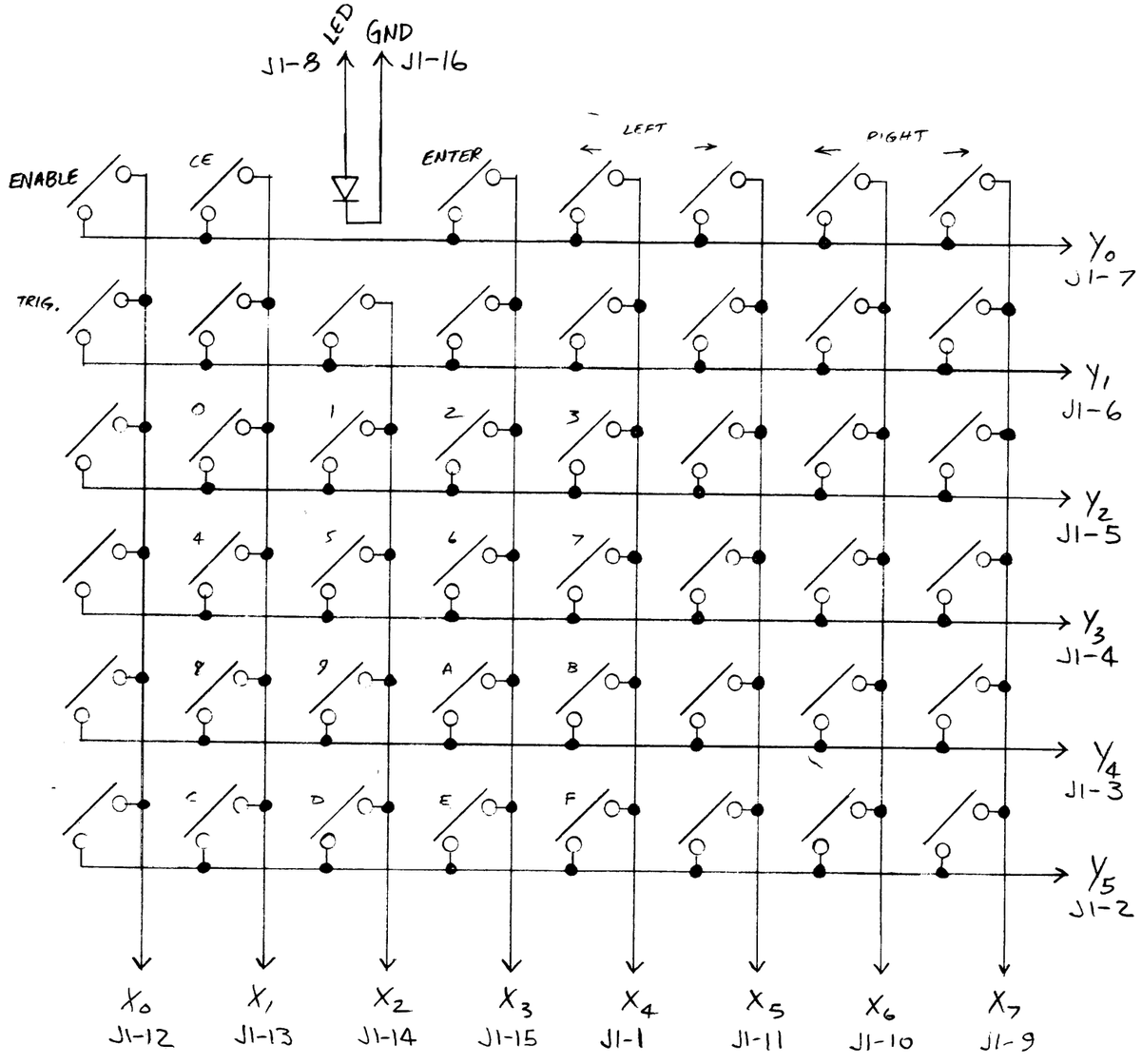
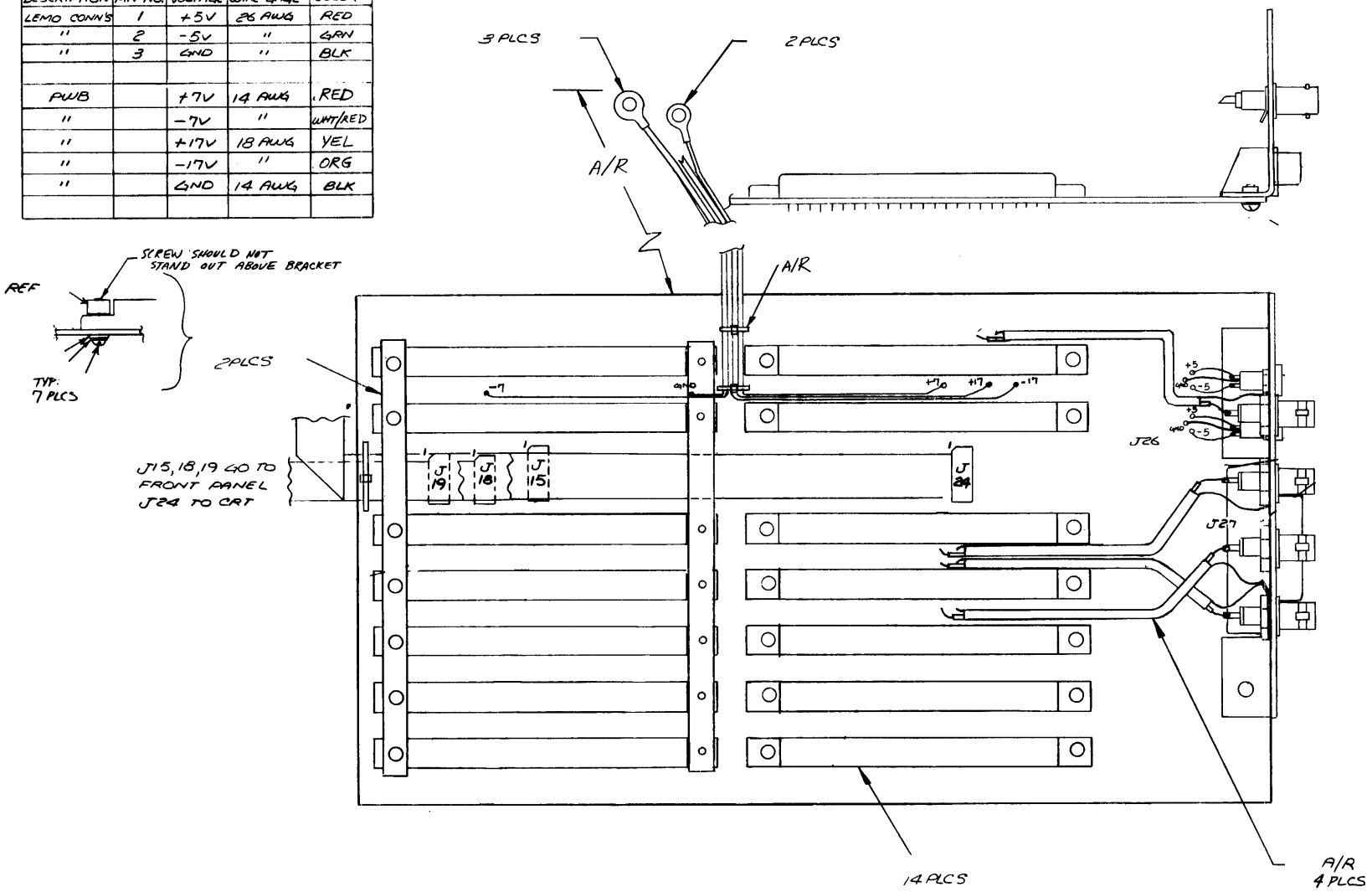


Figure 7.17 Keyboard Schematic, 0112-0121

WIRING CHART

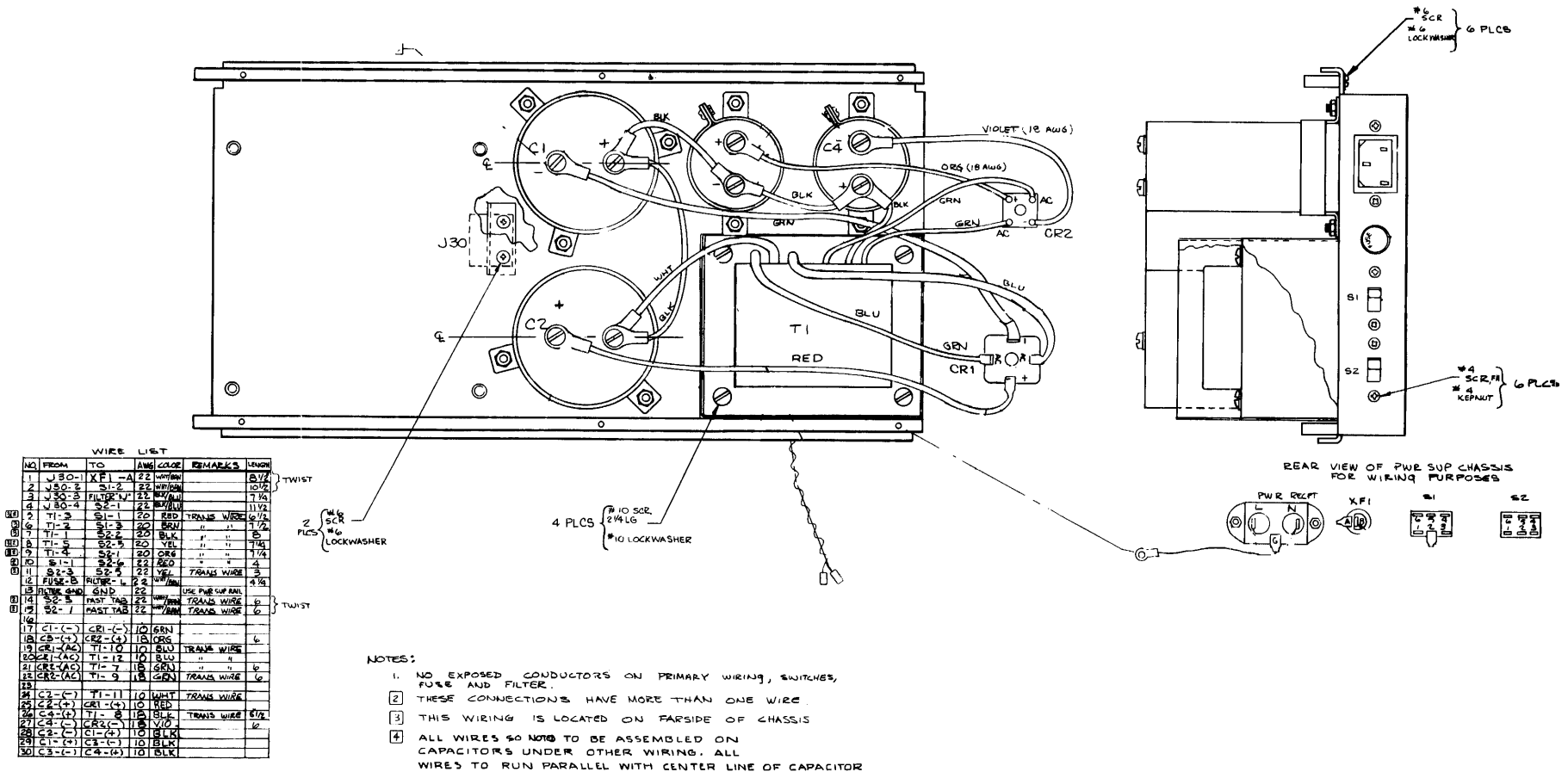
DESCRIPTION	PIN NO.	VOLTAGE	WIRE GAGE	COLOR
LEMO CONN'S	1	+5V	26 AWG	RED
"	2	-5V	"	GRN
"	3	GND	"	BLK
PWB		+7V	14 AWG	RED
"		-7V	"	WHT/RED
"		+17V	18 AWG	YEL
"		-17V	"	ORG
"		GND	14 AWG	BLK



NOTES:
1. ALL RIBBON CABLES PLUG INTO SOCKETS SOLDERED TO MOTHER BOARD
2. *KEEP SOLDER OUT OF J26 AND J27

Figure 7.18 Mother Board Assembly, 0112-0015

Figure 7.19 Mother Board Schematic
0112-0016



WIRE LIST

NO.	FROM	TO	AWG	COLOR	REMARKS	LENGTH	
1	J30-1	XF1-A	22	WHT/BRN		8½	TWIST
2	J30-2	S1-2	22	WHT/BRN		10½	
3	J30-3	FILTER N°	22	BLK/BLU		7¼	
4	J30-4	S2-1	22	BLK/BLU		11½	
[4] 5	T1-3	S1-1	20	RED	TRANS WIRE	6½	
[3] 6	T1-2	S1-3	20	BRN	" "	7½	
[3] 7	T1-	S2-2	20	BLK	" "	8	
[3][4] 8	T1-5	S2-5	20	YEL	" "	7¼	
[3][4] 9	T1-4	S2-1	20	ORG	" "	7¼	
[3] 10	S1-1	S2-6	22	RED	" "	4	
[3] 11	S2-3	S2-5	22	YEL	TRANS WIRE	3	
12	FUSE-B	FILTER-L	22	WHT/BRN		4½	
13	FILTER GND	GND	22		USE PWR SUP RAIL		
[3] 14	S2-5	FAST TAB	22	WHT/BRN	TRANS WIRE	6	TWIST
[3] 15	S2-1	FAST TAB	22	WHT/BRN	TRANS WIRE	6	
16							
17	C1-(-)	CR1-(-)	10	GRN			
18	C2-(+)	CR2-(+)	18	ORG		6	
19	CR1-(AC)	T1-10	10	BLU	TRANS WIRE		
20	CR1-(AC)	T1-12	10	BLU	" "		
21	CR2-(AC)	T1-7	18	GRN	" "	6	
22	CR2-(AC)	T1-9	18	GRN	TRANS WIRE	6	
23							
24	C2-(-)	T1-11	10	WHT	TRANS WIRE		
25	C2-(+)	CR1-(+)	10	RED			
26	C4-(+)	T1-8	18	BLK	TRANS WIRE	6½	
27	C4-(-)	CR2-(-)	18	VIO		6	
28	C3-(-)	C1-(+)	10	BLK			
29	C1-(+)	C3-(-)	10	BLK			
30	C3-(-)	C4-(+)	10	BLK			

NOTES:

1. NO EXPOSED CONDUCTORS ON PRIMARY WIRING, SWITCHES, FUSE AND FILTER.
2. THESE CONNECTIONS HAVE MORE THAN ONE WIRE
3. THIS WIRING IS LOCATED ON FARSIDE OF CHASSIS
4. ALL WIRES SO NOTED TO BE ASSEMBLED ON CAPACITORS UNDER OTHER WIRING. ALL WIRES TO RUN PARALLEL WITH CENTER LINE OF CAPACITOR

Figure 7.20 Power Supply Assembly, 0112-0035

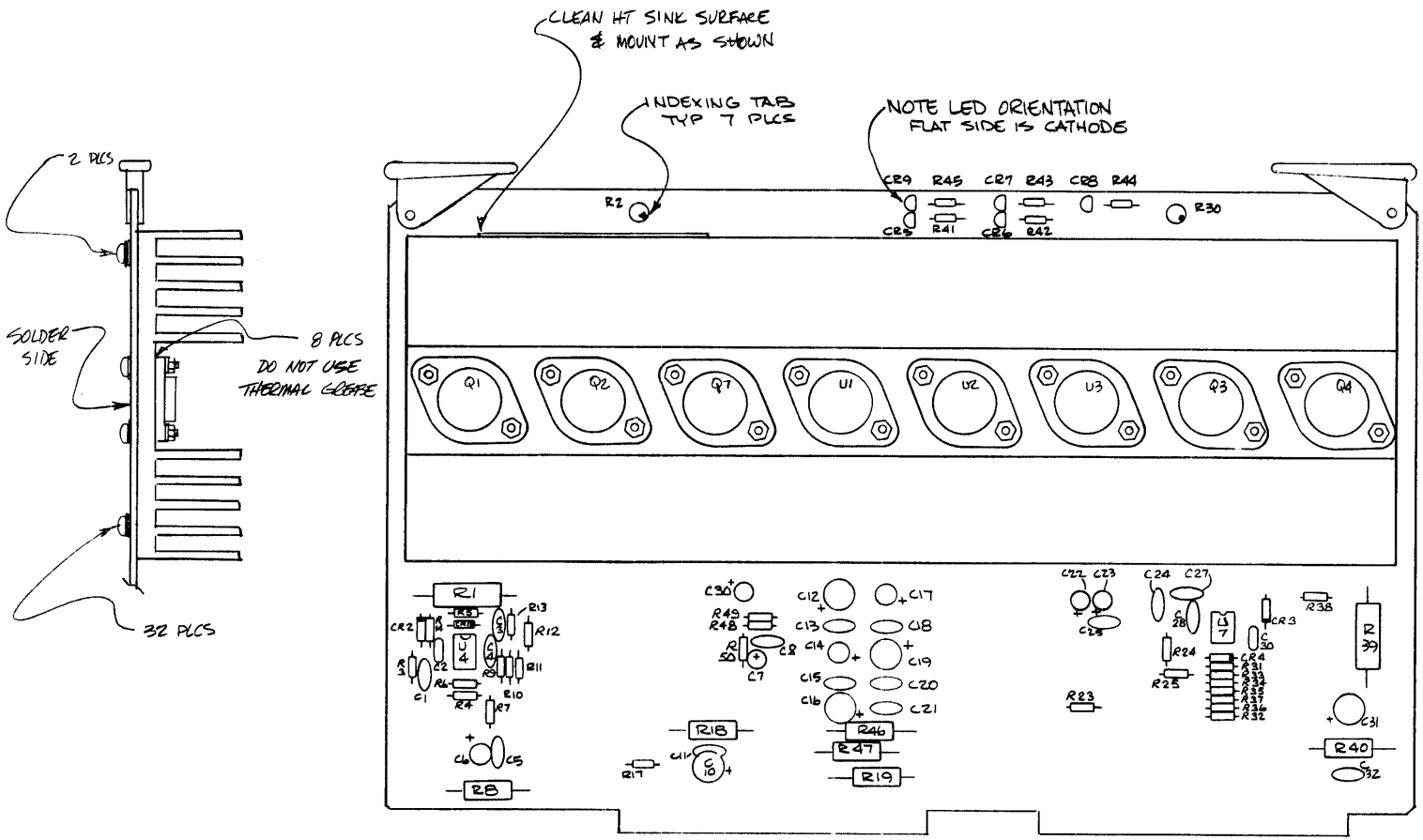
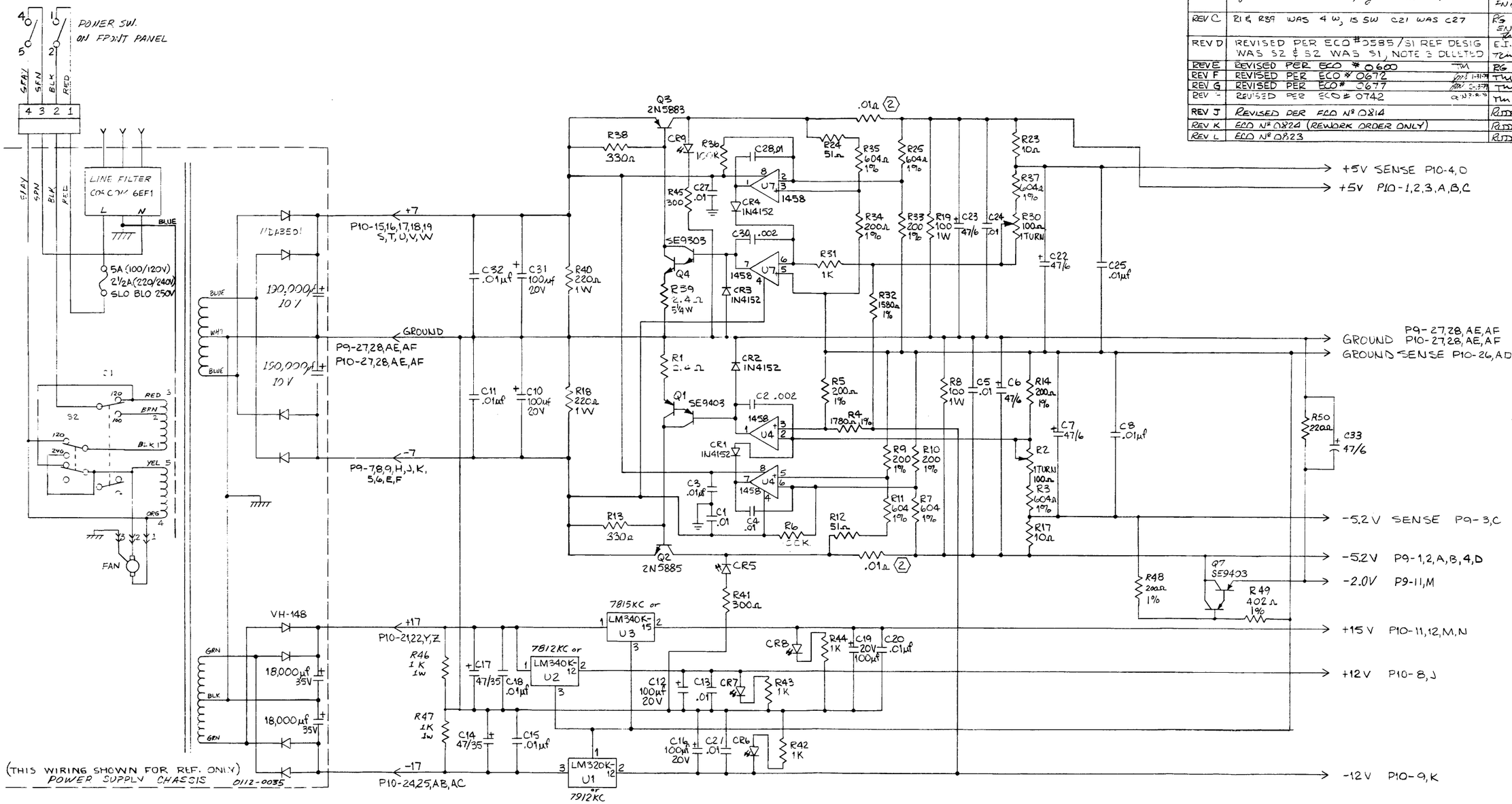


Figure 7.21 Regulator Board Assembly, 0112-0050

REV A	change TRANS. wiring, add R45, chg R27 from 30 to 39 chg R9 fm 400 to 150, chg C9 & C28 fm .1 to .01 chg R42, 43, 44 fm 300 to 1K, add Q7, R48-R50 & C32	CB 10-27-77
REV B	chg P/N from X100- to 0112-, chg CR2 to R51 (1K)	CB 7-19-78 ENO 852
REV C	R1 & R39 WAS 4 W, 1S SW C21 WAS C27	RG 8-28-78 ENO 881
REV D	REVISED PER ECO #0585/S1 REF DESIG WAS S2 & S2 WAS S1, NOTE 3 DELETED	E.I. 11-8-78 TM
REV E	REVISED PER ECO # 0600 TM	RG 11-16-78
REV F	REVISED PER ECO # 0672	TM 2/1/79
REV G	REVISED PER ECO # 0677	TM
REV H	REVISED PER ECO # 0742	TM
REV J	REVISED PER ECO Nº 0814	RJDELL 6-12-79
REV K	ECO Nº 0822 (REWORK ORDER ONLY)	RJDELL 6-12-79
REV L	ECO Nº 0823	RJDELL 6-12-79



NOTES

1. ALL RESISTORS ARE 1/4 W, 5% UNLESS OTHERWISE INDICATED.
2. .01Ω RESISTORS ARE FABRICATED AS AN INTEGRAL PART OF THE PWB (2 PLCS).

Figure 7.22 Regulator Board Schematic, 0112-0051

Top Assembly 0112-0003

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1			1	1	1	1	0112-0200	CHASSIS ASSY				L/M
2												
3												
4												
5												
6			1	1	1	1	0112-0040	THRESHOLD PWB ASSY				LM
7			1	1	1	1	0111-0016	HANDLE ASSY				LM
8												
9			2	2	2	2	0111-0059	KNOB BAIL				
10			—	1	—	1	7300-0022	FUSE			5 AMP S/B	
11			1	—	1	—	7300-0021	FUSE			2½ AMP S/B	
12												
13			—	—	1	1	0112-0010-10	FRONT END, PWB ASSY				LM
14			1	1	—	—	0112-0030-20	RECORD CONTROL PWB ASSY				LM
15			1	1	—	—	0112-0010-20	FRONT END PWB ASSY				LM
Ⓐ16			2	2	2	2	0112-0150	MEMORY PWB ASSY				LM
17			—	—	1	1	0112-0030-10	RECORD CONTROL PWB ASSY				LM
18			1	1	1	1	0112-0050	REG. PWB ASSY				LM
19			1	1	1	1	0112-0060	MPU PWB ASSEMBLY				LM
20												
21			1	1	1	1	0111-0111-10	TOP COVER				
22			1	1	1	1	0111-0111-20	BOTTOM COVER				
23												
24												
25												
26												
27												
28			12	12	12	12	7000-0365	SCREW			6-32 X 3/8 LG, 100° FLHD	
29			2	2	2	2	7000-0376	SCREW, SOC. HD. CAP.			1/4-20 X 3/4 LG.	
30			2	2	2	2	——	WASHER, SPLIT LOCK			1/4-20	
31												
32												
33												
34												
35												
36												

Cont. Top Assembly 0112-0003

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
37												
38			1	1	1	1	0112-0125-10	ASSY ACTIVE PROBE				LM
39			1	1	1	1	0112-0125-20					LM
40												
41			4	4	4	4	------	[illegible]				
42												
43			4	4	4	4	———	[illegible]				
44			40	40	40	40	9000-0041	GRABBER				
45			20	20	20	20	0112-0180-10	ASSY, SIGNAL WIRE			RED	LM
46			20	20	20	20	0112-0180-20	ASSY GND WIRE			BLK	LM

Assembly Front Panel 0112-0115

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1						1	0112-0117	PRINTED WIRING BD				
2												
3						4	6600-0068	SWITCH	S1,2,3,4	C&K 7215-J2-V3-CG	(ON)-ON-(ON)	
4												
5						1	6100-0069	TRNS. SOCKET	@ CR1			
6						A/R	———	TUBING	(LED)	1/16 DIA	3/4 IN. LONG	
7						2	6100-0019	SOCKET	J15, J25	CIRCUIT ASSY CA-165-105D		
8						1	6400-0044	LED	CR1	MV5774C	RED	
9						2	6000-0237	CONNECTOR	J20, 21		50 PIN PLUG	
10						2	6100-0010	SOCKET	J18, 19		14 PIN DIP	
11						2	6000-0271	CONNECTOR	J22, 23		20 PINS	
12												
13						2	1400-0019	TRANSISTOR	Q1, 2	2N3906		
14						1	1800-0107	INTEGRATED CIRCUIT	U3	74LS04		
15						1	1800-0240		U5	74LS244		
16						1	1800-0193		U4	74LS138		
17						2	1820-0025		U2,6	1451/3451		
18						1	1820-0053	INTEGRATED CIRCUIT	U1	4724		
19						1	1700-0026	INTEGRATED CIRCUIT	U7	NE521		
20												
21						2	3000-1002	RESISTOR	R3,4		10K, 1/4 W, 5%	
22						2	3000-3300		R1, 2		330Ω, 1/4W, 5%	
23						4	3100-2001		R5,6,7,8		2K, 1/8 W, 1%	
24												
25												
26						1	3000-1001	RESISTOR	R9		1K, 1/4, 5%	
27						2	3700-0015	RESISTOR, PAK	RP1, 2	BECKMAN 784-1-R10K	8 PIN SIP, 10K	
28												
29						5	4000-0005	CAPACITOR	C1, ,3,7,8,9		.01 MFD, 50V	
30						3	4300-0025	CAPACITOR	C2,5,6		47 MFD, 6V, 10%	
31												
32												

Front End PWB 0112-0010

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1					—	1	0112-0012-10	PWB				
2					2	2	6000-0271	HEADER, 20 PIN	J22, J23	3M 3428-2302	20 PIN 2 ROWS, .1 SPACING	
3					1	1	0112-0207-20	CABLE ASSY	P31			
4					1	1	1800-0105	I.C.	6K	74LS00		
5					9	9	1850-0043	I.C.	1A-5A, 8A-11A,	10216		
6					16	16	1850-0025	I.C.	1C-4C, 8C-11C 1B-4B, 8B-11B	10106		
7					9	9	1850-0051	I.C.	1E-5E, 8E-11E	10130		
8					10	10	1850-0019	I.C.	1H-5H, 8H-11H, 6H	10231		
9					27	27	1850-0030	I.C.	1J-5J, 8J-11J, 1K-5K, 8K-11K, 1M-5M, 8M-11M,	10121		
10					4	4	1850-0044	I.C.	7H, 7E, 7J, 7C	10211		
11					14	14	1820-0053	I.C.	1L-11L, 5B, 7B, 6J,	4724		
12					9	9	1850-0045	I.C.	1N-4N, 8N-11N 6E	10117		
13					2	2	1850-0023	I.C.	5N, 7K	10010		
14					1	1	0112-0207-10	CABLE ASSY.	P30			
15					14	14	1400-0019	TRANSISTOR	Q1-Q14	2N3906		
16					1	1	7200-0025	MOUSE TAIL			1" SMALL RND	
17					31	31	4000-0005	CAP.,	C1-C18, C20-C27 C32-C36		.01 µf /50V	
18					3	3	4300-0025	CAP.,	C29-C31		47µf /6V, 10%	
19					1	1	3000-5106	RES	R34		51Ω, 1/4W, 5%	
20					7	7	3000-8206	"	R19-24, R37		82Ω, 1/4W, 5%	
21					1	1	3000-1300	"	R47		130Ω, 1/4W, 5%	
22					28	28	3000-3300	"	R1-R16, R35, R36, R66, R67 R38, 40, 41, 43, 46, 48, 68, 69		330Ω, 1/4W, 5%	
23					9	9	3000-4700	"	R27-R33, R39, R45		470Ω, 1/4W, 5%	
24					2	2	3000-1002	"	R42, 44		10K, 1/4W, 5%	
25					1	1	3700-0021	RES, PACK	5C	BECKMAN 784-1-R470	8 PIN, SIP, 470Ω	
26					1	1	3700-0026	" "	7F	BECKMAN 784-1-R120	8 PIN, SIP,	
27					18	18	3700-0031	" "	1D-5D, 8D-11D, 1F-5F, 8F-11F,	BECKMAN 784-1-R330	8 PIN, SIP, 330Ω	
28					1	1	3700-0029	" "	7N	ALLEN/BRADLEY 316E221331	16 PIN	
29					6	6	3700-0038	" "	RP1-RP6	BECKMAN 764-1-R50	8 PIN, SIP, 51Ω	
30					18	18	3000-1001		R26, R49, R50-65		1K, 1/4W, 5%	
31					1	1	6000-0242	HOUSING, 3 CONTACTS		AMP 207359-1	Receptacle	
32					3	2	9000-0037-11	COAX ASSY	INT CLK SAMPLE CLK		11" PIN	
33					1	1	0112-0228-01	EJECTOR-STAMPED	A1			
34					1	1	7000-0120	EJECTOR				
35					A/R	A/R	——	WIRE INSULATED			24 AWG	
36					A/R	A/R	——	TWIST PAIR WIRE			24AWG BLK/WHT	

Cont. Front End PWB 0112-0010

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	60	-50	-40	-30	-20	-10						
37					1	—	0112-0012-20	PWB				
38												
39												
40					2	2	3000-3600	RES	R70,71		360Ω,1/4W,5%	
41					2	2	3000-2400	RES	R72,73		240Ω,1/4W,5%	
42					4	2	3000-7506	RES	R74,75,77,78		75Ω,1/4W,5%	
43					1	1	3000-1000	RES	R76		100Ω,1/4W,5%	
44					1	1	3000-2001	RES	R25		2K, 1/4W,5%	

Record Memory PCB 0112-0150

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1			\			1	0112-0152	RECORD MEMORY			A.C. BOARD	
2						2	3000-7506	RESISTOR	R32, 33		75Ω, 5%, 1/4W	
3						1	1800-0243	INTEGRATED CIRCUIT	18C	74S08	TI	
4						1	1800-0193		19C	74LS138	TI	
5						8	1800-0208		18A, 18B, 18D, 18E, 19A, 19B, 19D, 19E	74S161	TI (same as 1800-0102)	
6						1	1800-0240	INTEGRATED CIRCUIT	10F	74LS244	TI	
7						4	1300-0038	TRANSISTOR	Q1 THRU Q4	BFR91		
8						32	1800-0127	INTEGRATED CIRCUIT	9A-16A, 9D-16D 9B-16B, 9E-16E	82S117	SIGNETICS	
10						1	1850-0037		7C	10101		
11						8	1850-0023 / 1850-0055		3A, 3B, 3D, 3E 4A, 4B, 4D, 4E	10010 / 10016	EITHER PART MAY BE USED ON THIS ASS'Y.	
12						8	1850-0014		6A, 6B, 6D, 6E, 7A, 7B, 7D, 7E	10125		
13						5	1850-0019		4C, 9C, 11C, 14C, 16C	10231		
14						2	1850-0048		10C, 15C	10195		
15						3	1850-0043		1C, 2C, 3C	10216		
16						2	1850-0074	INTEGRATED CIRCUIT	13C, 18F	10125	(MOTOROLA ONLY)	
17						1	6000-0241	CONN. HOUSING PLUG		AMP 207360-1	3 POSITION	
18						2	9000-0037-11	COAX CABLE	C, R		11" LONG PIN	
19						2	3000-2200	RESISTOR	R23, 26, 51, 52		220Ω, 5%, 1/4W	
20						8	3000-3006		R8, 9, 10, 11, 16, 17, 18, 19		30Ω, 5%, 1/4W	
21						4	3000-1600		R22, 24, 25, 27		160Ω, 5%, 1/4W	
22						7	3000-3300		R34, 35, 36, 37, 48 R53, 54		330Ω, 5%, 1/4W	
23						9	3000-5106		R1, 3, 4, 28, 29, 30, 31, 38, 41		51Ω, 5%, 1/4W	
24						11	3000-1200	RESISTOR	R2, 5, 39, 40, 42-47 49		120Ω, 5%, 1/4W	
25						1	7200-0025	MOUSE TAIL				
26						9	3700-0026	RES./PACK	8A, 8B, 8D, 8E 17A, 17B, 17D, 17E, 17F		120Ω (8 PIN)	
27						11	3700-0038	RES./PACK	5A, 5B, 5C, 5D, 5E, 10a, 10b, 2D, 2E, 2B, 2A		51Ω (8 PIN)	
28						5	3700-0031	RES./PACK	RP1, 17C, 12C, 8C, 12F		330Ω (8 PIN)	
29						A/R	——	TWISTED/PAIR			24GA 3 TWISTS PER IN.	
30						8	3300-0048	POT	R6, R7, 12, 13, 14, 15, 20, 21	BECKMAN 82P-	2K, 1TURN	
31						1	6100-0023	SOCKET	J1	Burndy	16 PIN DIP	
32						4	4100-0006	CAPACITOR	C14, 17, 18, 21	DM10	20 pf, 5%	
33						5	4100-0019	CAPACITOR	C15, 16, 19, 20, 50	DM10	50pf, 5%	
34						23	4000-0025	CAPACITOR	C3, 4, 5, 6, 8, 9, 11, 12, 13, 22, 26, 27, 28, 30, 31, 33, 36, 37, 40, 41, 44, 45, 49		.1uf	
35						18	4300-0025	CAPACITOR	C1, 2, 7, 10, 23, 24, 25, 29, 32, 34, 35, 38, 39, 42, 43, 46, 47, 48		47uf, 6V	
36						1	7000-0120	EJECTOR		CALMARK		
37						1	0112-0228-02	EJECTOR, STAMPED				
38						1	3000-4700	RESISTOR	R55		470Ω ± 5% 1/4W	

Record Control Assembly 0112-0030

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1					—	1	0112-0032-10	PWB				
2					1	1	7000-0120	EJECTORS				
3					2	2	1800-0107	I.C.	6D, 11E		74LS04	
4					1	1	1800-0193	↕	8D		74LS138	
5					6	6	1800-0231	↕	2C, 3C, 5C, 6C, 7C, 8C		74LS273	
6					1	1	1800-0240	I.C.	9E		74LS244	
7					1	1	0112-0228-03	EJECTOR STAMPED	A3			
8					2	2	1820-0063	I.C.	12C, 13C		MC14518B	
9					1	—	0112-0032-20	PWB				
10					2	2	1850-0002	I.C.	12D, 18B		MC10102	
11					4	4	1850-0005	↕	4A, 9A, 12E, 14E		MC10105	
12					2	2	1850-0014	↕	9D, 10D		MC10125	
13					6	6	1850-0019	↕	8B, 9B, 10B, 12B, 13D, 13E		MC10231	
14					1	1	1850-0021	↕	5E		MC10124	
15					1	1	1850-0025	↕	9C		MC10106	
16					1	1	1850-0030	↕	5B		MC10121	
17					4	4	1850-0035	I.C.	4C, 15E, 16E, 17B		MC10210	
(D) 18					1	1	0112-0227-01	LABEL	A1			
19					1	1	1850-0045	I.C.	6B		MC10117	
20					3	3	1850-0041	I.C.	15C, 16C, 18C		MC10138	
21					1	1	1850-0042	I.C.	17C		MC10164	
22					8	8	1850-0055	I.C.	2A, 2B, 3A, 3B, 7A, 8A, 11D, 11C		MC10016	
23					1	1	0112-0227-02	LABEL	A2-1			
24					1	1	6600-0037	SWITCH	7E	AMP 4351666-5	16 PIN DIP SWI.	
25					1	1	0112-0227-03	LABEL	A2-2			
26					3	3	3700-0002	RESISTOR-PAK	1C, 5A, 7B		10K, 16 PIN DIP	
27					1	1	3700-0004	↕	4E		470Ω, 16 PIN DIP	
28					3	3	3700-0015	↕	RP1, 3, 5		10K, 8 PIN SIP	
29					2	2	3700-0027	↕	4B, 11B		330Ω, 16 PIN DIP	
30					1	1	3700-0029	↕	3E		220/330, 16 PIN DIP	
31					2	2	3700-0031	↕	RP2, 8		330Ω, 8 PIN SIP	
32					1	1	3700-0046	RESISTOR PAK	RP4		270Ω, 8 PIN SIP	
33					1	1	3300-0028	POT	R48		100Ω	
34					1	1	1000-0016	DIODE	CR1		1N4152	
35					1	1	1300-0038	TRANSISTOR	Q15	HARRIS	BFR-91	
36					16	16	1400-0016	TRANSISTOR	Q1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 16, 17	MOTOROLA	2N3906	

Cont. Record Control Assembly 0112-0030

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
37					1	1	2100-0011	COIL	L2	DELEVAN	22 µH	
38					1	1	2100-0014	COIL	L1	DELEVAN	.1 µh	
© 39					2	2	3000-1002	RESISTOR	R24,25		10K, 1/4W, 5%	
40					1	1	3000-2700	↑	R52		270 Ω ↑	
41					1	1	3000-1001		R11		1K	
© 42					13	13	3000-1300		R2,4,5,8,19,21,37, 38,39,41,43,45,50		130Ω	
43					1	1	3000-1800		R28		180Ω	
© 44					3	3	3000-2001		R10,30,47		2K	
45					1	1	3000-2006		R29		20Ω	
© 46					13	13	3000-3300		R14,15,16,23,26, 31-36,17,46		330Ω	
47					2	2	3000-5100	↓	R27,13		51Ω ↓	
48					12	12	3000-8206	RESISTOR	R1,3,6,7,18,20 40,42,44,12,9,49		82Ω, 1/4W, 5%	
49					1	1	4100-0010	CAP	C10		47 pf	
© 50					38	38	4000-0105	CAP	C1-9,12,13,15-27, 29,31-34,36-40,42-45		.1µf	
51					1	1	4600-0001	CAP, VARIABLE	C46		5.5 - 18 Pf	
© 52					1	1	4100-0006	CAP	C11		20 Pf	
© 53					4	4	4300-0025	CAP	C28,30,35,41		47µf/6V	
54					1	1	5100-0004	CYSTAL	Y1		100 MHZ	
55					2	2	9000-0025-07	COAX CABLE	A,C		7" LONG	
56					1	1	9000-0025-09	COAX CABLE	B		9" LONG	
57												
58					2	2	9000-0025-10	COAX CABLE	D,E		10" LONG	
59												
60					1	1	9000-0025-04	COAX CABLE	G		4" LONG	
61					2	2	9000-0025-06	COAX CABLE	R,F		6" LONG	
© 62												
63					36"	36"	——	WIRE, 24 AWG	E11 = 18" TP16 = 18"		TWISTED PAIR	
64					1	1	3000-3906	RESISTOR	R51		39Ω 1/4W 5%	
© 65					5	5	9000-0036-10	COAX ASS'Y	P1,P2,S,I,SX	10" LG	SOCKET	
© 66					2	2	9000-0036-19	COAX ASS'Y	C1,C2	19" LG	SOCKET	
© 67					3	3	6000-0241	CONNECTOR HOUSING, PLUG	P1,C1 → P33 S,I, → P32 P2,C2 → P34	AMP 207360-1		
© 68					1	1	9000-0025-14	COAX CABLE	I2			
69												
70					A/R	A/R	7200-0025	MOUSE TAILS				
71					1	1	6000-0183	HEADER 10 PIN				
72					1	1	6000-0184	HEADER 10 PIN				

MPU PCB Assembly 0112-0060

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1						1	0112-0062	PWB				
2						2	7000-0120	EJECTORS				
3						1	6100-0046	SOCKET	XD16		16 PIN DIP	
4						3	3700-0029	RES PK	D5, D14, C11	AB 316E	220Ω*330Ω	
5						1	1800-0179	I.C.	F3		74S65	
6						2	1820-0065	I.C.	C9, C10		4069, "FAIRCHILD ONLY"	
7						16	1800-0229	I.C.	B1-8, C1-8	MOSTEK MK4116P-4	16K RAM, 250nsec	
(E) 8												
(C) 9						1	1800-0260	I.C.	F2		74S20	
10						1	1800-0201	I.C.	D9	ADVANCED MICRO SYSTEM	MC6800	
11						1	0112-0064	I.C.	D16		82S123 PROM CRT CONTROLLER	
12						1	1800-0251	I.C.	D7		74165	
13						1	1800-0123	I.C.	E12		74LS14	
(D) 14						5	1800-0193	I.C.	D8, E6, E7, E8 B10		74LS138	
15						1	1800-0214	I.C.	B16		74LS11	
16						1	1800-0117	I.C.	E16		74LS86	
17						5	1800-0125	I.C.	B14, B15, C16, C17, D15		74LS161	
(C) 18						1	1800-0111	I.C.	E13		74LS20	
19						13	1800-0240	I.C.	B6, B11, B12, B13, C12-C15, D4, D6, D13, E9, E10		74LS244	
20						1	1800-0091	I.C.	E11		74123	
21						2	1800-0068	I.C.	B18, B17		74LS112	
22						3	1800-0234	I.C.	E1, E2, E3		74S112	
23						1	1800-0105	I.C.	B9		74LS00	
24						3	1800-0248	I.C.	D1, D3, E4		74S00	
25						2	1800-0107	I.C.	D17, E14		74LS04	
26						1	1800-0092	I.C.	D2		74S04	
27						1	1800-0060	I.C.	E5		74S10	
28						2	1800-0200	I.C.	E15, E17		7433	
29						1	3000-8206	RES.,	R12		82Ω, 1/4W, 5%	
30						1	3000-5106	RES.,	R13		51Ω, 1/4W, 5%	
(D) 31						7	3000-4701	RES.,	R20, 21, 24 R4, 5, 6, 16		4.7K, 1/4W, 5%	
(D)(C) 32						7	3000-4700	RES.,	R2, R3, 11, 25, 26, 29, 30		470Ω, 1/4W, 5%	
33						1	3000-1002	RES.,	R7		10K, 1/4W, 5%	
(E) 34						6	3000-6800	RES.,	R10, R14, R15, R31, R32, R33		680Ω, 1/4W, 5%	
35						1	3000-1800	RES.,	R9		180Ω, 1/4W, 5%	
36						1	3000-1506	RES.,	R17		15Ω, 1/4W, 5%	

Cont. MPU PCB Assembly 0112-0060

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
37						1	3000-7506	RES	R19		75Ω, 1/4W, 5%	
38						1	3300-0041	RES, POT	R18	BOURNS 3329H-1-103	10K	
39						1	3000-3300	RES	R23		330Ω, 1/4W, 5%	
40						1	3000-2200	RES	R22		220Ω, 1/4W, 5%	
41						1	1000-0002	DIODE	CR1	IN4152		
(D) 42						1	4100-0008	CAP.	C57		200pf, 5%, 500V	
43												
(C) 44						1	4000-0030	CAP.	C56		.002 µf	
(B) 45						34	4000-0025	CAP.	C1,4-11,13,15-18,21,23,25,27 28,30,32,34,36,38,40-43, 45-47,49,50,58		.1 uf	
(A) 46						16	4300-0025	CAP.	C2,3,12,14,19,20,22,24 26, 37,39,44,48,52,54,59		47/6, 10%	
47						5	4300-0026	CAP.	C29,31,33,35,51		15/20	
(D) 48						1	3000-3001	RES.	R27		3K, 1/4W, 5%	
49						1	1300-0028	TRANSISTOR	Q2	2N3904		
50						1	1400-0019	TRANSISTOR	Q1	2N3906		
(D) 51						1	5100-0011	CRYSTAL	Y1	CTS MP200	20 MHZ	
(D) 52						12	6100-0122	SOCKET	ROM Ø - ROM 11	BURNDY	24 PIN	
53						1	6100-0123	SOCKET	D9		40 PIN	
(D) 54						1	3000-5101	RES.	R28		5.1K, 1/4W, 5%	
55						1	0112-0101-10	I.C., R.O.M	ROM Ø		16K READ ONLY MEM	
56						1	-11		ROM 1			
57						1	-12		ROM 2			
58						1	-13		ROM 3			
59						1	-14		ROM 4			
60						1	-15		ROM 5			
61						1	-16		ROM 6			
62						1	-17		ROM 7			
63						1	-18		ROM 8			
64						1	-19		ROM 9			
65						1	-20		ROM A			
66						1	-21		ROM B			
67						1	3000-2700	RES.,	R8		270Ω, 1/4W, 5%	
68												
69												
70												
71												
72												

Assembly Threshold/GPIB Int. 0112-0040

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
1					1	1	0112-0042	P.W. BD.				
2					10	10	1700-0084	I.C.	1EA-5EA, 1EB-5EB		LF353BN	
3					2	2	1700-0033	"	9B,9C	3403		
4					1	1	1800-0107	"	9D	74LS74		
5					1	—	1800-0188	"	8E	74LS30		
6					1	1	1800-0193	"	8D	74LS138		
7					7	7	1800-0231	"	6A,6B,6C,6D 7B,7C,7D	74LS273		
8					3	1	1800-0240	"	6E,7A,7E	74LS244		
9					1	—	1800-0253	"	9E	74 S260		
10					1	—	1800-0262	"	10D	MC68488		
11					4	—	1800-0263	"	11D,11E,12D,12E	MC3448		
12					20	20	1820-0052	"	1-5 (A-D)	4051B		
13					2	2	1900-0006	I.C.	8B, 8C	MC1403L8		
14					7	7	6100-0044	SOCKET 14 PIN DIP	X1E-X5E, X9B, X9C			
15					4	4	3100-1002	RESISTOR	R45,46,57,58		10K, 1%	
16					2	2	3100-2001	"	R50, 54		2K, 1%	
17					1	1	3100-6040	"	R55		604Ω, 1%	
18					2	2	3100-3161	RESISTOR	R51, 52		3.16K, 1%	
19					2	2	3100-4531	RESISTOR	R49, 53		4.53K, 1%	
20					19	19	3100-4532	RESISTOR	R2,3,5,8,10,11,13,14,19,21,24,26 27,29,32,34,35,37,40		45.3K, 1%	
21					20	20	3100-1003	RESISTOR	R1,4,6,7,9,12,14,15,17,20,22,23 25,28,30,31,33,36,38,39		100K, 1%	
22					21	21	3300-0070	POT	R47,48,59-77	SPECTROL 64Z103	10K	
23					4	4	3300-0073	POT	R41-44 (A0,B0 A6,B6)	SPECTROL 64Z102	1K	
24					1	1	3100-4992	RESISTOR	R18		49.9K, 1%	
25					1	—	3700-0001	RES. PAK	8A	899-1-R10K	10K, 14 PIN	
26					1	—	3000-2006	RESISTOR	R80		20Ω, ¼W, 5%	
27					40	40	4000-0025	CAPACITOR	C1-15,17,18,20, 22-26,30-46		.1μf	
28					2	2	4300-0025	"	C16, 29		47/6	
29					2	2	4300-0026	CAPACITOR	C27, 28		15/20	
30					1	—	3000-5106	RESISTOR	R81		51Ω, ¼W, 5%	
31					1	—	6600-0037	SWITCH	9A	AMP 4351666-5	16 PIN DIP	
32					1	—	6100-0123	SOCKET	10D	Burndy	40 pin	
33					1	1	7000-0120	EJECTOR				
34					1	—	3000-1800	RESISTOR	R79		180Ω, ¼W, 5%	
35					1	—	3000-3300	RESISTOR	R78		330Ω ¼W, 5%	
36					1	—	1400-0019	TRANSISTOR	Q1		2N3906	
37					1	1	1100-0003	DIODE	CR1		IN751A	
38					1	1	0112-0228-04	EJECTOR, STAMPED	A4			

Data Display Monitor PCB Assembly 0113-0005

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1						1	0113-0007	P.W.B. DATA DISPLAY				
2						2	3000-4706	RESISTOR	R21,22		47Ω, 1/4W, 5%	
3						1	4700		R13		470Ω	
4						1	3307		R48		3.3Ω	
5						1	2703		R38		270K	
6						1	2001		R7		2K	
7						1	2701		R6		2.7K	
8						2	3301		R4,9		3.3K	
9						4	4701		R25,27,33,34		4.7K	
10						1	5601		R43		5.6K	
11						1	6801		R8		6.8K	
12						2	8201		R45,46		8.2K	
13						6	1002		R26,28-32		10K	
14						1	1202		R3		12K	
15						2	4702		R41,42		47K	
16						1	8202		R35		82K	
17						1	1503		R5		150K	
18						1	3000-2203	RESISTOR	R47		220K, 1/4W, 5%	
19						1	3000-6803	RESISTOR	R39		680K, 1/4W, 5%	
20						1	3000-5103	RESISTOR	R19		510K, 1/4W, 5%	
21						2	3000-1004	RESISTOR	R15,16		1M, 1/4W, 5%	
22												
23						1	3050-1007	RESISTOR	R44		1Ω, 1/2W, 5%	
24						1	3050-3906		R18		39Ω	
25						1	3050-3300		R1		330Ω	
26						1	3050-1001	RESISTOR	R11		1K, 1/2W, 5%	
27												
28						1	3050-4707	RESISTOR	R12		4.7Ω, 1/2W, 5%	
29						1	3080-7500	RESISTOR	R20		750Ω, 2W, 5%	
30												
31						1	3070-3907	RESISTOR	R17		3.9Ω ±5% 1W C.C.	
32												
33						2	3300-0089	TRIM POT	R24,10	D2C 101	100Ω - ALLEN BRADLEY	
34						1	3300-0084		R40	D2C 503	50K	
35						3	3300-0085	TRIM POT	R23,36,37	D2C 104	100K - ALLEN BRADLEY	
36												

Cont. Data Display Monitor PCB Assembly 0113-0005

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
37						1	3300-0087	TRIM POT	R2	D2C 502	5K ALLEN BRADLEY	
38						1	3300-0088	TRIM POT	R14	U201R105B	1M CTS CORP.	
39												
40						1	4100-0013	CAPACITOR	C24	ELMENCO DM10	33 Pf, 500V, MICA	
41						1	4100-0011	CAPACITOR	C28	ELMENCO DM10	150 Pf, 500V, MICA	
42						2	4100-0002	CAPACITOR	C8,17	ELMENCO DM15	470 Pf, 500V, MICA	
43												
44						5	4000-0009	CAPACITOR	C5,6,21,22,25		.1µf, 100V	
45						2	4000-0042		C7,20	PLESSEY 160C154J100	.15µf, 100V	
46						1	4300-0036		C4	MATSUO 221L2002-225 M7	2.2µf, 20V	
47						1	4300-0037		C1	MATSUO 221L3502-105 M7	1µf, 35V	
48						2	4000-0005		C13,19	NICHICON	.01µf, 100V	
49						4	4000-0043		C10,11,12,14	ILL. CAP SALES G.Q. .01/500V	.01µf, 500V	
50						1	4300-0038		C2	SPRAGUE 192P4729R8	.0047µf, 80V	
51						1	4300-0039		C3	SPRAGUE 192P6829R8	.0068µf, 80V	
52						1	4300-0041	CAPACITOR	C9	SPRAGUE 192P56394	.056µf, 400V	
53												
54						1	4400-0036	CAPACITOR	C26	ILL. CAP SALES 16R1000	1000µf, 16V	
55						2	4400-0037	CAPACITOR	C16,18	ILL. CAP SALES 25R470	470µf, 25V ELECT.	
56						1	4400-0038	CAPACITOR	C15	ILL. CAP SALES 100R10	10µf, 100V ELECT.	
57						1	4400-0039	CAPACITOR	C23	ILL. CAP SALES 16T10	10µf, 16V ELECT.	
58												
59						1	4700-0006	CAPACITOR	C27	SOUTHER ELECT M PE11-6.0MFD	6uf, 200V	
60												
61												
62						4	1200-0031	RECTIFIER	CR1-4	1N4937	MOTOROLA	
63						1	1200-0032	H.V. MULTIPLYER	CR5	M H911	VARO INC	
64						1	1300-0048	TRANSISTOR	Q1	2N4921	MOTOROLA	
65						1	1300-0049		Q2	BU 407	SGS-ATES SEMICONDUCTORS	
66						1	1300-0050	TRANSISTOR	Q3	MPS U10	MOTOROLA	
67												
68												
69						1	1700-0080	I.C.	U3	CA 3086	RCA TRANSISTOR ARRAY	
70						1	1700-0081	I.C.	U1	MC 1391 P	MOTOROLA HORIZ OSC	
71						1	1700-0082	I.C.	U2	TDA 1270	SGS-ATES SEMICONDUCTORS	
72												

Cont. Data Display Monitor PCB Assembly 0113-0005

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
73						1	0113-0011	COIL ASSY-HORIZ	L1		HORIZ. LIN COIL	LM
74						1	0113-0012	COIL ASSY-WIDTH	L2		WIDTH COIL	LM
75						1	6000-0230	CONNECTOR	P1	03-06-1061	MOLEX	
76						5	6000-0269	PINS	@P1	FEMALE 02-06-1103	MOLEX	
77						1	0113-0013	TRANSFORMER ASSY	T2		FLYBACK	LM
78						1	0113-0014	TRANSFORMER	T1			LM
79												
80						1	7000-0365	HEAT SINK	@Q2	6025 B-TT	THERMALLOY	
81						1	7000-0366	HEAT SINK	@ U2	V8-800	STAVER	
82						1	7000-0221	INS. WASHER	@ Q2			
83						1	6100-0118	DIP SOCKET	(U1)	AUGAT 508-A619D	8 PIN	
84						1	6100-0014	DIP SOCKET	(U3)	CKT ASSY CA-145-105D	14 PIN	
85						1	6100-0046	DIP SOCKET	J1	CKT ASSY CA-165-105D	16 PIN	
86						A/R	8200-0020	INSULATING VARNISH	@ T2-A			
87						1	7200-0017	INSULATOR	@Q2	CHOMERICS 69-11-4969-1674	TO220	
88						1	6100-0130	CRT SOCKET	P2	49-21H	EBY SALES	
89						1	6000-0233	H.V. CONN		AC-3	EBY SALES	

Keyboard Assembly 0112-0120

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
1						1	0112-0122	PWB				
2												
3						1	0112-0204	CABLE ASSY			KEYBD. TO F PANEL	
4												
5						1	6400-0039	L.E.D.		HP 5082-4684	RED	
6						47	6600-0083	SWITCH		DATANETICS DC61-01	4OZ	
7												
8						A/R	———	SLEEVING				
9												

Mother PWB Assembly 0112-0015

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1						1	0112-0017	PWB				
2						AA	6000-0198	PWB CONNECTOR	J1 - J14	VIKING 3VN28/1CE5	D 28 PIN PWB CONNECTORS	
3						1	0820-0105-80	RIBBON CABLE	J15	CA-D-16P-02-26-1-DC-012	16 PIN 12-IN.	
4						2	0920-0037-40	RIBBON CABLE	J18,19	CA-D-14P-02-26-1-DD-011	14-PIN 11-IN.	
5						1	0920-0037-60	RIBBON CABLE	J24	CA-D-16P-02-26-1-DD-016	16 PIN 20-IN.	
6						1	0112-0026	BNC BRACKET				
7						4	6000-0014	BNC		KINGS KC79-375	SHORT BASE	
8						2	6000-0181	LEMO CONNECTOR		LEMO RA-0303-HVL	3 PIN	
9						2	———	#6 SCREW PAN HEAD			6-32 x 1/4 LG	
10						2	———	#6 WASHER				
11						2	———	#6 L/WASHER				
12						2	0112-0027	CONN. BRACKET				
13												
14						A/R	7200-0025	MOUSE TAIL				
15						4	9000-0025-06	COAX CABLE	6" LONG		RG 316 A/U	
16						4	7000-0009	GND LUG			BNC	
17						3	6200-0031	TERMINAL #10 RING TONGUE	BLUE		FOR 14 AWG WIRE	
18						2	6200-0027	TERMINAL #10 RING TONGUE	RED		FOR 18 AWG WIRE	
19												
20						1	6000-0235	CONNECTOR	GPIB	AMP 552740-1	24 pin receptacle right angle P.C. mount	
21						2	—	SCREW	3/8" LONG		#4, SELF TAPPING	
22						7	—	SCREW, PAN HD.			4-40 x 9/16	
23						7	—	LOCK WASHER			#4 INT TOOTH	
24						7	—	FLAT WASHER			#4	
25						2	6100-0044	SOCKET, DIP	@ J18, J19	AUGAT 514 AG-10D	14 PIN	
26						2	6100-0046	SOCKET, DIP	@ J15, J24	AUGAT 516 AG-10D	16 PIN	

Power Supply Assembly 0112-0035

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1						1	0112-0036	PS SHELF				
2						2	7000-0302	CLAMP, CAP		SPRAGUE 4586-2	3" DIA.	
3						1	0112-0037	XMFR	T1	TRANEX 4-4043		
4						2	4400-0012	CAP	C1, C2	HARDWARE SUPPLIED	190,000 mfd / 10V	
5						8	6200-0034	RING TONGUE		PV10-10RX	#10 YELLOW	
6						2	4400-0016	CAP	C3, C4	HARDWARE SUPPLIED	18,000 mfl / 25V	
7						2	7000-0046	CLAMP, CAP		SANGAMO 11058-05	2" DIA.	
8						1	6000-0047	CORCOM		GEFI	PLUG, FILTER	
9								DELETED				
10						2	0112-0019	MOTHER PWB RAIL				
11												
12						1	1200-0025	RECTIFIER	CR2	VARCO VH-148		
13						A/R	—	10 AWG WIRE			BLK	
14						1	1200-0029	RECTIFIER	CR1	MOTOROLA MDA-3501	35 AMP 100V	
15						A/R	—	10 AWG WIRE		STRANDED	RED	
16						A/R	—	10 AWG WIRE		STRANDED	GRN	
17												
18												
19						1	0115-0087	CONNECTOR BRACKET				
20												
21						2	6200-0027	RING TONGUE	18 AWG	PV14-10RX	#10 RED	
22						1	6000-0023	CONN 4 PIN	J30	AMP 1-480425-0	PLUG	
23						4	6100-0006	CONTACT PIN	@ J30	AMP 61173-1	FEMALE PINS	
24												
25						1	7300-0013	FUSE HOLDER		342038 LITTLE FUSE		
26												
27						2	6200-0035	FAST TAB		DV10-188FI	.187 RED	
28						2	6700-0015	SWITCH DPDT		CW GF-626		
29						A/R	—	WIRE #18 AWG				
30						1	0112-0074	SHIELD TRANSFORMER				
31												
32						2	6200-0039	FACT TAB		DV10-250FI	.250 YEL	
33						2	6200-0024	RING TONGUE		PV-18-8RX	#4 RED	
34						4	6200-0041	FAST TAB		DNF18-110	.110 RED	
35												

Regulator Assembly 0112-0050

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1						1	0112-0052	PWB				
2						4	1000-0002	DIODE	CR1-4	IN4152		
3												
4						1	0112-0228-05	EJECTOR, STAMPED	A5			
5												
6						1	1300-0042	TRANSISTOR	Q2	2N5885	NPN, TO-3	
7						1	1300-0045	TRANSISTOR	Q4	SE9303	NPN, TO-3	
8						1	1400-0030	TRANSISTOR	Q3	2N5883	PNP, TO-3	
9						2	1400-0034	TRANSISTOR	Q1, Q7	SE9403	PNP, TO-3	
10						8	7200-0016	INSULATOR	used for mounting Q1,2,3,4,7,U1,U2,U3	Chomerics 60-11-4996-1666	TO-3	
11						2	1700-0018	I.C.	U4,7	1458	DUAL OP. AMP	
12												
13						1	1700-0057	I.C.	U1	7912 KC or LM320K-12	REGULATOR -12V	TO-3
14						1	1700-0058	I.C.	U2	7812 KC or LM340K-12	REGULATOR +12V	TO-3
15												
16						1	1700-0068	I.C.	U3	7815 KC or LM340K-15	REGULATOR +15V	TO-3
17						2	3000-3300	RESISTOR	R13,38		330Ω 1/4W 5%	
18						4	3000-1001	RESISTOR	R3,42,43,44		1K 1/4W 5%	
19						2	3000-1006	RESISTOR	R17,23		10Ω 1/4W 5%	
20						2	3000-1003	RESISTOR	R6,36		100K 1/4W 5%	
21						2	3000-3000	RESISTOR	R41,45		300Ω 1/4W 5%	
22						1	3100-1781	RESISTOR	R4		1.78K, 1/8W, 1%	
23						1	3100-1581	RESISTOR	R32		1.58K, 1/8W, 1%	
24						2	3070-1000	RESISTOR	R8,19		100Ω 1W 5%	
25						2	3070-2200	RESISTOR	R18,40,		220Ω 1W 5%	
26						2	3070-1001	RESISTOR	R46, R47		1K, 1W, 5%	
27												
28						2	3300-0002	RES VAR	R2, 30		100Ω, 1T	
29						7	3100-2000	RESISTOR	R9,10,14,33, 34,48, 5		200Ω 1/8W 1%	
30						1	3100-4020	RESISTOR	R49		402Ω 1/8W 1%	
31						6	3100-6040	RESISTOR	R3,7,11,25,35,37		604Ω 1/8W 1%	
32						2	3200-0024	RESISTOR	R1, 39		2.4Ω 5 1/4W 10%	
33												
34						2	3000-5106	RESISTOR	R12,24		51Ω, 1/4W, 5%	
35						16	4000-0005	CAPACITOR	C1,3,5,8, 11,13,14 15,18,20,21,24,25,	27,28,32	.01 μf	
36												

Cont. Regulator Assembly 0112-0050

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
37						2	4000-0030	CAPACITOR	C 2,30		.002 µf, 600V 1KV	
38						5	4300-0025	CAPACITOR	C6,7,22,23,33	196D476X9006	47 µf/6V	
39						5	4300-0028	CAPACITOR	C10,12,16,19,31	196D107X9020	100 µf/20V	
40						2	4300-0033	CAPACITOR	C14,17	196D476X9035	47µf/35V	
41						1	3000-2200	RESISTOR	R50		220Ω, 1/4W, 5%	
42						5	6400-0039	L.E.D., RED	CR5,6,7,8,9	5082-4684		
43												
44						1	0112-0054	HEATSINK				
45							———	PANHEAD SCREW	heat sink to PWB		# 4-40	
46							———	PANHEAD SCREW	TO-3 mounting		#6-32	
47							———	FLAT WASHER	heat sink to PWB		#4	
48							———	KEPNUT	TO-3 mounting		#6	
49						1	7000-0120	EJECTOR				
50							———	FLAT WASHER	TO-3 mounting		#6 FLAT WASHER	
51							———	LOCKWASHER	heat sink to PWB		#4 INT. TOOTHED	
52						1	9000-0038	LABEL, CAUTION			"TURN POWER OFF BEFORE REMOVING BOARDS"	
53												
54												