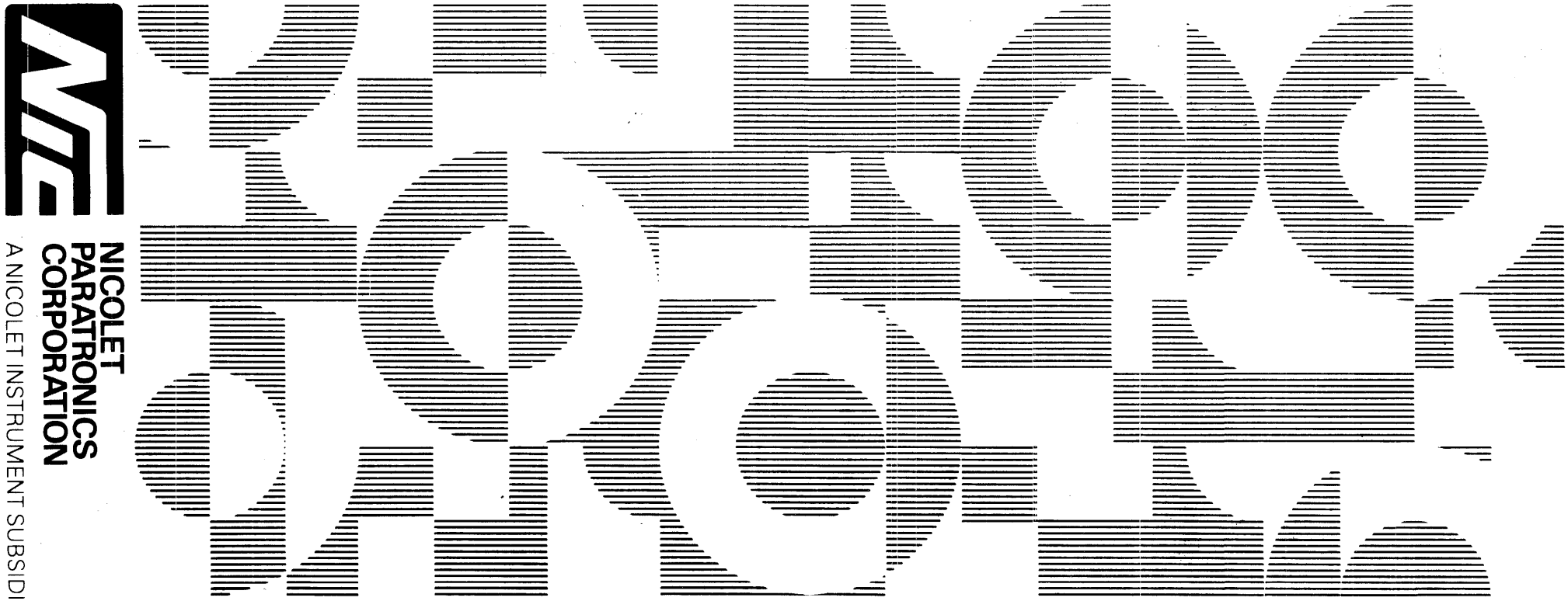
PI 540

Logic Analysis System

MAINTENANCE MANUAL



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1.0 INTRODUCTION

1.0 INTRODUCTION

The Paratronics PI 540 Logic Analysis System combines, in a single package, facilities for logic analysis of state, timing, and waveform information. Inputs are provided for 32 state channels, 8 timing (or additional state) channels, and 1 waveform channel. The state, timing, and waveform sections can be used independently as separate analyzers, or linked one to the other for interdependent triggering.

1.1 PRINCIPLES OF OPERATION

All three types of analyzers represented in the PI 540 are basically devices for collecting data under specified conditions and storing the data in memory for detailed examination. Data is stored in memory starting at the lowest address. If the memory is filled before data collection is terminated, storage starts at the beginning of memory again, writing over the data already there. Thus the memory always contains, at any given moment, the most recent memoryful of data. When data collection stops, in this overflow case the last address filled is treated as the "end" of memory, and the next address is treated as the "beginning" of memory for purposes of analysis.

To start data collection, the RESET key on the keyboard is pressed. When and if certain preestablished conditions (the trigger conditions) are met, the data collection is automatically halted by the analyzer. Or, it may be stipulated that the data collection continue for a brief period after the trigger event until a specified amount of posttrigger data has been collected. Once data collection has stopped, the data can be displayed in various ways for convenient analysis.

In the PI 540, each input channel (incoming data line) is, in effect, assigned its own strip of memory that is one bit wide and as long as the memory is deep (250 bits for the state memory and 1000 bits for the timing and waveform memory). There are 32 input channels in the state section, 8 more in the timing section, and 1 in the waveform section.

The varying data on the input channels is fed to IC latches where it is latched by clock pulses. At each clock pulse, a sample of the stabilized data is read from the latch into memory. The state and timing analyzers assume that data on the input channels is logic data; that is, that it is either TRUE or FALSE. If the input level is above a preselected threshold, the data is stored in memory as TRUE (logic 1); if below that threshold, it is stored as FALSE (logic 0).

For the State Analyzer, the TRUE or FALSE state of the data from bit to bit is the subject under investigation. Therefore, the clock pulses are taken from the system under test (the target system), are chosen so that the data of interest is stable at clock time, and are usually closely related to the master clock for that system. The source of clock pulses is external to the analyzer; and because the clock that is being fed to the analyzer's latches bears a fixed time relationship to the data being collected, the clocking is said to be synchronous.

For the Timing Analyzer, the subject under investigation is usually the time relationships of the transitions of logic data present on various data lines. The precision with which such data transitions (from TRUE to FALSE, or vice versa) can be located in relative time is a function of how often the data is sampled. Thus, the higher the frequency of the sampling clock, the higher the resolution of the timing information contained in the collected samples. The synchronous external clock used in the state mode is usually unsuitable for the timing mode because the transitions under examination are very often occuring at target-system clock intervals. Therefore, small time differences between transitions on the various incoming channels could be completely obscured if the target-system clock were used to sample the data.

Because of these considerations, an internal clock is provided from within the timing analyzer. This clock is asynchronous with respect to the incoming data. A maximum internal clock frequency of 50 MHz is available in the PI 540. However, slower internal clock rates may be selected in order to capture data over as long an interval of time as is consistent with the resolution required. (The lower the clock frequency, the longer the time interval represented by a 1000-bit memoryful of data samples.)

An external clock input is also provided on the timing analyzer, and external clocking may be selected if a suitable external clock is available and preferable for some reason. Furthermore, an alternate state-equivalent display is provided for the timing data. This alternate display, in conjunction with the external clock, allows the timing analyzer to be used as an 8-channel state analyzer with a 1000-word data collection memory.

For the Waveform Analyzer, the incoming data is no longer assumed to be logic data. The objective now is to capture and store a single-occurrance analog waveform so that it can later be continuously displayed for detailed analysis. As with the timing analyzer, high resolution is important, and the 50 MHz internal clock is used for data sampling. (Again, lower clock rates may be selected when some degree of resolution can be given up in exchange for a longer captured time interval.)

The voltage level on the waveform input channel is sampled at the selected clock rate, and the value of each sample is converted to digital form with 6-bit precision. The digital value of the sample is then stored in the 1000-word timing memory previously described. As with the state and timing analyzers, the occurrance of a designated trigger event stops the data collection after a preselected number of posttrigger samples. The captured waveform can then be displayed in selected ways under software control and with the aid of a special auxiliary video memory.

Aside from the state, timing, and waveform modes, the PI 540 has two broad operational modes; collection and display. While the analyzer is displaying data or a menu, it cannot collect data; and while it is collecting data it cannot display data or a menu. The analyzer enters the collection mode when the RESET key is pressed. At that time, any menu or data that was on the screen is replaced by the appropriate data format, but without data. While data is being collected, the only screen updating that occurs is the posting of short announcements of progress through the arm and trigger levels. When triggering occurs and any specified collection of posttrigger data is completed, or when the FORCE DISPLAY key is pressed, the analyzer stops data

collection and enters the display mode. It remains in the display mode, displaying either data or menus, until RESET is again pressed.

It should be mentioned that in the data display mode, only valid data is displayed. Valid data is data collected after the RESET key is pressed. This may or may not be a complete memoryful, depending on how soon triggering occurred and how much posttrigger data, if any, was specified.

1.2 OPERATIONAL FEATURES

A full-feature PI 540 may be configured from the keyboard to any of the following ten analyzer modes:

a. 8 STATE channels with 1000-word data capture
b. 16 STATE channels with 500-word data capture
c. 32 STATE channels with 250-word data capture
d. 40 STATE channels with 250-word data capture
e. 8 TIMING channels with 1000-sample data capture
f. 1 WAVEFORM channel with 1000-sample data capture
g. 16 500-word STATE channels + 8 1000-sample TIMING channels
h. 32 250-word STATE channels + 8 1000-sample TIMING channels
i. 16 500-word STATE channels + 1 1000-sample WAVEFORM channel
j. 32 250-word STATE channels + 1 1000-sample WAVEFORM channel

The 8-channel state mode is essentially the same as the 8-channel timing mode with the exception of the clock selection. In both modes (which are shown on the configuration menu as a single 8-channel tming/state dual mode) the data being displayed can be switched back and forth at will between the state and tming formats.

For 8-channel timing analysis, the clock will probably be selected as internal, and the Timing probe's clock and clock-qualifier inputs will not be connected to the system under test. (Clock qualification is not available when an internal clock is being used.)

When the 8-channel Timing Analyzer section is used as a state analyzer, the mode may be either an 8-channel mode, in which the Timing section is used by itself as a state analyzer, or it may be a 40-channel mode, in which the 8-channel Timing section is used in cascade with the 32-channel State section in a 40-channel state analyzer.

For 8-channel state analysis, the clock will probably be selected as external, and the Timing probe's clock input will be connected to the system under test in order to provide the external clock. The clock-qualifier input may also be connected if qualification of the clock signal is desired. But the qualifier signal cannot be applied to the arm or trigger words (as the State probe's qualifier signals can with the State section).

In the 40-channel state analysis mode, the 40-channel state analyzer is restricted to the more limited state analysis capabilities of the Timing Analyzer section. The clock will probably be selected as external, and the Timing probe's clock input will be connected to the system under test and will provide the external clock for both sections of the combined analyzer. (The

State section automatically receives the same clock selected for the Timing section.) The clock inputs of the two State probes cannot be used in the 40-channel mode and will not be connected. The two qualifier inputs on each of the two State probes can be used to qualify trigger words but cannot be used as clock qualifiers, and data-word clock qualification is not available. The clock-qualifier input of the Timing probe is the only clock qualifier that can be used. Keyboard control of the Timing probe's input threshold levels and hysteresis selection is still in effect.

In this 40-channel mode, only two levels of nested trigger words are available (called the arm word and trigger word in timing analysis) instead of the 16 levels that are ordinarily used in the State section. However, these two words are the full 40 bits long and can be qualified by the four State-probe qualifier bits and by the External and Waveform links. Also, the Timing section's delay functions can be applied. The memory depth is limited to the 250 words of the 32-channel State Analyzer.

Although these restrictions should be kept in mind for proper application, a 40-channel x 250-word state analyzer with a clock-qualifier bit and two levels of nested 40-bit trigger words with four qualifiers, two linkages, and a flexible delay function is nevertheless a very powerful instrument. It only seems limited in comparison with the unusually extensive features of the State Analyzer section.

Standard operational features, common to all modes unless otherwise noted, include:

a. Full keyboard control of system modes, display formats, and all variable parameters
b. Trigger and clock-qualifier linkage between state, timing, and waveform sections
c. Sixteen levels of nested triggering in state modes (except in the 40-channel mode, which has two levels)
d. Two levels of nested triggering in timing modes (called arm and trigger)
e. Extensive and varied trigger delay capabilities
f. Full data-width trigger words plus additional qualifiers
g. Extensive clock qualification in state modes (except 40-channel mode, which has one clock qualifier)
h. External input to trigger and clock-qualifier words
i. Glitch capturing in the timing mode
j. Comparison memories for various comparison functions
k. PI's brand of signature analysis
m. Fully controllable timing display (including channel order, movable expansion window, and equivalent-state format)
n. Controllable waveform display (including movable expansion window)
o. Selectable probe hysteresis and variable probe thresholds
p. State display formats interchangeable at will between hexadecimal, octal, binary, decimal, or ASCII

1.3 GENERAL DESCRIPTION

The physical configuration of the PI 540 is shown in figure 1-1. The four basic physical elements, as pointed out in the figure, are:

a. The Folding Keyboard
b. The Display Module
c. The Microcomputer Section
d. The Applications Section

The functional configuration of the PI 540 is shown in the block diagram of figure 1-2. Please refer to these two figures when appropriate during the following discussion. They are positioned at the end of the section for easy reference.

The FOLDING KEYBOARD, when not in use, folds up against the front of the case so that the face of the CRT and the keyboard working surface are both protected during transit or storage of the analyzer. (This arrangement also allows both the CRT and the keyboard itself to be larger than they could be if they shared the same front panel.) When the analyzer is placed horizontally on a bench or table, the carrying handle may be folded back underneath the unit to act as a stand. The keyboard is then unlatched from its protective position and folded down to rest on the table surface at a comfortable angle. In some situations, it may be more convenient to place the analyzer upright on the floor; there are four rubber feet on the back of the unit for this purpose, and the folded-under handle acts as a rest for the opened keyboard. (Caution: Take care that the cooling fan in the rear is not obstructed.)

The keys themselves are completely covered by a plastic overlay sheet which protects them from dust and other contamination and carries the key legends as well as other keyboard labels. The keys are of the thin, snap-action contact type, and at each key location there is a slight dome beneath the plastic overlay. This dome gives way when pressed, thus providing tactile feedback of the key actuation. An audio feedback tone is also provided (at the operator's option). If an illegal key entry is made during any operation, a dual-tone error signal is sounded.

The keys are connected as input devices to the microprocessor, and the function of each key is determined entirely by software. Many keys have two functions, one for each of two different analyzer operating modes in which the key may be called into play. Such keys have two legends on the keytop, one legend in green and one in red. Above the group of keys involved, a green or red light indicates which legend applies in the current operating mode.

Within the keyboard housing, but underneath the keyboard itself, is the Keyboard Interface Board. This circuit board contains: scanning circuitry that allows the microcomputer to periodically scan the keyboard for switch closures; latches that allow the microprocessor to control the LED indicator lights on the keyboard; and the audio tone generator and its drive and control circuits.

The DISPLAY MODULE contains a 9-inch CRT and the circuitry necessary to produce a raster scan. A composite video input signal is supplied from the Video Display Board in the Microcomputer Section. The only input power

required by the module is +12v, which is provided by the analyzer's power supply. High-voltage for the CRT is generated within the module by a circuit that operates from the +12 volts.

The MICROCOMPUTER SECTION is built up on the Microcomputer Motherboard. Mounted on the rear of this motherboard is a high-efficiency switching power supply that provides power for the entire PI 540. The remainder of the motherboard is equipped with card guides, sockets, and interconnections (the PI Standard Bus) for 8 circuit boards. Board locations are interchangeable on this motherboard, but typically, the circuit board complement is arranged as follows (top to bottom):

Slot	Circuit Board
1	Video Display Board
2	Processor Board
3	Extended Memory Board #1
4	Extended Memory Board #2
5—8	Available for options

The Video Display Board contains an LSI CRT controller (the Intel 8275), 1K bytes of screen-refresh RAM, a character-generator ROM, and various other related circuits. This board generates a composite video signal which, when sent to the Display Module, produces a memory mapped video display containing 16 rows of 64 alphanumeric characters, with each character occupying an 8 x 15 dot-matrix cell. In the timing display, line drawing is used in conjunction with the alphanumeric characters. (The waveform display, which also uses line drawing, is generated on another board, the Waveform Board, to be discussed later.)

The Processor Board contains an 8085 microprocessor, 4K bytes of program storage ROM, 256 bytes of system RAM, and various buffering circuits. This board, by means of the system Control Program, exercises control over all analyzer functions. These functions include keyboard input, CRT display formatting and updating, storage of collected data in memory, and implementation of all operational features.

Extended Memory Boards #1 and #2 provide additional program storage ROM and working RAM for the Processor Board. They are identical in their potential memory capacity of 24K bytes of ROM and 4K bytes of RAM per board. In the PI 540, #1 contains 12K bytes of ROM and 4K bytes of RAM, and #2 contains somewhat less, depending on the configuration of the particular instrument.

The remaining four board positions in the Microcomputer Section are available for optional circuit boards such as the Serial Interface and GPIB Interface boards.

The APPLICATIONS SECTION is built up on the Function Motherboard, which has card guides, sockets, and interconnections for 7 circuit boards. In effect, these circuit boards, in conjunction with the Control Program, define the functions of the analyzer. They are devoted primarily to signal conditioning circuits, functional control circuits, and data collection memory.

The Applications Section in a full-feature PI 540 contains the following circuit boards (listed from front to rear):

Slot	Circuit Board
G (Front)	Spare, for expansion
F	State Memory Board, B Group
E	State Control Board
D	State Memory Board, A Group
C	Timing Control Board
B	Timing Memory Board
A	Waveform Board

Circuit board locations on the Function Motherboard are not interchangeable. Therefore, the boards and sockets are keyed so that a board can only be inserted in its designated socket. (A partial exception is that State Memory Boards A and B are identical, and either board can be installed in either memory board slot, but not in any of the other slots.)

The two State Memory Boards, which are identical as just noted, each contain enough RAM to collect 250 bits of data from each of 16 state input channels. They also contain input data latches, RAM for trigger and qualifier word comparison (software implemented), and circuits for generating various control signals.

The State Control Board contains circuitry that controls the collection of the state data that is stored on the State Memory Boards. This board also implements (for the state analysis mode) clock qualification, the 16 levels of trigger words, and all delay functions.

The Timing Control Board contains circuitry that controls the collection of the timing data that is stored on the Timing Memory Board. This board also generates the internal clock used for collecting timing and waveform data. And, for the timing analysis mode, this board controls clock selection, and the trigger delay functions.

The Timing Memory Board contains a 1K-word x 8-bit RAM for storage of collected timing or waveform data. It also contains circuits that perform the glitch-capturing function, compare the incoming data with the arm and trigger words, and establish the voltage thresholds for the incoming timing channels.

The Waveform Board contains circuitry that samples data on the incomming waveform channel (using a clock signal obtained from the Timing Control Board) and converts the data samples to digital form. The digital data is stored in the memory on the Timing Memory Board. The Waveform Board also contains a 256 x 8-bit auxiliary video screen RAM. Once triggering has occurred, captured data is copied from the Timing Memory Board into this RAM in the course of the display manipulation that is under software and keyboard control. Circuitry on this board then converts the information in the auxiliary screen RAM into line-drawing video signals that are fed to the Video Display Board.

1.4 SELF-TESTS

The PI 540 provides several self-tests that can be useful in assessing the condition of the instrument. First, there is the automatic self-test that is performed every time power is turned on. Second, there is the series of self-tests that are evoked by holding down certain keyboard keys at the same time power is turned on. Third, there are the self-test probe ports on the back panel that are accessed through the Model 51A and Model 80 Probes by means of the Model 53 Self-Test Adaptors. Finally, there are the self-tests that can be performed with the Logic Analyzer Demo Card, Paratronics Inc. part number 143-0046-002.

1.4.1 Automatic Self-Test

The automatic self-test is performed during the first two seconds each time power is applied to the analyzer. This test goes through a set of performance checks of the PI 540 memories and other subsystems. All keyboard lights are lighted throughout the test to confirm their operation. The test also reads the power line frequency and sets the CRT vertical sync frequency to a matching 50 or 60 Hz. Although this automatic self-test does not provide an exhaustive check, it does offer a high confidence level that the analyzer is operating properly.

Successful completion of the test is announced by a short beep followed by a display of the Configuration Menu. If the test is not successful, the keyboard lights will remain on, there will be no beep, and there will be no display on the CRT. If the CRT vertical sync frequency cannot be set to approximate the power line frequency, a continuous beep will be emitted.

1.4.2 Keyboard Self-Tests

Each test in this series is initiated by holding down the specified key while turning the main power switch from OFF to ON, and keeping the key held down until the beep at the end of the automatic self-test is heard (about two seconds). At that point, the selected test begins. The available tests are as follows. (Unless otherwise noted, exit from the tests is made by pressing the CONFIG key.)

For the CRT Alignment Check, hold down the "0" key. This test is a fixed display of horizontal and vertical lines that are useful for evaluating and adjusting CRT alignment. (For details on using this test, refer to Display Module subsection 4.2.2.)

For the Keyboard Check, hold down the "1" key. This test can be used to check the performance of each key on the keyboard. To exit, turn off the power. (For details on using this test, refer to Keyboard subsection 3.2.)

For the Video-RAM and Character-Set Check, hold down the "2" key. This test verifies the integrity of the video refresh RAM and then uses the RAM to sequentially display a screenful of each character in the character set. To exit, turn off the power. (For details on this test, refer to Video Display Board subsection 5.4.)

For the Program ROM Signature Check, hold down the "X" key. This test performs a signature calculation on each program ROM. The CRT displays a tabulation of the ROM number, the starting address of the ROM, the correct signature, and the actual signature (which should, of course, match the correct one). If any signature is incorrect, it is displayed in reverse video.

Although, strictly speaking, the following items are not self-tests, they are given here because they are part of the series of key-hold-down-at-power-ON functions.

For the CRT V-Sync Frequency Override, hold down the "5" key or the "6" key. If the "5" key is held down, the CRT vertical sync frequency is set to 50 Hz. If the "6" key is held down, the setting is to 60 Hz. This setting is made after the Control Program's automatic setting and therefore remains in effect until power is turned OFF. (This function can be used to determine which of the two frequencies most closely matches the power mains frequency. For details, please refer to the Display Module subsection 4.2.1.)

For Key-press Tone Delete, hold down the "T" key. This turns OFF the beep tone that normally sounds when a key is pressed. The ERROR tone is not turned OFF. (If it is absolutely necessary for some reason, the ERROR tone can be turned OFF by setting the tone drive level to zero using variable resistor R1 on the Keyboard Interface Board. This requires disassembly of the keyboard. For details, please refer to the Keyboard section, 3.0.)

1.4.3 Self-Test Ports

There are two self-test ports located on the rear panel of the PI 540. One is labeled Data/Status, and the other is labeled Address. They consist of connectors which mate with the Model 53 Self-Test Adapters that attach to the Model 51A and Model 80 Probes. These ports provide access to the Processor Data Bus, certain status signals from the 8085 microprocessor, and the Processor Address Bus.

Either probe model can be connected (through a Model 53 Adapter) to either self-test port. The following tabulation lists, by channel number, the signals available to each of the probes from each of the self-test ports.

These signals can be used to investigate a certain aspect of the analyzer performance that is in question. Or they can be used to verify the overall performance of the analyzer by following the instructions given in section 6 of the Operator's Manual.

MODEL 51A CHANNEL	MODEL 80 CHANNEL	SELF-TEST PORTS DATA/STATUS	ADDRESS
0	0	A0	DB0
1		A1	DB1
2	1	A2	DB2
3		A3	DB3
4	2	A4	DB4
5		A5	DB5
6	3	A6	DB6
7		A7	DB7
8	4	A8	SO
9		A9	S1
10	5	A10	IO+/M-
11		A11	INTA-
12	6	A12	SID
13		A13	SOD
14	7	A14	GND
15		A15	GND
QTRIG (Q2)	QCLK	RD-	IO+/M-
QCLK (Q1)		IO+/M-	RD-
CLK	CLK	RW	RW

1.4.4 The Logic Analyzer Demo Card

The Paratronics Logic Analyzer Demo Card, Part Number 143-0046-002, can be used to perform a comprehensive performance test of the PI 540 Logic Analysis System. A suitable procedure is given in the following paragraphs. All steps necessary for a comprehensive evaluation are presented, including some that do not require the Demo Card.

(This procedure assumes some familiarity with the operation of the PI 540 Analyzer. If necessary, please refer to the Operator's Manual, particularly to section 6.)

a. Disconnect the power cord from the analyzer and visually inspect the power fuse and voltage card to determine that they are correctly installed for the current application. (For further details, please refer to the discussion of the Mains Module in the Chasis section, 2.1.) Reconnect the power cord.

b. To check the automatic CRT vertical sync setting, use the "5"-key and "6"-key power-ON-hold-down functions to determine that the automatic setting is the one that produces the least mains-frequency interference with the CRT display. (For details, please refer to the Display Module subsection 4.2.1.)

c. To evaluate the Display Module, turn the power ON while holding down the "0" key. Appraise the resulting CRT test pattern using the criteria presented in Display Module subsection 4.2.3, steps 5 through 10. If adjustments are needed, make them in accordance with the WARNING and instructions in the same subsection.

d. To verify the contents of the program ROMs, turn the power ON while holding down the "X" key. (For details, please refer to preceding subsection 1.4.2.)

To evaluate the State Analyzer section, connect two Model 51A Probes to the analyzer. Connect the A and B probe pods to edge connectors A and B, respectively, on the Logic Analyzer Demo Card. Set the probe Data Select switches to TRUE and the probe Threshold Select switches to TTL. Turn the analyzer power ON and proceed as follows:

e. Select the 32-CHANNEL STATE configuration and set up the menu as shown below.

```
                    32 CHANNEL STATE MENU

 DISPLAY FORMAT:  AAAAAAAA AAAAAAAA BBBBBBBB BBBBBBBB
           A HEX  B HEX
 CLOCK SELECT:    A CHNL: 1   B CHNL: A    QUALIFIERS: -AABB ET
 CLOCK QUAL:  0040 0000 -0XXX X
           OR 000X XXXX -XX0X X
 PRE-TRIG MEMORY (0-249): 000 WORDS
 RESTART:  OFF
 TRIGGER:
0         0040 0000 -XXXX XX
END
```

f. Test the Signature function by pressing RESET. When the STATE display appears, the signature should be 0D10 0A90.

g. Test the Format function by pressing, in turn, the ASC, BIN, OCT, DEC, and HEX keys. Choose one of the data lines and confirm that the displays on that line are correct. (Start with the ASC display and scroll to a line that has all standard ASCII characters. Then switch to BIN, write down the bits, and work from there. Realize that DEC does not assume BCD, but uses straight binary conversion of the eight bits in the block. Also, OCT assumes a ninth MSB of 0 in each block.)

h. Test the Location function as follows: Press the LOC key and then the E (End) key. The memory location of the display window should change from 000 at the top of the screen to +243 at the top of the screen, and the reverse-video LOC field should contain +243. Press LOC again, then B (Bottom). The memory location should return to 000 (which is Bottom in this setup because PRE-TRIG is 000).

i. Test the Scrolling function as follows: Press and release the key marked with the green up-arrow. The display should step up one memory location. Hold down the up-arrow key for two seconds, then release. The data should scroll up continuously. Stop the scrolling by pressing either the up- or down-arrow key. Repeat these steps using the down-arrow key. The action should be similar, but down.

j. Test the Repeat function by holding down the RESET key for two seconds. The data collection should reset repeatedly at a rate of about once per second. The signature should remain constant at the value 0D10 0A90. Exit from Repeat by pressing the STATE key. Press RESET once and check the signature again.

To test the Hold-if-Not-Equal function, perform the following steps k through s.

k. Press SAVE, then press ALT. The words MAIN and AUX should appear alternately about once per second at the upper left of the screen. The data should remain constant. (The data saved in AUX memory is the same as the data in MAIN memory.)

m. Press MAIN to stop the alternating, then press HOLD ≠. The data should disappear from the screen and the flashing word SAMPLING should appear. (The analyzer does not trigger because the data being sampled is equal to the data that was saved.)

n. On the Logic Analyzer Demo Card, install a short to ground on the A-channel bit 0. (Leave this short installed until otherwise instructed.) At the instant the short is made, the analyzer should trigger, and data and the flashing word HOLDING should appear on the screen.

o. Press the DIFF key. Data words in the display that are the same as the saved data should drop back to half intensity; data words that are different should remain at full brightness.

p. Press LOC, then D (Difference). Each time LOC and D are pressed, the data should scroll up so that the next different (full-brightness) word is at the top of the screen.

q. On the Logic Analyzer Demo Card, remove the short to ground from A-channel bit 0 and install it on B-channel bit 7. (Leave this short installed until otherwise instructed.)

r. Press HOLD ≠. The analyzer should retrigger and flash the word HOLDING. (Saved data is still in the AUX memory from step k.)

s. Move the data so that there are both half- and full-intensity data words on the screen. Press ALT. The full-intensity (different) words should alternate back and forth between their MAIN and AUX values; the half-intensity words should not change.

To test the Restart and Restart- functions, perform the following steps t through y.

t. Connect a Model 80 Probe to the Timing input of the analyzer, and connect the Timing pod to the B connector of the Demo Card in place of the B State pod. (Leave the B State probe connected to the analyzer but disconnected from the Demo Card.)

u. Select the 32 CHNL STATE/8 CHNL TIMING configuration and set up the STATE menu as follows:

```
                    32 CHANNEL STATE MENU

 DISPLAY FORMAT:  AAAAAAAA AAAAAAAA BBBCCDDD DEEEEEEE
          A HEX  B OCT  C DEC  D BIN  E ASC
 CLOCK SELECT:   A CHNL:     B CHNL: A    QUALIFIERS: -AABB ET
 CLOCK QUAL:  OFF
          OR OFF
 PRE-TRIG MEMORY (0-249): 010 WORDS
 RESTART:  OFF
 TRIGGER:
0        0040 X X XXXX XX -XXXX XX
1 THEN   0041 X X XXXX XX -XXXX XX          ON 0257 CLOCKS
2 THEN   0042 X X XXXX XX -XXXX XX       BEFORE 0002 CLOCKS
3 THEN   0043 X X XXXX XX -XXXX XX        AFTER 1000 CLOCKS
4 THEN   0044 X X XXXX XX -XXXX XX       OCCURS 0020 TIMES
5 THEN   0045 X X XXXX XX -XXXX XX       NOT ON 0002 CLOCKS
END
```

v. Press the RESET key. The signature of the collected data should be 083D 0A07.

w. Return to the STATE menu and set up the RESTART word as follows:

```
RESTART:  XXXX 0 X XXXX   -XXXX XX
```

x. Press the RESET key. The analyzer should not trigger, and the stack level should remain at 0 (announced on the display).

y. Return to the STATE menu and select RESTART- (the .NOT. function of RESTART). Press RESET. The analyzer should now trigger and the data signature should be 083D 0A07 (the same as in step v).

To evaluate the Timing Analyzer section, select the TIMING menu (still in the 32 CHNL STATE/8 CHNL TIMING configuration) and set up the parameters as shown in the following display. Then perform the remaining steps.

```
                    8 CHNL TIMING/STATE MENU

            EXT  CLOCK    CLK QUAL: 0
TRIGGER WHEN
              TRIG OCCURS _ 0100 CLOCKS AFTER FIRST ARM
                        CHNL NO. 76543210   FILTER  LINKAGE
       ARM (0,1,X):              10000000   OFF     S
       TRIG (0,1,X):             11011000   OFF     NONE
       INPUT MODE (S,L):         SSSSSSSS
       PRE-TRIGGER (0-9): 10%

       DISPLAY ORDER (0-7,X):    76543210
       DISPLAY POLARITY (+,-):   ++++++++
       THRESHOLD:     CH 0-3,Q,CK    CH 4-7      HYSTERESIS
  (-6.4V - +6.35V)      +1.60          +1.60         ON
```

z. Press RESET to obtain a data display. Then, by pressing the appropriate keys, test the left/right motions and position read-outs of: the cursor, the expansion indicator, and the display window.

aa. To test the Expansion function, press in turn X2, X5, X10, and X20. The data in the display window (that is, the data on the screen) should expand accordingly. The location in memory of the expanded data should be marked by a reverse-video block on the display's time scale. (NOTE: The selected magnification will always be used for the entire display window. The left boundry of the expanded window will fall at the expansion indicator provided the right boundry would not thereby extend past location 1000. Otherwise, the right boundry of the expanded window will fall at location 1000 and the window will extend to the left as necessary.)

ab. Test the Arm, Trigger, and Delay functions as follows: Position the cursor at location 000 (clocks, words). The data read-out (just to the right of the data lines) for location 000 should be the arm word, or 80. (This is because the arm word is 100 clocks before the trigger word, and with pretrigger at 10% x 1000 words, the trigger word is at 100.) Move the cursor to location 100. The data read-out should be the trigger word, or D8.

ac. Test the Correlation function as follows: Press the SAVE key, then the COR key. The correlation figure displayed at the right of each channel should be 1.000 for all eight channels.

On the Demo Card, remove the short to ground from B-channel bit 7 and install it on B-channel bit 5.

Press RESET, then COR. The correlation figures on three of the channels should change as follows:

Channel 3, 0.504
Channel 4, 0.760
Channel 5, 0.504

ad. Test the Alternate function by pressing the ALT key. The data in channels 3, 4, and 5 should change as the display alternates back and forth between MAIN and AUX.

ae. To test the Arm, Trigger, and Delay functions with internal clock, return to the Timing menu and change CLOCK and PRE-TRIGGER to

1mS CLOCK
PRE-TRIGGER: 20%

Press RESET. Under these menu conditions, the data read-out at cursor position 100 should be the arm word, 80; and the data read-out at cursor position 200 should be the trigger word, D8.

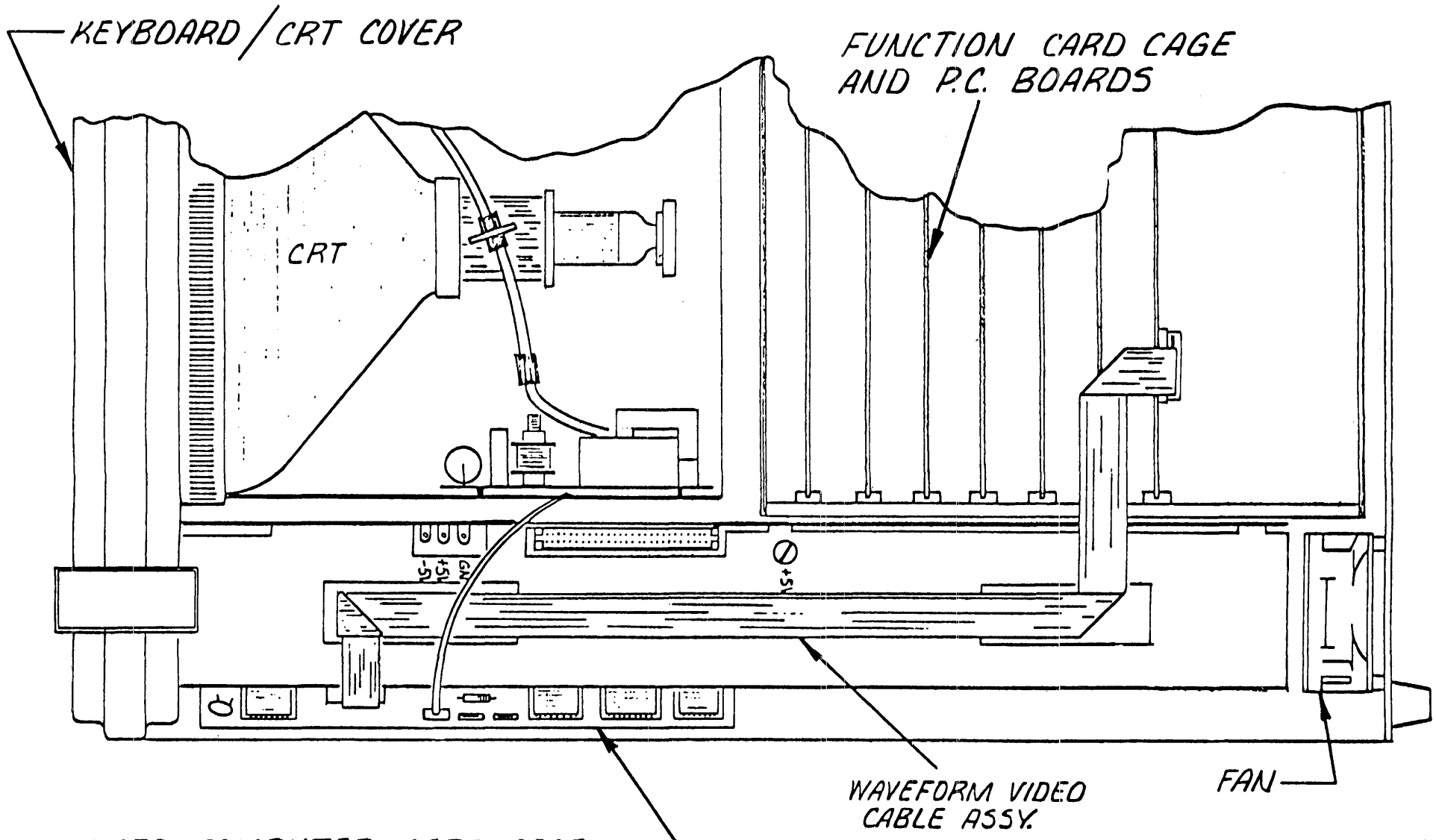
af. To test the Timing Linkage function, return to the Timing menu and change the delay and the ARM LINKAGE to

TRIG OCCURS ≥ 2500 CLOCKS AFTER FIRST ARM
. . . . . LINKAGE
ARM . . . . NONE

Return to the State menu. As shown below, add a Timing link to the trigger word in the 5th trigger level.

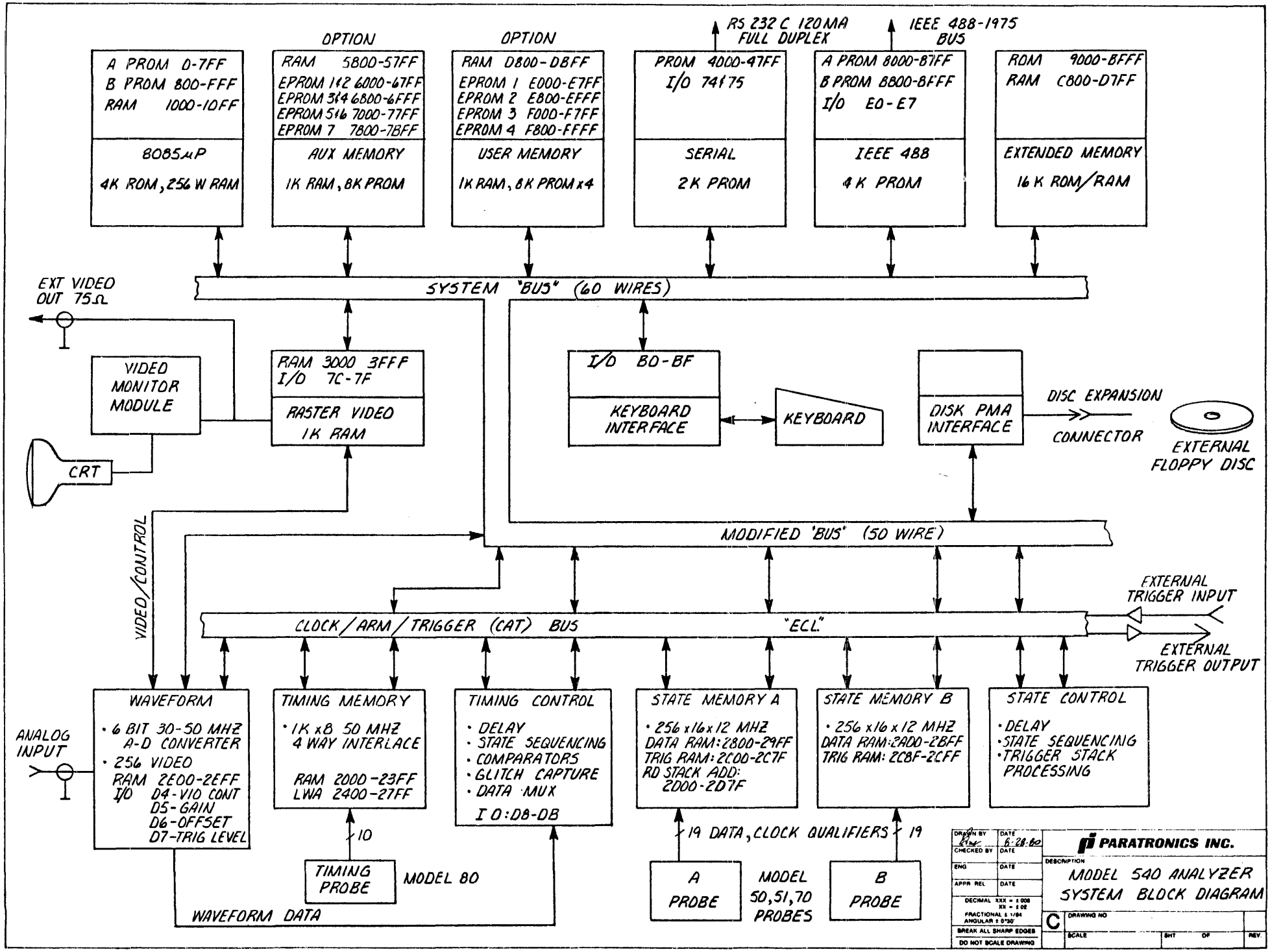
TRIGGER:
. . . . . .
. . . . . .
. . . . . .
5 THEN . . . . . -XXXX X1 . . . . . .

Press RESET. Because of the time delay set into the Timing menu and the Timing linkage set into the State trigger-level 5, the progress announcements at the bottom of the State display should make evident a 2.5-second delay at STATE: STACK LEVEL 5. (There should also be a 1-second delay at level 3 as specified in the State menu.)



REV	DESCRIPTION	DATE	APPROVED

DRAWN BY [illegible]	DATE 9-3-80	PARATRONICS INC.
CHECKED BY KBP	DATE 9-3-80	DESCRIPTION: M540 PHYSICAL CONFIGURATION
ENG	DATE	
APPR REL	DATE	
DECIMAL .XXX = ±.005 .XX = ±.02 FRACTIONAL ± 1/64 ANGULAR ± 0°30' BREAK ALL SHARP EDGES DO NOT SCALE DRAWING	A	DRAWING NO. 146-0004-001 SCALE NONE SHT 1 OF 1 REV


A PROM 0-7FF
B PROM 800-FFF
RAM 1000-10FF
8085 μP
4K ROM, 256 W RAM
OPTION
RAM 5800-57FF
EPROM 1&2 6000-67FF
EPROM 3&4 6800-6FFF
EPROM 5&6 7000-77FF
EPROM 7 7800-7BFF
AUX MEMORY
1K RAM, 8K PROM
OPTION
RAM D800-DBFF
EPROM 1 E000-E7FF
EPROM 2 E800-EFFF
EPROM 3 F000-F7FF
EPROM 4 F800-FFFF
USER MEMORY
1K RAM, 8K PROM x4
RS 232 C 120MA FULL DUPLEX
PROM 4000-47FF
I/O 74175
SERIAL
2K PROM
IEEE 488-1975 BUS
A PROM 8000-87FF
B PROM 8800-8FFF
I/O E0-E7
IEEE 488
4K PROM
ROM 9000-BFFF
RAM C800-D7FF
EXTENDED MEMORY
16K ROM/RAM
EXT VIDEO OUT 75Ω
SYSTEM "BUS" (60 WIRES)
VIDEO MONITOR MODULE
RAM 3000 3FFF
I/O 7C-7F
RASTER VIDEO 1K RAM
I/O B0-BF
KEYBOARD INTERFACE
KEYBOARD
DISK PMA INTERFACE
DISC EXPANSION CONNECTOR
EXTERNAL FLOPPY DISC
CRT
VIDEO/CONTROL
MODIFIED 'BUS' (50 WIRE)
EXTERNAL TRIGGER INPUT
CLOCK/ARM/TRIGGER (CAT) BUS "ECL"
EXTERNAL TRIGGER OUTPUT
WAVEFORM
• 6 BIT 30-50 MHZ A-D CONVERTER
• 256 VIDEO RAM 2E00-2EFF
I/O D4-VIO CONT
D5-GAIN
D6-OFFSET
D7-TRIG LEVEL
ANALOG INPUT
TIMING MEMORY
• 1K x 8 50 MHZ 4 WAY INTERLACE
RAM 2000-23FF
LWA 2400-27FF
TIMING CONTROL
• DELAY
• STATE SEQUENCING
• COMPARATORS
• GLITCH CAPTURE
• DATA MUX
I O: D8-DB
STATE MEMORY A
• 256 x 16 x 12 MHZ
DATA RAM: 2800-29FF
TRIG RAM: 2C00-2C7F
RD STACK ADD: 2D00-2D7F
STATE MEMORY B
• 256 x 16 x 12 MHZ
DATA RAM: 2A00-2BFF
TRIG RAM: 2C8F-2CFF
STATE CONTROL
• DELAY
• STATE SEQUENCING
• TRIGGER STACK PROCESSING
10
TIMING PROBE
MODEL 80
WAVEFORM DATA
19 DATA, CLOCK QUALIFIERS 19
A PROBE
MODEL 50, 51, 70 PROBES
B PROBE
PARATRONICS INC.
MODEL 540 ANALYZER SYSTEM BLOCK DIAGRAM
DRAWN BY
CHECKED BY
ENG
APPR REL
DATE
6-28-80
DECIMAL XXX = ± .008 XX = ± .02
FRACTIONAL ± 1/64
ANGULAR ± 0°30'
BREAK ALL SHARP EDGES
DO NOT SCALE DRAWING
DRAWING NO
SCALE
SHT
OF
REV.

2.0 CHASSIS, MOTHERBOARDS, AND POWER SUPPLY

2.1.0 CHASSIS

2.1.1 INTRODUCTION

The chassis provides a strong supporting structure for attachment of the Folding Keyboard, the Display Module, the Microcomputer subassembly, and the Applications subassembly. The cover, which is considered a part of the chassis, encloses the top and two sides, giving complete protection to the inner components and adding to the structural strength of the completed assembly.

2.1.2 FUNCTIONAL DESCRIPTION

When appropriate during the following discussion, please refer to the drawings, interconnection diagram, and parts list that are included at the end of this section. Also, tables of connector pins versus signal names for all motherboard connectors are provided in section 15 along with an alphabetical list of all interboard signals. And, should the need arise, a Glossary in section 16 offers explanations for acronyms or terms that may be unfamiliar.

The units that will be discussed as part of the chassis group are the chassis itself, the cover, the carrying handle, the Mains Module, the cooling fan, the auxiliary power transformer, and the interconnecting wiring.

The Chassis consists of a heavy guage aluminum bottom plate bent up at a right angle at the rear to form an integral back plate. The front of the bottom plate is attached to a heavy cast-aluminum front plate. The upper corners of the front plate are joined to those of the back plate by longitudinal tie rods of 3/8 diameter aluminum. There is a large rectangular hole in the front plate through which the CRT screen is viewed. A plastic face plate is inset into the front plate and covers the entire front surface. This face plate protects the CRT and is lightly tinted to enhance the contrast of the CRT display. The main power switch is attached to the rear of the front plate, and its handle extends through a hole in the front plate and face plate.

The Folding Keyboard attaches by hinges to the bottom edge of the front plate. The Keyboard folds up against the front plate and is secured by two latches that are attached to the top edge of the front plate.

The Display Module is mounted to the bottom plate by four threaded studs set into the bottom plate. The Microcomputer subassembly is mounted to the bottom plate by five flathead screws through the bottom plate. The Applications subassembly is mounted to the bottom plate by four screws into short threaded spacers set into the bottom plate.

The cooling fan fastens to the back plate by four screws through the back plate. The auxiliary power transformer fastens to the back plate by two threaded studs set into the back plate. The Mains Module mounts into a rectangular hole in the back plate with snap-in fasteners. The BNC connector for external video output mounts in a hole in the back plate. When present, connectors for the optional serial and GPIB interfaces mount into rectangular holes in the back plate with screws through the back plate. There are seven round clearance holes in the back plate through which BNC connectors, mounted

on the Applications subassembly, extend. There is also a rectangular clearance hole in the back plate through which a 50-pin ribbon connector extends when present. This connector is for interface expansion and mounts on the Applications subassembly.

WARNING: DISCONNECT THE AC POWER CORD AT THE BACK OF THE CHASSIS BEFORE REMOVING THE COVER. THE DISPLAY MODULE CONTAINS A VERY HIGH VOLTAGE OF 9 kV WHICH CAN BE LETHAL. EXTREME CAUTION MUST BE USED WHENEVER POWER IS APPLIED TO THE PI 540 WITH THE COVER REMOVED.

The cover folds around the top and two sides of the instrument. It overhangs the back plate 1/4 inch and fits into a 3/8-inch recess in the front plate. The bottom edges bend around underneath the bottom plate on each side and overlap it by 3/4 inch. The cover is held in place by six screws, three on each side, that pass through holes in these overlapping flanges and the bottom plate and thread into captive nuts on the inside surface of the bottom plate. There are vent slots in strategic places in the sides of the cover for fan air intake. There is a larger slot in the side of the cover that provides access to the Probe connectors on the Applications subassembly.

The carrying handle attaches by pivot pins to the side edges of the front plate. When the analyzer is in use, the handle can be folded back underneath the bottom plate to act as a stand. This props up the front of the instrument so the keyboard rests at a convenient working angle.

The Mains Module (please refer to figure 2.1-1 and to the chassis wiring diagram) is mounted into a rectangular cutout in the back plate and held in place by snap-in fasteners attached to the sides of the Module.

A voltage card in the Mains Module is used to select the power mains voltage with which the instrument is to be supplied. (The sliding cover for this voltage card can only be opened when the power cord is unplugged from the Module.) Voltage designations are etched in copper near the edges of the voltage card. The voltage designation that is visible on the upper rear edge of the card when it is in place is the voltage for which the instrument is programmed.

WARNING: BEFORE APPLYING POWER TO THE PI 540, MAKE CERTAIN THAT THE PROGRAMMED MAINS VOLTAGE CORRESPONDS TO THE VOLTAGE BEING USED. OTHERWISE SERIOUS DAMAGE TO THE INTERNAL POWER SUPPLY MAY RESULT.

To change the voltage programmed, remove the card, change its orientation, and reinsert it. The voltages available for selection are:

Voltage Programmed	Nominal Mains Voltage	Nominal Mains Frequency
100 V ac	95—110 V ac	50 or 60 Hz
115 V ac	110—120 V ac	50 or 60 Hz
230 V ac	220—240 V ac	50 or 60 Hz

The power-mains fuse is located in the Mains Module just above the voltage card. The rating of the fuse depends on the voltage programmed. The required fuse ratings are as follows:

Programmed Mains Voltage	Fuse Rating
100 or 115 V	3 A, 250 V
230 V	1.5 A, 250 V

The auxiliary transformer is mounted by threaded studs set into the back plate just above the Mains Module. The primary of this transformer acts as an autotransformer to supply a nominal 115 V ac to the fan motor regardless of the programmed mains voltage. The secondary supplies a nominal 17 V ac (also regardless of programmed mains voltage) to the Power Supply for an auxiliary supply circuit.

The cooling fan is mounted in a 3-inch square hole in the back plate and is supplied with 115 V ac power from the auxiliary transformer. There are air vent slots in the cover; one group beside the front of the Microcomputer subassembly and one group beside the Applications subassembly. The fan draws air in through these vent slots and exhausts it from the fan mounting hole. This air flow lowers operating temperatures within the cabinet to safe levels.

WARNING: IF THE FAN IS NOT FUNCTIONING, DO NOT OPERATE THE PI 540 WITH THE COVER ON. DOING SO MAY RESULT IN SERIOUS DAMAGE TO COMPONENTS THROUGHOUT THE INSTRUMENT. HOWEVER, EXTREME CAUTION MUST BE USED WHEN OPERATING THE PI 540 WITHOUT THE COVER BECAUSE OF LETHAL HIGH VOLTAGE USED IN THE DISPLAY MODULE. SUCH OPERATION SHOULD ONLY BE UNDERTAKEN BY EXPERIENCED MAINTENANCE PERSONNEL FOR MAINTENANCE PURPOSES.

The interconnecting wiring is shown in the wiring diagram at the end of this section. All interconnections to the Display Module, Microcomputer subassembly, and Application subassembly are made through connectors, so any of these units can be removed without unsoldering wires.

2.1.3 DRAWINGS, DIAGRAMS, & PARTS LIST

Drawings, diagrams, and parts list for the Chassis are contained on the following pages.

2.2.0 MOTHERBOARDS

2.2.1 INTRODUCTION

There are two motherboards in the PI 540; the Microcomputer Motherboard and the Function Motherboard. These motherboards are relatively large printed circuit boards which contain sockets, card guides, and supporting structure for the numerous individual PC boards that constitute the analyzer.

2.2.2 FUNCTIONAL DESCRIPTION

When appropriate during the following discussion, please refer to the schematic diagrams, board layouts, and parts lists which are included at the end of this section. Also, tables of connector pins versus signal names for all motherboard connectors are provided in section 15 along with an alphabetical list of interboard signals. And, should the need arise, a Glossary in section 16 offers explanations for acronyms or terms that may be unfamiliar.

The two motherboards will be discussed separately in the following subsections. Also, the Power Supply, whose PC board is an integral part of the Microcomputer Motherboard but whose function is entirely separate, will be discussed separately in section 2.3.

2.2.2.1 Microcomputer Motherboard

The Microcomputer Motherboard contains sockets, card guides, and interconnections for eight circuit boards. Four of these board positions are available for optional PC boards such as the Serial Interface Board and the GPIB Interface Board. The remaining four positions are occupied by four PC boards that constitute the Microcomputer Section of the analyzer.

The slot assignments for individual PC boards are interchangeable on this motherboard. But typically, the board complement is arranged as follows (with slot 1 at the top of the motherboard):

Slot	Circuit Board
1	Video Display Board
2	Processor Board
3	Extended Memory Board #1
4	Extended Memory Board #2
5—8	(available for options)

The PC board sockets and card guides are located on the forward 2/3 of the motherboard. The rear 1/3 is occupied by the Power Supply, which is discussed in section 2.3. Some forward motherboard area not occupied by sockets and wiring is allocated to the Power Supply overvoltage protection circuits. The components (Q6, Q7, and the other items grouped around them) are shown on the board layout drawing. The circuits are shown on the Power Supply schematic and discussed in the Power Supply section, 2.3. Also, Power

Supply test points TP6, 7, and 8 are placed at the top edge of the forward part of the board.

Some additional area in the forward part of the board is allocated to driver circuits for the keyboard connecting cable. The components are U3, U4, U5, and C36, shown on the board layout drawing. This circuitry is shown on the motherboard schematic but is discussed in the Keyboard section, 3. The signals that must be sent to the Keyboard are fed to a connector near the front edge of the board. This connector mates with another on a flat ribbon cable that comes from the Keyboard.

The PC board sockets are interconnected in an arrangement called the PI Standard Bus (shown in the schematic and used in other PI instruments as well as the PI 540). Signals that must be sent to the Function Motherboard are fed to a connector near the top edge of the Microcomputer Motherboard. This connector mates with another on a flat ribbon cable that interconnects the two motherboards.

The motherboard is supported by a sheet metal shell which includes a vented case that completely encloses the component side of the Power Supply portion of the board. The noncomponent side of the Power Supply portion of the board is protected by a sheet of plastic mounted on short plastic spacers. The sheet metal shell fastens to the chassis bottom plate with five flathead screws through the bottom plate. (Instructions for dismounting this motherboard subassembly from the chassis bottom plate are given in the Power Supply section, 2.3.)

2.2.2.2 Function Motherboard

The Function Motherboard contains sockets (two per circuit board), card guides, and interconnections for seven circuit boards. One of these board positions is available for future expansion. The remaining six positions are occupied by six PC boards that constitute the analyzer's Applications Section. These six circuit boards, in conjunction with the Control Program, define the functions of the analyzer.

The slot assignments for individual PC boards are not interchangeable on this motherboard. One socket in each socket pair is keyed so that only the correct circuit board can be inserted. The Applications Section of a full-feature PI 540 contains the following circuit boards (listed front to rear):

	Slot	Circuit Board
(Front)	G	(for expansion)
	F	State Memory Board B
	E	State Control Board
	D	State Memory Board A
	C	Timing Control Board
	B	Timing Memory Board
	A	Waveform Board

Two sheet metal end plates, as wide as the motherboard and extending upward to the height of the inserted circuit boards, are fastened to the motherboard at front and rear. Two cross pieces on each side, running fore and aft, are attached to the end plates and support the card guides. The result is a rigid card-cage assembly.

Seven BNC female connectors are mounted on the rear end plate and extend through clearance holes in the chassis back plate. One of these connectors is a spare, and the remaining six are for the following signals:

Timing Comparator Out
State Comparator Out
Timing Trigger Out
State Trigger Out
External Trigger In
Waveform Probe In

Driver circuits for the two Comparator outputs and a pullup resistor for the External Trigger input are located near the rear edge of the motherboard. These components are shown on the board layout drawing and on the schematic. If the analyzer is equipped with an expansion interface, the 50-pin ribbon connector for that interface is also mounted on the rear end plate and extends through a clearance hole in the chassis back plate.

There are several round clearance holes in the front end plate that, when the Applications circuit boards are removed, provide access to maintenance adjustments on the Display Module.

The Function Motherboard subassembly fastens to the chassis bottom plate with four screws into short threaded spacers set into the bottom plate.

2.2.3 SCHEMATICS, BOARD LAYOUTS, & PARTS LISTS

The schematic diagrams, board layouts, and parts lists for the motherboards are contained on the following pages.

2.3.0 POWER SUPPLY

2.3.1 INTRODUCTION

The Power Supply is an integral part of the Power Supply Motherboard and occupies the rear 1/3 of the board area, directly behind the Microcomputer Section. The Power Supply is a pulse-width modulated, half-bridge, 20 kHz switching circuit operating directly off the ac power line. It supplies ±5 V and ±15 V to the Keyboard, Applications, and Microcomputer Sections, and it supplies +12 V to the Display Module. Also, it provides very effective overvoltage and overcurrent protection for both the Power Supply itself and the circuits that it supplies.

2.3.2 FUNCTIONAL DESCRIPTION

When appropriate during the following discussion, please refer to the schematic diagram, board layout, and parts list which are included at the end of this section. Also, tables of connector pins versus signal names for all motherboard connectors are provided in section 15 along with an alphabetical list of all interboard signals. And, should the need arise, a Glossary in section 16 offers explanations for acronyms or terms that may be unfamiliar.

As shown on the schematic diagram, the major functional units of the Power Supply circuit are the High Voltage Section, Control Section, and Output Section. These units are discussed further in the following subsections.

WARNING: THIS POWER SUPPLY CIRCUIT IS CONNECTED DIRECTLY TO THE AC MAINS WITH NO INTERVENING ISOLATION TRANSFORMER. IT CONTAINS LETHAL VOLTAGES AND ENERGY STORAGE UNITS. ONLY QUALIFIED SERVICE PERSONNEL FAMILIAR WITH LINE-OPERATED SWITCHING POWER SUPPLIES SHOULD UNDERTAKE SERVICE OF THIS SUPPLY, AND THEN ONLY WITH THE ISOLATING TEST SETUP DESCRIBED IN THE FOLLOWING SUBSECTION, 2.3.2.1. FAILURE TO OBSERVE THESE PRECAUTIONS MAY RESULT IN SERIOUS INJURY OR DEATH.

2.3.2.1 Test Setup

The 110 or 220 Vac input power is fed directly from the mains to the CR19 rectifier circuit without an intervening isolation transformer. Therefore, before any test equipment is connected to the High Voltage Section, it is essential that an isolation transformer be incorporated in the test setup as shown in figure 2.3-1 which is in subsection 2.3.3.

WARNING: MEASUREMENTS OR TESTS UNDERTAKEN WITHOUT THE USE OF AN ISOLATION TRANSFORMER AS SHOWN IN FIGURE 2.3-1 MAY RESULT IN EXTENSIVE DAMAGE TO EQUIPMENT OR SERIOUS INJURY OR DEATH TO PERSONNEL.

To gain access to the Power Supply and prepare it for service, proceed as follows (please read the entire procedure once before taking action):

a. Disconnect the power cord.

b. Close and latch the keyboard. Stand the analyzer on the keyboard end and remove the cover. Return the analyzer to the horizontal position.

c. At the Video Display Board, disconnect the video cable to the Display Module, and, if installed, disconnect the flat cable to the Waveform Board. Remove the holddown bar and all the circuit boards from the Microcomputer Section

d. Disconnect the 50-conductor flat cable from the top of the Microcomputer Motherboard. Disconnect plug P12 in the 2-conductor cable running from the rear of the Power Supply to the Display Module.

e. Remove the three rear circuit boards from the Applications Section for later access to the P9 power supply plug connected to the rear of the Function Motherboard.

f. Stand the analyzer on its rear feet and remove the five flathead screws that hold the Microcomputer Motherboard subassembly to the analyzer bottom plate. While giving support to the loosened subassembly, return the analyzer to the horizontal position.

g. Being careful of the keyboard cable still connected to the front of the motherboard, swing the subassembly slightly outward at the rear to gain access to P9 on the Function Motherboard and P13 in the small cable to the Mains Module. Disconnect these two plugs.

h. Swing the subassembly out a little more and slightly to the rear, and disconnect the keyboard flat cable. Move the subassembly clear of the analyzer and place it bottom-up on the work bench.

i. Remove the white plastic cover from the Power Supply end of the motherboard, being careful to save the four screws and plastic spacers that held the cover away from the board.

j. The entire sheet metal structure is spotwelded together and comes off as one piece. Remove the remaining four screws holding the motherboard to the sheet metal. Lift the motherboard free and carefully place it bottom-down on a soft, insulating pad on the bench.

CAUTION: Abnormal voltages will be produced unless some current is drawn from the Power Supply. But do not risk damage to valuable circuit boards by using the analyzer as a test load for the sake of convenience. Use resistors as suggested in the following paragraph. (Note that no load is needed on the +12 V supply unless it is specifically under investigation)

---

k. To load the Power Supply outputs, obtain a mating connector for P9 (see parts list) and make an adapter with which to connect the load resistors between the various outputs and ground returns. For your convenience, suitable load resistance values are given in the following tabulation:

Output	Current	Resistance	Rating	
+5 V	1 A	5 ohms	5 W	
-5 V	1 A	---	---	(R38, built in)
+12 V	---	---	---	(no load needed)
+15 V	100 mA	150 ohms	2 W	
-15 V	100 mA	150 ohms	2 W	

m. To bring primary and auxiliary power to the Power Supply, obtain a matching plug and socket set for P13 and make a jumper cable. Use this cable to bring power to P13 from the Mains Module and auxiliary transformer via S13. Connect the Mains Module through an ISOLATION TRANSFORMER to the power mains. PLEASE SEE PRECEDING WARNING NOTICES!

2.3.2.2 High Voltage Section

The High Voltage Section consists of: CR19, a GE PD-80 bridge rectifier; Q1 and Q2, both Motorola MJE13005 power switching transistors; CR1,2, both 1N3600 diodes; CR3,4, both 1N4008 diodes; transformers T1 and T2; thermistors R1 and R2; and various resistors and capacitors.

This circuitry converts a nominal 100, 110, or 220 Vac, 50 or 60 Hz mains voltage to a center-tapped nominal ±162 Vdc. This dc voltage is converted (by the action of Q1, Q2, T2, and the Control Section) to a constant-frequency, pulse-width modulated, ac voltage across T1. The output voltages at the secondaries of T1 are a nominal 5 and 15 Vac rms at a nominal frequency of 20 kHz.

Input from the power mains is fed directly to the CR19 rectifier with no intervening isolation transformer. Consequently, all components within the High Voltage Section are at mains potential! PLEASE SEE PRECEDING WARNING NOTICES! A Mains Module, shown on the Chassis schematic diagram in section 2.1, contains a voltage card that is used to select the ac mains voltage that will be used to power the analyzer. The three selection options are 100, 110, and 230 Vac. (Please refer back to figure 2.1-1 in Chassis section 2.1.)

If a mains voltage of 230 Vac is selected, it is applied across input terminals E25 and E26 via connector pins P13-2 and P13-6. With this connection, CR19 acts as a full-wave bridge rectifier and produces a nominal 325 Vdc across filter capacitors C3 and C4 connected in series. The junction of C3 and C4 is a centertap of the 325 Vdc, providing ±162 Vdc for the switching circuit and transformer T1. R3 and R4 stabilize the centertap and act as bleeders. C5 and C6 are for EMI reduction. Fuse F1, a 2 A fast-blow type, provides circuit board protection in case Q1 or Q2 shorts out (any failure of Q1 or Q2 will happen faster than the fuse can blow).

If a mains voltage of 100 or 110 Vac is selected, it is applied across input terminals E25 and E27 via connector pins P13-2 and P13-3. With this connection, CR19 acts as a full-wave doubler rectifier and produces a nominal 325 Vdc across series-connected C3 and C4 as before.

By means of transformer T2, the Control Section turns transistor Q1 ON and OFF in alternation with Q2. The cycle time is a nominal 50 us. (Take note that Q1 and Q2 are never both ON at the same time.) This alternately applies +162 Vdc and -162 Vdc across the primary of transformer T1. (Typical waveforms at various points in the circuit are shown on the schematic diagram) The resulting ac voltages across the secondaries of T1 are rectified and averaged in the Output Section. Therefore, the longer Q1 and Q2 are ON during each cycle, the higher the dc output voltages from the Output Section. The width of the ON-pulse thus provides a means of voltage control which is used by the Control Section for very close voltage regulation.

Capacitor C10 blocks any dc bias that might otherwise result from a mismatch between Q1 and Q2. Components R37 and C35 reduce ringing and transient spikes. CR2-R6-C19 and CR1-R5-C18 speed up the turnoff times for Q1 and Q2.

2.3.2.3 Control Section

The Control Section consists of: U1, a National DS3632 dual peripheral driver; U2, a Silicon General SG3524 regulating pulse-width modulator; Q3, a 2N3904 transistor; Q4, a 2N3905 transistor; Q5, a Motorola MCR101 SCR; CR5 and 6, 1N3600 diodes: CR 7 and 8, 1N4009 diodes; CR9,18,24, all 1N3600 diodes; CR10, a 1N588 zener diode; and CR20, a GE PD-10 bridge rectifier.

This circuit provides drive pulses through transformer T2 that switch Q1 and Q2 ON and OFF. And by controlling the width of these drive pulses in response to voltage feedback from the Output Section, the circuit provides good voltage regulation of the output voltages. Also, it detects any overcurrent condition and reacts by shutting down the Power Supply.

The nucleus of the Control Section is the LSI circuit U2. It is powered by a nominal +20 V from the bridge rectifier CR20; and CR20 is fed, via P13-3 and 4, with a nominal 17 Vac at 50-60 Hz from a small transformer, T3, mounted on the chassis (ref. Chassis schematic diagram in section 2.1). Circuit U2 produces drive pulses at outputs CA and CB (pins 12 and 13) that are used, via U1 and transformer T2, to turn Q1 and Q2 ON and OFF. The repetition rate of the pulses is established by an oscillator in U2 whose frequency is set by the values of R34 and C13 at pins 6 and 7 to a nominal 40 kHz. And, because there are two U2 drive pulses for one cycle of the Q1-Q2 switching circuit, this sets the switching frequency of the power supply to a nominal 20 kHz. (However, as a glance at the waveform across T1 will indicate, the rise times and attendant potential for EMI are more nearly those of a 40 kHz signal than a 20 kHz signal.)

The drive pulses from U2 act as follows. When CA is low and CB is high, U1 output 5 is turned OFF and U1 output 3 is turned ON. The +20 V applied through R8 drives a current through winding 2-3 of T2 in the direction making the dot end of the winding positive. This current in 2-3 induces voltages in

windings 7-4 and 6-1, making their respective dot ends positive. The connections to these windings are such that Q2 is turned ON and Q1 remains OFF (the base of Q1 is driven even further negative).

The -162 Vdc applied to the emitter of Q2 drives a current through the transformer windings T1 3-9 and T2 8-5 in the direction making the dot end of 8-5 positive. This regenerative action reinforces the base drive to Q2. Transformer T2 acts as a current transformer, so the base drive current to Q2 is proportional to the T1 primary current through T2 8-5. The current ratio is such that Q2 is assured of being fully ON and well out of the linear region. Due to energy storage in inductive elements of the circuit, the T1 primary current that goes through T2 8-5 increases throughout the ON time of Q2. This sustains the high level of Q2 base drive supplied from T2 6-1.

Q2 is turned OFF again by the action of the blanking pulse within U2 which brings CA high along with CB. This turns U1 output 5 ON along with output 3, thus short circuiting winding T2 2-3 and cutting off the Q2 base drive current in T2 6-1. This short circuit condition lasts for at least the duration of the blanking pulse (a nominal 4 us), and during this time Q2 and Q1 are both forced to remain OFF. This insures that Q1 cannot be turned ON until Q2 is well OFF. The turn-on time of this type of transistor is shorter than the turn-off time. So without an adequately long blanking pulse, it would be possible for Q1 to turn ON while Q2 was still ON (for example, under conditions of low mains voltage and a compensating maximum pulse width for the switching circuit). This would put a short circuit across the ±162 V supply with undesirable results.

The next half of the 20 kHz switching cycle starts with the leading edge of the blanking pulse, but any drive pulse that would turn Q1 ON is inhibited within U2 for the duration of the blanking pulse. At the end of the blanking pulse, the voltage regulation circuitry in U2 is again in control, and as soon as that circuitry determines that it is time to start the Q1 drive pulse, CB is brought low. This turns U1 output 3 OFF and starts a current through winding 2-3 of T2 in the direction to turn Q1 ON and hold Q2 OFF. The rest of the action is analogous to that of the first half cycle.

Inputs to the U2 voltage regulation circuit are V+, pin 2, and V-, pin 1. The V+ input is supplied with a nominal +2.5 V reference voltage obtained, via R9 and variable resistor R17, from a well regulated +5 V output of U2 at pin 16. (This pin-16 output is also used as a source of +5 V power for other parts of the circuit.) The V- input is supplied with a nominal +2.5 V of negative feedback, via R32 and R25, from the regulated +5 V output of the power supply. (For phase correction purposes, R20 is used to adjust the ac impedance from U2-1 to ground to a value different from the dc resistance.) If the feedback voltage to V- rises above the reference at V+, the circuitry in U2 acts to reduce the drive pulse width, thereby reducing the output voltages of the power supply. If the feedback voltage at V- falls below the reference at V+, the action is just the opposite. This regulating action does not appreciably affect the 20 kHz switching frequency, only the ON times of Q1 and Q2.

The variable resistor R17 is adjusted so that the Power Supply output voltage measured at TP7 is +5.0 V ±.05 V. (Test jacks TP6, TP7, and TP8 are

conveniently placed together at the top edge of the motherboard in the Microcomputer Section.) This adjustment is made with both Power Supply output plugs connected to the analyzer, all circuit boards in place, and after the analyzer has had power applied for a warm-up period of 30 minutes.

As mentioned previously, the U2 clock frequency is set to a nominal 40 kHz by R34 and C13. The clock signal is a short-duty-cycle pulse which is also used as the blanking pulse. The pulse length is only about 0.5 us, which is not long enough for the blanking pulse in our application. The output node of the clock oscillator circuit is made available at pin 3, and the Q3-Q4 circuit connected to this pin is used to stretch the clock/blanking pulse to a nominal 4 us which provides adequate blanking protection for Q1 and Q2.

The SCR Q5, zener diode CR10, and diodes CR5 and CR6 constitute an overcurrent shutdown circuit which functions as follows. There is a component of the voltage across winding 2-3 of T2 that is proportional to the current in winding 8-5. In normal operation, the total voltage across winding 2-3 is such that voltage fed to the cathode of zener diode CR10 via diode CR5 or CR6 is always less than 7.5 V. However, if the current in winding 8-5 (which is also the current in the T1 primary) exceeds rated value by as little as 20%, the voltage at the CR10 cathode will exceed 7.5 V and CR10 will fire through either CR5 or CR6 (CR5 if Q1 is ON or CR6 if Q2 is ON). When CR10 fires, SCR Q5 is triggered and shorts both sides of winding 2-3 to ground through CR5 and CR6. This holds both Q1 and Q2 OFF, thus shutting down the power supply indefinitely until the power is turned OFF. When the power is turned back ON, the power supply will function normally again if the cause of the shutdown has been removed.

The gain of the error amplifier in U2 is set by R24 connected to pin 9. R23 and C33 provide phase compensation.

Diode CR18 connected to input terminal E24 feeds a mains-frequency signal to the SID (Serial Input Data) input of the 8085 processor. This signal is used by the Control Program to set the video vertical sync frequency to match the mains frequency (as discussed in Display Module subsection 4.2.1).

Diodes CR7 and CR8 serve to clip any ringing voltages that appear at winding 2-3 of T2.

2.3.2.4 Output Section

The Output Section consists of: VR1 and VR2, both LM340T-12 positive-voltage 12 V series regulators; CR21, a Varo VH248 bridge rectifier; CR11 and CR12, both 1N4008 diodes; CR13, a 1N5538 18 V zener diode; CR14,15,16, and 17, all 1N3889 rectifiers; CR22 and CR23, both 1N753A 6.2 V zener diodes; and Q6 and Q7, both TI TIC116F SCRs.

This section contains rectifier-and-filter systems for the four major output voltages of +5 V, -5 V, +15 V, and -15 V. These systems are fed with 20 kHz pulse-width modulated power from secondary windings on the switching transformer T1. This section also contains a low-power series regulator that is fed from the regulated +15 V and that provides +12 V to the Display Module.

There is also an optional low-power series regulator for a +30 V supply. The current ratings for these supply voltages are as follows:

Voltage	Max Current
+5 V	12.0 A
-5 V	11.0 A
+15 V	0.6 A
-15 V	1.5 A
+12 V	1.0 A
+30 V	0.1 A

CR21 acts as a full-wave bridge rectifier for both the +15 V and the -15 V supplies. It is fed from a pair of secondary windings, 8-5 and 2-11, on the switching transformer T1. L1-C18 and L2-C20 act as pulse-averaging and ripple filters for the +15 V and -15 V supplies, respectively. R21 is a bleeder resistor for the -15 V supply; VR1 serves incidentally as a bleeder for the +15 V supply.

Series regulator VR1 drops part of the +15 V output to +12 V for the Display Module. C19 provides additional filtering and decoupling for the +12 V.

If the optional +30 V supply is installed, C23, CR11, CR12, and C21 are fed from 15 V winding 2-11 of T1 and act as a voltage doubler to drive the 12 V series regulator VR2. Zener diode CR13 raises the ground terminal of regulator VR2 18 V above circuit ground, thus producing a regulated output of +30 V. C22 provides decoupling and filtering for the output. R26 limits the charging current of C23 and C21.

The two diodes CR14 and CR15 are rectifiers for the +5 V supply. They are each fed independently from separate 5 V secondary windings, 7-6 and 12-1, on the switching transformer T1. The outputs of the two diodes are connected in parallel to the L3-C28-C29 pulse-averaging and ripple filter. R28-C24 and R29-C25 act to limit slew rates and clip transient spikes for the two diodes.

Zener diode CR23 and SCR Q7 form a crowbar shutdown circuit for overvoltage protection. If the +5 V output voltage rises above the +6.2 V firing voltage of the zener diode CR23, SCR Q7 is triggered and puts a dead short across the +5 V output. The resulting rise in the primary current in transformer T1 activates the overcurrent shutdown circuit in the Control Section. Thus the entire Power Supply is shut down in just a few microseconds, and the current in the crowbar short across the +5 V supply does not have time to reach damaging proportions.

The -5 V output circuit is the same as for +5 V except for the circuit differences necessary to accomodate the opposite polarity. R38 provides a 1 A minimum load on the -5 V supply in order to maintain regulation in those configurations of the analyzer that do not have a Timing Analyzer section (which is the primary load on the -5 V supply).

Resistor R38 and the two crowbar shutdown circuits are mounted at the front of the motherboard under the circuit boards in the Microcomputer Section.

The feedback voltage for the Control Section is taken from the +5 V output through the phase compensation network R32-C32. The +5 V output is therefore tightly regulated. The other output voltages are still very well regulated, but to a lesser degree than the +5 V output. The +12 V and +30 V outputs benefit, of course, from the additional regulation afforded by the series regulators VR1 and VR2.

2.3.3 SCHEMATIC, BOARD LAYOUT, & PARTS LIST

The schematic diagram, board layout, and parts list for the Power Supply are contained on the following pages.

REV	DESCRIPTION	DATE	APPROVED

PARATRONICS INC.

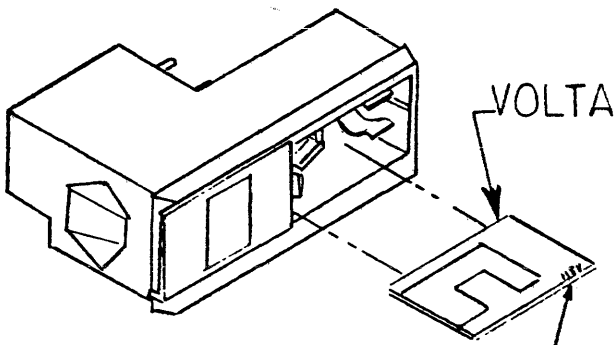
DESCRIPTION: MAINS MODULE WITH VOLTAGE SELECTOR CARD

DRAWN BY	DATE	
CHECKED BY	DATE	
ENG	DATE	
APPR. REL.	DATE	

DECIMAL .XXX = ±.005
.XX = ±.02
FRACTIONAL ± 1/64
ANGULAR ± 0°30'
BREAK ALL SHARP EDGES
DO NOT SCALE DRAWING

DRAWING NO. A

SCALE | SHT | OF | REV



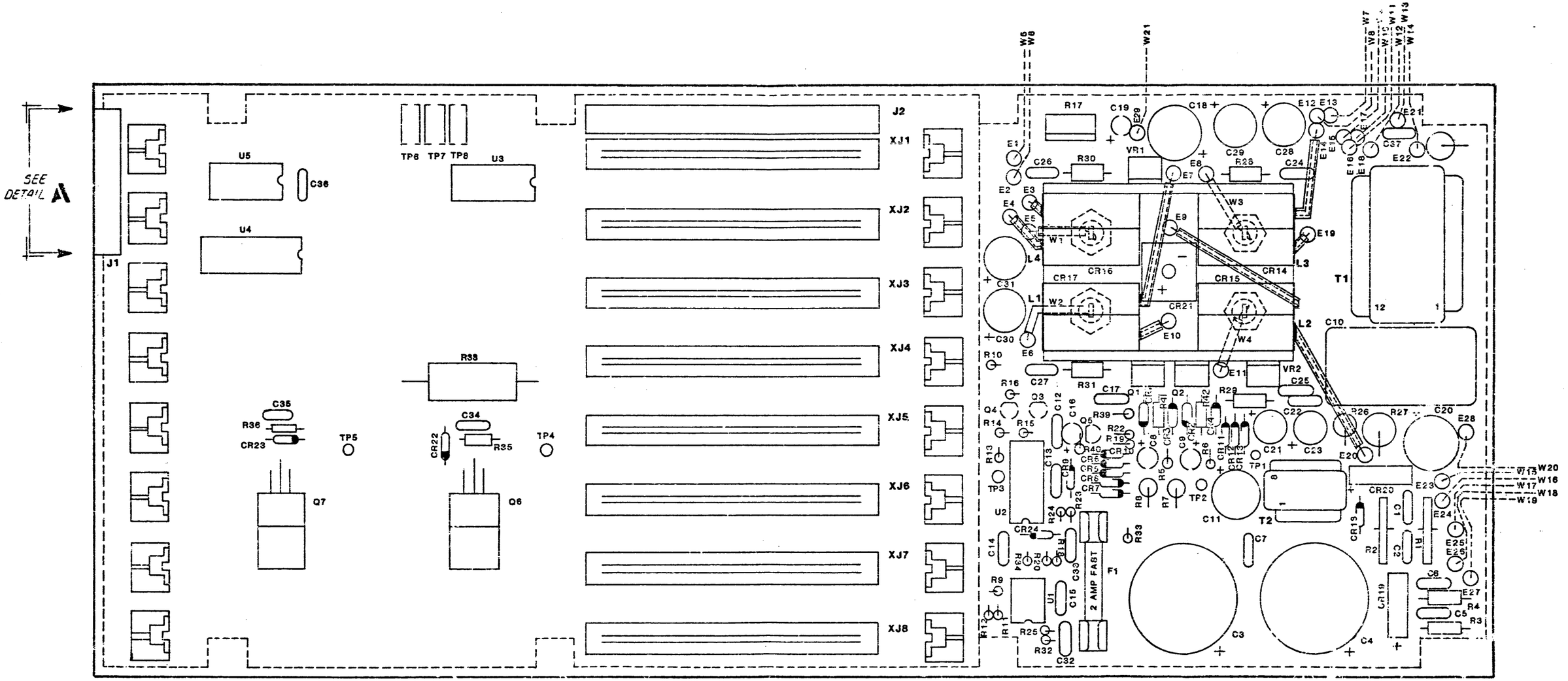
SELECT:

100V Nominal
115V Nominal
230V Nominal

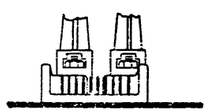
As Appropriate

NOTE: THE CARD MUST BE ORIENTED SO THAT THE SELECTED VOLTAGE CAN BE READ WITH THE CARD INSTALLED.

REV	DESCRIPTION	DATE	APPROVED
B	PER ECO 082	11-9-79	
C	REV PER ECO 123	2-27-80	
D	REV. PER ECO 140	3-31-80	
E	REV. PER ECO 148	4-29-80	



WIRE CONNECTION LIST								
WIRE	FROM	TO	WIRE	FROM	TO	WIRE	FROM	TO
1	CR16C	E5	9	E15	P2-4	15	E23	P1-1
2	CR17C	E6	11	E17	P2-10	16	E24	P1-4
3	CR14A	E8	13	E21	P2-11	17	E25	P1-2
4	CR15A	E11	14	E22	P2-9	18	E26	P1-6
			21	E29	P2-12	19	E27	P1-3
5	E1	P2-5				20	E28	P1-5
6	E2	P2-6	10	E16	P3-2			
7	E12	P2-1	12	E18	P3-1			
8	E13	P2-2						



DETAIL A
ROTATED C.C.W. 90° FOR CLARITY
SCALE = 1/2

DRAWN BY	DATE	PARATRONICS INC.
CHECKED BY	DATE	DESCRIPTION: LEGENDMASTER PWR.SPLY. MOTHERBD.
APPR. REL.	DATE	
DECIMAL .XXX ± .005 .XX ± .02		D 126-0055-201 E
FRACTIONAL ± 1/64 ANG. ALLR ± 0°30'		SCALE 2/1 SHT 1 OF 1 REV
BREAK ALL SHARP EDGES		

REV	DESCRIPTION	DATE	APPROVED
B	PER ECO 082	11-9-79	CFH
C	REV PER ECO 123,122,131	8-24-80	CFM
D	REVISED PER ECO 148	4-27-80	CFM

REV PER ECO 177 8-21-81

HIGH VOLTAGE SECTION

P13 W17 E25 W18 E26 W19 E27 W20 E28

R1 10Ω@25°C, R2 10Ω@25°C, C1 .01 500V, C2 .01 500V, CR19

R3 220K 1/2W, R4 220K 1/2W, C3 380 250V, C4 380 250V, C5 .02 500V, C6 .02 500V, C7 .0047 1KV

F1 2A FAST, +HV, -HV

C10 5, 200V MYLAR, T1, R37 56 2W, C35 .001 1KV

Q1, Q2, CR3, CR4, R41, 100, R5 4.7 1/2W, R6 4.7 1/2W, R42 100, C9 10 6V, CR1, CR2, TP1, TP2

CAUTION: ALL CIRCUITRY THIS SECTION AT AC MAINS POTENTIAL

T2

CONTROL SECTION

W16 E24 W15 E23 P13

CR20, C11 470 25V, CR18

R33 9.1K → TO SID ON BUS PIN25

R8 470 1W, R7 470 1W, CR8, CR7, CR6, CR5, CR10

R39 1000, R19 2000, R40 100, Q5

U1 DS 3632

C16 33 6V, R22 1000, C17 .01

R11 4.7K, R12 4.7K, CR9, R18 100K, CR24

R13 10K, Q3, R14 10K, R15 8.2K, C12 180pf, Q4, R16 10K

R9 220, R17 200 +5V ADJ., R10 220, C14 .1, C15 .1, R34 2.4K, C13 .01

U2 SG3524 (Vin, V+, VREF, CA, CB, COMP, RT, CT, OSC, EA, EB, CL+, CL-, V-)

R23 15K 1/4W 5%, R24 68K 1/4W 5%, C33 .1, TP3

R20 15K, R25 9.1K

OUTPUT SECTION

VR-1 LM 340T-12, C19 22 16V TANT, E18 W12 → P12 +12V, E16 W10 → P12 GND

L1 .9mH, C18 470 25V, TP8, E29 W14 → P9 +15V, E15 W9 / E17 W11 → P9 GND

CR21, L2 .9mH, C20 470 25V, R27 150 2W, E22 W21 → P9 -15V

"OPTIONAL 30V CIRCUITRY"

R26 15, 1W, C23 33, 63V, CR11, CR12, VR2 LM 340T-12, C21 33 63V, CR13 IN5338, C22 .1 50, E21 W13 → P9 +30V

L3 4μH, TP7, E12 W7 / E13 W8 → P9 +5V

E8 W3 CR14, R28 4.7 1/2W, C24 .1 50V, E19, CR23, TP5, Q7, R36 82, C35 .01

E11 W4 CR15, R29 4.7 1/2W, C25 .1 50V

C28 1000 10V, C29 1000 10V

L4 4μH, TP6, E1 W5 / E2 W6 → P9 -5V

CR16 W1 E5, R30 4.7 1/2W, C26 .1 50V, E3, E4, TP4, R35 82, C34 .01, Q6

CR17 W2 E6, R31 4.7 1/2W, C27 .1 50V, CR22

C30 1000 10V, C31 1000 10V, R38 5 5W

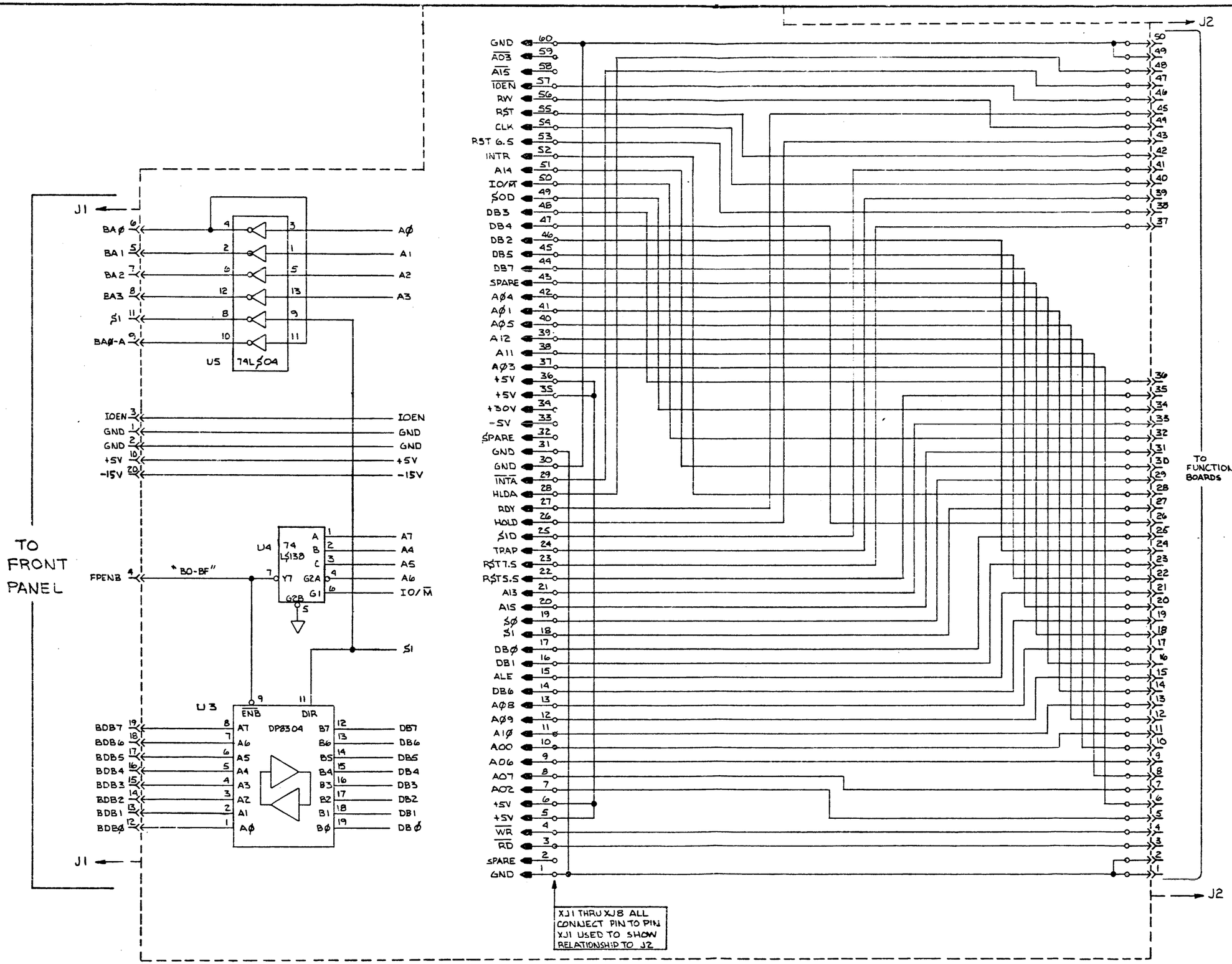
R32 22K, C32 .01

NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL CAPS IN μFARRADS
2. ALL RES 1/4W 5%

DRAWN BY	DATE	PARATRONICS INC.
CHECKED BY	DATE	
ENG	DATE	DESCRIPTION: SCHEMATIC DIAGRAM
APPR REL	DATE	540 PWR SPLY MOTHERBD
DECIMAL XX = ±.015, XX = ±.02		
FRACTIONAL ± 1/64, ANGULAR ± 0°30'		D DRAWING NO 127-0055-001 E
BREAK ALL SHARP EDGES		SCALE FWT 1 OF 2 REV
DO NOT SCALE DRAWING		

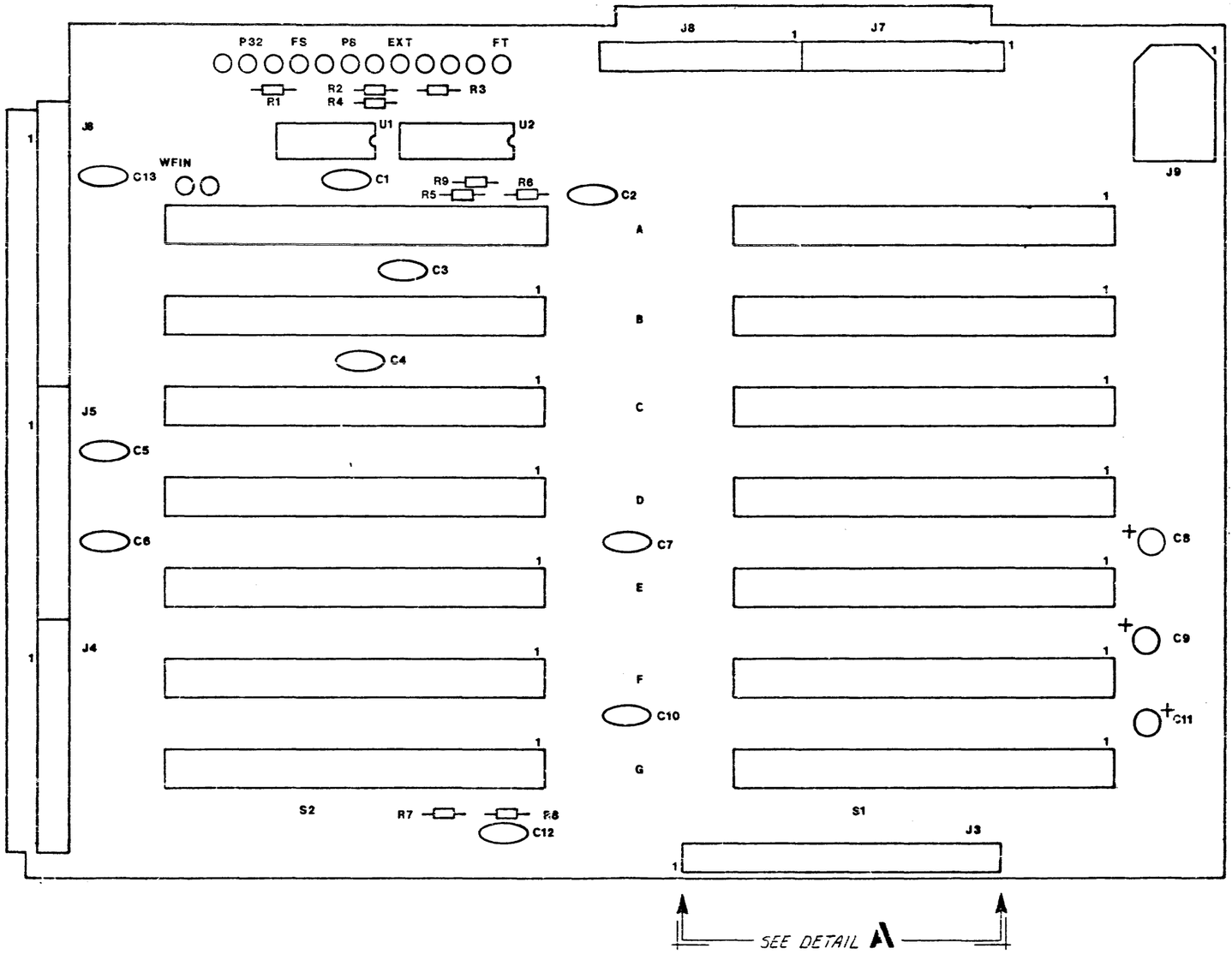
REV	DESCRIPTION	DATE	APPROVED
C	PER ECO 082	11-2-79	GEM
D	SEE SHT. 1		

IC	TYPE	Vcc	GND
U3	DP8304	20	10
U4	74LS138	16	8
U5	74LS04	14	7



DRAWN BY	DATE 9-14-79	PARATRONICS INC.	
CHECKED BY	DATE 11-10-79	DESCRIPTION	SCHEMATIC DIAGRAM
ENG	DATE 11-1-79		540 PWR SPLY MOTHERBD
APPR. REL	DATE 11-7-79	D	DRAWING NO. 127-0055-001 D
DECIMAL XXX = ± .005 XX = ± .02			
FRACTIONAL ± 1/64 ANGULAR ± 0°30'			SCALE SHT 2 OF 2 REV.
BREAK ALL SHARP EDGES			
DO NOT SCALE DRAWING			

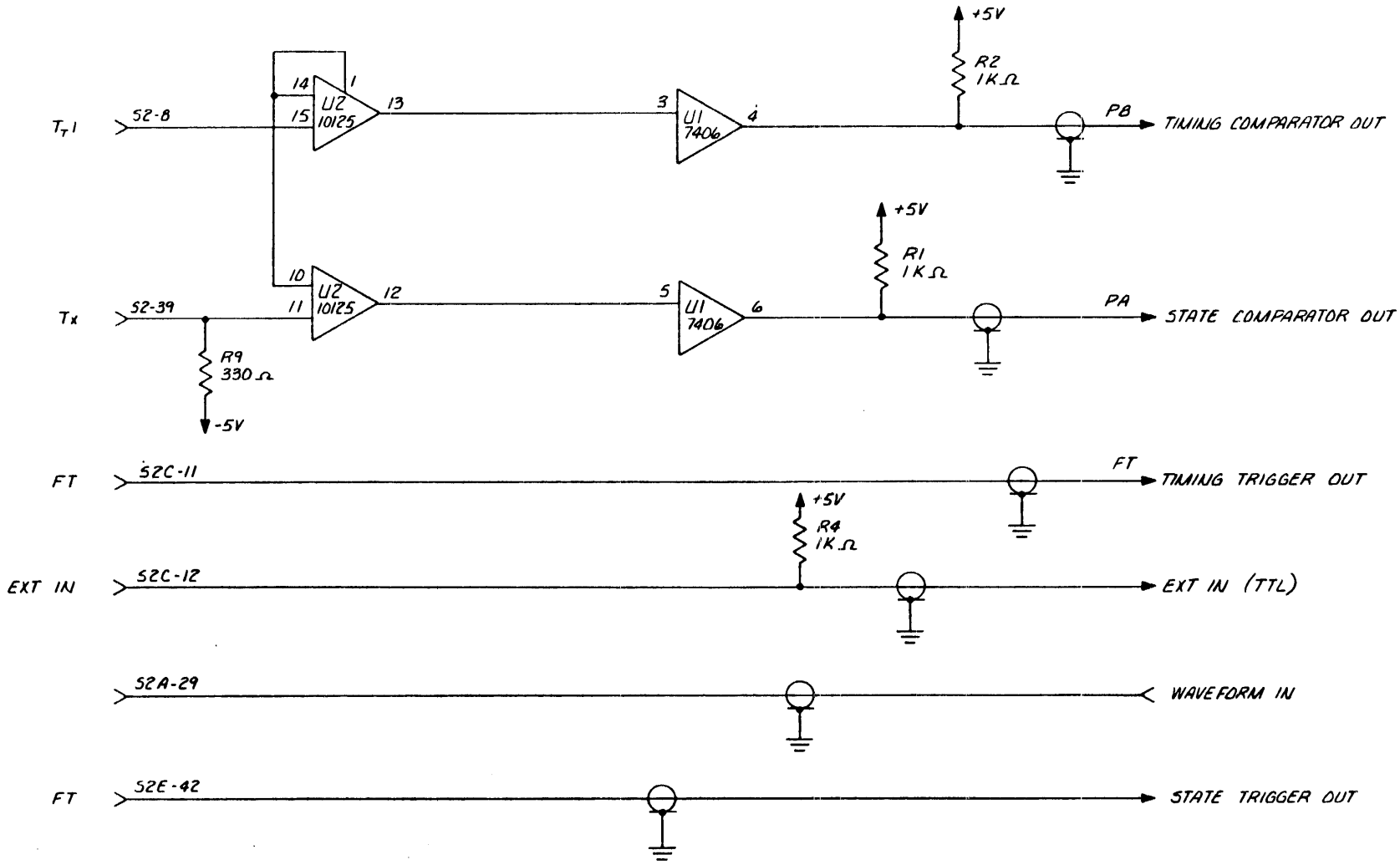
REV	DESCRIPTION		DATE	APPROVED
B	REV. PER EN 067	G.C.	10-24-79	
C	REV. PER ECO 140	BW	5-31-80	CH1



DETAIL A
SCALE = 1/2

DRAWN BY	DATE	PARATRONICS INC.	
CHECKED BY	DATE	DESCRIPTION	LEGENDMASTER
ENG	DATE		FUNCTION MOTHERBOARD
APPR. ENG.	DATE		
DECIMAL .XXX = ± .005 .XX = ± .02		D	DRAWING NO 126-0054-201 C
FRACTIONAL ± 1/16 ANGULAR ± 0°30'			SCALE 2/1 SHT 1 OF 1 REV
BREAK ALL SHARP EDGES			
DO NOT SCALE DRAWING			

REV	DESCRIPTION	DATE	APPROVED
B	REV PER ECO 121	2/4/82	WCG



1. CONNECTOR PINOUTS AND SIGNAL DESIGNATIONS DESCRIBED IN MAINTENANCE MANUAL.

NOTES: UNLESS OTHERWISE SPECIFIED

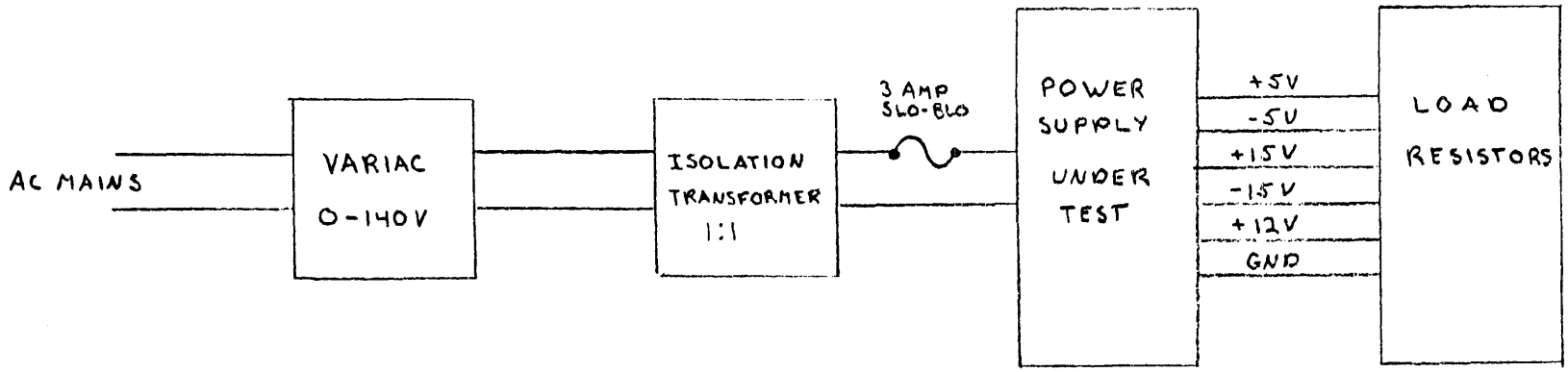
DRAWN BY	DATE 7-1-80
CHECKED BY	DATE
ENG	DATE
APPR. ISEL	DATE
DECIMAL XX = ± .010 XXX = ± .005	
FRACTIONAL ± 1/64 ANGULAR ± 0°30'	
BREAK ALL SHARP EDGES	
DO NOT SCALE DRAWING	

PARATRONICS INC.

DESCRIPTION: ELECTRICAL SCHEMATIC, 540 FUNCTION MOTHER

DRAWING NO 127-0054-001 B

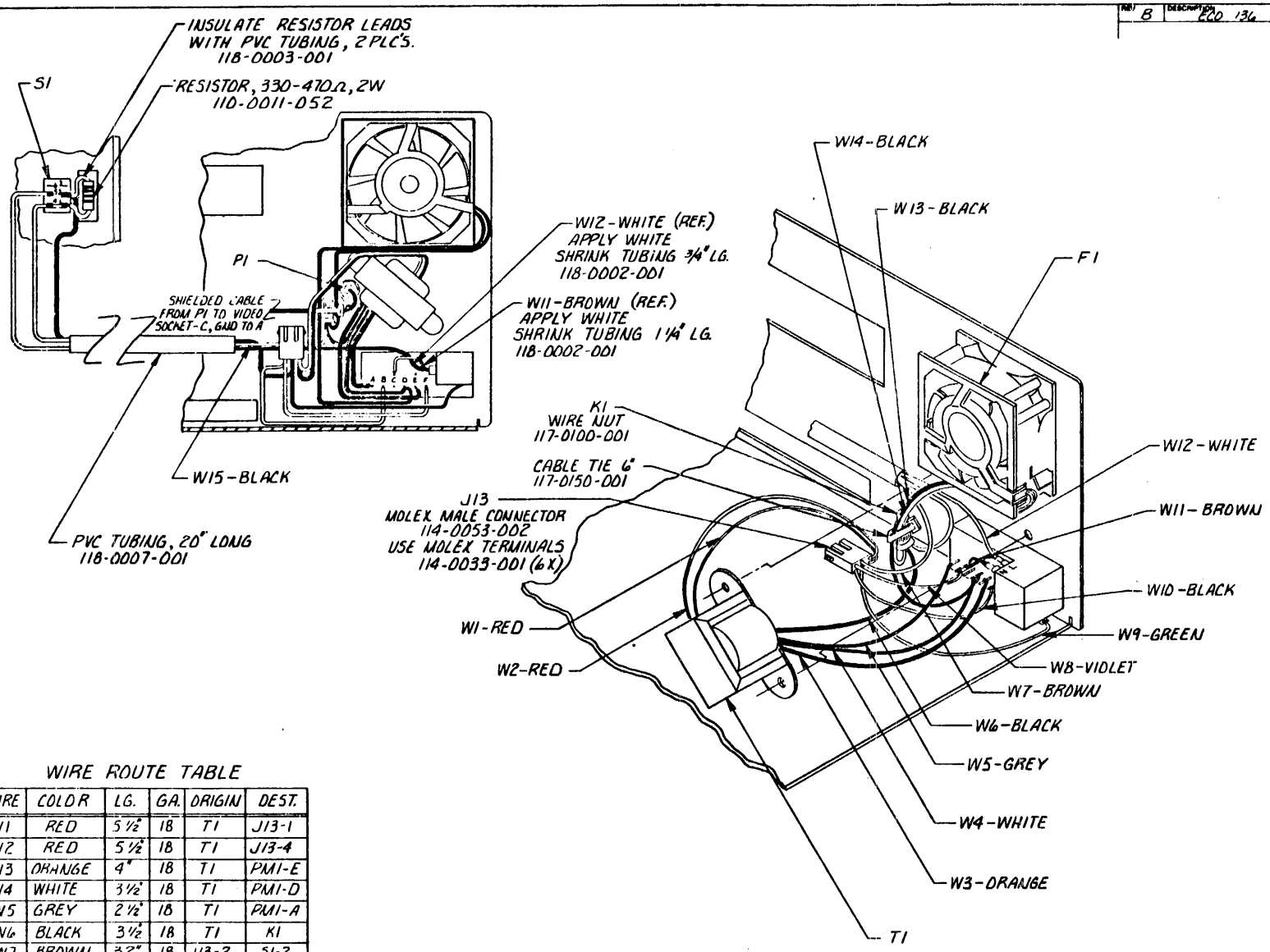
SCALE NONE SHT 1 OF 1 REV



REV	DESCRIPTION	DATE	APPROVED

DRAWN BY KSP	DATE 9-5-80	PARATRONICS INC.
CHECKED BY	DATE	
ENG	DATE	DESCRIPTION: POWER SUPPLY TEST SET-UP
APPR. REL.	DATE	
DECIMAL .XXX = ±.005 .XX = ±.02 FRACTIONAL ± 1/64 ANGULAR ± 0°30'		A DRAWING NO.
BREAK ALL SHARP EDGES DO NOT SCALE DRAWING		SCALE / SHT OF / REV

REV	DESCRIPTION		DATE	APPROVED
B	ECO 136		5-1-80	



WIRE ROUTE TABLE

WIRE	COLOR	LG.	GA.	ORIGIN	DEST.
W1	RED	5 1/2"	18	T1	J13-1
W2	RED	5 1/2"	18	T1	J13-4
W3	ORANGE	4"	18	T1	PM1-E
W4	WHITE	3 1/2"	18	T1	PM1-D
W5	GREY	2 1/2"	18	T1	PM1-A
W6	BLACK	3 1/2"	18	T1	K1
W7	BROWN	32"	18	J13-2	S1-2
W8	VIOLET	2"	18	J13-3	PM1-B
W9	GREEN	3 1/2"	18	J13-5	PM1-GND
W10	BLACK	2 1/2"	18	J13-6	PM1-F
W11	BROWN	2"	18	PM1-N	PM1-C
W12	WHITE	32"	18	PM1-L	S1-1,4
W13	BLACK	8"	18	F1	PM1-D
W14	BLACK	6"	18	F1	K1
W15	BLACK	32"	18	K1	S1-5

DRAWN BY	DATE 5-1-80	PARATRONICS INC.
CHECKED BY	DATE 5/1/80	DESCRIPTION: MODEL 540 MAIN CHASSIS ASSY.
ENGR	DATE	
APPR REL	DATE	
DECIMAL XXX = ± .005 XX = ± .02 FRACTIONAL ± 1/64 ANGULAR ± 0°30'		C DRAWING NO. 143-0073-001 B
BREAK ALL SHARP EDGES		SCALE NONE SHT 1 OF 1 REV.
DO NOT SCALE DRAWING		

REV	DESCRIPTION	DATE	APPROVED
A	NEW RELEASE ECO 139	3-27-80	

330-470Ω 2W

SW-1

KEYBOARD

J10 20 COND

P10 20 COND

20 WIRES FLAT RIBBON

CRT

CRT MONITOR

P1 20 COND

J1 20 COND

540 POWER SUPPLY, 143-0055-001
MOTHER BOARD

SERIAL 143-0012-001

IEEE 488, 143-0013-001

SPARE

143-0070-002 EXTENDED MEM. #2

143-0070-001 EXTENDED MEM. #1

CPU, 143-0008-001

143-0042-001 RASTER VIDEO

J14 2 COND

J15, 16 PIN DIP PLUG

J17, 16 PIN DIP PLUG

J11, 16 PIN DIP PLUG

J16, 24 PIN DIP PLUG

J18 25 PIN DELTA

J19 24 PIN RIBBON

24 WIRE FLAT RIBBON

16 WIRE FLAT RIBBON

110 TAP

COM.

110 PWR

AUX AC

AUX AC

RED BRN

RED GRN BLK

EARTH GND

1 2 3 4 5 6 P13

6 COND J13 1 2 3 4 5 6

J2 50 COND

P2 50 COND

J11 10 COND.

COAX

2 WIRES #18 STRAND

J12 2 COND

P12 2 COND

10 WIRES #18 STRAND

P12 50 COND

J3 50 COND

J4 P4 26 26 COND COND

J5 P5 26 26 COND COND

J6 P6 34 34 COND COND

PROBE MODEL 50/51A

PROBE MODEL 50/51A/70

PROBE MODEL 80

SPARE	G	
STATE MEMORY-B	F	143-0060-002
STATE CONTROL	E	143-0069-001
STATE MEMORY-A	D	143-0060-001
TIMING CONTROL	C	143-0071-001
TIMING MEMORY	B	143-0065-001
WAVE FORM VIDIO	A	143-0072-001

FUNCTIONAL P.C. BACK PLANE

12 12 COND COND P9 J9

16 PIN DIP PLUG P21

REAR PANEL

SELF TEST 20 COND J7

SELF TEST 20 COND J8

STATE PATERN OUT

TIMING PATERN OUT

SPARE

TIMING TRIGGER OUT

EXT. TRIGGER IN

STATE TRIGGER OUT

WAVEFORM IN

220 V ORN.

115V WHITE

100V GRAY

BLACK COM

P13-4

P13-1

FAN

TRANSFORMER

F E D C B A

POWER MODULE

FOR CONNECT
100V A, B, C
115V B, C, D
220V C, E, F

N

L

NEUT

EARTH

LINE

EXT. VIDEO

FUSE: 100/115V 3A SLOW BLOW
230V 1.5A SLOW BLOW

NEUT

EARTH

LINE

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES	DR G.S.	3-11-80	PARATRONICS INC.
	CH		540 CONNECTOR/ CABLES DIAGRAM
MAT'L	APPR		
FINISH	BREAK ALL SHARP EDGES DECIMAL ANGULAR XX ± .1 ° XXX ± .1 DO NOT SCALE DRAWING		DRWG NO 127-5223-001 REV A SCALE NONE SHT 1 OF 1

D

SINGLE LEVEL EXPLOSION

09/04/80

PAR143-0055-0090-00 DESCRIPTION : P.S. MOTHER PCB-OUTSIDE ASSY ECO#: 150 REV.CU.: F

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
111-0207-0103-00	D	22 UF 16V CAP. ELECTRO.,RAD.	1	1	0	08/21/80	OPEN	0	C19
110-0005-0107-00	D	68K OHM 1/4 W CF RES	1	1	0	03/06/80	OPEN	0	R24
110-0005-0063-00	D	1K OHM 1/4W 5% CF RES	2	1	0	02/16/80	OPEN	0	R22
R39									
110-0005-0070-00	D	2 K OHM 1/4W 5% CF RES	1	1	0	02/16/80	OPEN	0	R19
112-0251-0001-00	D	TRANSISTOR, 2N5060,MCR101	1	1	0	02/16/80	OPEN	0	Q5
111-0006-0072-01	D	.1UF 50V CAP. UK50-104	5	1	0	02/16/80	OPEN	0	C24
C25 C26 C27	C36								
112-0210-0001-00	D	1N958B 7.5V ZENER DIODE	1	1	0	OPEN	OPEN	0	CR10
111-0313-0072-00	D	CAP. CW20C104K, CENTRALAB	3	1	0	01/15/80	OPEN	0	C14
C15 C33									
110-0024-0008-00	D	5 OHM,5W, WW RES. DALE CP-5	1	1	0	OPEN	OPEN	0	R38
110-0005-0095-00	D	22K OHM 1/4 W CF RES	1	1	0	OPEN	OPEN	0	R32
110-0005-0086-00	D	9.1K 1/4W,5% RES. C	1	1	0	OPEN	OPEN	0	R25
110-0005-0091-00	D	15K OHM 1/4 W CF RES	2	1	0	03/06/80	OPEN	0	R20
R23									
110-0005-0085-00	D	8.2 K OHM 1/4 W CF RES	1	1	0	OPEN	OPEN	0	R15
111-0012-0050-00	D	.001UF 1KV, CD. CAP	1	1	0	OPEN	OPEN	0	C37
110-0015-0033-00	D	56 OHM 2W 5% CF RES	1	1	0	OPEN	OPEN	0	R37
110-0015-0043-00	D	150 OHM 2W,5% RES. CF,MF	1	1	0	OPEN	OPEN	0	R27
117-0117-0001-00		FUSE CLIP, 102068, L'FUSE	2	1	0	OPEN	OPEN	0	
115-0001-0001-00	D	SOCKET,8 PIN	1	1	0	OPEN	OPEN	0	U1
110-0005-0037-00	D	82 OHM 1/4 W 5% CF RES	2	1	0	OPEN	OPEN	0	R35
R36									
111-0417-0089-00	D	CAP 5 UF 200V MYLAR SPRG 277P	1	1	0	OPEN	OPEN	0	C10
110-0005-0039-00	D	100 OHM 1/4W 5% CF RES	1	1	0	OPEN	OPEN	0	R40
110-0005-0047-00	D	220 OHM 1/4W 5% CF RES	2	1	0	OPEN	OPEN	0	R10
R9									
110-0005-0072-00	D	2.4 K OHM 1/4 W CF RES	1	1	0	OPEN	OPEN	0	R34
110-0005-0079-00	D	4.7 K OHM 1/4 W CF RES	3	1	0	OPEN	OPEN	0	R11
R12 R33									
110-0005-0087-00	D	10K OHM 1/4 W CF RES	3	1	0	OPEN	OPEN	0	R13
R14 R16									
110-0005-0111-00	D	100K OHM 1/4 W CF RES	1	1	0	OPEN	OPEN	0	R18
110-0007-0007-00	D	4.7 OHM 1/2 W CF RES	6	1	0	OPEN	OPEN	0	R28
R29 R30 R31	R5	R6							
110-0007-0119-00	D	220KOHM 1/2 W CF RES	2	1	0	OPEN	OPEN	0	R3
R4									
110-0009-0055-00	D	470 OHM,1 W 5% RES. CF	2	1	0	OPEN	OPEN	0	R7
R8									
110-0103-0001-00	D	THERMISTOR,MIDWEST COMP. 2D754	2	1	0	OPEN	OPEN	0	R1
R2									
110-0200-0001-00	D	POT, CRC # TSC1BB251C	1	1	0	OPEN	OPEN	0	R17
111-0004-0066-00	D	.01 UF 25V CAP. CD	1	1	0	OPEN	OPEN	0	C34
C35									
111-0011-0066-00	D	.01 UF 500V CAP.CD	2	1	0	OPEN	OPEN	0	C1

PARATRONICS INC.

SINGLE LEVEL EXPLOSION

09/04/80

	PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
C2										
	111-0011-0068-00	D	.02 UF 500V CAP.CD	2	1	0	OPEN	OPEN	0	C5
C6										
	111-0012-0033-00	D	180 PF 1KV CAP. CD	1	1	0	OPEN	OPEN	0	C12
	111-0012-0062-00	D	.0047 UF 1KV CAP. CD	1	1	0	OPEN	OPEN	0	C7
	111-0050-0096-00	D	10 UF 6V TANT. DROP CAP.	2	1	0	OPEN	OPEN	0	C8
C9										
	111-0050-0107-00	D	33 UF 6V TANT. DROP CAP.	1	1	0	OPEN	OPEN	0	C16
	111-0413-0066-00	D	.01 UF 50V CAP. MYLAR	3	1	0	02/16/80	OPEN	0	C13
C17	C32									
	112-0100-0001-00	D	TRANSISTOR, 2N3904	1	1	0	02/16/80	OPEN	0	Q4
	112-0101-0001-00	D	TRANSISTOR, 2N3905	1	1	0	OPEN	OPEN	0	Q3
	112-0200-0002-00	D	DIODE BRIDGE, MDA208 MOT	1	1	0	OPEN	OPEN	0	CR19
	112-0200-0003-00	D	MDA 100A RECTIFIER	1	1	0	OPEN	OPEN	0	CR20
	112-0201-0001-00	D	DIODE, 1N753A	2	1	0	OPEN	OPEN	0	CR22
CR23										
	112-0204-0001-00	D	DIODE ,1N3600	9	1	0	OPEN	OPEN	0	CR1
CR18	CR2 CR24	CR5	CR6 CR7 CR8 CR9							
	112-0208-0001-00	D	DIODE ,1N4006	2	1	0	02/16/80	OPEN	0	CR3
CR4										
	112-0370-0001-00	D	CARD GUIDE END, 67762-2 AMP	16	1	0	OPEN	OPEN	0	
	114-0002-0002-00	D	PC HEADER, 3492-2003, 3M	1	1	0	OPEN	OPEN	0	
	114-0005-0001-00	D	CONN.30PIN,DUAL,H421021-30 TI	8	1	0	OPEN	OPEN	0	
	114-0026-0001-00	D	PC HEADER, 3496-1003, 3M	1	1	0	OPEN	OPEN	0	
	115-0003-0001-00	D	SOCKET,14PIN	1	1	0	OPEN	OPEN	0	U5
	115-0005-0001-00	D	SOCKET,16PIN	2	1	0	OPEN	OPEN	0	U2
U3										
	115-0009-0001-00	D	SOCKET,20PIN	1	1	0	OPEN	OPEN	0	U4
	117-0008-0003-00	D	TEST JACK, HHS 402-105 BLUE	1	1	0	OPEN	OPEN	0	
	117-0008-0001-00	D	TEST JACK, HHS 402-102 RED	1	1	0	OPEN	OPEN	0	
	117-0008-0002-00	D	TEST JACK, HHS 402-103 BLK	1	1	0	OPEN	OPEN	0	
	117-0875-0001-00	D	NYLON WASHER, 2670, HHS	16	1	0	OPEN	OPEN	0	
	117-0903-0001-00	D	6-32 (1/4) AF, HEX NUT,STL/CAD	16	1	0	OPEN	OPEN	0	
	117-1302-0001-00	D	6-32X 3/4PHMS,STL/CAD PHILLIPS	16	1	0	OPEN	OPEN	0	
	121-0009-0001-00	D	MAIN TRANSFORMERR	1	1	0	OPEN	OPEN	0	T1
	121-0010-0001-00	D	DRIVE TRANSFORMER	1	1	0	OPEN	OPEN	0	T2
	126-0055-0001-00	D	POWER SUPPLY MOTHER PCB FAB	1	1	0	OPEN	OPEN	0	

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SINGLE LEVEL EXPLOSION

09/04/80

PAR143-0055-0001-00 DESCRIPTION : POWER SUPPLY MOTHER PCB ASSY ECO#: 150 REV.CU.: F

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
117-0906-0001-00	D	10-32 HEX NUT, STL/CAD	4	1	0	OPEN	OPEN	0	
110-0005-0039-00	D	100 OHM 1/4W 5% CF RES	2	1	0	OPEN	OPEN	0	
117-0012-0001-00	D	NYLON BUSHING, 3103 KEYSTONE	3	1	0	06/08/80	OPEN	0	
117-0013-0001-00	D	BELVIEW WASHER 5808-4-15 SEA.	3	1	0	05/21/80	OPEN	0	
122-0064-0001-00	D	FIBRE WASHER	2	1	0	05/22/80	OPEN	0	
117-1202-0005-00	D	4-40X3/8 PHMS,PHILLIPS,STL/CAD	5	1	0	OPEN	OPEN	0	
117-1602-0004-00	D	10-32X 5/16 PHMS,PHILLIPS	4	1	0	01/29/80	OPEN	0	
117-1354-0020-00	D	6-32 PHMS,SLOTTED,STAINLESS	2	1	0	OPEN	OPEN	0	
117-0903-0004-00	D	6-32 HEX NUT, STANLESS STL.	2	1	0	OPEN	OPEN	0	
117-0903-0001-00	D	6-32 (1/4) AF, HEX NUT,STL/CAD	1	1	0	OPEN	OPEN	0	
110-0005-0063-00	D	1K OHM 1/4W 5% CF RES	1	1	0	OPEN	OPEN	0	R22
111-0004-0066-00	D	.01 UF 25V CAP. CD	1	1	0	OPEN	OPEN	0	C17
111-0204-0155-00	D	1000 UF 10V, ELECT. RADIAL	4	1	0	OPEN	OPEN	0	C28
C29 C30 C31									
117-0902-0001-00	D	4-40 HEX NUT, STL/CAD	5	1	0	OPEN	OPEN	0	
117-1302-0007-00	D	6-32X 1/2PHMS,STL/CAD PHILLIPS	1	1	0	OPEN	OPEN	0	
111-0209-0143-00	D	470 UF 25V, ELECT. RADIAL	3	1	0	OPEN	OPEN	0	C11
C18 C20									
112-0364-0002-00	D	FUSE,2A,250V, 2AGC	1	1	0	OPEN	OPEN	0	
112-0212-0001-00	D	1N3889 DIODE	4	1	0	OPEN	OPEN	0	CR14
CR15 CR16 CR17									
121-0012-0001-00	D	.9 MH INDUCTOR	2	1	0	OPEN	OPEN	0	L1
L2									
121-0011-0001-00	D	41 MH INDUCTOR	2	1	0	OPEN	OPEN	0	L3
L4									
117-0150-0001-00	D	TIE WRAP, PLT 1.5M-CP	5	1	0	OPEN	OPEN	0	
113-0027-0002-00	D	LM340T-12	1	1	0	02/16/80	OPEN	0	VR1
112-0252-0001-00	D	VJ148X RECTIFIER, VARO	1	1	0	OPEN	OPEN	0	CR21
112-0250-0001-00	D	SCR TIC 116F	2	1	0	OPEN	OPEN	0	Q6
Q7									
112-0110-0001-00	D	TRANSISTOR, MJE13005,MJE13007	2	1	0	OPEN	OPEN	0	Q1
Q2									
117-0865-0001-00	D	#10 FLAT WASER, STL/CAD	4	1	0	OPEN	OPEN	0	
124-0032-0001-00	A	540 PS/MB 12 V POWER PLUG ASSY	1	1	0	OPEN	OPEN	0	
124-0033-0001-00	A	540 DC POWER PLUG ASSY	1	1	0	OPEN	OPEN	0	
124-0031-0001-00	A	540 AC POWER PLUG ASSY	1	1	0	OPEN	OPEN	0	
112-0363-0002-00	D	SIL PAD 400, 3223-07FR-54	3	1	0	OPEN	OPEN	0	
117-0112-0001-00	D	SIL-PAD, 7403.09FR.20.BERQUIST	4	1	0	OPEN	OPEN	0	
117-0032-0001-00	D	BUSHING, B51547F012, MOT	1	1	0	OPEN	OPEN	0	
122-0045-0001-00	D	540 PS/MB HEAT SINK	1	1	0	OPEN	OPEN	0	
111-0218-0139-00	D	CAP ELECT 380 UF 250 V	2	1	0	OPEN	OPEN	0	C3
C4									
113-0003-0004-00	D	I.C., 74LS04	1	1	0	OPEN	OPEN	0	U5
113-0003-0138-00	D	I.C., 74LS138	1	1	0	OPEN	OPEN	0	U3
113-0014-0001-00	D	I.C., DP8304N, NSC, AMD,	1	1	0	OPEN	OPEN	0	U4
113-0049-0001-00	D	IC,SG3524, TI, SG	1	1	0	OPEN	OPEN	0	U2

S I N G L E L E V E L E X P L O S I O N

09/04/80

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
113-0050-0001-00	D	IC,DS3632, NSC	1	1	0	OPEN	OPEN	0	U1
143-0055-0090-00	D	P.S. MOTHER PCB-OUTSIDE ASSY	1	1	0	OPEN	OPEN	150	

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P A R A T R O N I C S I N C .

S I N G L E L E V E L E X P L O S I O N

09/04/80

PAR143-0054-0001-00 DESCRIPTION : FUNCTIONAL MOTHER BOARD ASSY. ECO#: 122 REV.CU.: C

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
111-0207-0103-00	D	22 UF 16V CAP. ELECTRO.,RAD.	2	1	0	08/21/80	OPEN	0	C11
C8									
110-0005-0051-00	D	330 OHM 1/4W 5% CF RES	1	1	0	OPEN	OPEN	0	R9
113-0001-0006-00	D	I.C., 7406	1	1	0	12/31/79	OPEN	0	U1
114-0054-0002-00	D	WAFERCON,09.18.5121,MOLEX	1	1	0	OPEN	OPEN	0	J9
110-0005-0049-00	D	270 OHM 1/4W 5% RES	2	1	0	OPEN	OPEN	0	R6
R8									
110-0005-0063-00	D	1K OHM 1/4W 5% CF RES	4	1	0	OPEN	OPEN	0	R1
R2 R3 R4									
110-0005-0045-00	D	180 OHM 1/4W 5% CF RES	2	1	0	OPEN	OPEN	0	R5
R7									
111-0006-0072-00	D	.1 UF 50V CAP. CD	10	1	0	OPEN	OPEN	0	C1
C10 C12 C13 C2		C3 C4 C5 C6 C7							
113-0200-0125-00	D	I.C., MC10125	1	1	0	OPEN	OPEN	0	U2
114-0002-0001-00	D	CONN., 20 PIN, 3492-1003, 3M	2	1	0	OPEN	OPEN	0	J7
J8									
114-0004-0001-00	D	CONN.26PIN,609-2617 ANSLEY	2	1	0	OPEN	OPEN	0	J4
J5									
114-0005-0001-00	D	CONN.30PIN,DUAL,H421021-30 TI	14	1	0	OPEN	OPEN	0	S1A
S1B S1C S1D S1E		S1F S1G S2A S2B S2C S2D S2E S2F S2G							
114-0028-0001-00	D	3494-1003,34 PIN CONN., 3M	1	1	0	OPEN	OPEN	0	J6
114-0029-0001-00	D	3496-2003,50 PIN CONN., 3M	1	1	0	OPEN	OPEN	0	J3
126-0054-0001-00	D	FUNCTION MTHR BCKPLN PC FAB	1	1	0	OPEN	OPEN	0	

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LEGEND KEY: A=W/PARTS LIST D=W/O PARTS LIST R=REFERENCE DOCUMENT S=SPECIFICATION

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3.0 KEYBOARD

3.0 KEYBOARD

3.1 INTRODUCTION

During the following discussion, please refer to either the keyboard itself or the picture of the keyboard in figure 3-1.

They keys on the keyboard are completely covered by a plastic overlay sheet which proteacts them from dust and other contamination. This sheet is dark gray in color and has keytop-sized rectangular patches of white or light gray where keys are located. These patches carry the keytop legends. There are other labelings on the dark background, and there is also a row of small, round, clear ports through which LED indicator lights show when lighted.

At each key location there is a slight dome underneath the plastic overlay. This dome gives way with a snap when pressed, thus providing tactile feedback of the key closure. An audio feedback tone is also provided. (The operator can disable this audio tone by holding the "T" key depressed for 2 seconds while the main power is turned ON.) If an illegal key entry is made during any operation, a dual-tone error signal is sounded and the ERROR light comes on. (The error tone is not disabled by the "T"-key procedure.)

The keys are connected as input devices to the microprocessor, and the function of each key is determined entirely by software. Many keys have two functions, one for each of two different analyzer operating modes in which the key may be called into play. Such keys have two legends on the keytop, one legend in green and one in red. Above the group of keys involved, a green or red light turns on to indicate which legend applies in the current operating mode.

3.2 PHYSICAL DESCRIPTION

The keys are of the snap-action, contact type. Each key consists of a thin, dome-shaped piece of spring metal attached to a printed circuit board. Directly under each dome is another piece of metal, the base tab, which is electrically isolated from the dome. When the dome collapses with a snap under finger pressure, it makes electrical contact with this base tab. The keys are laid out on a rectangular grid of 6 rows running across and 14 columns running up and down. All the key domes in a given row are connected together electrically, providing 6 row-input lines. All the base tabs in a given column are connected together electrically, providing 14 column-input lines. (The use of these input lines is discussed in the Functional Description section.)

The keyboard PC board is bonded to a heavy-guage (approximately 0.1") panel of aluminum, with the key domes on the side away from the aluminum. The plastic, keytop overlay sheet is bonded to the key-dome side of the PC board. This bonded sandwich construction produces a particularly invulnerable keyboard. However, it also means that individual keys are not replaceable; if a key becomes inoperative for any reason, the entire keyboard panel must be replaced.

The keyboard PC board contains holes for insertion of the LED indicator lights, as well as solder points for their connection. It also contains two input lines running to solder points for connection of the audio tone generator, which is mounted on the back side of the aluminum panel. The aluminum panel has clearance holes for the LED's and their leads, and for the tone generator leads. It also has 1/8" test-probe holes under all key positions. On axis with these holes are holes in the PC board which are plated-through and connected to the base tabs. Test-contact with the base tabs can thus be made by probing the pads of the plated-through holes. And test-contact with the key domes, which are directly above, can be made by inserting an insulated needle probe through the plated-through holes.

The Keyboard Interface Board (approximately 4" square) is mounted on the right side of the bottom surface of the aluminum panel. There are clearance holes in this board for two LED's mounted on the keyboard PC board in that area. There is a socket at the right edge of the Keyboard Interface Board that mates with a plug bringing the row and column lines from the keyboard PC board. There is a header soldered to the Keyboard Interface Board that terminates a 20-conductor flat cable. This cable carries I/O and control signals to and from the computer, and it plugs into a socket on the Microcomputer Motherboard.

The whole keyboard assembly is mounted to the analyzer cabinet by two hinges that are fastened to the keyboard's aluminum backing panel. Four threaded spacers are fastened to the aluminum panel, and to these spacers is mounted the keyboard case, which is molded of tough, fibre-filled plastic. It folds up around the edges of the keyboard panel assembly and extends about 1/8" out from the keyboard working surface. The keyboard case carries mating parts of the two keyboard-closing latches; and the four screws that mount the case to the aluminum panel also mount four rubber feet on the outside surface.

3.3 SELF-TEST

A processor-controlled keyboard self-test is provided with which you can test the operation of each key from the keyboard itself and without any dismantling. To initiate this self-test, hold the "1" key down while turning the main power switch from OFF to ON, and keep the "1" key held down until you hear the beep (about 2 seconds). After the computer has finished its own power-ON self-test (which takes the 2 seconds) and has so indicated with a beep, it finds the "1" key down and jumps to the keyboard self-test program. (Actually, you can turn the power ON first and then, within 2 seconds, hold down the "1" key. Just so the "1" key is already down at the instant when the processor finishes its own self-test.)

Test results are displayed as messages on the CRT:

With no key depressed, the message is, "KEY DEPRESSED: NONE".
With a key held depressed, the message is, "KEY DEPRESSED: x x",

where the x's represent the depressed key's location expressed as row and column numbers. As mentioned earlier, the keys are laid out on a rectangular grid of 6 rows and 14 columns. Row 1 is at the top, and column 1 is at the left. (The gap running across, underneath row 2, is not given a row number.)

Thus, if you depress the key in the lower right corner, the display will read, "KEY DEPRESSED: 6 14".

This test allows you to varify, for any given key, that the key closes and that the closure is being detected by the computer. Also, all the LED indicator lights, except the ERROR light, remain lighted during the test, which allows you to varify that the LED's are functioning. (The ERROR light comes on, along with the other lights, while the computer is performing its 2-second power-ON self-test. You can varify the ERROR light at that time.)

To exit from the keyboard self-test, turn the main power switch OFF. (This is the only way; all the keys are committed to simply telling you where they are.)

3.4 DISASSEMBLY

To disassemble the keyboard, it will be necessary to lay the instrument down on its side. The handle pivot-knobs do not provide a stable base, and some sort of support must be placed under the front of the instrument to raise the pivot-knob up off the bench top. It is strongly urged that you obtain a 2" x 2" piece of wood about 10" long for this purpose. Such an item is handy to have around the lab, anyway. After obtaining the 2" x 2", proceed as follows:

a. Particular pains must be taken to support the front of the analyzer if the cover is off. For this reason, the cover should be left on (or put back on) unless you are reasonably sure that you will need access inside the cover after you have disassembled the keyboard. If in doubt, start with the cover on; you can take it off later if you have to.

b. Latch the keyboard closed and swing the handle straight out. Place the analyzer on its side on the bench, with the bottom facing you, the keyboard to the right, and the front end resting temporarily on the handle pivot-knob (if you are left handed, read "right" as "left" here and in the rest of the instructions).

c. If the cover is off at this point, skip to step f.

d. Raise the front end off the bench and slide the 2" x 2" underneath so that it is extending across the instrument. It should be behind the handle pivot-knob, but with its midsection up against the pivot-knob. This arrangement provides a stable base for the analyzer, and you can now proceed with the keyboard disassembly without fear of damage to the keyboard or the rest of the analyzer. Also, the analyzer can now be moved around on the bench when desired by placing one hand on each end of the 2" x 2" and using it as a stearing bar.

e. Skip over the cover-off instructions to step k.

f. If the cover is off, adjust the position of the analyzer so that the long axis is at about a 45-degree angle with the front edge of the bench, the keyboard is still to your right, and the pivot-knob is

resting about 1" in from the edge of the bench. The handle should still be straight out.

g. With the "2 x 2" handy, squat down so that your head is about on a level with the bench top and you can see under the analyzer. Place your left hand under the lower end of the handle and lift up the front of the analyzer just enough to slide the 2" x 2" under with the other hand -- but don't lower the analyzer yet.

h. Keeping your head where you can watch the right front corner, angle the 2" x 2" so that the far end is under the edge of the bottom plate, the mid section is against the pivot-knob, and the near end is under the silver front casting -- not the long top-edge tie rod, which might bend or break off at the mounting stud. Now ease the analyzer front end down onto the 2" x 2".

i. Make sure that the 2" x 2" is angled enough so that it is clear of the tie rod, but keep its mid section against the pivot-knob. The analyzer is now in a stable position that will allow you to proceed with the keyboard disassembly without fear of damage to the keyboard or the rest of the analyzer.

j. If you should have occasion to move the analyzer around on the bench, grasp the 2" x 2" with one hand at each end, place the left thumb against the rubber foot on the bottom plate and the right thumb against the corner of the closed keyboard, and snug the 2" x 2" up against the pivot-knob. Then slide the 2" x 2" around on the bench to the desired position, with the thumb pressure ensuring that the analyzer goes with it.

k. Swing the handle to the right until it bumps the 2" x 2". Leave the keyboard latched closed, and remove the four rubber feet from the keyboard case. Obtain four machine screws of the same thread size as those just removed and about 1" long, and screw them about 1/4" into the four holes just vacated.

l. Unlatch the keyboard and swing it open about 90 degrees. Remember that the key panel is fastened to the hinges and that the black keyboard case is going to come away from the panel. Place a thumb on each of the two top screws you just inserted, and place the finger tips of each hand on the edges of the open face of the black keyboard case, trying not to overlap onto the key panel.

m. Gently pull the case edges with your fingers against the pressure of your thumbs on the two screws until you feel the case begin to come away slightly from the key panel. Now alternate this procedure between the upper and lower pair of screws until the case comes free.

n. Swing the keyboard closed again, back out the four pushing screws, and set the case aside. Remove the four outer spacers that are on the threaded case-mounting spacers (note that the shorter ones come from the hinge side) and place them in the upturned case for safe keeping.

o. As you examine the exposed parts, identify the items mentioned in the discussion at the beginning of the Keyboard section.

p. To dismount the Keyboard Interface Board, remove the four mounting screws and the cable hold-down strip. The board is now held by the plug-and-socket interconnection to the keyboard PC board.

q. Using a small shirt-pocket or jewler's screwdriver, very gently pry between the board edge and the plug leads at one end of the connector until you have opened up a small gap at that end between the black plastic of the plug and the black socket body. Stop when the gap is just large enough to admit the screwdriver blade.

r. Now pry between the plastic of the plug and the plastic of the socket, working your way along the length of the plug to keep the gap even. Pry by rotating the blade rather than by levering it. Switch to a larger blade as soon as the gap is wide enough. As the board begins to impinge on the two LED's in their clearance holes, you will have to tilt the board very slightly to clear them. But hold off on the tilting as long as possible because it tightens up the plug contacts. Keep working back and forth along the gap, keeping it even, until the board comes free.

s. The board can now be mounted in a circuit-board holder placed close to the keyboard. Try to avoid disconnecting the far end of the flat cable because this involves dismounting the Microcomputer Motherboard. If this should become necessary, take the cover off as described below, and then refer to Power Supply subsection 2.3.2.1 for instructions on dismounting the Microcomputer Motherboard.

t. If you find that you need to take the cover off the analyzer at this point, proceed as follows. Otherwise skip to step w.

u. Fasten the keyboard panel closed with a cord or wire wrapped around one of the case latches and one of the case mounting spacers. If the Keyboard Interface Board has been removed, temprorarily remount it with a screw put through the hole in the corner by the row/column socket, but screwed into the spacer that normally goes under the corner by the three resistors and a diode.

v. While the analyzer is still on its side, remove the six screws that fasten the cover to the bottom plate. Lift up the analyzer, place it on its four bottom-plate feet, and slide the cover off to the rear. Now go back to step b for instructions on how to place the coverless analyzer on its side without damaging the top-edge tie rod.

w. Reassembly has no particular problems. Just check to make sure that the LED's are all straight in their holes and that their leads are not touching the aluminum panel, paying particular attention to the two under the Keyboard Interface Board. Also, when remounting the keyboard case, make sure that the shorter outer spacers are at the hinges.

3.5 FUNCTIONAL DESCRIPTION

When appropriate during the following discussion, please refer to the schematic diagrams, board layout, and parts list which are included at the end of this section. (Note that an extra copy of the schematic for the Microcomputer Motherboard is included here because some parts for the keyboard circuitry are shown on it.) Also, tables of connector pins versus signal names for all motherboard connectors are provided in section 15 along with an alphabetical list of all interboard signals. And, should the need arise, a Glossary in section 16 offers explanations for acronyms or terms that may be unfamiliar.

From a functional standpoint, the keyboard must be considered a combination of hardware and software. Each individual key is, in effect, connected as an input device to the microprocessor (an Intel 8085 on the Processor Board in the Microcomputing Section), and the function of each key is determined entirely by software. The hardware portion of this arrangement is implemented as follows.

As discussed in the Physical Description section, the keys are of the snap-action contact type, consisting of a dome contact (which snaps) and a base tab contact (which doesn't). The keys are arranged as a matrix of 8 rows and 14 columns, but only 6 of the rows contain keys in this implementation of the keyboard. In each row, all the domes in the row are electrically connected together, producing 8 row-input lines (two of which are inactive). In each column, all of the base tabs in the column are electrically connected together, producing 14 column-input lines.

These 22 matrix input lines are connected from the keyboard panel, via J2, to the Keyboard Interface Board. On the Interface Board, each row line has a 10K pullup resistor, in SIP RN1, and is connected to an input pin of U4, a 74LS244 octal buffer. Each column line is connected to an output pin of U1 or U2, 74LS138 3-to-8 decoders. The column lines have now become output lines from the standpoint of the processor.

A 20-conductor flat cable is soldered to the Keyboard Interface Board and plugs into connector J1 on the Microprocessor Motherboard. The outputs of the row-line octal buffer, U4, connect through J1 to the processor's 8 buffered data-bus lines BDB0—BDB7. The U4 buffer has 3-state outputs controlled by 1/4 of U5, a 74LS32 quad 2-input OR gate, with this section being used as a negative-logic AND gate. The control inputs to U1, U2, and U5 come from the Microprocessor Motherboard through J1.

There are some circuits on the Microprocessor Motherboard that are so closely associated with the Keyboard Interface Board that they will be discussed in this section. Their IC U-numbers will be preceded by Mp/Mb. One of these circuits is Mp/Mb U5, a 74LS04 hex invertor, which supplies inverted low-nyble address bits BA0- through BA3- to U1 and U2. It also supplies non-inverted address bit BA0 to U2, and inverted status signal S1- to U5. There is also Mp/Mb U3, a DP8304 transceiver, which buffers the data-bus lines in either direction and connects them to J1 as BDB0—BDB7.

A complex decoder for a family of I/O ports is formed by U1, U2, and Mp/Mb U4, all 74LS138 3-to-8 decoders. The I/O port address for the family is

Eh, where h represents any hex number. Fourteen addresses in the Eh set are assigned to the 14 columns of the keyboard matrix. These addresses are used in the operation of the keyboard as follows.

At frequent intervals (several hundred times per second) the Control Program tests all the keyboard keys to see if any are depressed. Tracing one query in the sequence will illustrate this scanning process. To determine, for example, if there is a key closure in column 5, the Control Program issues an input instruction to I/O port E6. (The Control Program knows from the assignment table that to query column 5 it must send input-port address E6.) The high-order nyble, E, of the I/O port address is decoded by Mp/Mb U4 to produce the front-panel-enable signal, FPENB-, at J1-4. This signal also enables the Mp/Mb U3 transceiver, which is for the exclusive use of the Eh I/O port family. At the same time the port address is sent, the Processor Board automatically issues an I/O-enable signal, IOEN-, on J1-3.

The signals FPENB- and IOEN- partially enable U1 and U2. In the low-order nyble of the I/O port address (0110 inverted to 1001), BA0- is high, selecting U1 at U1-6; and BA0 is low, deselecting U2. The remaining three inverted address bits BA1-, BA2-, and BA3-, are fed to U1 inputs A, B, and C as low, low, high. The 74LS138 truth table shows that this input brings output Y4 low at U1-11. This in turn brings all keyboard base tabs in column 5 from high to low.

Now suppose, for example, that the row-2 key in column 5 is depressed. The dome on this key is contacting the base tab, which is low. The row-2 input at pin 6 of row-line buffer U4 is therefore low (it had been held high by pullup RN1-8). FPENB- and S1- at the inputs to AND gate U5 have enabled the outputs of U-4. The row-2 signal is therefore applied to buffered data-bus line BDB2 and fed to transceiver Mp/Mb U3. The transceiver has been enabled in the read direction by signals S1 and FPENB-, and the keyboard signal is fed on to the processor as FB (binary 1111 1011). The Control Program sees something other than FF come back, so it goes to a lookup table. There it finds that "Query E6; get back FB," means "PREV", so it jumps to the PREV routine.

If more than one key in column 5 had been depressed, the lookup table would have sent the Control Program to an ERROR routine. If no key had been depressed, U4 would have sent back FF. If a key in some column other than 5 had been depressed, U4 would still have sent back FF because the base tab under this depressed key would have been high, resulting in no change at the input to U4.

Whenever a query is answered by FF, the Control Program goes on (in due course) to query the next column. This all happens very rapidly. Even though the Control Program does many other things between queries, it still scans the full 14 columns often enough to sense a key closure within a few milliseconds of first contact.

The L1 LED for POWER ON is driven by the +5v supply, with the current limited by R4. The other keyboard LED's are driven by U3, a 74LS374 edge-clocked latch, through current limiting resistors R5-R10. The inputs to U3 are connected to the buffered data bus in parallel with U4. With all-0's latched into U3 (the startup condition), all LED's are ON. To turn OFF, for

example, the L5 ERROR LED, the Control Program sends output port address E1 and puts a 1 on data bus line DB3, at the same time holding all other data bus bits unchanged. The E1 address is decoded by the U1, U2, Mp/Mb U4 decoder to produce a low output at U2-7. The high-to-low transition of this signal, applied to U3-11, clocks the data on the U3 inputs into the latches. U3-9 goes high, and the ERROR light goes out. (Transceiver Mp/Mb U3 has been enabled in the write direction by FPENB- and S1 which is low for a write operation. Because S1- is high, U4 outputs are not enabled this time and therefore do not interfere with the LED-drive data on the bus.)

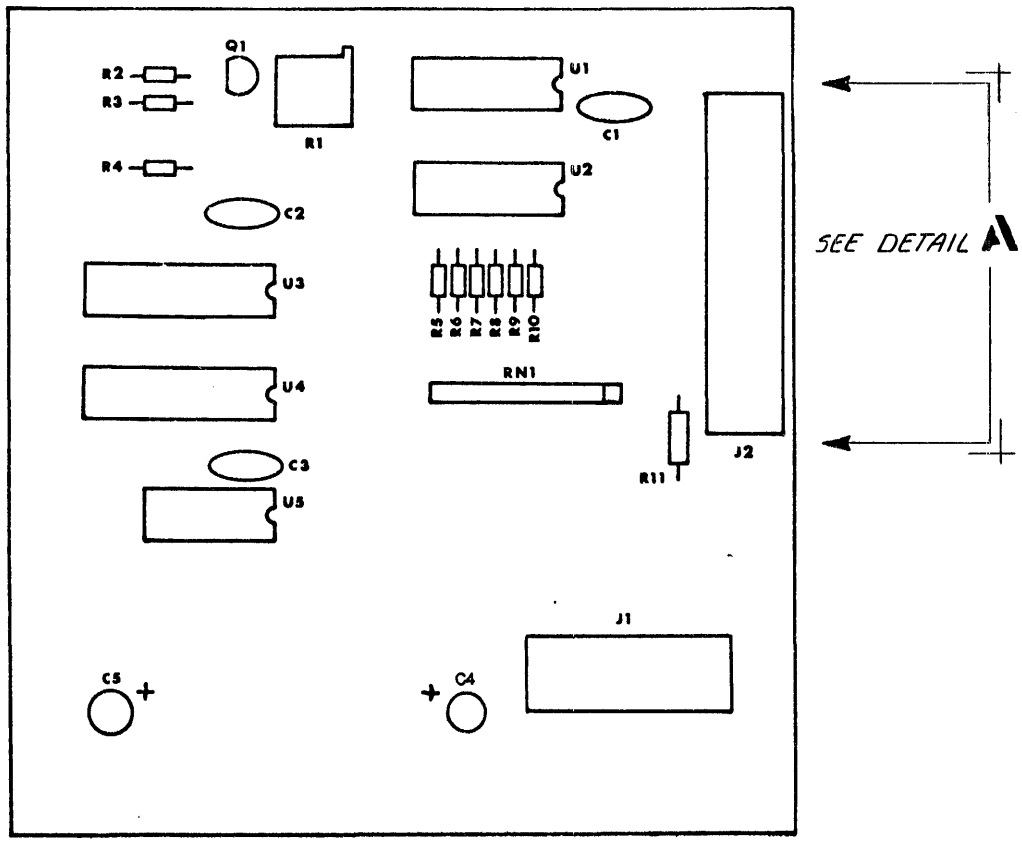
The keyboard audio tone generator, SPKR, is turned off and on (in the same way as the LED's) by a signal on BDB7. The Control Program produces a tone from the tone generator by repeatedly turning the dc drive level off and on at an audio rate. The ERROR tone can therefore easily be different from the "key-pressed" tone. Q1, a 2N3905, acts as an amplifier/driver for the tone generator.

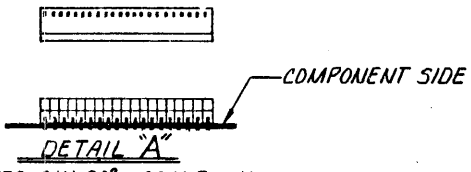
The variable resistor R1 adjusts the audio output level of the tone generator from OFF to full. The level is set so that the tone is easily heard by the analyzer operator but is not annoying to other persons in the area. (The R1 adjustment is also a means of turning the ERROR tone off if it is wanted off along with the key-press feedback tone.)

3.6 SCHEMATIC, BOARD LAYOUT, & PARTS LIST

The schematic diagrams, board layout, and parts list for the Keyboard are contained on the following pages.

REV	DESCRIPTION	DATE	APPROVED
A	PER ECO 078	11-9-79	G.S.
B	PER ECO 084 G.S.	11-27-79	G.S.
C	ECO 140 Bruce	5-31-80	G.S.





DETAIL "A"
ROTATED C.W. 90° SCALE = 1/2

DRAWN BY G.S.	DATE 11-9-79	
CHECKED BY	DATE	
ENG	DATE	
APPR. REL	DATE	
DECIMAL .XXX = ± .005 .XX = ± .02		
FRACTIONAL ± 1/64 ANGULAR ± 0°30'		
BREAK ALL SHARP EDGES		
DO NOT SCALE DRAWING		

PARATRONICS INC.

DESCRIPTION
LEGEND MASTER
540 KEYBOARD INTERFACE

DRAWING NO.	REV.
126-0062-201	C
SCALE 1/1	SHT 1 OF 1

REV.	DESCRIPTION	DATE	APPROVED
B	PER ECO 0845	4-27-77	KFA

POWER			
REFDES	IC	+5V	GND
U1	74LS374	20	10
U2	74LS244	20	10
U3 U4	74LS138	16	8
U5	LS32	14	7

NOTES UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS - 1/4 W. 5%
2. ALL CAPS CERAMIC DISC-20%

KEYBOARD INTERFACE PCB
143-0062-001

KEYBOARD
143-0061-001

SWITCH MATRIX

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR L. M. BOYD 5-28-76
MAT'L	CK [illegible] 6/8/76
FINISH	APPR [illegible]
	BREAK ALL SHARP EDGES. DECIMAL ANGULAR .XX = ± .XXX = ± DO NOT SCALE DRAWING

PARATRONICS INC.

SCHEMATIC DIAGRAM
540 KEYBOARD INTERFACE
AND KEYBOARD

DRWG NO 127-0062-001 REV B
SIZE D SCALE NONE SHT 1 OF 1

SINGLE LEVEL EXPLOSION

09/04/80

PAR143-0062-0090-00 DESCRIPTION : 540 KEYBOARD INTER, OUTSIDE ECO#: 100 REV.CU.: D

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
111-0207-0103-00	D	22 UF 16V CAP. ELECTRO.,RAD.	2	1	0	08/21/80	OPEN	0	C4
C5									
126-0062-0001-00	D	KEYBOARD INTERFACE PC FAB	1	01	0	OPEN	OPEN	0	
114-0021-0001-00	D	36 CONDUCTOR FEMALE CONN	1	01	0	OPEN	OPEN	0	J2
110-0007-0007-00	D	4.7 OHM 1/2 W CF RES	1	1	0	OPEN	OPEN	0	R11
110-0300-0001-00	D	RES. NETWORK,STKPOLE S10-9-1	1	1	0	OPEN	OPEN	0	RN1
110-0005-0047-00	D	220 OHM 1/4W 5% CF RES	7	1	0	OPEN	OPEN	0	R10
R4 R5 R6	R7	R8 R9							
110-0005-0063-00	D	1K OHM 1/4W 5% CF RES	1	1	0	OPEN	OPEN	0	R3
110-0005-0055-00	D	470 OHM 1/4W 5% CF RES	1	1	0	OPEN	OPEN	0	R2
110-0201-0001-00	D	POT, BOURNS 3386P-1-102	1	1	0	OPEN	OPEN	0	R1
111-0004-0072-00	D	.1 UF 25V CAP. CD	3	1	0	OPEN	OPEN	0	C1
C2 C3									
112-0101-0001-00	B	TRANSISTOR, 2N3905	1	1	0	OPEN	OPEN	0	Q1

LEGEND UM : 01=EACH 02=INCH 03=FEET 04=BULK 05=AS REQUIRED 06=OTHER
LEGEND KEY: A=W/PARTS LIST D=W/O PARTS LIST R=REFERENCE DOCUMENT S=SPECIFICATION

****

P A R A T R O N I C S I N C .

S I N G L E L E V E L E X P L O S I O N

09/04/80

PAR143-0062-0001-00 DESCRIPTION : 540 KEYBOARD INTERFACE ECO#: 100 REV.CU.: D

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
143-0062-0090-00	D	540 KEYBOARD INTER, OUTSIDE	1	01	0	OPEN	OPEN	100	
127-0062-0001-00	D	SCHEMATIC	1	01	0	OPEN	OPEN	0	
124-0024-0001-00	D	INTERFACE CABLE ASSY	1	01	0	OPEN	OPEN	0	J1
113-0003-0032-00	D	I.C., 74LS32	1	1	0	OPEN	OPEN	0	U5
113-0003-0244-00	D	I.C., 74LS244	1	1	0	OPEN	OPEN	0	U4
113-0003-0374-00	D	I.C., 74LS374	1	1	0	OPEN	OPEN	0	U3
113-0003-0138-00	D	I.C., 74LS138	2	1	0	OPEN	OPEN	0	U1
U2									

LEGEND UM : 01=EACH 02=INCH 03=FEET 04=BULK 05=AS REQUIRED 06=OTHER
LEGEND KEY: A=W/PARTS LIST D=W/O PARTS LIST R=REFERENCE DOCUMENT S=SPECIFICATION

****

4.0 DISPLAY MODULE

4.0 DISPLAY MODULE

4.1 INTRODUCTION

The Display Module is a Motorola Model M2000-155 CRT Monitor with a 9" CRT. It accepts a composite video signal from the Video Display Board and produces a raster-scan video display. No operator controls are required, but internal controls for maintenance adjustments are provided. The only input power required by the Module is +12 V at 900 mA from the PI 540 Power Supply.

CAUTION: A VERY HIGH VOLTAGE OF 9 kV IS USED IN THE DISPLAY MODULE. EXTREME CAUTION MUST BE USED WHENEVER POWER IS APPLIED TO THE PI 540 WITH THE COVER REMOVED.

4.2 FUNCTIONAL DESCRIPTION

Full details of the Display Module are contained in Motorola's Service Manual for the M2000 series, a copy of which is included at the end of this section. A block diagram may be found on page 6 of that document, component layouts on pages 12 and 13, and a schematic diagram on page 14. A detailed description of CRT replacement and adjustment is given on page 4. However, please read the following Self-Test and CRT Adjustment sectionss before making any adjustments.

4.2.1 AC Mains Frequency

While the Display Module itself does not use any mains power, primary mains power is brought into the PI 540 to operate the Power Supply. As a consequence, there are mains-frequency fields within the instrument which may produce minor interaction with the CRT display. To minimize this interaction, the frequency of the vertical sync signal produced on the Video Display Board is adjusted as closely as possible to the mains frequency. (The vertical sync signal is contained in the composite video signal fed to the Display Module from the Video Display Board.)

This adjustment of the vertical sync frequency is automatically made by the Control Program at power-ON time (for details, refer to the Sync Generator discussion in the Video Display section). However, the automatic adjustment can be overridden by power-ON hold-down of the "5" key to set 50 cycles or the "6" key to set 60 cycles. (Please see the following subsection for details.)

(The sync frequency override can be done experimentally to observe the effects of the wrong frequency. Hold down the "0" key simultaneously with the "5" or "6" key at power-ON. There should be a barely discernible flicker of the display when the wrong frequency is used. This flicker is more apparent when viewed with peripheral vision, as when the eye is fixed on the "Timing" key in the top row on the keyboard. However, if there are strong mains-frequency fields being produced nearby, the effects of the improper sync

frequency may be more drastic. Sometimes there will be a noticeable swimming of the image in addition to the flicker.)

4.2.2 Self Test

A special self-test function for the Display Module can be initiated from the keyboard by holding down the "0" key as the power switch is turned from OFF to ON. Keep the key depressed (for about 2 seconds after the power is ON) until a beep is heard. The CRT screen will be filled with a uniform pattern of horizontal and vertical lines. Use this pattern to appraise the quality of the display. If necessary, make adjustments as described in the following subsection.

4.2.3 CRT Adjustment Procedure

The Display Module, and in particular the CRT, is subject to component aging and may require occasional adjustment. Any adjustments that are found necessary should be made in accordance with the following instructions.

WARNING: THE DISPLAY MODULE CONTAINS A VERY HIGH VOLTAGE OF 9 kV WHICH CAN BE LETHAL. THE FOLLOWING PROCEDURES SHOULD ONLY BE UNDERTAKEN BY EXPERIENCED TECHNICAL PERSONNEL FAMILIAR WITH TELEVISION OR CRT MONITOR ADJUSTMENT PROCEDURES.

---

1. With the power switch OFF, unplug the power cord. Close and latch the keyboard and stand the analyzer on the keyboard end. Remove the 6 cover screws located on the bottom of the instrument. Remove the cover by sliding it to the rear of the instrument (upwards).

2. Return the instrument to normal operating position but leave the cord unplugged. In preparation for removing the Application subassembly, take a pair of slip-joint pliers and carefully unplug the power supply connector, P9, from the Function Motherboard. Also, taking note of the orientation for later reinsertion, carefully remove the wide ribbon cable that interconnects the two motherboards. Remove the four screws that fasten the Function Motherboard to the chassis and carefully lift out the Application subassembly. This opens up a space that permits adjustment of the various controls in the Display Module.

3. Make all adjustments with PLASTIC adjusting wands designed for the purpose. DO NOT USE METAL SCREWDRIVERS OR ANY METAL TOOL. If you do not have suitable instruments, postpone the adjustments until you can get them.

4. Unlatch the keyboard and place it in operating position. Make sure that the power switch is OFF and then plug in the power cord. Bring the self-test pattern to the CRT screen by holding down the "0" key at power-ON as described in the foregoing Self-Test section.

5. If the grid pattern on the CRT shows skewing of the horizontal lines at the top of the screen, adjust R35, the HORIZONTAL HOLD control, to remove

the skewing. (Please refer to the Component Layouts on pages 12 and 13 of the Motorola Service Manual for the location of this and other controls.) Turn the power OFF for a few seconds and then back ON again with the "0" key down. If the horizontal sync does not lock in quickly and reliably, readjust the R35 control for reliable sync without skewing.

6. There should be approximately 1/4" margin to the grid pattern at the top and bottom of the screen when viewed from the normal angle (probably about 15 degrees downward). If the margins are improper, adjust R52, the VERTICAL SIZE control. (Do not be concerned with exact centering at this point.)

7. If the spacing between horizontal lines is not approximately equal from the top of the screen to the bottom, adjust R57, the VERTICAL LINEARITY control for best linearity. (There is some interaction between R57 and R52, above. Readjust each in turn until proper settings are obtained.)

8. There should be approximately 1/4" margin to the grid pattern at the left and right sides of the screen. If the margins are improper, adjust the L1 tuning slug, the HORIZONTAL WIDTH control. (Do not be concerned with exact centering at this point.)

9. If the grid pattern is not approximately centered on the screen when viewed from the normal angle, adjust the two tabbed, flat metal rings, called RASTER CENTERING MAGNETS, that encircle the CRT neck directly behind the deflection yoke (see figure 1 on page 5 of the Motorola Manual). Before starting this adjustment, TURN THE POWER OFF and mark the present setting of the rings (for orientation and for possible return), then turn the power back ON with the "0" key down. KEEP YOUR HANDS WELL CLEAR OF THE 9 kV TRANSFORMER AND LEAD and be sure to use a PLASTIC tool. This adjustment will affect pincushion distortion, and the two rings must be adjusted alternately to obtain reasonable centering with a minimum of distortion.

10. Press the CONFIG key and select the 8 CHNL TIMING/STATE menu to produce a display that is well populated with characters, reverse video, etc. If necessary, adjust controls R63 (BRIGHTNESS), R5 (CONTRAST), and R61 (FOCUS) as discussed below. There is interaction between these controls, and some iteration may be necessary.

Adjust FOCUS for the best compromise between maximum sharpness at the center and maximum sharpness at the edges.

Adjust CONTRAST and BRIGHTNESS with the following points in mind.

a. The background should be dark enough that the raster scan lines are not visable in normal room light.

b. Too much brightness will cause the reverse-video fields to bloom and partially obscure the dark characters.

c. Too-bright characters will not focus well.

Change to the 32 CHNL STATE menu and press RESET. With the State circuit boards removed, a false triggering will occur and the display will have all Fs for data. Make sure that the CONTRAST and BRIGHTNESS adjustments are such

that there is a marked difference between the half-brightness of the memory addresses and the full-brightness of the data.

Change back to the 8 CHNL TIMING/STATE menu and check for a good overall display.

11. TURN THE POWER OFF AND UNPLUG THE POWER CORD. Replace the ribbon cable that interconnects the two motherboards. Taking careful note of the keying so that you do not try to force the wrong card into a slot, replace the Applications circuit boards. Replace the cover, and plug in the power cord.

4.3 SCHEMATIC, BOARD LAYOUT, & PARTS LIST

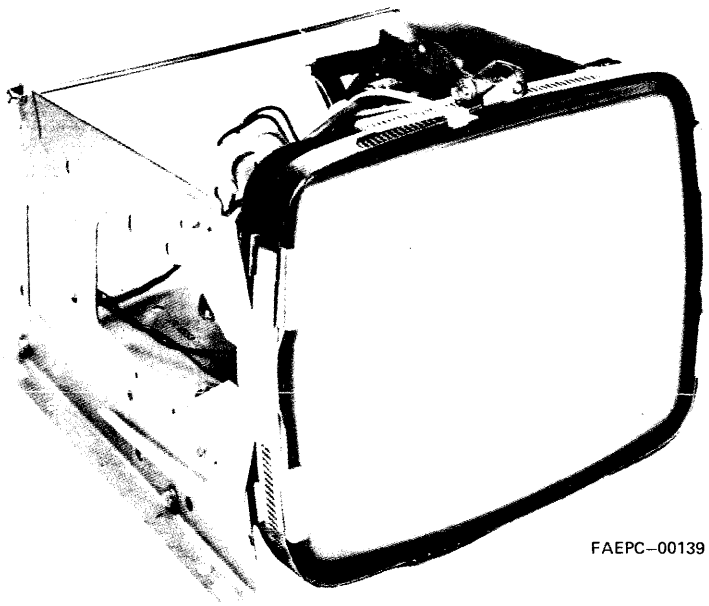
The schematic diagram, component layouts, and parts list for the Display Module are contained in the Motorola Service Manual which is immediately following. The schematic diagram is on page 14; the component layouts are on pages 12 and 13; and the parts list is on pages 17 and 18.

MOTOROLA INC.

Service Manual

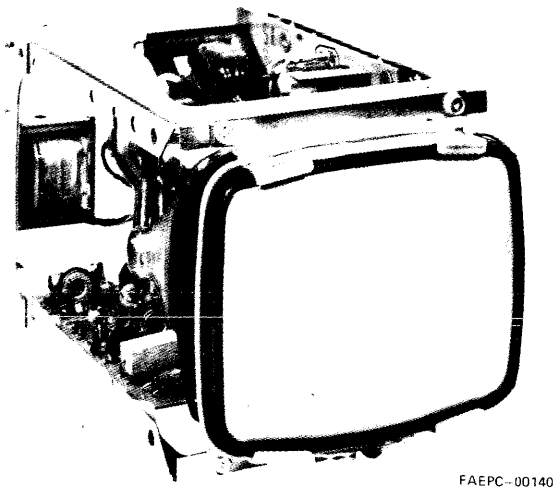
M1000 and M2000 SERIES

(See Table 1)



FAEPC–00139

MODEL M2000 (9"– CRT)



FAEPC–00140

MODEL M1000 (5" – CRT)

TABLE 1

MODEL	SIGNAL INPUT	*CRT SIZE & PHOSPHOR
M1000–100	TTL	5" P4
M1000–155	COMPOSITE	5" P4
M1000–190	DIRECT DRIVE	5" P4
M2000–100	TTL	9" P4
M2000–155	COMPOSITE	9" P4
M2000–355	COMPOSITE	9" P31

*All CRT's are without anti-reflective faceplates.

CAUTION

NO WORK SHOULD BE ATTEMPTED ON ANY EXPOSED MONITOR CHASSIS BY ANYONE NOT FAMILIAR WITH SERVICING PROCEDURES AND PRECAUTIONS.

GENERAL INFORMATION

The models described herein are fully transistorized (except CRT) and applicable for displaying alphanumeric characters. All models will accept TTL or composite video inputs depending on jumper positioning. The exception is Model M1000-190 which is designed for direct drive applications only.

NOTE: The Model M2000-100 (TTL) is supplied factory wired as a model M2000-155 (composite video) version. See schematic diagram for jumper locations.

The CRT'S employed are of the magnetic deflection type with integral implosion protection. An operating voltage of 12 volts DC @ 650 mA (typical) is required from an external power supply for the M1000 models. The M2000 models require an external 12 volts DC @ 900 mA (typical).

Input and output connections for these models are made through a 10–pin edge connector on the signal circuit card. Output connections are provided for an optional remote brightness control, except on the Model M1000–190.

Two plug–in etched circuit cards are utilized, a signal circuit card and a deflection circuit card. Components are mounted on the top of the circuit cards and copper foil on the bottom. Schematic reference numbers are printed on the top and bottom of each circuit card to aid in the location and identification of components for servicing. All standard operating/adjustment controls are mounted in a convenient manner on both circuit cards.

MOTOROLA INC.

Display Systems

1155 Harvester Rd., West Chicago, IL. 60185 (312) 231-4400

VP16
2/79

PART NO. 68P25253A23–3
PRINTED IN U.S.A.

SAFETY WARNING

CAUTION: NO WORK SHOULD BE ATTEMPTED ON AN EXPOSED MONITOR CHASSIS BY ANYONE NOT FAMILIAR WITH SERVICING PROCEDURES AND PRECAUTIONS.

1. SAFETY PROCEDURES should be developed by habit so that when the technician is rushed with repair work, he automatically takes precautions.

2. A GOOD PRACTICE, when working on any unit, is to first ground the chassis and to use only one hand when testing circuitry. This will avoid the possibility of carelessly putting one hand on chassis or ground and the other on an electrical connection which could cause a severe electrical shock.

3. Extreme care should be used in HANDLING THE PICTURE TUBE as rough handling may cause it to implode due to atmospheric pressure (14.7 lbs. per sq. in.). Do not nick or scratch glass or subject it to any undue pressure in removal or installation. When handling, safety goggles and heavy gloves should be worn for protection. Discharge picture tube by shorting the anode connection to chassis ground (not cabinet or other mounting parts). When discharging, go from ground to anode or use a well insulated piece of wire. When servicing or repairing the monitor, if the cathode ray tube is replaced by a type of tube other than that specified under the Motorola Part Number as original equipment in this Service Manual, then avoid prolonged exposure at close range to unshielded areas of the cathode ray tube. Possible danger of personal injury from unnecessary exposure to X-ray radiation may result.

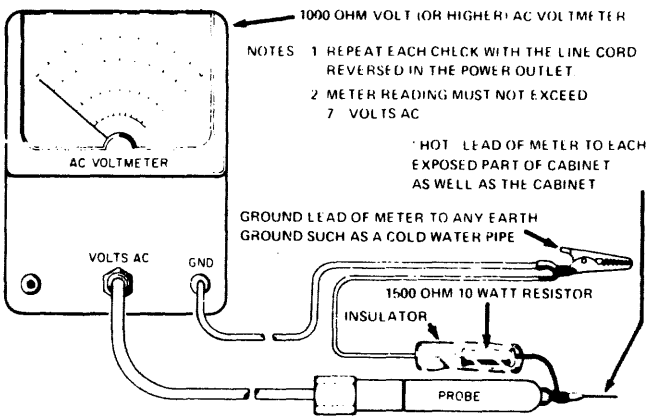
4. An ISOLATION TRANSFORMER should always be used during the servicing of a unit whose chassis is connected to one side of the power line. Use a transformer of adequate power rating as this protects the serviceman from accidents resulting in personal injury from electrical shocks. It will also protect the chassis and its components from being damaged by accidental shorts of the circuitry that may be inadvertently introduced during the service operation.

5. Always REPLACE PROTECTIVE DEVICES, such as fishpaper, isolation resistors and capacitors and shields after working on the unit.

6. If the HIGH VOLTAGE is adjustable, it should always be ADJUSTED to the level recommended by the manufacturer. If the voltage is increased above the normal setting, exposure to unnecessary X-ray radiation could result. High voltage can accurately be measured with a high voltage meter connected from the anode lead to chassis.

7. BEFORE RETURNING A SERVICED UNIT, the service technician must thoroughly test the unit to be certain that it is completely safe to operate without danger of electrical shock. DO NOT USE A LINE ISOLATION TRANSFORMER WHEN MAKING THIS TEST.

In addition to practicing the basic and fundamental electrical safety rules, the following test, which is related to the minimum safety requirements of the Underwriters Laboratories should be performed by the service technician before any unit which has been serviced is returned.



Voltmeter Hook-up for Safety Check

A 1000 ohm per volt AC voltmeter is prepared by shunting it with a 1500 ohm, 10 watt resistor. The safety test is made by contacting one meter probe to any portion of the unit exposed to the operator such as the cabinet trim, hardware, controls, knobs, etc., while the other probe is held in contact with a good "earth" ground such as a cold water pipe.

The AC voltage indicated by the meter may not exceed 7½ volts. A reading exceeding 7½ volts indicates that a potentially dangerous leakage path exists between the exposed portion of the unit and "earth" ground. Such a unit represents a potentially serious shock hazard to the operator.

The above test should be repeated with the power plug reversed, when applicable.

NEVER RETURN A MONITOR which does not pass the safety test until the fault has been located and corrected.

ELECTRICAL SPECIFICATIONS *

	MODEL M1000	MODEL M2000
PICTURE TUBE (CRT):	5" measured diagonally (127 mm); 13 sq. in. viewing area (84 sq. cm); 55° deflection angle; P4 phosphor standard	9" measured diagonally (228 mm); 44 sq. in viewing area (284 sq.cm); 90° deflection angle; integral implosion protection; P4 phosphor standard except P31 phosphor in Model M2000-355.
POWER INPUT:	12V DC at 650 mA	12V DC at 900 mA
INPUT SIGNALS:	COMPOSITE VIDEO INPUT: 0.5V to 2.5V composite P/P, sync negative (input impedance: 74 ohms terminated, 12k ohms unterminated), or TTL INPUT: 2.5V to 5.0V P/P, video drive, sync positive at input (input impedance: 75 ohms video termination, >2k ohms vertical and horizontal) DIRECT DRIVE INPUT: 2.5V to 5.0V P/P, video drive, negative vertical sync (190 uSec min., 1.4 uSec max.), positive horizontal drive (25 uSec min. to 30 uSec max.). (Input impedance: 75 ohms video termination, >330 ohms horizontal drive, >2k ohms vertical sync.)	
RESOLUTION:	650 lines center, 500 lines corners	
VIDEO RESPONSE:	Within −3 dB, 10 Hz to 12 MHz	
LINEARITY:	Within 2% as measured with standard EIA ball chart and dot pattern	
HIGH VOLTAGE:	9.0 kV at 50 uA beam current, nominal	
HORIZONTAL RETRACE TIME:	11.0 uSec maximum	
SCANNING FREQUENCY:	Horizontal: 15,750 Hz ±500 Hz; Vertical: 50/60 Hz	
ENVIRONMENT:	Operating temperature: 0° C to 50° C Storage temperature: −40° C to +65° C Operating altitude: 10,000 feet maximum (3048 meters) Designed to comply with applicable DHEW rules on X-Radiation Designed to enable listing under UL Specification 478	
TYPICAL DIMENSIONS:	4.60" H, 5.12" W, 8.68" D (without power supply) (117 x 130 x 220 mm)	7.25" H, 9.50" W, 9.48" D (184 x 241 x 241 mm)

* Specifications subject to change without notice.

TABLE OF CONTENTS

SERVICE NOTES

CIRCUIT TRACING

Component reference numbers are printed on the top and bottom of the plug-in circuit cards to facilitate circuit tracing. In addition, control names and circuit card terminal numbers are also shown and referenced on the schematic diagrams in this manual.

Transistor elements are identified as follows:

E – emitter, B – base, and C – collector.

COMPONENT REMOVAL

Removing components from an etched circuit card is facilitated by the fact that the circuitry (copper foil) appears on one side of the circuit card only and the component leads are inserted straight through the holes and are not bent or crimped.

It is recommended that a solder extracting gun be used to aid in component removal. An iron with a temperature controlled heating element would be desirable since it would reduce the possibility of damaging the circuit card foil due to overheating.

The nozzle of the solder extracting gun is inserted directly over the component lead and when sufficiently heated, the solder is drawn away leaving the lead free from the copper foil. This method is particularly suitable in removing multi-terminal components.

POWER TRANSISTOR REPLACEMENT

When replacing the "plug-in" transistor, please observe the following precautions:

1. The transistor heat sink is not "captive", which means that the transistor mounting screws also secure the heat sink. When installing the transistor, the heat sink must be held in its proper location.

2. When replacing the plug-in transistor, silicone grease (Motorola Part No. 11M490487) should be applied evenly to the top of the heat sink and bottom of the transistor.

3. The transistor mounting nuts must be tight before applying power to the monitor. This insures proper cooling and electrical connections. NON–COMPLIANCE WITH THESE INSTRUCTIONS CAN RESULT IN FAILURE OF THE TRANSISTOR AND/OR ITS RELATED COMPONENTS.

– NOTE –

Use caution when tightening transistor mounting nuts. If the screw threads are stripped by excessive pressure, a poor electrical and mechanical connection will be made.

CRT REPLACEMENT

Use extreme care in handling the CRT as rough handling may cause it to implode due to high vacuum. Do not nick or scratch glass or subject it to any undue pressure in removal or installation. Use goggles and heavy gloves for protection. In addition, be sure to disconnect the monitor from all external voltage sources.

1. Discharge CRT by shorting 2nd anode to ground; then remove the CRT socket, deflection yoke and 2nd anode lead.

2. Remove CRT from chassis by loosening the one screw that secures the CRT mounting strap or retaining ring.

3. Install new CRT and proceed to horizontal linearity, centering and beam alignment procedures.

HORIZONTAL OSCILLATOR ADJUSTMENT

– NOTE –

Not applicable to Model M1000–190.

Step 1. Turn on monitor and set up for normal operation.

Step 2. Locate the HORIZ. HOLD control, R35, on the Signal circuit card.

Step 3. Begin rotating R35 CCW until the video display is out of horizontal sync. At this point rotate R35 back CW until the video display just locks in horizontally; then stop. Using tape, mark the left–hand edge of the video display (not the raster edge) of the CRT faceplate.

Step 4. Continue rotating R35 CW until the video display is out of horizontal sync again in the opposite direction. At this point rotate R35 back CCW until the video just locks in horizontally; then stop. Mark the left–hand edge of the video display on the CRT faceplate again.

Step 5. Observe the distance between the two marks on the CRT faceplate. The object is to rotate the HORIZ. HOLD control, R35, until the left–hand edge of the video display is centered between the two marks on the CRT faceplate.

VIDEO BIAS ADJUSTMENT

– NOTE –

Not applicable to Model M1000–190.

Step 1. With the monitor operating, rotate the CONTRAST CONTROL, R6,for minimum contrast; then disconnect the input signal(s).

Step 2. Connect a voltmeter across R18 (negative probe toward the collector of Q4).

Step 3. Adjust the VIDEO BIAS control, R14, for a $+2.0 \pm .05$ volt indication.

Step 4. Disconnect the voltmeter.

Step 5. Reconnect the input signal(s) and adjust the CONTRAST control, R6, for desired contrast.

HORIZONTAL LINEARITY ADJUSTMENT

– NOTE–

This adjustment procedure is required only when a CRT and/or deflection yoke have been replaced.

PROCEDURE

Step 1. Disconnect monitor from power supply.

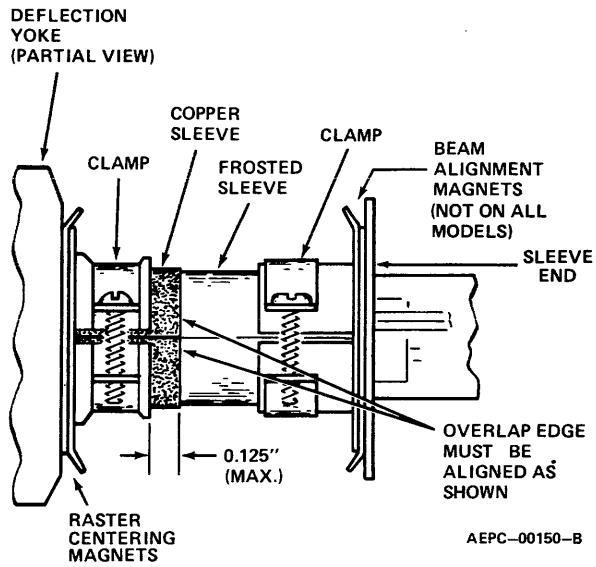


Figure 1. Partial View of CRT Neck/Deflection Yoke for Horiz. Linearity Adjustment

Step 2. (M2000 ONLY) Locate the S–SHAPING transformer, T3, on the deflection circuit card; then rotate its slug down to the bottom. (This action temporarily minimizes the effect of T3 being in the circuit.)

Step 3. (Refer to Figure 1.) Loosen the deflection yoke clamp screw just enough to permit sliding the copper sleeve on the CRT neck back and forth.

Step 4. (Refer to Figure 1.) Position the copper sleeve so that only 1/8" (.125") extends out past the rear lip of the deflection yoke. In addition, be sure that the overlap edge of the copper sleeve is aligned properly and not twisted.

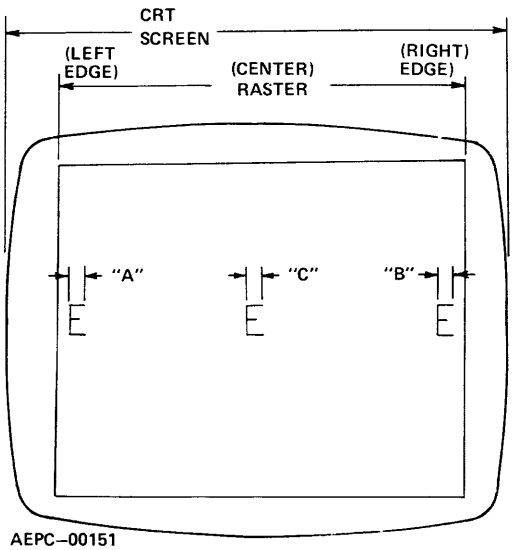


Figure 2. Partial CRT Raster Display of Characters for Adjustment

Step 5. Tighten the clamp screw carefully so as not to disturb the yoke position.

Step 6. Connect the monitor to its power supply and set up for normal operation.

Step 7. (Refer to Figure 2.) Observe the extreme left-hand edge characters (designated "A" in Figure 2). Its width should be equal to the width of the right–hand edge characters (designated "B" in Figure 2). If character "A" is wider than character "B", the copper sleeve is extending out too far. If "A" is narrower than "B", the copper sleeve should be pulled out further. In any event, the copper sleeve may have to be repositioned by trial and error if the 0.125–inch dimension does not provide desired linearity. Continue until the width of character "A" is equal to the width of character "B".

— NOTE —

Steps 8–11 are applicable only for the M2000 monitor.

Step 8. With the M2000 monitor turned on and operating normally, observe the width of the center character (designated "C" in Figure 2). It should be narrower than characters "A" and "B".

Step 9. Connect an oscilloscope (AC coupled) between the blue wire pin (on deflection circuit card) and chassis ground. A parabolic waveform should appear.

Step 10. Begin rotating the slug of T3 upward (away from circuit card) until the amplitude of the waveform is 125 volts P–P. This setting will equalize the width of character "C" to that of characters "A" and "B".

Step 11. Disconnect oscilloscope.

RASTER CENTERING (Figure 1)

– NOTE –

For Model M1000–190 refer to video centering. For models without beam alignment magnets, proceed to Step 2. Raster centering is factory set and should not normally require further adjustment.

Step 1. Position the tabs of the beam alignment magnets such that they are horizontally opposing.

Step 2. Adjust vert. size (R52) and horiz. width (L1) such that all edges of the raster are visible.

Step 3. Position raster centering magnets for best centering of raster.

Step 4. Readjust size to specified dimensions or approximately 3 3/4" wide x 2 5/8" high for M1000 series and 6½" wide x 4" high for M2000 series monitors.

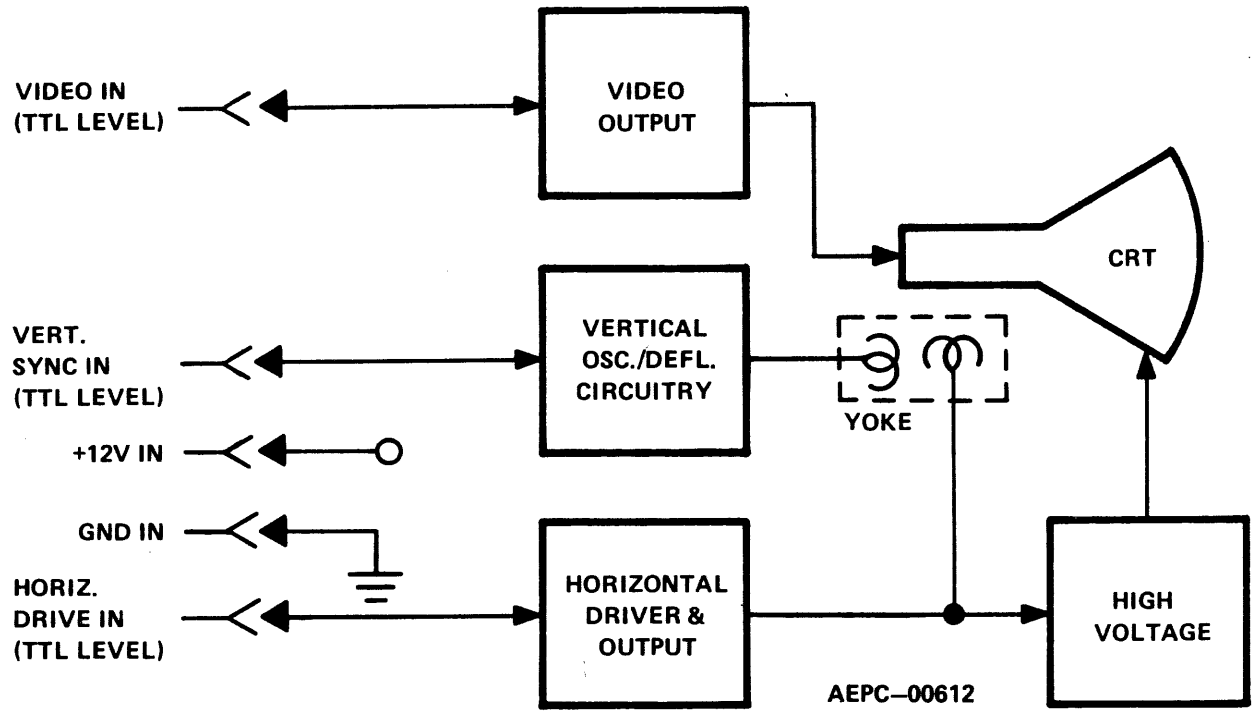
VIDEO CENTERING (For M1000–190 only) (Figure 1)

– NOTE –

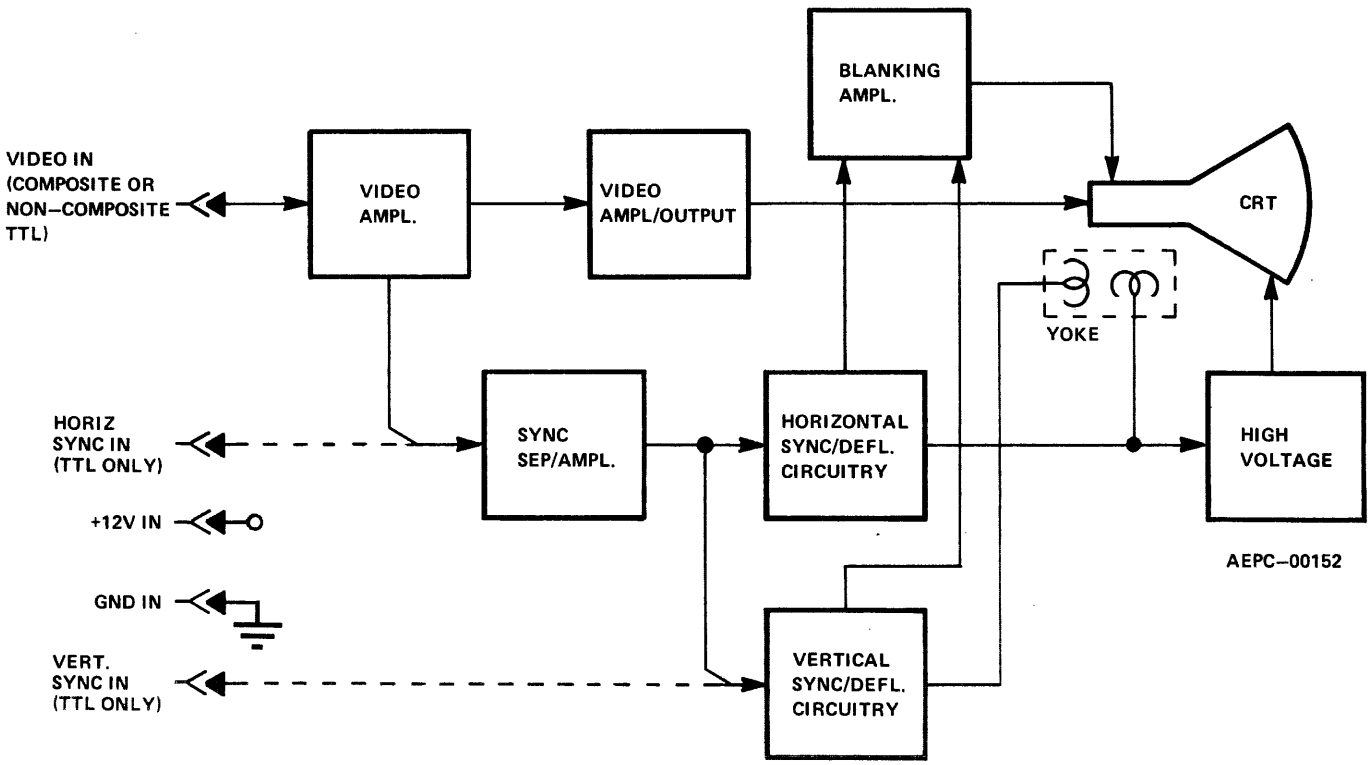
For models without beam alignment rings, proceed to Step 2. Video centering is factory set and should not normally require further adjustment.

Step 1. Position the tabs of the beam alignment magnets such that they are horizontally opposing.

Step 2. Adjust vert. size (R52) and horiz. width (L1) such that all edges of the video are visible.



Block Diagram (Model M1000–190 only)



Block Diagram (All Models except M1000–190)

Step 3. Position raster centering magnets for best centering of video.

Step 4. Readjust size to specified dimensions or approximately 3 3/4" wide x 2 5/8" high for M1000 series and 6 ½" wide x 4" high for M2000 series monitors.

CRT BEAM ALIGNMENT (Figure 1)

For optimum character quality in the corners of the video display, a beam alignment magnet may be used on the monitor CRT. If not used disregard the following procedure.

– NOTE –

Adjustment of the raster centering rings must precede the adjustment of the beam alignment magnet.

PROCEDURE

The beam alignment magnet should be positioned on the neck of the CRT between the deflection yoke and the tube base. The correct location of the rings is approximately over the second grid of the electron gun (Figure 1).

Step 1. Adjust the display brightness for optimum viewing.

Step 2. Adjust the focus voltage for optimum overall focus.

Step 3. Loosen the beam alignment magnet clamping screw just enough to allow the assembly free movement on the CRT neck.

Step 4. While observing the tails on the dots in the corners of the display, rotate the focus rings to minimize the tails.

Step 5. Tighten the clamping screw.

THEORY OF OPERATION

GENERAL

The following circuit description is applicable to monitors using a composite video input signal. For monitors using TTL inputs, the description is basically the same. However, the horizontal and vertical sync pulses are coupled from an external source through separate inputs. In addition, jumpers JU 1 and JU2 will be relocated to the TTL position.

The direct drive model M1000–190 utilizes only output circuitry. The development and processing of the driving signals is performed externally from the monitor and applied to separate inputs similar to the TTL models. Therefore, the following circuit descriptions are also applicable to the direct drive version. (See block diagrams.)

VIDEO AMPLIFIER CIRCUIT (Figure 3.)

The video amplifier consists of four stages that include Q1, Q2, Q3 and Q4. The first stage, Q1, functions as an emitter follower. The low output impedance of this first stage permits use of a low resistance CONTRAST control, R6, which furnishes flat video response over its entire range without the need for compensation. The collector output of Q1 is used to drive the sync separator, Q5. Capacitor C2 provides high frequency roll–off to limit the collector output to the bandwidth required to pass synchronization signals.

Transistors Q2 and Q3 form a direct coupled amplifier with frequency compensation provided by C40 and C41. The output from Q3 is capacitively coupled (C5) to the base of Q4, video output stage. The video bias control, R14, is used to set the quiescent collector current of Q4. Frequency compensation is provided by R17 and C6. The combined action of clamping diode D1 and capacitor C5 provide DC restoration for the video signal.

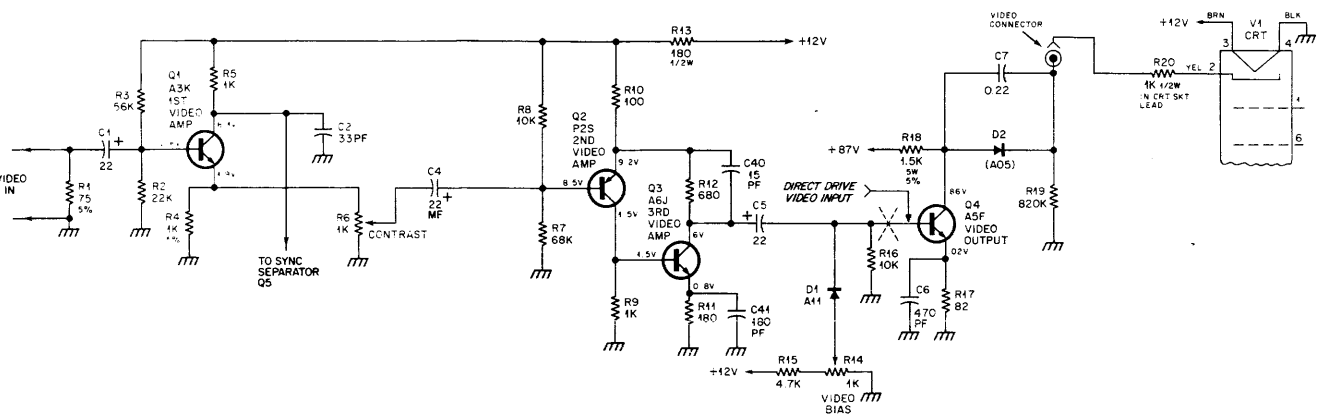


Figure 3. Video Amplifier Circuit

Components C7, D2 and R19 provide CRT beam current limiting. Diode D2 is normally forward–biased; therefore, as Q4 conducts, its collector voltage drops. This causes a larger beam current to flow through R19, which in turn causes its voltage drop to rise. If excessive beam current flows, the voltage developed across R19 becomes greater than the collector voltage of Q4. This action reverse-biases D2, which prevents a further increase in beam current. Capacitor C7 helps couple video to the CRT cathode, pin 2, through R20. Resistor R20 is used to isolate Q4 from transients that may occur as a result of CRT arcing.

SYNC SEPARATOR/AMPLIFIER CIRCUIT

(Reference Figure 4.)

The sync separator employs two stages. Transistor Q5 is the sync separator and Q6 is the sync amplifier. The video input to the sync separator is black positive. Capacitor C3 is charged by the peak base current that flows when the positive peak of the input takes Q5 to saturation. This charge depends on the peak to peak input to Q5 and thus makes the bias for Q5 track the amplitude of the input signal. As a result, Q5 amplifies only the positive peaks of the input signal. The initial bias current through R23 sets the clipping level.

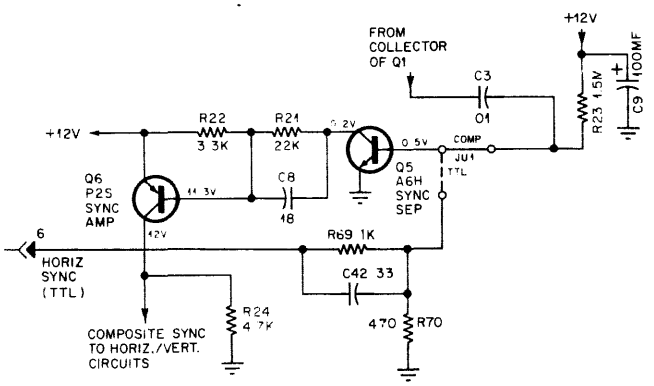


Figure 4. Sync Separator/Amplifier Circuit

PHASE DETECTOR (AFC)

(Reference Figure 5.)

The phase detector control consists of two diodes (D3 & D13) in a keyed clamp circuit. Two inputs are required to generate the required output, one from the sync amplifier, Q6, and one from the horizontal output circuit, Q8. The required output must be of the proper polarity and amplitude to correct phase differences between the input horizontal sync pulses and the horizontal time base. The horizontal output (Q8) collector pulse is integrated into a sawtooth by R28, C13 and R29. During horizontal sync time, both diodes conduct, which shorts C13 to ground. This effectively clamps the sawtooth on C13 to ground at sync time. If the horizontal time base is in phase with the sync (waveform A), the sync pulse will occur when the sawtooth is passing through its AC axis and the net charge on C13 will be zero (waveform B). If the horizontal time base is lagging the sync, the sawtooth on C13 will be clamped to ground at a point negative from the AC axis. This will result in a positive DC charge on C13 (waveform C). This is the correct polarity to cause the horizontal oscillator to speed up to correct the phase lag. Likewise, if the horizontal time base is leading the sync, the sawtooth on C13 will be clamped at a point positive from its AC axis. This results in a net negative charge on C13, which is the required polarity to slow the horizontal oscillator (waveform D).

Passive components R30, R31 and C16 comprise the phase detector filter. The bandpass of this filter is chosen to provide correction of horizontal oscillator phase without ringing or hunting. Optional capacitor C14 (when present) times the phase detector for correct centering of the picture on the raster.

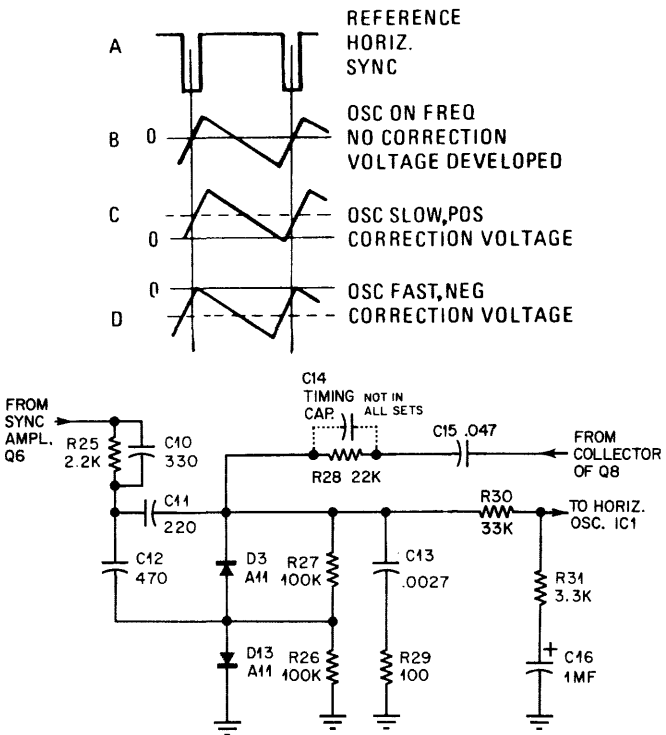


Figure 5. Phase Detector (AFC) Circuit

HORIZONTAL OSCILLATOR AND DRIVER

(Reference Figure 6.)

The horizontal oscillator consists of integrated circuit IC1, which is essentially a voltage controlled oscillator with variable mark–space ratio (duty cycle) and internal voltage reference. The reference voltage is present at pin 6, while resistors R37 and R38 determine the mark–space ratio. The main oscillator timing capacitor is C17, with its charging current derived from three sources: (a) a fixed current from R33, (b) a variable current from R34 and HORIZ. HOLD control R35, (c) and a correcting current from the phase detector (AFC) network through R32. The combination of these three charging currents and C17 determine the horizontal frequency.

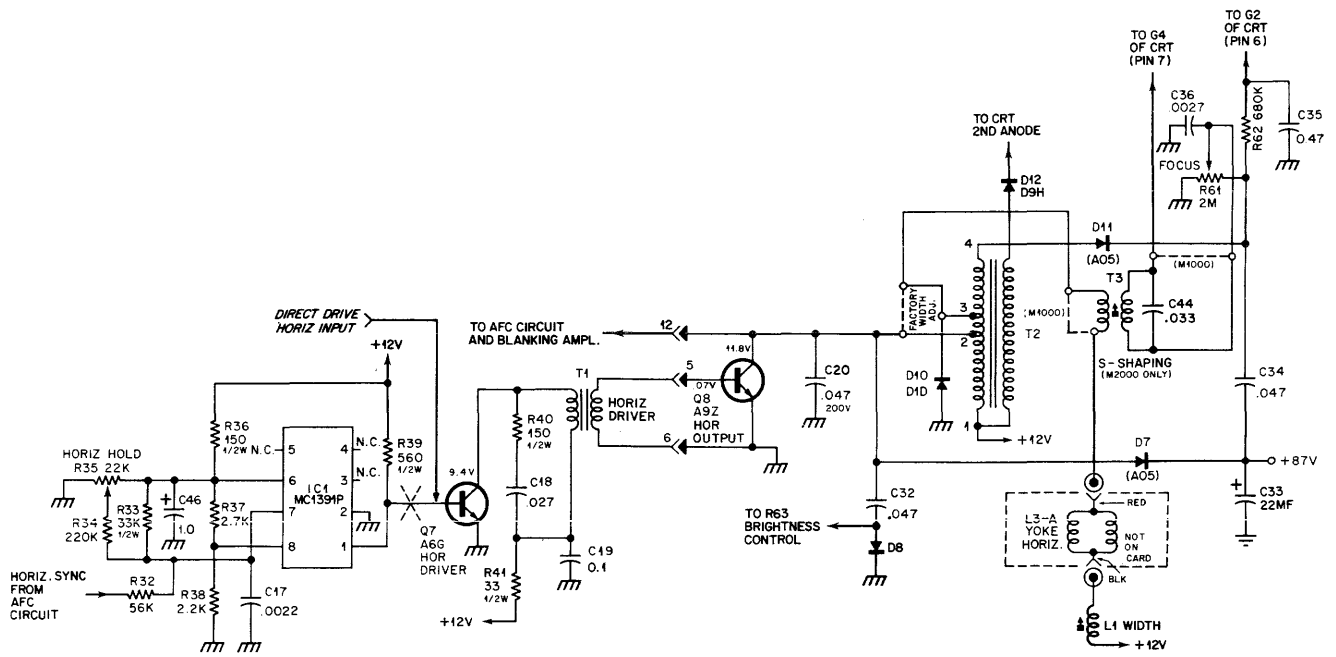


Figure 6. Horizontal Circuit

The output from IC1 (pin 1) is a square wave of proper frequency and duration, which is applied to the base of horizontal driver Q7. The output from Q7 is coupled via the horizontal driver transformer T1 (current step–up) to the base of horizontal output device Q8. Components R41 and C19 provide current limiting, while components R40 and C18 provide transformer damping to suppress ringing in the primary of T2 when Q7 goes into cutoff.

HORIZONTAL OUTPUT

(Reference Figure 6.)

The secondary of T1 provides the required low drive impedance for Q8. Once during each horizontal period, Q8 operates as a switch that connects the supply voltage across the parallel combination of the horizontal deflection yoke (L3–A) and the primary of the high voltage transformer, T2. The required sawtooth deflection current (through the horizontal yoke) is formed by the L–R time constant of the yoke and primary winding of transformer T2. The horizontal retrace pulse charges C33 through D7 to provide +87V.

Momentary transients at the collector of Q8, should they occur, are limited to the voltage on C33 since D7 will conduct if the collector voltage exceeds this value.

The damper diode, D10, conducts during the period between retrace and turn on of Q8. Capacitor C20 is the retrace tuning capacitor. Coil L1 is a series HORIZ. WIDTH control. Components C32 and D8 generate a negative voltage necessary to properly bias the CRT. A copper sleeve on the neck of the CRT shapes the horizontal magnetic field for proper linearity.

Pin 4 of the high voltage transformer, T2, is a boost winding, which together with components D11 and C34, develops a +400 volts for G2 of the CRT. This same +400 volts is also always present on the high side of FOCUS control R61.

— NOTE —

In the M2000 monitor (only), an S–shaping transformer, T3, and capacitor C44 provide additional shaping of the horizontal deflection yoke current for proper linearity.

DYNAMIC FOCUS (M2000 ONLY) (Reference Figure 6.)

Due to the geometry of a CRT, the electron beam travels a greater distance when deflected to a corner as compared to the distance traveled at the center of the CRT screen. As a result of these various distances traveled, optimum focus can be obtained at only one point. An adequate adjustment can be realized by setting the focus while viewing some point midway between the center of the CRT screen and a corner, thus optimizing the overall screen focus. One of the simplest methods for improvement is to modulate the focus voltage at a horizontal sweep rate. Now optimum focus voltage is made variable on the horizontal axis of the CRT, which compensates for the beam travel along this axis.

In the M2000, the secondary of T3 generates a parabolic voltage, which together with a fixed voltage from the FOCUS control R61, is applied to the focus grid of V1. This system dynamically changes the value of focus voltage from the CRT screen center to screen edge, which will always provide an optimum amount of voltage for best overall focus.

VERTICAL OSCILLATOR, DRIVER AND OUTPUT

(Reference Figure 7.)

Composite sync pulses from the collector of Q6, Sync Ampl., are applied to the double integrating network of R45, C23, R46 and C24. The horizontal component of the sync signal is removed, leaving only the vertical sync pulses. The vertical sync pulses are coupled to the free running ver-

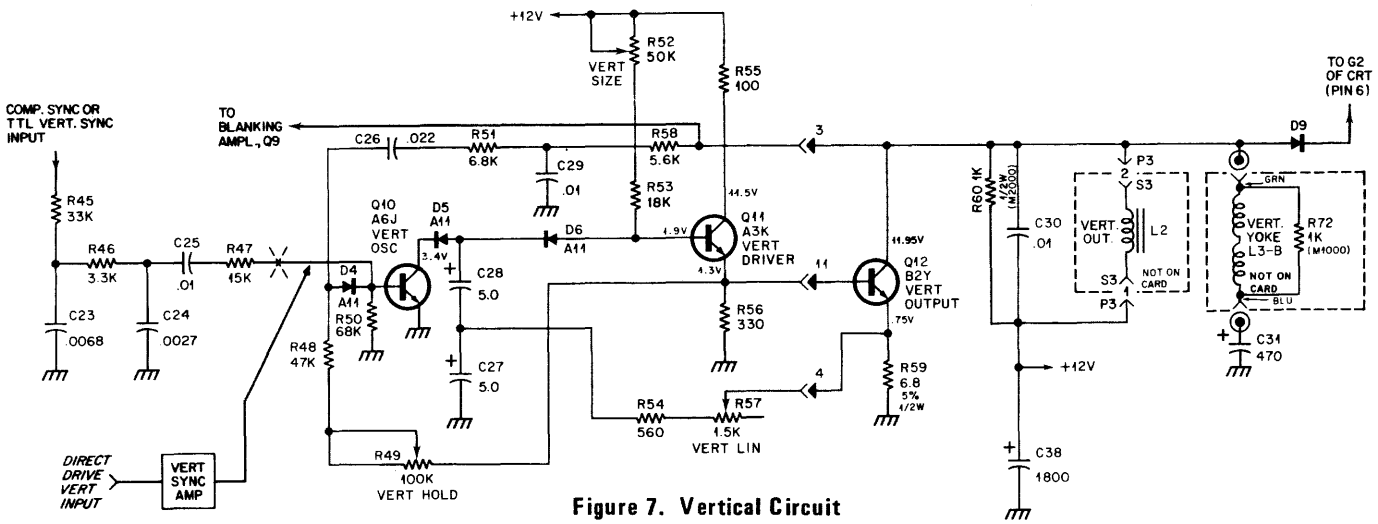
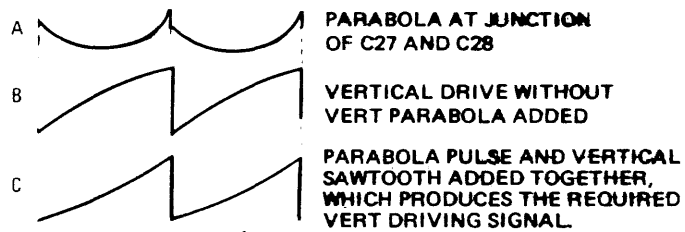


Figure 7. Vertical Circuit



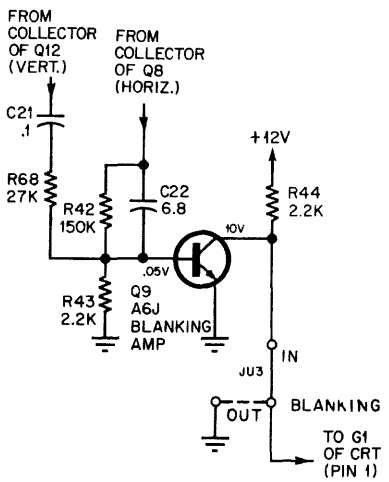


Figure 8. Blanking Amplifier

tical oscillator stage, Q10, by C25 and R47. Transistors Q10 and Q12 are connected as a multivibrator. Transistor Q11 is used as an emitter follower that provides a low impedance drive for the vertical output stage, Q12. The series combination of capacitors C27 and C28 are initially charged to the supply voltage through R53 and the VERT. SIZE control, R52, which generates an exponential ramp of voltage.

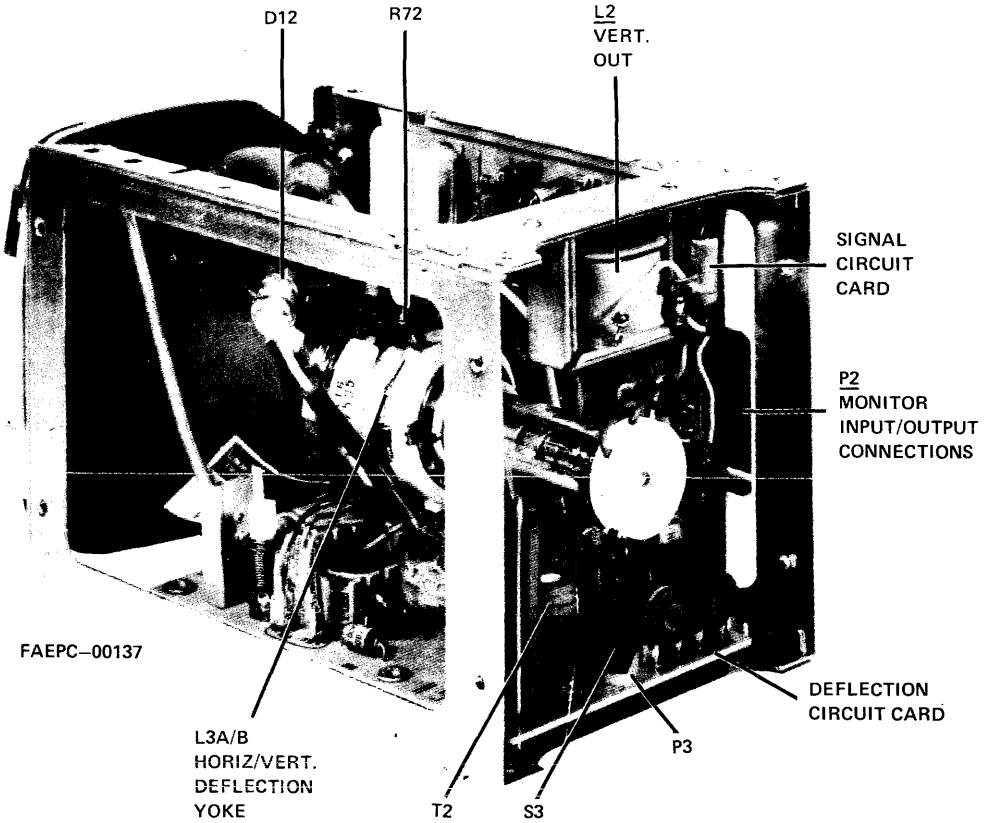
When a positive vertical sync pulse is applied to the base of Q10, it begins conducting, which immediately discharges C27 and C28. This action turns off Q11 and causes a sudden decrease in the collector current of Q12, which also decreases the vertical deflection current through deflection yoke (L3–B) and vertical choke (L2). The resultant rapidly collapsing field in L2 generates a large voltage spike that is used for vertical retrace. Components R58, C29, R51 and C26 shape this spike to ensure that Q10 remains conducting until retrace is carried out to completion. Diode D4 couples the shaped spike to the base of Q10. At this point, Q10 reverts to its non–conducting state and the cycle repeats. The VERT HOLD control, R49, and R48, provide a feedback signal to Q10 to maintain oscillation in the event vertical sycn pulses are not present. Diodes D5 and D6 provide the proper voltage drops to operate Q12 class A.

Vertical linearity is maintained by applying the ramp voltage generated across R59, through R57 (VERT LIN control) and R54, to the junction of C27 and C28. Since this path is resistive, the waveform will be integrated into a parabola by C27 (Waveform A). This results in a predistortion of the ramp waveform (waveform C). (Waveform B illustrates the drive sawtooth without parabola shaping.) Parabolic shaping is necessary to compensate for the nonlinear charging of C27 and C28, and the impedance change occuring in L2 with current. Capacitor C31 serves to remove the DC component of the vertical deflection yoke current. Diode D9 clamps the collector voltage of Q12 to a safe level.

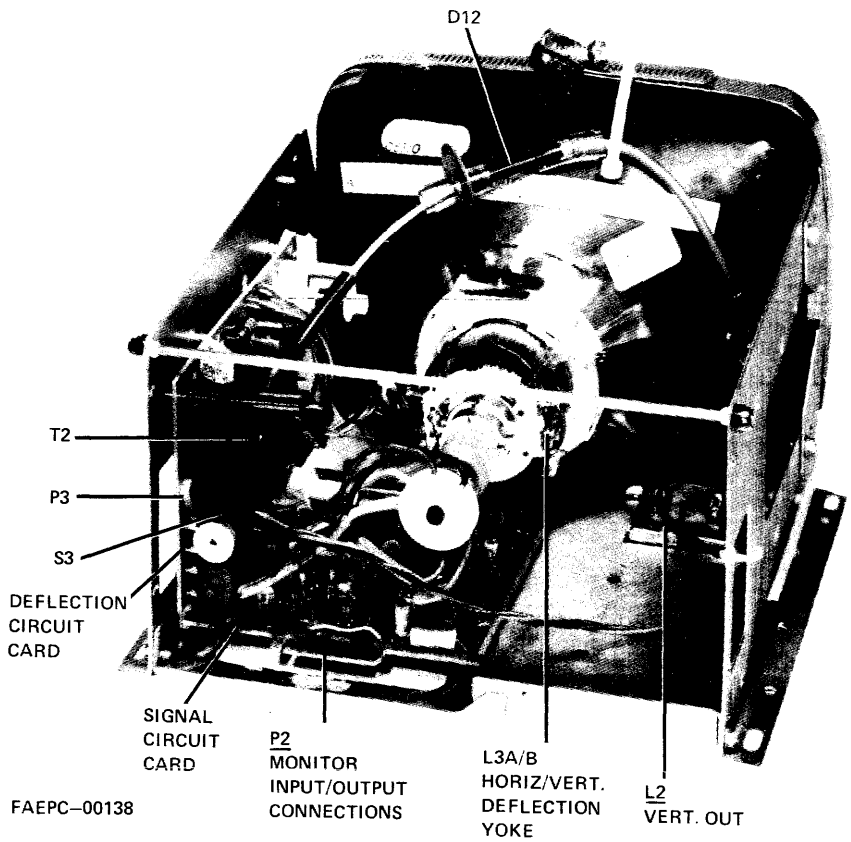
RETRACE BLANKING (NOT ON M1000–190)

(Reference Figure 8.)

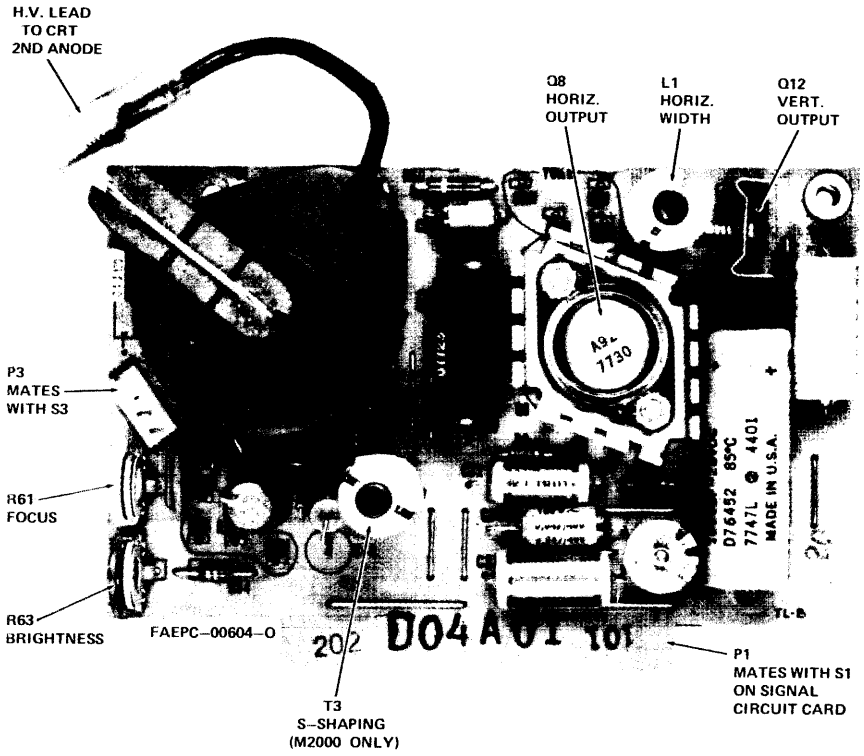
Retrace blanking is provided by negative–going horizontal and vertical rate pulses applied to G1 of the CRT. The collector pulse from the horizontal output stage, Q8, is developed across R43 through R42 and C22. The collector pulse from the vertical output stage, Q12, is differentiated by C21 to remove the sawtooth portion of the waveform. The remaining pulse appears across R43. The mixed vertical and horizontal pulses on R43 are amplified and inverted by the blanking amplifier, Q9, and applied to G1 of the CRT.



Model M1000 – Rear Chassis View

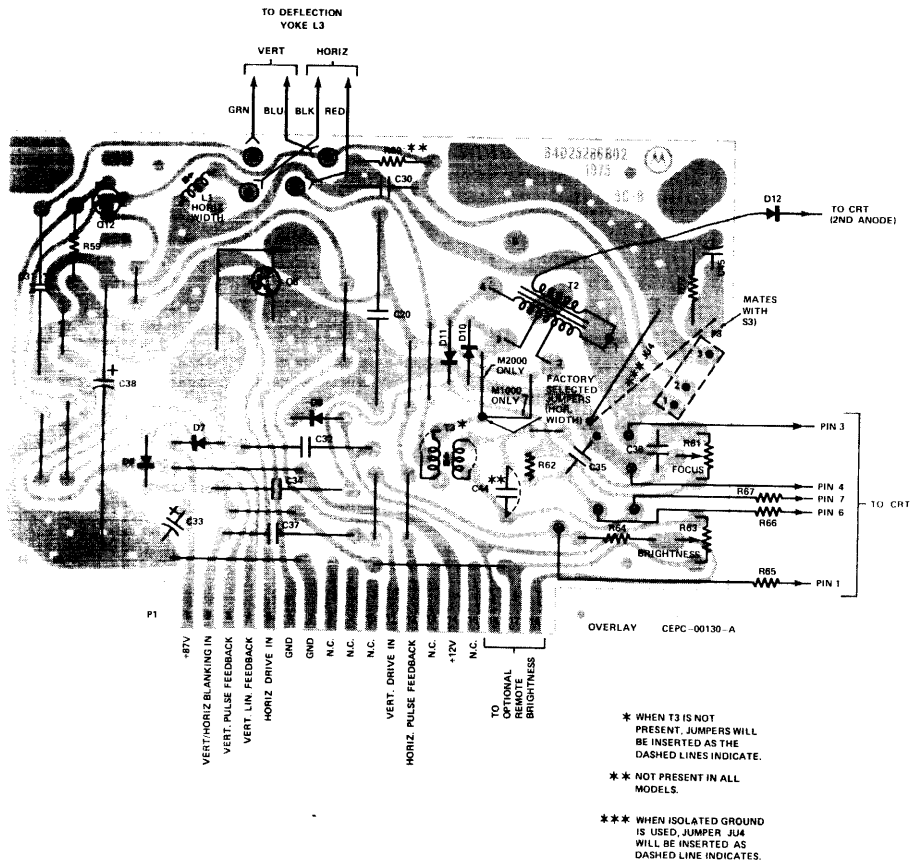


Model M2000 – Rear Chassis View



Deflection Circuit Card — Component Side

—SOLDER SIDE SHOWN—

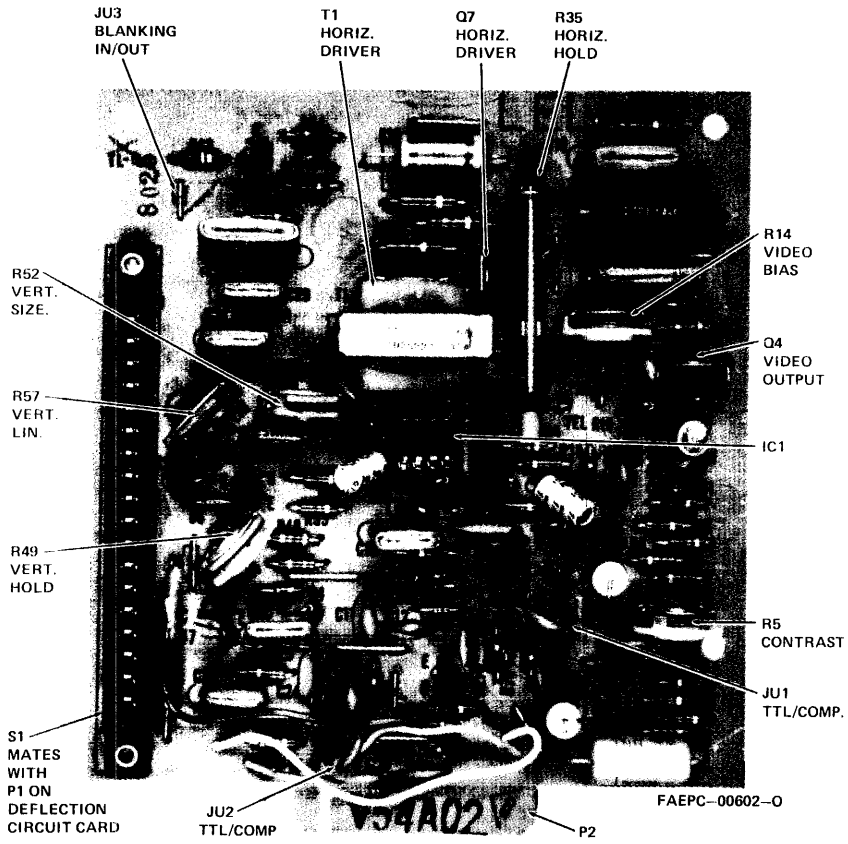


* WHEN T3 IS NOT PRESENT, JUMPERS WILL BE INSERTED AS THE DASHED LINES INDICATE.

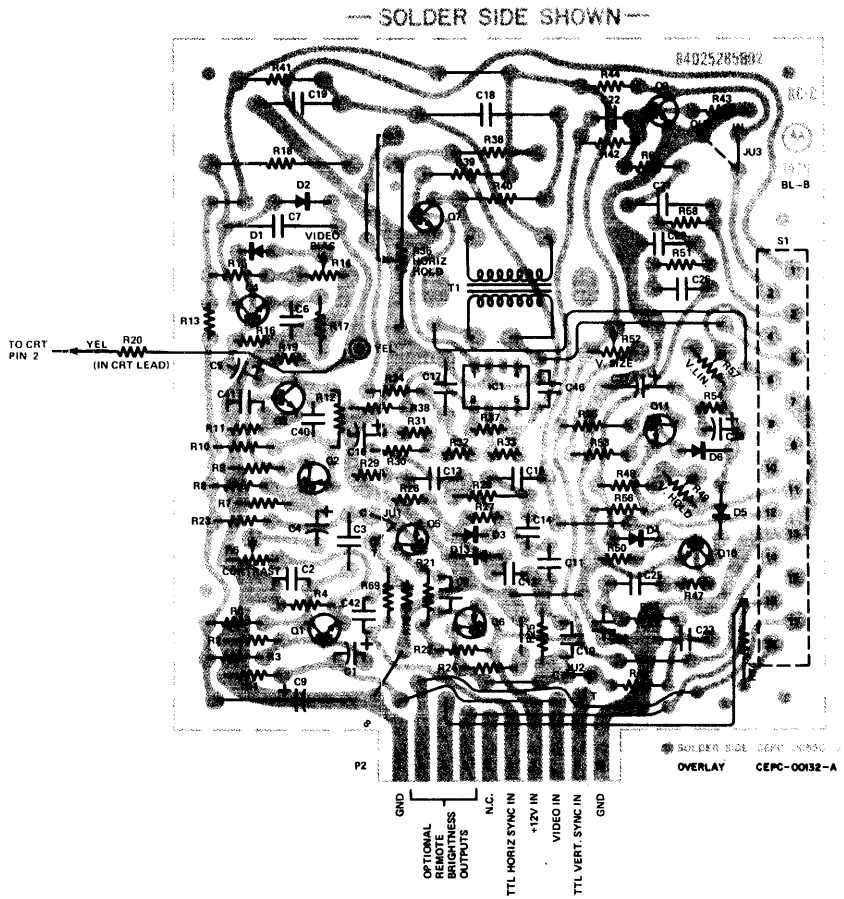
** NOT PRESENT IN ALL MODELS.

*** WHEN ISOLATED GROUND IS USED, JUMPER JU4 WILL BE INSERTED AS DASHED LINE INDICATES.

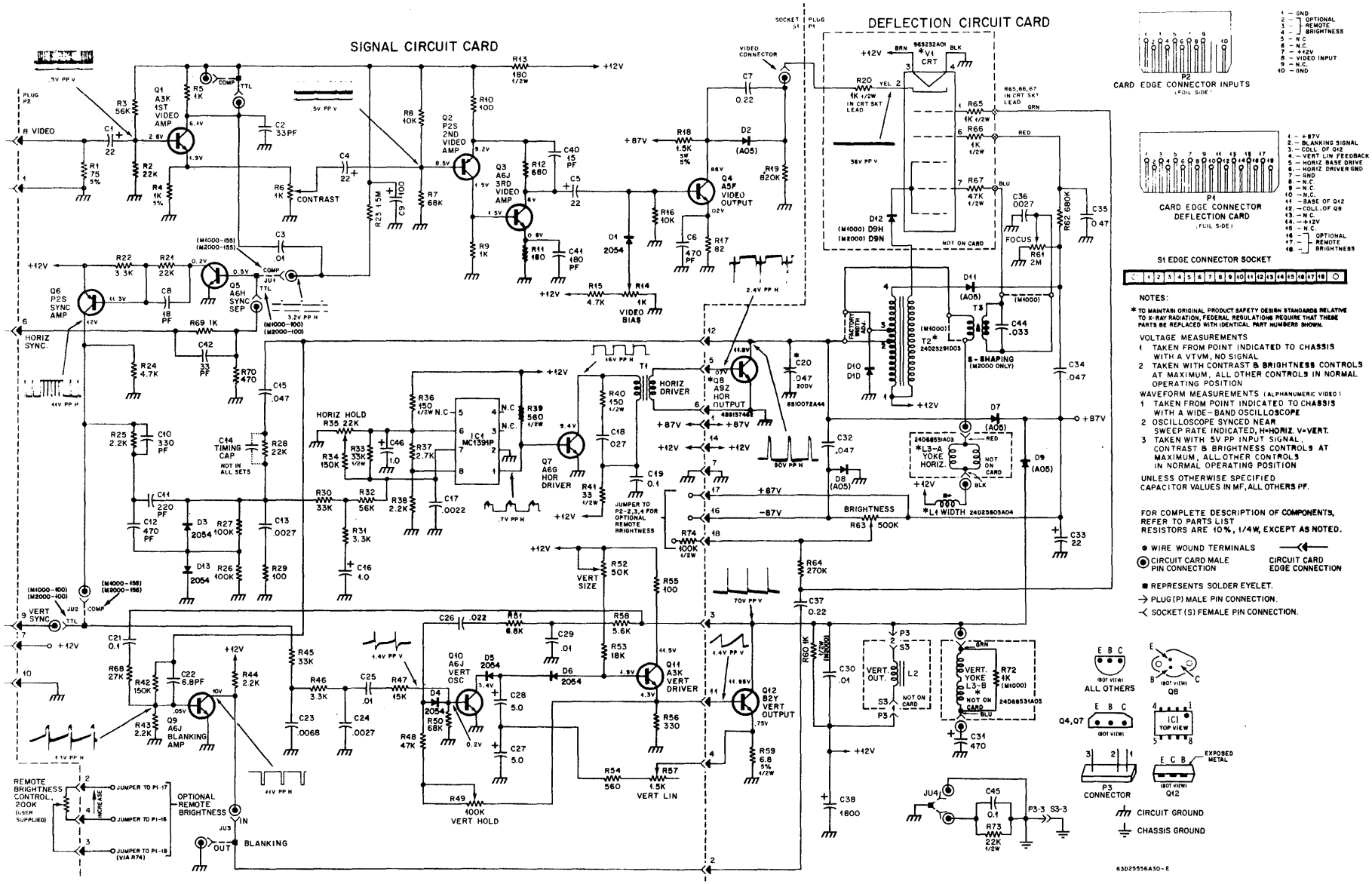
Deflection Circuit Card — Solder Side



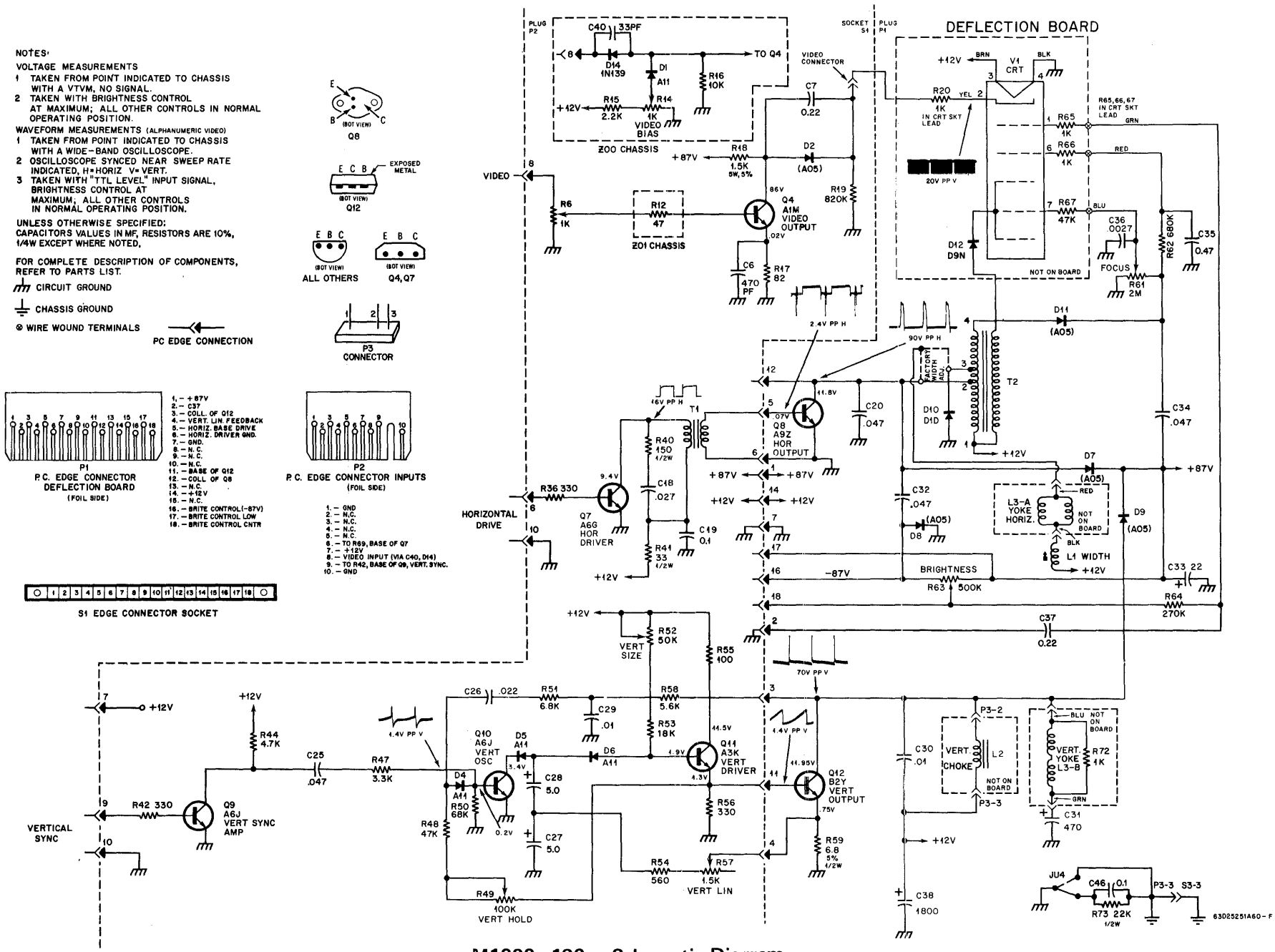
Signal Circuit Card – Component Side (All Models except M1000–190)



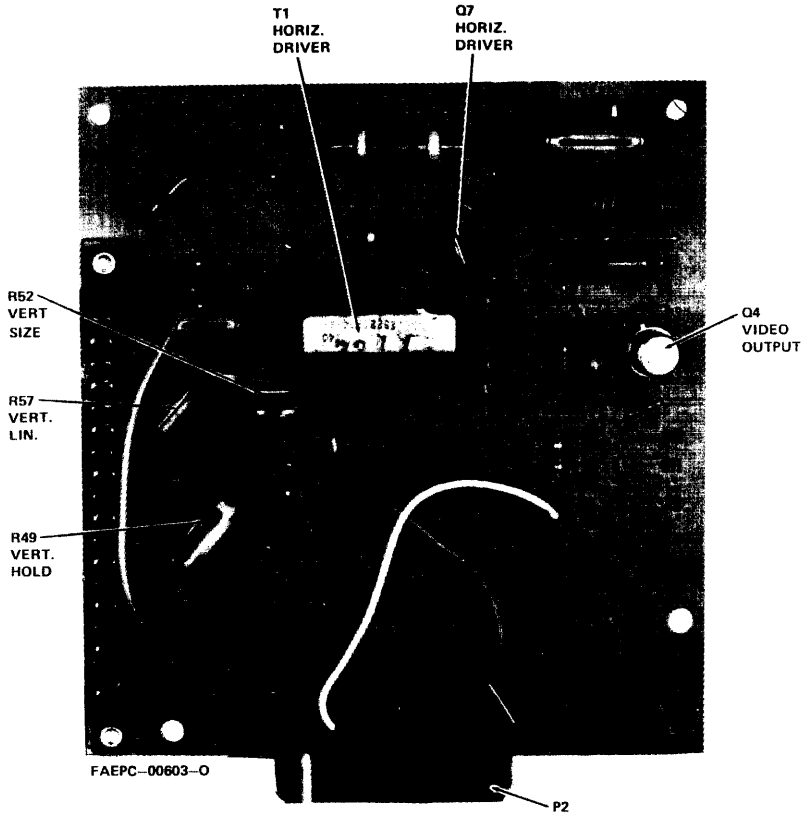
Signal Circuit Card – Solder Side (All Models except M1000–190)



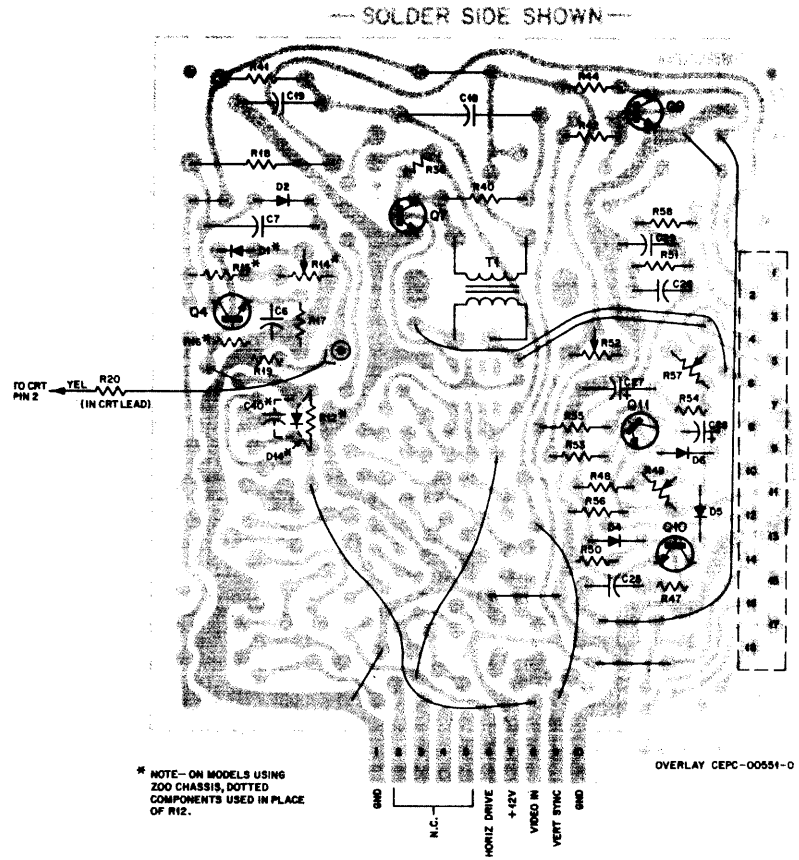
M1000 – 100, 155 and M2000 – 100, 155, 355 – Schematic Diagram



M1000—190 — Schematic Diagram



Signal Circuit Card – Component Side (Model M1000–190)



Signal Circuit Card – Solder Side (Model M1000–190)

REPLACEMENT PARTS LIST

REF. NO.	PART NUMBER	DESCRIPTION
CIRCUIT CARD ASSEMBLIES:		(COMPLETE WITH ALL COMPONENTS)
	84V25013A05	Deflection Circuit Card (Cpt.) (M1000–100, 155)
	84V25551A68	Deflection Circuit Card (Cpt.) (M1000–190)
	84V25014A90	Deflection Circuit Card (Cpt.) (M2000–155, 355)
	84V25013A70	Signal Circuit Card (Cpt.) (All models except M1000–190)
	84V25551A67	Signal Circuit Card (Cpt.) (M1000–190)
CAPACITORS:		(All values are in microfarads unless otherwise noted.)
C1	23S187A26	22, 40V; lytic
C2	21S180C64	33 pF 10%, N750, 100V; Cer. Disc.
C3	8S10191B98	.01 10%, 250V; Polyester
C4, 5	23S187A26	22, 40V; lytic
C6	21S180B53	470 pF 10%, X5F; Cer.Disc
C7	8S10212A91	0.22 10%, 250V; Mtlz Poly
C8	21S180C52	18 pF 5%, NPO; Cer. Disc
C9	23S10255A06	100, 16V; lytic
C10	21S131625	330 pF 10%, X5F; Cer.Disc
C11	21S180B87	220 pF 10%, X5F; Cer.Disc
C12	21S180B53	470 pF 10%, X5F; Cer. Disc
C13	21S180C41	.0027 10%, Z5F; Cer.Disc
C15	8S10191B91	.047 10%, 250V; Polyester
C16	23S10229A32	1.0, 16V; Tant. lytic
C17	8S10299B24	.0022 10%, 400V; Poly Carb
C18	8S10191B88	.027 10%, 400V; Polyester
C19	8S10191C02	0.1 10%, 250V; Polyester
C20	8S10072A44	.047 10%, 200V; Polyester
C21	8S10191C02	0.1 10%, 250V; Polyester
C22	21S180D93	6.8 pF ±0.5 NPO; Cer.Disc
C23	8S10191B97	.0068 10%, 400V; Polyester
C24	21S180C41	.0027 10%, Z5F; Cer. Disc
C25	8S10191B98	.01 10%, 250V; Polyester
C25	8S10191B91	.047 10%, 250V; Polyester (M1000–190 only)
C26	8S10191B89	.022 10%, 250V; Polyester
C27, 28	23S10218A31	5.0, 15V; Tant. lytic
C29	8S10191B98	.01 10%, 250V; Polyester
C30	8S10191A16	.01 10%, 400V; Polyester
C31	23S10255A29	470, 16V; lytic
C32	8S10191B07	.047 10%, 400V; Polyester
C33	23S10255A74	22, 160V; lytic
C34	8S10191B07	.047 10%, 400V; Polyester
C35	8S10212B20	0.47 10%, 400V; Mtlz. Poly.
C36	21S180C41	.0027 10%, Z5F, 500V; Cer.Disc
C37	8S10191A53	0.22 10%, 160V; Polyester
C38	23S10255B83	1800, 16V; lytic
C40	21S180C07	15 pF 10%, N150; Cer.Disc
C40	21S180C82	33 pF 10%, N150; Cer.Disc (M1000–190 only)
C41	21S180B89	180 pF 10%, Z5F 100V; Cer. Disc
C42	21S180C82	33 pF 10%, N150; Cer. Disc
C44	8S10169B71	.033 10%, 400V; Mylar (M2000 only)
C45	8S10212D52	0.1, 100V; Cer. Disc
C46	23S10229A32	1.0, 16V; lytic
DIODES:		
D1	48R02054A00	Diode, Low Power; 2054
D2	48S191A05	Rectifier, Silicon; 91A05
D3-D6	48R02054A00	Diode, Low Power; 2054
D7-D9	48S191A05	Rectifier, Silicon; 91A05
D10	48S134921	Diode, D1D
D11	48S191A05	Rectifier, Silicon; 91A05
D12	48S137608	Diode, D9H (M1000 only)
D12	48S137622	Diode, D9N (M2000 only)
D13	48R02054A00	Diode, Low Power; 2054
D14	48S137495	Diode, 1N139 (M1000–190 only)
INTEGRATED CIRCUITS:		
IC1	51S10778A01	MC1391P; T3L
COILS/CHOKES:		
L1	24D25603A03	Coil, Horiz. Width (M1000 only)
L1	24D25603A04	Coil, Horiz. Width (M2000 only)
L2	25D25221A09	Choke, Vert. Out
L3 A/B	24D25290A02	Yoke, Deflection (M1000 only)
L3 A/B	24D68531A03	Yoke, Deflection (M2000 only)
TRANSISTORS:		
Q1	48S134997	1st Video Ampl.; A3K
Q2	48S137127	2nd Video Ampl.; P2S
Q3	48S137172	3rd Video Ampl.; A6J
Q4	48S137093	Video Output; A5F
Q4	48S134919	Video Output; A1M (M1000–190 only)
Q5	48S137171	Sync Sep.; A6H
Q6	48S137127	Sync. Ampl.; P2S
Q7	48S137169	Horiz. Driver; A6G
Q8	48S137462	Horiz. Output; A9Z
Q9	48S137172	Blanking Ampl.; A6J
Q9	48S137172	Vert. Sync; A6J (M1000–190 only)
Q10	48S137172	Vert. Osc.; A6J
Q11	48S134997	Vert. Driver; A3K
Q12	48S137598	Vert. Output; B2Y
RESISTORS/CONTROLS:		
Note:		Only power or special resistors are listed. Use the description when ordering standard values of fixed carbon resistors up to 2 watts.
R6	18D25245A02	Control, Contrast 1k
R14	18D25245A02	Control, Video Bias 1k
R18	17S10731A03	1.5k 5%, 5W; Wire Wound
R35	18C25267B01	Control, Horiz. Hold 22k
R49	18D25245A15	Control, Vert. Hold 100k
R52	18D25245A20	Control, Vert. Size 50k
R57	18D25245A10	Control, Vert. Lin. 1.5k
R61	18D25245A12	Control, Focus 2 Meg.
R63	18D25245A07	Control, Brightness 500k
TRANSFORMERS:		
T1	25D25221A04	Transformer, Horiz. Driver

REPLACEMENT PARTS LIST (Continued)

REF. NO.	PART NUMBER	DESCRIPTION
T2	24D25291E02	Transformer, High Voltage (M1000 only)
T2	24D25291D03	Transformer, High Voltage (M2000 only)
T3	24C25602B01	Transformer, S-Shaping (M2000 only)
MISC. ELECTRICAL PARTS:		
V1	96S10769A01	5"- CRT, Type No.140ANB4 (M1000 only)
V1	96R2500A14	9"-CRT,Type M24-304W/10TS5497A (M2000–155 only)
V1	96S252A01	9"-CRT, Type No. VADP31 (M2000–355 only)
MECHANICAL PARTS:		
	14B25751A01	Collar, "C" (CRT Neck)
	42D25298A03	Connector, Anode (M1000 only)
	42D25298A08	Connector, Anode (M2000 only)
S1	9S10768A01	Connector, Receptacle; Header
P3	28S10586A14	Conn., Circuit Card; 3-contacts
	26C25198A03	Heat Sink (for Q8)
	26S10251A08	Heat Sink (for Q12)
S3	15S10183A87	Housing, Recept.; 3-contacts (less contacts)
	39S10184A72	Contact, Recept. (3 req'd.for S3)
	14A25340A01	Insulator, Hi-Voltage Standoff (M2000 only)
	59C25465A02	Magnet, Focus (M2000 only)
	2S10054A36	Nut, Clip-on No.8-18 (M1000 only)
	42C25258A01	Retainer, CRT (M1000 only)
	3S138210	Screw, No. 8-18 x 1-¼" (M1000 only)
	26C25323A01	Shield, Linearity (CRT)
	9D25241A04	Socket, CRT (Incl. leads & resistors R20, R65, R66 & R67)
	41B25268A03	Spring, CRT Aquadag (M1000 only)
	41D65987A01	Spring, Special; CRT Aquadag gnd. (M2000 only)
	42D67027A14	Strap, CRT Mtg.(M2000 only)
	7S10747A02	Support Guide, Circuit Card

5.0 VIDEO DISPLAY BOARD

5.0 VIDEO DISPLAY BOARD

5.1 INTRODUCTION

The Video Display Board produces a composite video signal for a raster scan, memory mapped, CRT display of 16 rows of characters with 64 characters per row. This signal is sent to the Display Module.

For those unfamiliar with the way a raster scan display is generated (a television picture is a raster scan display), the following explanation is offered. The CRT electron beam begins at the upper left corner of the raster (the rectangular image area on the face of the CRT) and sweeps across to the right at a linear rate. When the beam reaches the right side of the raster, it has produced one scan line. At the same time it is moving across, the beam moves down by a slight amount so that by the end of the scan line it has moved down one line height.

From the right side, the beam quickly flys back to the left side. During this fly back time, the beam is turned off, or blanked, so that the retrace is not visable. The beam now produces another scan line one line height below the previous scan line. This process continues until the entire raster is filled with approximately-horizontal scan lines. Then the beam quickly flies back in a vertical retrace to the upper left corner.

A full raster is called a frame, and the frame is reconstructed, or refreshed, at a rate of approximately 50 or 60 Hz. (The frame rate is chosen to approximately match the power mains frequency in order to minimize the effect of unwanted mains-frequency magnetic fields.) The horizontal and vertical sweep voltages that move the beam are generated by circuitry in the Display Module. However, these sweep voltages are synchronized to the display information by timing control signals from the Video Display Board.

During its traverse across a scan line, the beam is changed in intensity so that the finished raster will convey information of some kind. In the television application, the beam is modulated over the range from black to white so as to produce a picture. However, in our production of alphanumeric characters and graph lines it is merely necessary to turn the beam off and on (with the occasional use of half-on). In the world of nanoseconds, it takes a finite time to get the beam turned on to the point of lighting up the screen phosphor, and it takes a finite time to get it turned back off again. So for any given piece of equipment, a specific time interval is established for creating a dot in the mosaic of the finished raster. The inverse of this dot interval is the dot rate, the basic building block for the various timing control signals.

As we have seen, the image produced on the screen is made up of dots strung out across the screen as scan lines. In the case of the menu displays, this image appears as alphanumeric characters formatted as 16 rows of 64 characters each. Each row of characters contains 15 scan lines, including some blank lines for space above and below the characters themselves. This means that there are 15 x 16 = 240 scan lines making up the full raster. Our dot rate will fit 512 dots on a raster-width scan line. Since each scan line contains 64 characters, this gives us 512 / 64 = 8 dots per character. We

therefore have a matrix that is 8 dots wide by 15 scan lines high in which to construct a character and the space around it.

A row of characters is built up scan line by scan line. The top scan line contains the top 8-dot line from the matrix of each successive character in the character row, all strung together as a single line of 512 dots. The second scan line strings together the second 8-dot line from each character matrix. And so on, for 15 scan lines; then a new character row is started.

The menu and state displays are implemented with alphanumeric characters. The timing display is implemented with special graphics characters and a few alphanumeric characters. The waveform display, however, because of the higher resolution required, is produced as a composite. The standard character-display method is used for the annotation and axes, and the resulting dot stream is OR'd with a special dot stream fed in from the Waveform Board. This waveform-display dot stream produces lines on a dot-by-dot basis rather than by piecing together graphics characters to form the desired pattern of lines as in the timing display.

5.2 FUNCTIONAL DESCRIPTION

A block diagram of the Video Display Board is shown in figure 5-1. When appropriate during the following discussion, please refer to this figure and to the schematic diagram, board layout, and parts list which are included at the end of this section. Also, tables of connector pins versus signal names for all motherboard connectors are provided in section 15 along with an alphabetical list of interboard signals. And, should the need arise, a Glossary in section 16 offers explanations of acronyms or terms that may be unfamiliar.

As shown in the block diagram, the major functional units of the Video Display Board circuitry are the CRT Controller, the Timing Generator, the Data Transceiver, the Address Counter, the Screen-Refresh RAM, the Character-Set ROM, Video Control, Cursor Control, Sync Generator, Address Decoder, and DMA Controller. These units are discussed further in the following subsections.

5.2.1 CRT Controller

The CRT Controller, an Intel 8275 LSI circuit, supplies a substantial portion of the board's overall function. The rest of the circuitry on the board is, essentially, in support of this controller. Some functions of the CRT Controller (CRTC) are programmable, and these functions are set up by the processor in the initialization phase. (Please refer to Intel's data sheets on the 8275 for complete details.)

5.2.2 Timing Generator

The Timing Generator consists of the Dot Clock Oscillator (crystal Y1, U5D,E,F, and U3D), the Dot Counter U13, NAND gate U9C, and latches U24C,D. U5 and U3 are 74LS04 hex inverters, U13 is a 74LS161 synchronous, 4-bit counter, U9 is a 74LS10, and U24 is a 74LS174.

The oscillator operates at a frequency of 10.368 MHz and provides two identical output signals, DOTCLK and DCLK2, which are 10.368-MHz square waves.

DOTCLK is used onboard, and DCLK2 is supplied to external users (such as the Waveform Board) at J1-2. The Dot Counter divides DOTCLK by 2, 4, and 8. The 8-count is output as the character clock, CCLK. (Each character on the screen is 8 dots wide.) All three counts are fed to Cursor Control and to the decoder U9C. U9C produces the character-rate load signal, LD-, which goes low for one dot count at the beginning of each character.

5.2.3 Data Transceiver

The Data Transceiver, U20, a National DP8304 8-bit transceiver with Tri-state outputs, provides an 8-bit interface between the bidirectional Onboard Data Bus and the bidirectional Processor Data Bus. The direction of the transceiver (transmit or receive) is controlled by the processor through the signal S1. Also, the transceiver outputs are enabled indirectly by the processor in that whenever the processor addresses a device on the Video Display Board, AND the CRTC is not using the Onboard Data Bus (signal WAITEN from the DMA Controller is inactive), the Address Decoder produces signal DBE- which enables the transceiver outputs. This arrangement allows the processor to read from or write to the Screen-Refresh RAM and the CRTC, and to write to the latch U26.

5.2.4 Address Counter

The Address Counter consists of U6, U14, and U19, all 74LS193 4-bit binary counters. These counters are are connected in cascade to form a 12-bit binary counter that supplies 10 address bits to the Screen-Refresh RAM. The counter is advanced each time signal DACK- goes high, thereby stepping the count through the 1024 addresses of the RAM as the CRTC requires refresh characters.

The counters are placed in the parallel-load mode by signal LDCTR-. In this mode, the counters act as transparent latches, passing addresses from the Processor Address Bus to the Screen-Refresh RAM. This allows the Control Program to load the RAM with display information. Both loading and counting take place under control of the DMA Controller.

5.2.5 Screen-Refresh RAM

The Screen-Refresh RAM is made up of two 2114 1K-word x 4-bit static RAM's, U7 and U15, connected as 1K x 8 bits. This RAM holds the 8-bit codes of 1024 characters that are in a 1:1 position relationship with the characters on the CRT screen (whose 16 rows x 64 columns = 1024 characters). When the Control Program is ready to produce or update a CRT display, it loads the Screen-Refresh RAM with 8-bit character codes in the same relative positions in the RAM that they will occupy on the CRT screen as visable characters. In this processor-load phase, the DMA Controller holds the Address Counter in the load mode with signal LDCTR-. Thus, the addresses are passed from the Processor Address Bus to the RAMs. (As we will see later, the DMA Controller allows this processor-to-RAM loading to occur only during CRT vertical retrace time.)

The CRTC has two internal buffers that each hold a screen-width row of character codes. The CRTC steps through the Refresh RAM (with the aid of the DMA Controller and the Address Counter), reading characters from the RAM into

the first buffer. When the buffer is full, the CRTC begins to feed character codes from the buffer to the Character-Set ROM in synchronism with the raster-scan control signals being generating for the CRT. At the same time, the CRTC begins to load character codes from the Refresh RAM into the second internal buffer. By the time the first buffer is empty, the second buffer is full, and the two buffers exchange places to continue the process until the entire screen has been filled. Vertical retrace then occurs, and the CRTC starts over again with the next frame. During the vertical retrace, the processor may or may not update the information in the Screen-Refresh RAM.

5.2.6 Character-Set ROM

The Character-Set ROM, U10, stores a dot patern for each character configuration (A, B, C, etc.) in the library of characters that may be used to make up the CRT display. The ROM is a Synertec 51212, which is organized as 4K words x 8 bits. This means that each of the 4K address positions will output 8 bits of data. The 4K address positons are arranged in a matrix of 16 rows x 256 columns (the third dimension of the matrix is the 8 data-bits per address position), with the least significant 4 address bits decoding to the rows and the remaining 8 address bits decoding to the columns.

Each character cell on the CRT screen is 8 dots across and 15 scan lines down. In the ROM storage arrangement, the 8-dots-across are obtained from the 8 data bits at each address. The 15-scan-lines-down are matched to the 16 addressable rows (with one row unused). This leaves the 256 addressable columns to be matched to the characters. The 128 addresses for the ASCII character set can be encoded with only 7 bits. Therefore, by using the 8th column-address bit (A11) as a set selector, we have storage space for two 128-character sets, one full ASCII set and one special set for graphics. (Not all 128 special characters have been defined, but those that have, and the full ASCII set, are displayed in the screen-RAM test evoked by holding down the "2" key at power ON.)

To extract a desired dot pattern from the Character-Set ROM, the CRTC sends the character code (which was read from the Screen-Refresh RAM) from its outputs CC0—CC6 to the ROM address lines A4—A10. The CRTC then sends the current scan-line count in the current screen character row from its outputs LC0—LC3 to the ROM address lines A0—A3. Thus addressed, the ROM sends the 8 dots for the scan line to the shift register, U11. (When appropriate, the processor selects the ASCII character set by embedding a command character in the character string sent to the Screen-Refresh RAM. This command character causes the CRTC to send CHARSET, from its GPA0 attribute output, to the ROM address input A11, pin 18. This line is normally low, the condition that selects the special character set.)

5.2.7 Video Control

Video Control consists of: character shift register U11, a 74166; attribute latch U23, a 74LS174; dot logic PROM U17, an MMI 6301-1 256-word x 4-bit PROM; latchs U24A,B,E,F, which are sections of a 74LS174 hex D flip-flop; NAND gate U9B, 1/3 of a 74LS10; quad OC NAND gate U4, a 74LS01; and transistor Q1, a TIS64A.

A selected 8-dot line from a selected character dot pattern stored in Character-Set ROM U10 is fed in parallel to shift register U11. The parallel 8-dot input is loaded into U11 on the DOTCLK occuring while LD- is low, and subsequent DOTCLKs shift the dots out as a serial stream, named DOT, to the Dot Logic PROM U17.

Any field attributes (blinking, reverse video, half intensity, and underline, all implemented by the CRTC) that apply to the current character have been previously latched into U23 at the time the command character that specified them was encountered in the character string. A cursor-enable signal, CURSEN-, is generated by U9B from the three MSBs of the character code (all cursor-producing graphics characters have their three MSBs high). This signal is also latched into U23. A cursor count (which is the dot position in the 8-dot horizontal line of a graphics character at which a vertical timing-display cursor is to appear if CURSEN- is active) is fed from Cursor Control and latched into U24B as signal CURCT. All these latched signals (some may be active, others not) are fed to the Dot Logic PROM along with DOT and EXTVID- (a dot stream from the Waveform Control Board that is active in the analyzer's Waveform mode).

The Dot Logic PROM combines these signals in accordance with the Boolean formula

VIDEO-=((DOT.OR.EXTVID-.OR.(CURTC.AND.CURSEN-).OR.LTEN).XOR.RVV).AND.VSP-

and outputs the result as video signal VIDEO-. Signals VIDEO- and HALF (the half-intensity attribute signal that is fed straight thru the PROM from U23) are resynchronized in latches U24E,F by DOTCLK. The two signals are then fed to U4A,B whose outputs are combined with the horizontal and vertical sync signals, HSYNC and VSYNC, at the base of transistor Q1. The output of Q1 is the composite video signal, which is sent to the Display Module from J2-2.

5.2.8 Cursor Control

Cursor Control consists of: U26, a 74LS173 4-bit D register; and U25, a National DM8160 6-bit magnitude comparator. The primary function of this circuitry is to control the horizontal position of the movable vertical cursor in the timing display. (This cursor is created by turning on all the dots in a certain dot column in all the characters in a certain character column in the screen display.) Just before the start of each frame of a timing display, the processor writes into register U26 the dot position, in the 8-dot horizontal rows of the character cell, for the current cursor position in the screen column containing the cursor graphics characters (graphics characters with the three MSBs high; that is, characters with a code in the 7x family.)

This count is fed from the register to three of the A inputs to the U25 comparator. The horizontal dot count for each character is fed from the U13 dot counter to the corresponding B inputs of the comparator. CHARSET is fed to an A input whose corresponding B input is grounded. This means that a compare can only be equal for a graphics character (CHARSET is low for graphics characters). At the correct dot count in every dot row of every graphics character on the screen, the comparator outputs the signal CURCT. However, as previously described, U17 Dot Logic PROM only turns on the cursor dot when both CURCT and CURSEN- are active. CURSEN- is only active for character codes

in the 7x family, and the processor has only placed 7x graphics characters in the character column that should contain the cursor. Thus the cursor appears in the position intended.

An auxiliary function of Cursor Control is the generation of signal DMARST-, which turns off the DMA Controller and allows the processor unrestricted access to the Onboard Data Bus. (The display screen will be blank as long as the DMA Controller is off.) To implement this function, processor address bit A8 is fed to one input of the U26 register. The corresponding output produces signal DMARST-. The register is enabled by CUR-, which is produced when the processor writes to either port 7E or 7F. A write to 7E activates DMARST-, which holds the DMA Controller in the cleared condition. (This is also the condition at power-on when signal RST clears the U26 register.) A write to 7F turns on the DMA Controller (or leaves it on). This 7F port write is therefore used by the processor to turn on the initial display activity and subsequently to load the cursor count into the U26 register.

5.2.9 Sync Generator

The Sync Generator consists of U12 and U18, both 74LS165 shift registers. U12, the HSYNC Generator, is clocked at character rate by LD-. Shifting is started at the positive-going edge of the CRTC-supplied horizontal retrace signal, HRTC, which is high throughout the horizontal retrace period. The parallel load inputs of U12 are hard wired to produce a positive pulse that is 6 character-times wide and starts one character-time after HRTC goes high. This output pulse, HSYNC, is fed through buffer U4D to the base of composite-video transistor Q1.

U18, the VSNYC Generator, is clocked at horizontal line rate by HRTC. Shifting is started at the positive going edge of the CRTC-supplied vertical retrace signal, VRTC, which is high throughout the vertical retrace period. The parallel load inputs of U18 are hard wired to produce a positive pulse that is 3 horizontal sweep-times wide and starts 3 horizontal sweep-times after VRTC goes high. This output pulse, VSYNC, is fed through buffer U4C to the base of Q1.

The repetition rate of signal VRTC from the CRTC is programmed into the CRTC by the Control Program at initialization. At power-on time, the Control Program reads the power line frequency from a signal fed to the processor's SID input. The Control Program then commands the CRTC to use a VRTC rate that is the closest dotclock subharmonic of either 50 or 60 Hz, depending on the power line frequency.

5.2.10 Address Decoder

The Address Decoder consists of: U21, an MMI 6301-1 256-word x 4-bit PROM; U8A,B,D, 3/4 74LS00 quad NAND gate; U16B, 1/4 74LS01 quad NAND gate; and U9A, 1/3 74LS10 triple NAND gate. Certain I/O port addresses from the processor (see table on schematic) produce signal CRTC- (CRTC I/O enable) and signal CUR- (Cursor Control input enable). Also, either WAITEN- from the DMAC or IO-/M+ high from the processor produces the signal RAM-. Further, any processor address to an onboard device (I/O port, CRTC, or Screen-Refresh RAM) produces the PROCACC signal. PROCACC .AND. WAITEN+ .AND. ALE (Address Latch Enable from the 8085 processor) produce DBE- (Data Bus Enable). PROCACC .AND.

WAITEN- bring RDY low. Finally, WR- from the processor is inverted to WR; and WR .AND. WAITEN+ procude WRI-. (WR is for a processor write to the CRTC, and WRI- is for a processor write to the Screen-Refresh RAM.)

5.2.11 DMA Controller

The DMA Controller (DMAC) consists of: U1, an MMI 6331-1 32-word x 8-bit PROM; U2, a 74LS273 octal D-latch; U8C, 1/4 of a 74LS00 quad NAND gate; U3A,C, sections of a 74LS04 hex inverter; and U16A,D, sections of a 74LS01 OC NAND gate. The DMAC acts to resolve conflicts between the processor and the CRTC in demands for access to the Onboard Data Bus. It operates as follows.

At power on, the U2 latch is cleared by DMARST- from Cursor Control. This inactivates all DMAC output signals except LDCTR-, which puts the Address Counter in the load mode so that processor-generated addresses are fed through to the Screen-Refresh RAM. The CRTC has not yet received a start command from the processor and therefore remains idle. As soon as the processor has initialized the CRTC (by writing various commands to its input ports) and has loaded the Screen-Refresh RAM, it sends a start command to the CRTC and a write to port 7F which inactivates DMARST- and starts the DMAC. The CRTC sends a data request, DRQ, to the DMAC. The DMAC responds as follows:

a. WAITEN- is activated, which causes the Address Decoder to enable the Screen-Refresh RAM with RAM-, and which will cause the processor to be held at WAIT if it should try to access the Video Display.

b. The Address Counters are cleared to zero with CLRCTR.

c. The data acknowledge signal, DACK-, is sent to the CRTC which lowers DRQ.

d. The write signal, WR-, is sent to the CRTC which loads the RAM data at the counter address into the CRTC internal buffer.

e. The WR- signal is returned to high.

f. The DACK- signal is returned to high, which advances the Address Counter.

g. When the CRTC is ready, it raises DRQ again.

h. Steps c through g are repeated until the address count reaches the end of screen and signal EOS is sent to the DMAC.

i. The load-counter signal, LDCTR-, is lowered, which turns the Address Counter into a buffer for the processor addresses.

j. WAITEN is inactivated, which allows the processor access to the board again.

The CRTC takes about 15 ms to refresh the screen, during which time the processor is denied access to the Video Display. During the nominal 2 ms of vertical retrace time between frames, the processor has full access to the board. If the processor can do all the updating necessary (by loading new

characters into the Screen-Refresh RAM) in the 2 ms, the updating will appear to be instantaneous. However, if a great many characters need to be changed, or if for some other reason the processor takes longer than one vertical retrace time to update the RAM, the updating will appear as a wave moving down the screen.

If the processor is accessing the board when the CRTC sends DRQ, the DRQ is held off from the U1 PROM by DBE- at gate U8C. In no more than a very few microseconds, the processor will drop the board-accessing address to go for another instruction fetch. When this happens, DBE- will go high and the DRQ will take effect at the foregoing step a, with WAITEN holding the processor off from any further access until the next vertical retrace.

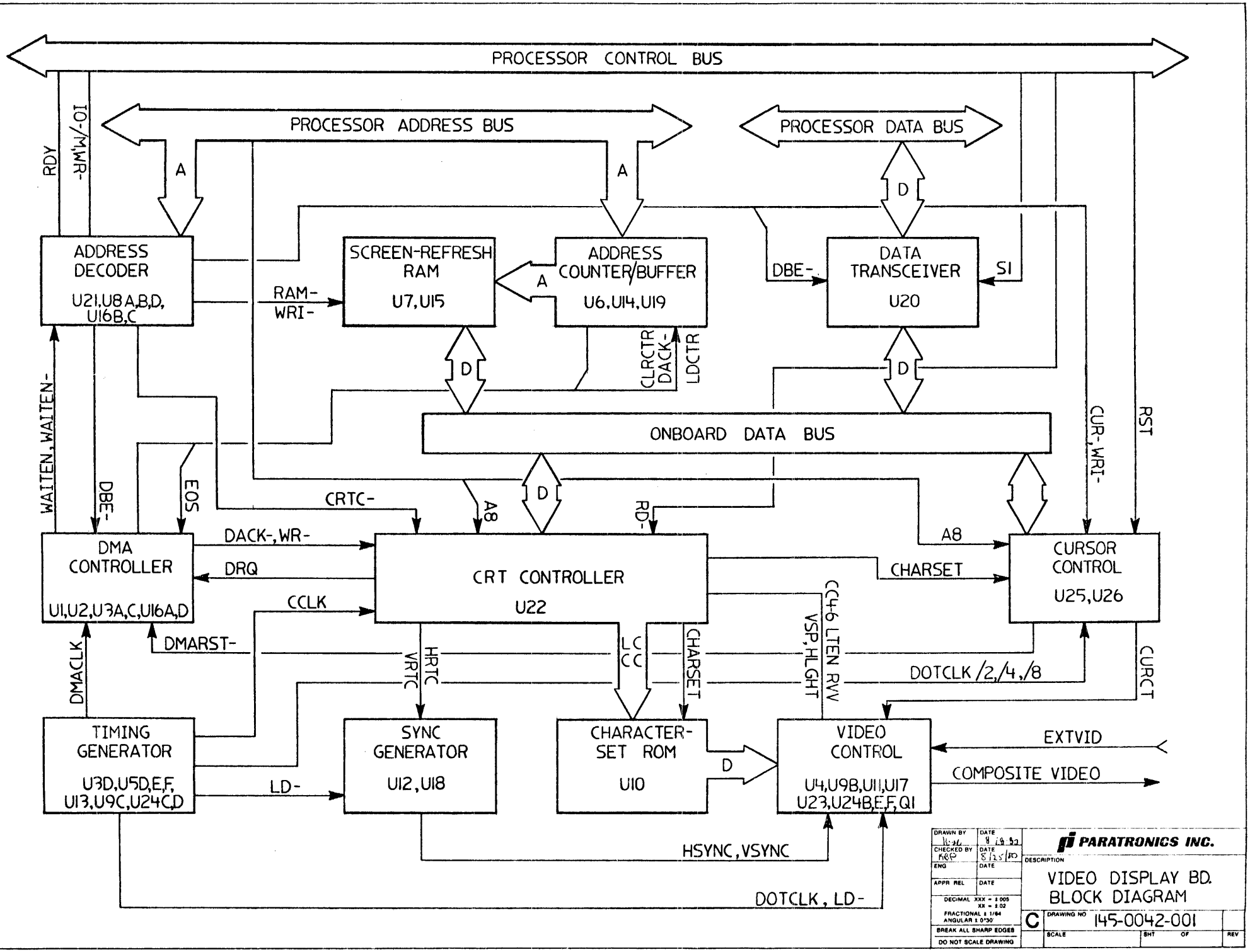
5.3 VIDEO SELF TEST

The self-test of the Screen-Refresh RAM and the Character-Set ROM is initiated by holding down the "2" key while turning the main power switch from OFF to ON, and keeping the key held down for about two seconds until a beep is heard. First, the Control Program writes 00 into all Screen-Refresh RAM addresses and then reads them back for varification. Next, the Program writes FF into all addresses and reads them back. The time interval required for this test is so short that it is not discernible. (If a failure occurs during this RAM varification phase, a continuous tone is sounded.)

After successful completion of the RAM verification test, the Program fills the RAM with a single character from the Character-Set ROM, displays the screenful of that character for about 2.5 seconds, then goes on to the next character in the set. This continues until all characters in the ROM have been displayed, special characters first, then ASCII characters. Then the character display sequence starts over again. Visual inspection of the displayed characters confirms the validity of the ROM set. Exit from the test is by turning OFF the power.

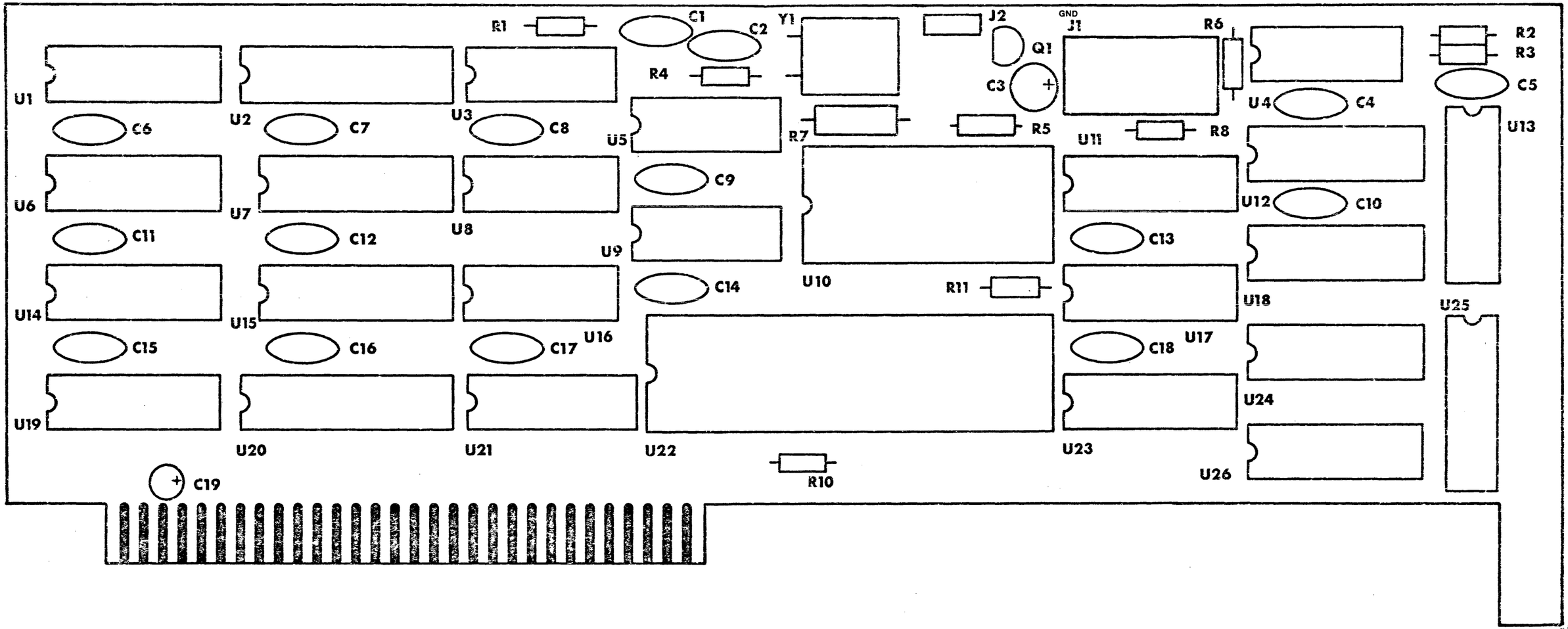
5.4 SCHEMATIC, BOARD LAYOUT, & PARTS LIST

The schematic diagrams, board layout, and parts list for the Video Display Board are contained on the following pages.



DRAWN BY	DATE	PARATRONICS INC.
CHECKED BY	DATE	DESCRIPTION
ENG	DATE	VIDEO DISPLAY BD. BLOCK DIAGRAM
APPR REL	DATE	
DECIMAL XXX = ±.005 XX = ±.02		C DRAWING NO 145-0042-001
FRACTIONAL ± 1/64 ANGULAR ± 0°30'		SCALE SHT OF REV
BREAK ALL SHARP EDGES		
DO NOT SCALE DRAWING		

REV	DESCRIPTION	DATE	APPROVED
A	PER ECO 078	11-9-79	CPM
B	PER ECO 118		



UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR G.L.S.		PARATRONICS INC.
	CK		LEGENDMASTER
	APPR		RASTER VIDEO
MAT'L	BREAK ALL SHARP EDGES		
	DECIMAL ANGULAR		
FINISH	XX ± .1 °		
	XXX ± .01		
	DO NOT SCALE DRAWING	DRWG NO 126-0042-201	REV B
		D SCALE 4/1	SHT 1 OF 1

REV	DESCRIPTION	DATE	APPROVED
B	REV PER ECO 077	11-1-79	WCS
C	REV PER ECO 093 G.S.	12-17-79	GFM
D	REV PER ECO 114	2/6/80	WCS
E	REV PER ECO 118, 127	3/28/80	WCS
F	REV PER ECO 153	9/26/80	R.EE

U3 LS04 — 22 → WAITEN

U20 DDB304 — DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 81 → D7 D6 D5 D4 D3 D2 D1 D0; T/R; DBE

ADDRESS COUNTERS

U6, LS193 — A15 A14 A13 A12 A11 A10 A9 A8 → QD QC QB QA; N.C; EOS; CB; +5V

U14 LS193 — A7 A6 A5 A4 → QD QC QB QA; C7 C6 C5 C4; +5V

U19, LS193 — A3 A2 A1 A0 → QD QC QB QA; C3 C2 C1 C0; +5V; DACK

U7, 2114 — A9 A8 A7 A6 A5 A4 A3 A2 A1 A0; I04 I03 I02 I01; D7 D6 D5 D4; WE; CE; WR1; RAM

U15, 2114 — A9 A8 A7 A6 A5 A4 A3 A2 A1 A0; I04 I03 I02 I01; D3 D2 D1 D0; WE; CE; WR1; RAM

55 → RST; +5V; 5 6 35 36; 1 31 30 60; A8; LDCTR

ALE → U3 LS04 → 11 10

ADDRESS DECODING

IO/M → S0; A14 A11 A10 A9 A15 A13 A12; WAITEN; U8 LS00; U21 6301-1 → D3 D2 D1 D0 → CUR RAM CRTC; PROC ACC

15 ALE → ALE; 3 RD → RD; 27 RDY; 4 WR → WR

WAITEN → U16 LS01 → U8 LS00 → WRI; WR; DBE

C4 C5 C6 C7 C8 .1 — C7-C16 .1

+5V — C19 33uf, 6V

TYPE	ADDR	DEVICE
I/O	7C, 7D	CRT CONTROLLER
I/O	7E	CURSOR & START DISPLAY
MEM	3000-33FF 3000-3FFF	(ACTUAL) SCREEN (VIDEO) RAM ALLOCATED
I/O	7F	STOP DISPLAY

DMA CONTROLLER-ARBITER

CLR CTR — U13 LS161 — DOT QA; CTR QB; QC; CLR FP FB; LD

Y1 10.050 MHz — C2 15pF — C1 .001 — R9 330 — R1 330

U5 LS04 — DMACLK; DCLK2

U26 LS173 — WBD; CVR; G1 G2; RST; DMA RST; CHARSET

U25 DM8160 — STB; R3 4.7K

U24 LS174 — CURCT; CCLK; LD; EXT VID

R8 4.7K — EXT VID

DCLK 2 → J1-4; CCLK → J1-2; VRTC → J1-5; HRTC → J1-3; J1-1

J1-14 J1-13 J1-12 J1-11 J1-10 J1-9

DOT CLK

U22 8275 — CCLK; DO DI D2 D3 D4 D5 D6 D7; LC0 LC1 LC2 LC3 CC0 CC1 CC2 CC3 CC4 CC5 CC6

U10 2532 — AO A1 A2 A3 A4 A5 A6 A7 A8 A9 A10; D0 D1 D2 D3 D4 D5 D6 D7; CS CS; CHARSET

U11 74-1666 — LD; CLR; A B C D E F G H; IN CIQH; DOT

U9 LS10

U23 LS174 — EXT VID; CUR CT; LTEN; RVV; VSP; HLGT; HRTC; CURSEN; VIDEO; HALF; DOT CLK

U17, 6301-1 DOT LOGIC — AO A1 A3 A2 A4 A6 A7 AS; D3 D2 D1 D0; N.C.; N.C.; VIDEO; HALF; DOT CLK

LS01 U4 — R2 1K; R6 1K; R5 470; Q1 TIS 69A; C3 33uf; R7 75 1/2W; J2-1 J2-2 J2-3

VRTC → YRTC; GPA0 → CHARSET

R11 1K

SYNC GENERATORS

U12 74LS165 — LD; S/L; S1; A B C D E F G H; CI; H SYNC 3-5-8

U18 74LS165 — VRTC; S/L; S1; A B C D E F G H; CI; V SYNC 2-3-25

+5V

2. * - DENOTES OPEN COLLECTOR.
1. ALL RESISTORS 1/4W, 5%.
NOTES: UNLESS OTHERWISE SPECIFIED.

U REF	TYPE	+5	GND	*	QTY
22	8275	40	20	40	1
10	2332	24	12	24	1
7,15	2114	18	9	18	2
20	DP8304	20	10	20	1
2	LS273	20	10	20	1
1	6331-1	16	8	16	1
21	6301-1	16	8	16	1
17	6301-1	16	8	16	1
6,14,19	LS193	16	8	16	3
23,24	LS174	16	8	16	2
26	LS173	16	8	16	1
12,18	LS165	16	8	16	2
13	LS161	16	8	16	1
9,16	LS01	14	7	14	2
9	LS10	14	7	14	1
3,5	LS04	14	7	14	2
11	LS166	16	8	16	1

U REF	TYPE	+5	GND	*	
8	LS00	14	7	14	1
25	DM8160	16	8	16	1

PARATRONICS INC.

DRAWN BY KCH 8-8-79; CHECKED BY FM 11-22-79; ENG FM 11-22-79; APPR. REL FM 11-27-79

DECIMAL XXX = ±.005, XX = ±.02; FRACTIONAL ± 1/64; ANGULAR: ±0°30'; BREAK ALL SHARP EDGES; DO NOT SCALE DRAWING

DESCRIPTION: SCHEMATIC DIAGRAM — RASTER VIDEO

DRAWING NO 127-0042-001; SIZE D; REV F; SCALE —; SHT —; OF —

P A R A T R O N I C S I N C .

S I N G L E L E V E L E X P L O S I O N

09/04/80

PAR143-0042-0090-00 DESCRIPTION : RASTER VIDEO BD., OUTSIDE ECO#: 118 REV.CU.: E

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
111-0207-0103-00	D	22 UF 16V CAP. ELECTRO.,RAD.	2	1	0	08/21/80	OPEN	0	C19
C3									
112-0310-0001-00	D	10.368 MHX CRYSTAL	1	1	0	05/28/80	OPEN	0	Y1
117-0030-0001-00	D	TERMINAL, 120-1032-04, CAMBION	1	1	0	OPEN	OPEN	0	TP1
111-0004-0072-00	D	.1 UF 25V CAP. CD	15	1	0	OPEN	OPEN	0	C10
C11 C12 C13	C14	C15 C16 C17 C18	C4	C5	C6	C7	C8	C9	
112-0105-0001-00	D	TRANSISTOR, TIS 64A,TI	1	1	0	OPEN	OPEN	0	Q1
111-0012-0013-00	D	15 PF 1KV CAP. CD	1	1	0	OPEN	OPEN	0	C2
126-0042-0001-00	D	PCB VIDEO DISPLAY FAB	1	1	0	OPEN	OPEN	0	
110-0007-0036-00	D	75 OHM 1/2W 5% RES	1	1	0	OPEN	OPEN	0	R7
115-0003-0001-00	D	SOCKET,14PIN	7	1	0	OPEN	OPEN	0	J1
U16 U3 U4	U5	U8 U9							
115-0005-0001-00	D	SOCKET,16PIN	14	1	0	OPEN	OPEN	0	U1
U11 U12 U13	U14	U17 U18 U19 U21	U23	U24	U25	U26	U6		
115-0008-0001-00	D	SOCKET,18PIN	2	1	0	OPEN	OPEN	0	U15
U7									
115-0009-0001-00	D	SOCKET,20PIN	2	1	0	OPEN	OPEN	0	U2
U20									
115-0011-0001-00	D	SOCKET,24PIN	1	1	0	OPEN	OPEN	0	U10
115-0013-0001-00	D	SOCKET,40PIN	1	1	0	OPEN	OPEN	0	U22
111-0006-0050-00	D	.001UF 50V CAP. CD	1	1	0	OPEN	OPEN	0	C1
110-0005-0055-00	D	470 OHM 1/4W 5% CF RES	1	1	0	OPEN	OPEN	0	R5
110-0005-0063-00	D	1K OHM 1/4W 5% CF RES	3	1	0	OPEN	OPEN	0	R11
R2 R6									
110-0005-0051-00	D	330 OHM 1/4W 5% CF RES	2	1	0	OPEN	OPEN	0	R1
R4									
110-0005-0079-00	D	4.7 K OHM 1/4 W CF RES	3	1	0	OPEN	OPEN	0	R10
R3 R8									

LEGEND UM : 01=EACH 02=INCH 03=FEET 04=BULK 05=AS REQUIRED 06=OTHER
LEGEND KEY: A=W/PARTS LIST D=W/O PARTS LIST R=REFERENCE DOCUMENT S=SPECIFICATION

****

SINGLE LEVEL EXPLOSION

09/04/80

PAR143-0042-0001-00 DESCRIPTION : RASTER VIDEO BOARD ECO#: 118 REV.CU.: E

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
114-0023-0002-00	D	STF CON. CA-S03-SP100-230-430	1	1	0	OPEN	OPEN	0	
143-0042-0090-00	D	RASTER VIDEO BD., OUTSIDE	1	01	0	OPEN	OPEN	118	
113-0003-0166-00	D	I.C., 74LS166	1	1	0	OPEN	OPEN	0	U11
113-0047-0001-00	D	32K ROM, SY2332, SYNERTEK	1	1	0	OPEN	OPEN	0	U10
113-0024-0001-00	D	I.C., DM8160, NSC	1	1	0	OPEN	OPEN	0	U25
113-0003-0000-00	D	I.C., 74LS00	1	1	0	OPEN	OPEN	0	U8
113-0003-0004-00	D	I.C., 74LS04	2	1	0	OPEN	OPEN	0	U3
U5									
113-0003-0010-00	D	I.C., 74LS10	1	1	0	OPEN	OPEN	0	U9
113-0003-0001-00	D	I.C., 74LS01	2	1	0	OPEN	OPEN	0	U16
U4									
113-0003-0161-00	D	I.C., 74LS161	1	1	0	OPEN	OPEN	0	U13
113-0003-0165-00	D	I.C., 74LS165	2	1	0	OPEN	OPEN	0	U12
U18									
113-0003-0173-00	D	I.C., 74LS173	1	1	0	OPEN	OPEN	0	U26
113-0003-0174-00	D	I.C., 74LS174	2	1	0	OPEN	OPEN	0	U23
J24									
113-0003-0193-00	D	I.C., 74LS193	3	1	0	OPEN	OPEN	0	U14
U19 U6									
113-0035-0002-00	D	I.C., 6301-1(35-002).N82S129F	1	1	0	OPEN	OPEN	0	U17
113-0035-0001-00	D	6301-1 MMI PROM	1	1	0	OPEN	OPEN	0	U21
113-0034-0003-00	D	I.C., 6331-1(34-003).N82S123F	1	1	0	OPEN	OPEN	0	U1
113-0003-0273-00	D	I.C., 74LS273	1	1	0	OPEN	OPEN	0	U2
113-0014-0001-00	D	I.C., DP8304N, NSC, AMD,	1	1	0	OPEN	OPEN	0	U20
113-0006-0001-00	D	I.C., C2114	2	1	0	OPEN	OPEN	0	U15
U7									
113-0036-0001-00	D	I.C., P8275, INT. CRT CONTRLR	1	1	0	OPEN	OPEN	0	U22

6.0 PROCESSOR BOARD

6.0 PROCESSOR BOARD

6.1 INTRODUCTION

The Processor Board controls all analyzer functions including keyboard control, display formating, and interface functions. The Processor Board consists of the 8085 microprocessor, 4K bytes of PROM program memory, 256 bytes of RAM memory, and buffering logic. The Processor Board can be inserted in any slot on the Microcomputer Motherboard and interfaces to all subsystems via the bus. Interrupt capability is included but is not used in the basic analyzer Control Program.

6.2 FUNCTIONAL DESCRIPTION

When appropriate during the following discussion, please refer to the schematic diagram, board layout, and parts list which are included at the end of this section. Also, tables of connector pins versus signal names for all motherboard connectors are provided in section 15 along with an alphabetical list of all interboard signals. And, should the need arise, a Glossary in section 16 offers explanations for acronyms or terms that may be unfamiliar.

The program execution function is supplied by U11, the Intel 8085 microprocessor. A 6.144 MHz crystal, Y1, generates the basic clock frequency of 3.072 MHz for all 8085 timing.

R9, C5, and CR1 form the POWER-ON RESET circuitry which, along with U15 and the 8085, generates a positive-going TTL reset pulse to pin 55 of the bus each time power is cycled to the analyzer.

Address latching and buffering is provided by U9 which demultiplexes the 8085 address/data signals and presents a stable 16-bit address to the bus. Upper address buffering is provided by U14 and control signal buffering by U15. Bidirectional data buffering is provided by octal transceiver U10. For future applications, 8085 signal HLDA (Hold Acknowledge) places the address, data, and control signal buffers in the high Z state to permit other active bus sources to control the bus.

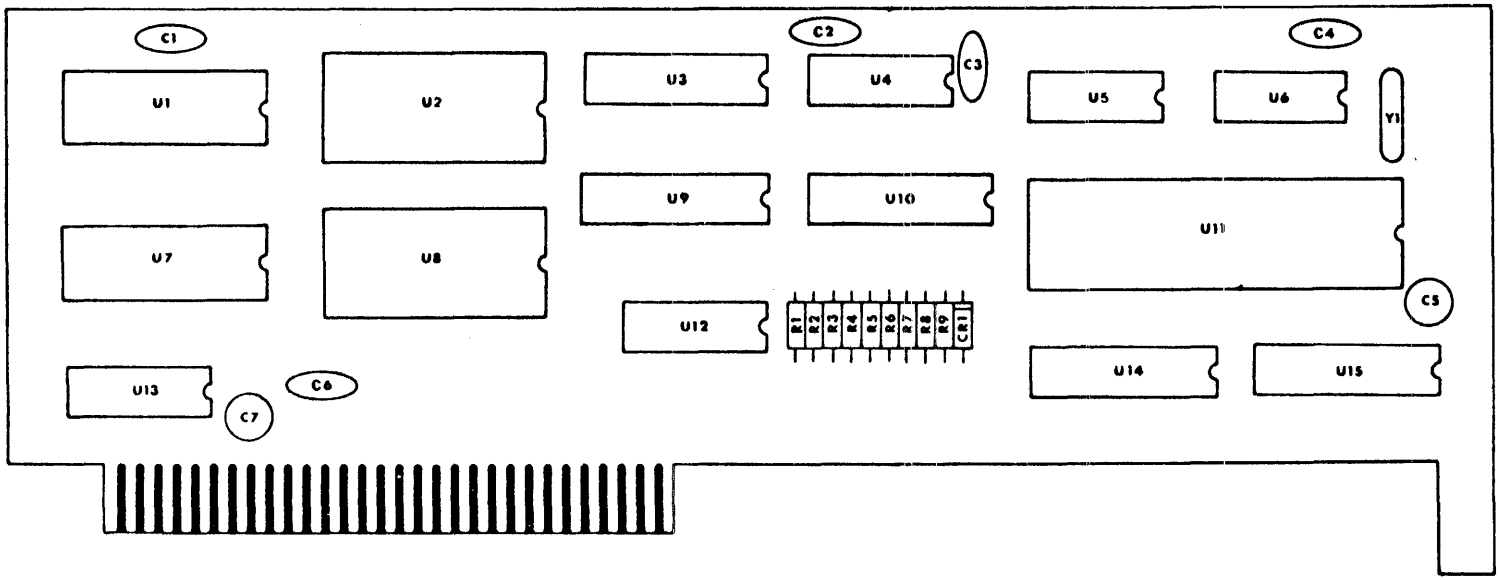
The 4K-byte program memory is contained in PROMS U2 and U8 which occupy address spaces 0000—07FF and 0800—FFF, respectively. RAMs U1 and U7 form a 256-byte scratch pad area for temporary flag storage as well as the stack area used in subroutine linkage. The scratch pad area occupies the first 256 bytes of address segment 1000—17FF. ROM and RAM address decoding is performed by U12 and U13. Buffering of ROM and RAM data is performed by U3. U4 pulls up the data bus, which assures stable logic levels under no-source (i.e., high Z) conditions. U5 and U6 provide control signal generation and buffering.

The processor uses only +5 V power, and no connection is made to the other voltages. The 8085 SID (Serial Input Data) signal is used to sense the the mains frequency when requested by the Control Program. Trap, interrupt, hold, and serial output signals from the 8085 are brought to the bus for future expansion.

6.3 SCHEMATIC, BOARD LAYOUT, & PARTS LIST

The schematic diagram, board layout, and parts list for the Processor Board are contained on the following pages.

REV	DESCRIPTION	DATE	APPROVED
A	RELEASE	2-7-80	



DRAWN BY		DATE 1-30-80
CHECKED BY		DATE 2-7-80
ENG		DATE 2-7-80
APPR REL		DATE 2-7-80

DECIMAL XXX = ±.005 XX = ±.02
FRACTIONAL ± 1/64
ANGULAR ± 0°30'
BREAK ALL SHARP EDGES
DO NOT SCALE DRAWING

PARATRONICS INC.

DESCRIPTION
LEGENDMASTER 532 PROCESSOR

DRAWING NO 126-0008-201 REV A
SCALE FULL SHT 1 OF 1

/1117

U-NUM	+5V	GND
U1	22	8
U2	21,24	12
U3	20	10
U4	16	-
U5	14	7
U6	14	7
U7	22	8
U8	21,24	12
U9	20	10
U10	20	10
U11	40	20
U12	16	8
U13	16	8
U14	20	10
U15	20	10

PARATRONICS, INC.

127-0009-001 PROCESSOR

SIZE		INIT.	DATE	REV NO.	
D	DRAWN	GFM	4/30/78	REV A	12/11/78
	CHECK	GFM	4/30/78	REV B-149	4-22-80
	DESIGNER	GFM	4/30/78		

S I N G L E L E V E L E X P L O S I O N

09/04/80

PAR143-0008-0090-00 DESCRIPTION : PROCESSOR PCB ASSY OUTSIDE ECO#: 149 REV.CU.: B

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
111-0004-0072-00	D	.1 UF 25V CAP. CD	5	1	0	OPEN	OPEN	0	C1
C2 C3 C4 C6									
126-0008-0001-00	D	PROCESOR PCB FAB	1	1	0	OPEN	OPEN	0	
115-0013-0001-00	D	SOCKET,40PIN	1	1	0	OPEN	OPEN	0	U11
115-0011-0001-00	D	SOCKET,24PIN	2	1	0	OPEN	OPEN	0	U2
U8									
115-0010-0001-00	D	SOCKET,22PIN	2	1	0	OPEN	OPEN	0	U1
U7									
115-0009-0001-00	D	SOCKET,20PIN	5	1	0	OPEN	OPEN	0	U10
U14 U15 U3 U92									
115-0005-0001-00	D	SOCKET,16PIN	3	1	0	OPEN	OPEN	0	U12
U13 U4									
115-0003-0001-00	D	SOCKET,14PIN	2	1	0	OPEN	OPEN	0	U5
U6									
112-0301-0001-00	D	CRYSTAL, 6.1440 MHZ, NE-18PA	1	1	0	OPEN	OPEN	0	Y1
112-0204-0001-00	D	DIODE ,1N3600	1	1	0	OPEN	OPEN	0	CR1
111-0050-0107-00	D	33 UF 6V TANT. DROP CAP.	2	1	0	OPEN	OPEN	0	C5
C7									
110-0005-0107-00	D	68K OHM 1/4 W CF RES	1	1	0	OPEN	OPEN	0	R9
110-0005-0088-00	D	11K 1/4 W 5% CF RES	7	1	0	OPEN	OPEN	0	R1
R2 R3 R4 R5		R6 R7							
110-0005-0079-00	D	4.7 K OHM 1/4 W CF RES	1	1	0	OPEN	OPEN	0	R8

LEGEND UM : 01=EACH 02=INCH 03=FEET 04=BULK 05=AS REQUIRED 06=OTHER
LEGEND KEY: A=W/PARTS LIST D=W/O PARTS LIST R=REFERENCE DOCUMENT S=SPECIFICATION

****

PARATRONICS INC.

SINGLE LEVEL EXPLOSION

09/04/80

PAR143-0008-0002-00 DESCRIPTION : M540 PROCESSOR PC ASSY. ECO#: 149 REV.CU.: B

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#
110-0315-0001-00	D	2.2KOHM RES NET CTS761-1-R2.2K	1	1	0	OPEN	OPEN	0
113-0003-0000-00	D	I.C., 74LS00	1	1	0	OPEN	OPEN	0
113-0003-0008-00	D	I.C., 74LS08	1	1	0	OPEN	OPEN	0
113-0003-0138-00	D	I.C., 74LS138	1	1	0	OPEN	OPEN	0
113-0003-0139-00	D	I.C., 74LS139	1	1	0	OPEN	OPEN	0
113-0003-0244-00	D	I.C., 74LS244	3	1	0	OPEN	OPEN	0
113-0003-0373-00	D	I.C., 74LS373	1	1	0	OPEN	OPEN	0
113-0005-0001-00	D	I.C., P2101A-2	2	1	0	OPEN	OPEN	0
113-0007-0001-00	D	I.C., 2716	2	1	0	OPEN	OPEN	0
113-0012-0001-00	D	I.C., P8085, INT., NEC.	1	1	0	OPEN	OPEN	0
113-0014-0001-00	D	I.C., DP8304N, NSC, AMD,	1	1	0	OPEN	OPEN	0
143-0008-0090-00	D	PROCESSOR PCB ASSY OUTSIDE	1	1	0	OPEN	OPEN	149

LEGEND UM : 01=EACH 02=INCH 03=FEET 04=BULK 05=AS REQUIRED 06=OTHER
LEGEND KEY: A=W/PARTS LIST D=W/O PARTS LIST R=REFERENCE DOCUMENT S=SPECIFICATION

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7.0 EXTENDED MEMORY BOARDS #1 AND #2

7.0 EXTENDED MEMORY BOARD

7.1 INTRODUCTION

All configurations of the PI 540 Analyzer require more memory than is provided by the Processor Board. The necessary additional memory is supplied by two Extended Memory Boards. The two boards are identical except for the population of memory devices. The maximum memory capacity of the board is 24K bytes of PROM or ROM (assuming 32K-bit devices) and 4K bytes of RAM. In the PI 540, Board #1 contains 12K bytes of PROM/ROM and 4K bytes of RAM, and Board #2 contains somewhat less, depending on the configuration of the particular instrument. These boards may be installed in any of the board positions on the Microcomputer Motherboard.

7.2 FUNCTIONAL DESCRIPTION

A block diagram of the Extended Memory Board is shown in figure 7-1. When appropriate during the following discussion, please refer to this figure and to the schematic diagram, board layout, and parts list which are included at the end of this section. Also, tables of connector pins versus signal names for all motherboard connectors are provided in section 15 along with an alphabetical list of all interboard signals. And, should the need arise, a Glossary in section 16 offers explanations for acronyms or terms that may be unfamiliar.

As shown in the block diagram, the major functional units of the Extended Memory Board circuitry are the Address Decoder, the Data Buffer, the Read-Only Memory, and the Read/Write Memory. These units are discussed further in the following subsections.

7.2.1 Data Buffer

The Data Buffer consists solely of U12, a National DP8304B 8-bit bidirectional transceiver with Tri-State outputs. This buffer provides selectable bidirectional interconnection between the Processor Data Bus and the Onboard Data Bus.

The buffer's T+/R- (Transmit + / Receive -) input, U12-11, is fed with signal S1 (data bus Status bit 1) from the Processor Control Bus. S1 is high for a processor read and low for a processor write. Therefore, the U12 outputs are connected so that its T+ mode transmits data to the Processor Data Bus and its R- mode receives data from the Processor Data Bus. The output enable, U12-9, is fed with signal MEMEN- (Memory Enable -) from the Address Decoder. When any memory on the board is addressed by the processor, the Address Decoder brings MENEN- low, thereby enabling the buffer output in the direction that has been selected by S1.

7.2.2 Read-Only Memory

The Read-Only Memory consists of six PROM or ROM devices which may contain either 2K or 4K bytes, depending on the type of device used. A typical

device is the 2716, a 2048-word x 8-bit EPROM (UV-Erasable Read-Only Memory) with 3-state outputs.

The address inputs A10 through A0 of all six PROM/ROMs are connected in parallel to the corresponding address bits on the Processor Address Bus. Pin 21 of the PROM/ROMs is left unconnected or is jumpered to either +5 v or address bit A11, depending on the type of PROM/ROM device. (Refer to the table titled "U13 PROM Output Codes" on the schematic diagram.) Pin 18 of all PROM/ROMs is connected to the D4 output of U13 in the Address Decoder. The D4 output, signal ROMP18, is driven high or low or is supplied with address bit A11, depending on the type of PROM/ROMs installed. The OE- (Output Enable -) line, pin 20, of each PROM/ROM is connected to the appropriate output of the U14 second-stage decoder (ROM0-, ROM1-, ROM2-, ROM3-, ROM4-, or ROM5-).

When the 1K address block residing in one of the PROM/ROMs is addressed by the processor, the OE- line of that device is brought low by U14, and S1 directs the Data Buffer to transmit data to the processor. Address bit A10 (and A11 if the PROM/ROM is a 4K device) selects the 1K block within the device, and address bits A9 through A0 select the desired byte.

7.2.3 Read/Write Memory

The Read/Write Memory consists of eight 2114 1024-word x 4-bit static RAMs with 3-state bidirectional input/output. The eight RAMs are arranged as four pairs, with each pair connected to form a 1024-word x 8-bit block of read/write memory.

The address inputs of all eight RAMs are connected in parallel to address bits A9 through A0 of the Processor Address Bus. The WE- (Write Enable -) lines of all eight RAMs are connected in parallel to the WR- (Write -) line of the Processor Control Bus. The I/O data lines of the two RAMs in each pair are connected in cascade to the Onboard Data Bus. The CS- (Chip Select -) lines of the two RAMs in each pair are connected in parallel to the appropriate output of the U14 second-stage decoder (RAM6-, RAM7-, RAM8-, or RAM9-).

When the 1K address block occupied by one of the RAM pairs is addressed by the processor, the CS- line of that pair is brought low by U14. Address inputs A9 through A0 contain the address of the desired byte within the 1K block. If the operation is a read, S1 directs the Data Buffer to transmit data to the processor and the WR- line is high. If the operation is a write, S1 directs the Data Buffer to receive data from the processor and the WR- line is pulsed low.

7.2.4 Address Decoder

The Address Decoder consists of: U13, an MMI 6309-1 256-word x 8-bit static PROM; and U14, a 74LS42 4-line-BCD to 10-line decoder. This circuitry allows the processor to address any of the memory devices on the board in accordance with an established address allocation programmed into the U13 PROM.

The U13 PROM is fed by signals IO+/M- (Input/Output + / Memory -) and S1 from the Processor Control Bus and by signals A15 through A10 from the Processor Address Bus. IO+/M- is low for all processor memory operations, and S1 is high for read operations and low for write operations. Address bits A15 through A10 decode down to the level of 1K-word blocks. The U13 decoder PROMs on the two boards are programmed to recognize the following hex address blocks:

Board #1	RAM	C800—D7FF (4K)		PROM/ROM	9000—BFFF (12K)
Board #2	RAM	C000—C7FF (2K)		PROM/ROM	5000—7FFF (12K)

As correlative information, the memory address blocks on other boards are:

Proc. Bd.	RAM	1000—1FFF (4K)		PROM/ROM	0000—0FFF (4K)
Video Bd.	RAM	3000—3FFF (4K)			
Waveform Bd.	RAM	2E00—2FFF (1/2K)			

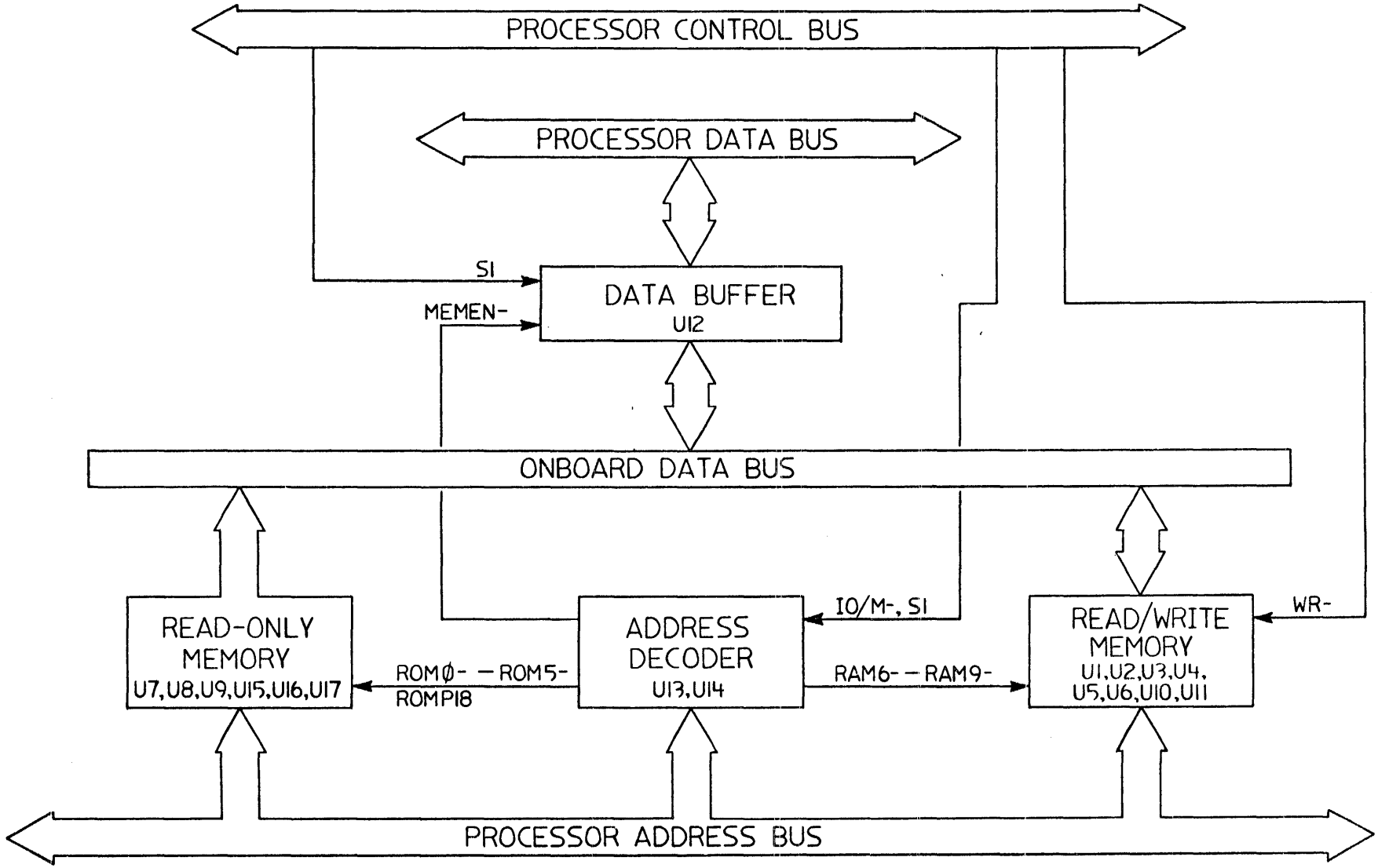
(On Extended Memory Board #2, none of the allocated RAM is currently used, and only 5000—6FFF (8K) of the allocated 12K block of PROM/ROM is currently used. On the Processor Board, only 1000—10FF (1/4K) of the allocated 4K block of RAM is currently used. On the Video Board, only 3000—33FF (1K) of the allocated 4K block of RAM is currently used.)

PROM U13 output D7 (signal MEMEN-) enables the Data Buffer for all memory operations on the board. Outputs D6 and D5 are not connected. Output D4 is fed to pin 18 of all PROM/ROM devices and acts either as a device select or as address bit A11, depending on the type of device installed on the board. (Because the U13 PROM is programmed differently for different PROM/ROM devices, once U13 is programmed, only the PROM/ROM types compatible with this programming can be installed on the board.)

Outputs D3 through D0 of PROM U13 encode the board position number of the device(s) containing the addressed 1K block of memory. These four output lines feed the second stage decoder, U14, which supplies ten enable signals to the memory devices as follows. The six PROM/ ROMs are assigned board position numbers 0 through 5 and are enabled by signals ROM0- through ROM5-. (Since the PROM/ROMs each contain more than one 1K memory block, the U13 PROM is programmed to activate the same enable line for all 1K blocks within a given PROM/ROM. The 1K blocks are separated within the PROM/ROMs by address bit A10 for 2K devices, or address bits A10 and A11 for 4K devices.) The four RAM pairs are assigned board position numbers 6 through 9 and are enabled by signals RAM6- through RAM9-. The schematic diagram contains a table, titled "U13 PROM Output Codes", that summarizes the U13 PROM outputs in relation to the type of PROM or ROM device used.

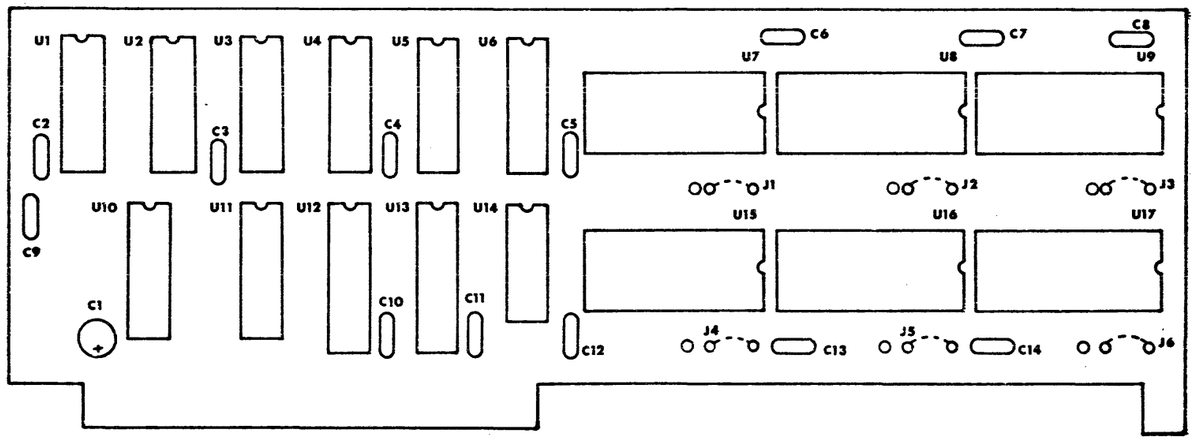
7.3 SCHEMATIC, BOARD LAYOUT, & PARTS LIST

The schematic diagram, board layout, and parts list for the Extended Memory Board are contained on the following pages.



DRAWN BY Pat	DATE 8-28-80	PARATRONICS INC.
CHECKED BY KSD	DATE 8/25/80	DESCRIPTION: EXTENDED MEMORY BD. BLOCK DIAGRAM
ENG	DATE	
APPR REL	DATE	
DECIMAL XXX = ± 005, XX = ± 02		C — DRAWING NO 145-0070-001
FRACTIONAL ± 1/64, ANGULAR ± 0°30		SCALE — SHT OF — REV
BREAK ALL SHARP EDGES		
DO NOT SCALE DRAWING		

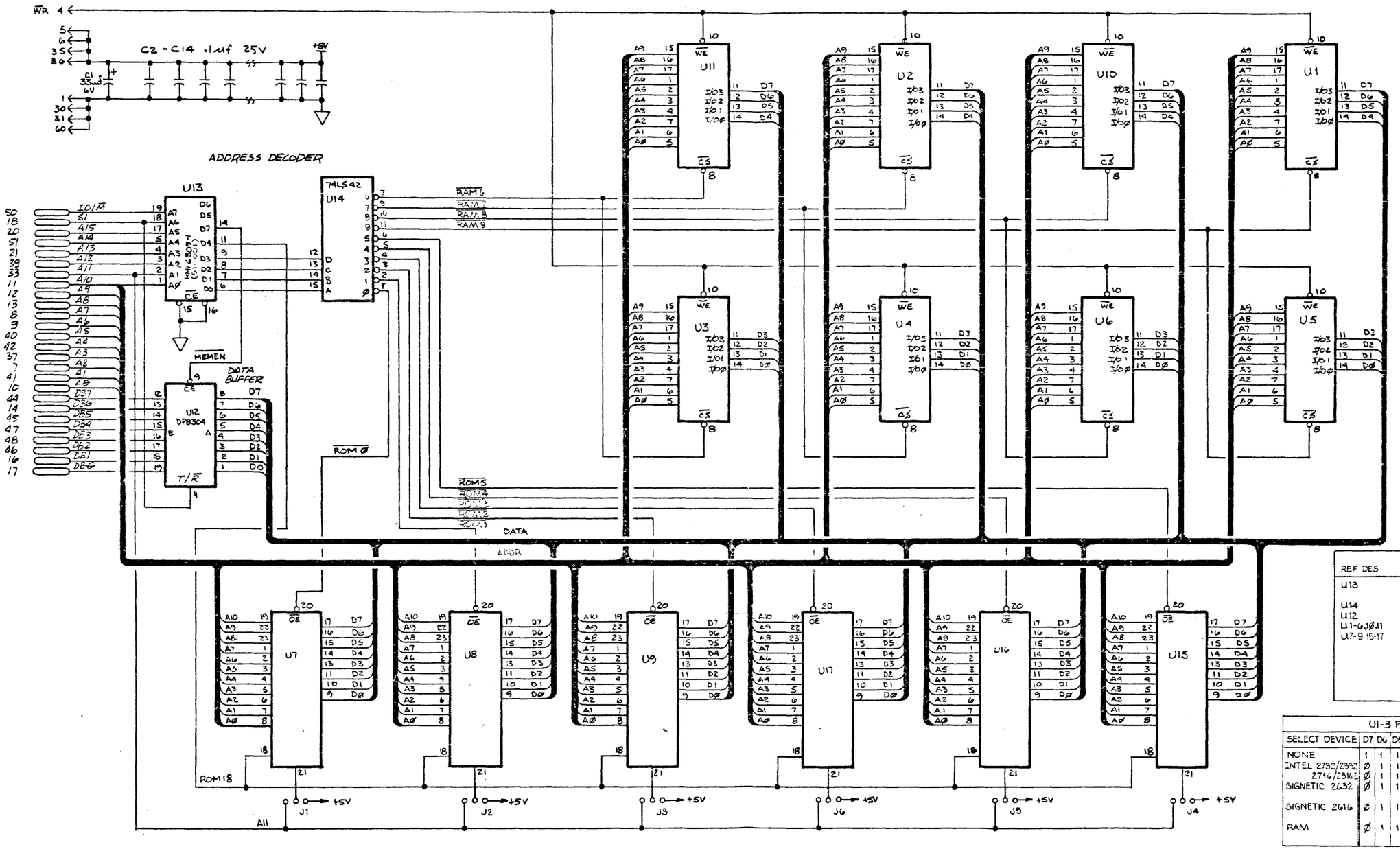
REV	DESCRIPTION	DATE	APPROVED



DRAWN BY	DATE 9-12-7[illegible]	PARATRONICS INC.	
CHECKED BY	DATE		
ENG [illegible]	DATE [illegible]	DESCRIPTION LEGENDMASTER EXTENDED MEMORY	
APPR. REL	DATE		
DECIMAL .XXX ± .005 .XX ± .02		D DRAWING NO 126-0070-201	A
FRACTIONAL ± 1/64 ANGULAR ± 0°30'		SCALE 2/1 SHT 1 OF 1	REV.
BREAK ALL SHARP EDGES			
DO NOT SCALE DRAWING			

REV	DESCRIPTION	DATE	APPROVED
B	REV PER E.C. 179	10/12/79	[illegible]

READ WRITE MEMORY



READ-ONLY MEMORY

REF DES	PIN # +5V	PIN # GND	DEVICE TYPE
U13	20	10	MM1 6309-1 PROM OR EQUIV
U14	16	8	74LS42
U12	20	10	DP8304
U1-6,10,11	18	9	2114 RAM
U7-9 15-17	24	12	2K OR 4K X8 ROM/PROM 2716, 2732, 2516E, 2332 SIG 2616, SIG 2632

U1-3 PROM OUTPUT CODES.

SELECT DEVICE	D7	D6	D5	D4	D3	D2	D1	D0	PIN21	NOTES
NONE	1	1	1	1	1	1	1	1	N/C	
INTEL 2732/2332	0	1	1	0	S	S	S	S	A11	
2716/2516E	0	1	1	0	S	S	S	S	+5	
SIGNETIC 2632	0	1	1	A11	S	S	S	S	N/C	PIN 20=$\overline{CS}$,
SIGNETIC 2616	0	1	1	0	S	S	S	S	N/C	20=$\overline{CS}$,
RAM	0	1	1	1	S	S	S	S	N/A	

A11 = ADDRESS BIT A11.
SSSS = BCD SOCKET SELECT CODE (0-5 = ROM/PROM, 6-9 = RAM)

= P1

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES

MAT'L

FINISH

BREAK ALL SHARP EDGES
DECIMAL XX = ± —
XXX = ± —
ANGULAR ± —

DO NOT SCALE DRAWING

DR K. Stamm 10/12/79
CK [illegible] 10/16/79
APPR [illegible] 10/16/79

PARATRONICS INC.

SCHEMATIC DIAGRAM

EXTENDED MEMORY BOARD

DRWG NO 127-0070-001 REV B
D SCALE NONE SHT 1 OF 1

PARATRONICS INC.

SINGLE LEVEL EXPLOSION

09/04/80

PAR143-0070-0090-00 DESCRIPTION : EXTENDED MEMORY BD, OUTSIDE ECO#: 0 REV.CU.: A

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
111-0207-0103-00	D	22 UF 16V CAP. ELECTRO.,RAD.	1	1	0	08/21/80	OPEN	0	C1
126-0070-0001-00	D	EXT MEMORY P.C.B.	1	1	0	OPEN	OPEN	0	
115-0011-0001-00	D	SOCKET,24PIN	6	1	0	OPEN	OPEN	0	U15
U16 U17 U7	U8	U9							
115-0009-0001-00	D	SOCKET,20PIN	2	1	0	OPEN	OPEN	0	U12
U13									
115-0008-0001-00	D	SOCKET,18PIN	8	1	0	OPEN	OPEN	0	U1
U10 U11 U2	U3	U4 U5 U6							
115-0005-0001-00	D	SOCKET,16PIN	1	1	0	OPEN	OPEN	0	U14
111-0004-0072-00	D	.1 UF 25V CAP. CD	13	1	0	OPEN	OPEN	0	C10
C11 C12 C13	C14	C2 C3 C4 C5	C6	C7	C8	C9			

LEGEND UM : 01=EACH 02=INCH 03=FEET 04=BULK 05=AS REQUIRED 06=OTHER
LEGEND KEY: A=W/PARTS LIST D=W/O PARTS LIST R=REFERENCE DOCUMENT S=SPECIFICATION

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P A R A T R O N I C S I N C .

S I N G L E L E V E L E X P L O S I O N

09/04/80

PAR143-0070-0001-00 DESCRIPTION : EXTENDED MEMORY BD ECO#: 0 REV.CU.: A

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
143-0070-0090-00	D	EXTENDED MEMORY BD, OUTSIDE	1	01	0	OPEN	OPEN	0	
113-0007-0001-00	S	I.C.,. 2716	6	1	0	OPEN	OPEN	0	U15
U16 U17 U7 U8		U9							
113-0006-0001-00	D	I.C., C2114	8	1	0	OPEN	OPEN	0	U1
U10 U11 U2 U3		U4 U5 U6							
113-0014-0001-00	D	I.C., DP8304N, NSC, AMD,	1	1	0	OPEN	OPEN	0	U12
113-0003-0042-00	D	74LS42	1	1	0	OPEN	OPEN	0	U14
113-0051-0001-00	D	MMI 6309-1 PROM	1	1	0	OPEN	OPEN	0	U13

LEGEND UM : 01=EACH 02=INCH 03=FEET 04=BULK 05=AS REQUIRED 06=OTHER
LEGEND KEY: A=W/PARTS LIST D=W/O PARTS LIST R=REFERENCE DOCUMENT S=SPECIFICATION

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8.0 STATE CONTROL BOARD

8.0 STATE CONTROL BOARD

8.1 INTRODUCTION

Hardware registers, counters, and RAMs on the State Control Board are loaded by the Control Program in accordance with information entered from the keyboard under the guidance of the State menu. Using the parameters and modes thus specified, the State Control Board directs associated circuitry in the implementation of the various State analysis features.

8.2 FUNCTIONAL DESCRIPTION

A block diagram of the State Control Board is shown in figure 8-1. When appropriate during the following discussion, please refer to this figure and to the schematic diagram, board layout, and parts list which are included at the end of this section. Also, tables of connector pins versus signal names for all motherboard connectors are provided in section 15 along with an alphabetical list of all interboard signals. And, should the need arise, a Glossary in section 16 offers explanations for acronyms or terms that may be unfamiliar.

As shown in the block diagram, the major functional units of the State Control Board circuitry are the Processor Interface, Stack Management, Clock Control, the Collection Address Counter, the Posttrigger Counter, the Restart Generator, and Trigger Delay Control. These units are discussed further in the following subsections.

8.2.1 Processor Interface

The Processor Interface (see schematic sheet 1) comprises the Address Decoder, the Status Ports, the Interface Output Ports, and the Interface Shift Register. This circuitry allows the processor, under the direction of the Control Program, to load user-supplied information (entered from the keyboard with the aid of the menu) into registers, RAMs, and counters in order to prepare the analyzer for the intended application. Also, it allows the processor to interrogate various status and signal lines and to send various control signals when appropriate.

The Address Decoder consists of: U31, a 74LS10 triple 3-input NAND gate; U1A,C, sections of a 74LS00 quad NAND gate; and U42 and U43, 74LS138 3-to-8 decoders. This circuitry allows the processor to write to the Interface Output Ports and read from the Interface Status Ports by using I/O write and read commands. Also, one port output signal, RDABMEM (U42-15), is used in the Collection Address Counter to be discussed later.

The Interface Output Ports, U44 and U45, are both 74LS374 octal D flip-flops. Both store software-generated control signals; U44 for the State Control Board, and U45 for the A and B Probes and the A and B State Memory Boards.

The Status Ports, U46 and U47, are both 74LS244 octal line receivers. The processor reads status signals from the State Control Board through most

of U46, and from the A and B Probes through U46-11,17. The processor reads data-collection addresses from the State Control Board through U47.

The Interface Shift Register has a part shown on each sheet of the schematic. It consists of: U36, a 74LS164 8-bit shift register (on sheet 1); U30B, 1/2 of a CMOS 4015 dual 4-bit shift register (on sheet 2); U11, a 4015 (on sheet 3); and U25, U26, and U30A, all 4015s (on sheet 4). These 5 devices have parallel readout and allow the processor to store 5 sets of 8 control bits using only one daisy-chained data line (Interface Output Port U44-19) instead of running the 8-bit Processor Data Bus to each of the 5 devices. This 40-bit shift register stores control bits (U36, U30A) and preset counts (U30B, U11, U25, U26) for use by various circuits on the State Control Board. The last bit in the last shift register, U36-13, is fed back into the Status Port at U46-6 so the Control Program can monitor the Shift Register load status.

8.2.2 Stack Management

Stack Management (schematic sheet 2) comprises the Stack Address Counter, Stack Address Latches, and Stack Control circuits. This circuitry maintains the stack pointer (by means of the Stack Address Counter) and evaluates a number of input signals to determine when it is appropriate to POP (advance) or reset the stack pointer.

The Stack Address Counter, U41, a 74S169 synchronous four-bit binary counter, generates signal NSA (Next Stack Address). This signal is fed to the address inputs of the Delay Count RAM on this board and of the Trigger Stack RAM on each of the two State Memory Boards. The trigger stack address on the circuit board is the equivalent of the trigger level on the menu.

The stack RAMs are treated (non-conventionally) as first-in-first-out, push-down stacks whose terminal addresses are OF hex (15 dec). The Stack Address Counter is preset by the Control Program (through the U30B section of the Interface Shift Register) with the correct address for the already-PUSHed stack; and the counter always operates in the POP direction; that is, it always counts up. For example, if the menu specified trigger levels 0 thru 8, the Stack Address Counter would be preset with OF - 8 = 07. This RAM location, address 07, would contain the word for the first trigger level entered on the menu, level 0. The last address reached by the counter, OF, would contain the word for the last trigger level entered on the menu, level 8. At count OF, the counter's ripple-carry out of pin U41-15 produces the stack-empty signal, STKE-, which is used by the Stack Control circuitry.

The Stack Address Latches, U51 and U52, are both 74S74 dual D flip-flops. They latch the address produced by the Stack Address Counter so it is properly stabilized for the Trigger- and Qualifier-Word RAMs on the State Memory Boards.

The Stack Control circuits consist of: U50A,B,D, sections of a 74S86 quad exclusive-OR gate; U35C,D, sections of a 74S02 quad NOR gate (here used as inverters); U29, a 74S02 quad NOR gate (sections A and B are here used as negative-input AND gates); U38B, 1/2 of a 74S74 dual D flip-flop; U27, a

74S64 4-2-3-2 AND-NOR gate; U28, a 74S74 dual D flip-flop; and U21B, a section of a 74LS32 quad OR gate.

This circuitry produces a number of signals used by Stack Management and a number of signals used elsewhere on the board. In particular, it produces: POPEN- (POP Enable -), which advances the level in the trigger-delay stack on this board and in the trigger- and qualifier-word stacks on the two State Memory Boards; POPSTK+ (POP Stack +, a clock derived from POPEN-), which advances the level in the delay-mode stack; and PTENB+ (Posttrigger Enable +, derived from the Stack Address Counter's ripple-carry signal, STKE-), which is fed to the Posttriger Counter where it starts the count for collecting the specified number of posttrigger data words.

8.2.3 Clock Control

Clock Control comprises the Clock Multiplexer (see schematic sheet 2) and the Clock Qualifier Gate (see schematic sheet 3). This circuitry implements the keyboard-entered selection of clock source and provides the final logic in the process of clock qualification.

The Clock Multiplexer consists of: U37, a 74S64 4-2-3-2 AND-NOR gate; U39A, 1/2 of a 74S51 dual AND-NOR gate; and U40, 1/4 of a 10125 quad ECL-to-TTL translator. With the aid of software-generated CLKSEL signals from Interface Shift Register U36, the Clock Multiplexer implements menu selection of clocks for probe-data latches on the A and B Memory Boards. The A-Board clock, ALATCHCLK, may be menu-selected from either the positive- or negative-going edge of APROBCLK (the A-Probe incoming clock). The B-Board clock, BLATCHCLK, may be menu-selected from either APROBCLK or the positive- or negative-going edge of BPROBCLK (the B-Probe incoming clock). In the 40-bit State mode, the Control Program forces both the A- and B-Board clocks to CT, the Timing clock (which may be either the internal clock or the positive- or negative-going edge of the Timing Probe incoming clock).

The Clock Qualifier Gate, U39B (top of schematic sheet 3), 1/2 of a 74S51 dual AND-NOR gate, produces signals ACLKQUALIN- and BCLKQUALIN-, which go to State Memory Boards A and B, respectively, where they enable clocking of data collection. BCLKQUALIN- (B Clock Qualifier In) is generated if the incoming clock qualifier signals ACQ1 .AND. BCQ1 are active, .OR. if ACQ2 .AND. BCQ2 are active. ACLKQUALIN- is hard-wired active low by the ground connection to pin S2-8. (The implications of this connection are discussed in the description of the State Memory Boards in section 9.)

The signals ACQ1,2 and BCQ1,2 come from pre-collection comparator RAMs on the State Memory Boards A and B. In the 32-bit mode, ACQ1 is active high if, in the first clock-qualifier word specified in the menu, the first 16 data bits, first 2 qualifier bits, and 1 link bit are matched by the bits coming in on the A-Probe lines. BCQ1 is high if, in the first clock-qualifier word specified in the menu, the second 16 data bits and second 2 qualifier bits are matched by the bits coming in on the B-Probe lines. If the entire first clock-qualifier word is matched, ACQ1 and BCQ1 are both high and BCLKQUALIN goes active low. In the 16-bit mode, the A- and B-Probe lines are connected in parallel, and ACQ1 and BCQ1 act as if tied together. In the 40-bit mode,

the clock-qualifier words are not allowed and BCLKQUALIN- is always low (the Control Program treats the clock-qualifier words as all Xs).

Similarly, ACQ2 and BCQ2 represent the second clock-qualifier word on the menu.

It is important to note the distinction between qualifier words, associated with the menu, and qualifier bits, associated with the probe leads. The A and B probes each have two qualifier leads. Each of the two leads on each of the probes can be used for either trigger qualification or clock qualification or both. The selection is made on the State menu. On the 32-channel State menu, the qualifier bits appear in the clock-qualifier word or trigger word as -XXXX. The X's mark the positions, left to right, of AQ1, AQ2, BQ1, BQ2. If, in the clock-qualifier word, a value is given to the first X, such as -OXXX, then AQ1 is thereby assigned as a clock qualifier. (If the first X is also given a value in a trigger word, then AQ1 is thereby also assigned as a trigger qualifier.)

The two OR-logic clock-qualifier words on the State menu consist of all the data bits as well as the qualifier bits and the Timing link bit. As previously stated, the ACQ1 family of signals is associated with the entire clock-qualifier word, not just the qualifier bits.

8.2.4 Collection Address Counter

The Collection Address Counter (see schematic sheet 3) consists of: U48 and U49, 74LS191 synchronous 4-bit binary counters; U24C, 1/4 of a 74S00 quad NAND gate (here used as a negative-input OR gate); and U14B and U38A, each 1/2 of a 74S74 dual D flip-flop. During the collection process, this circuitry supplies 256 sequential storage addresses for the Data Collection RAMs on the State Memory Boards. During display and analysis, the same circuitry allows the processor to address those RAMs when reading the collected data.

The two 4-bit counters are connected in cascade to form an 8-bit counter with a capacity of 256 counts. The counter's parallel outputs, RA0 through RA7, are fed as address bits to the Data Collection RAMs on the two State Memory Boards. In the load mode, the counters pass the input levels straight through to the outputs, thus allowing the processor to directly address the RAMS. This load mode is initiated by RDABMEM- (Read A or B Memory -), a Control Program signal from the Processor Interface. Just before the Control Program releases RDABMEM-, it places all-zeros on the counter input lines. Thus, when RDABMEM- is released to high, the counter is preset to 00.

With the RDABMEM- load signal inactive (high) the counters are ready to generate sequential addresses for the Data Collection RAMs. The count is advanced with each BWE+ clock pulse. BWE+ (B Write Enable +) is the qualified data collection clock. It comes from State Memory Board B where it is enabled by BCLKQUALIN-, which in turn was sent to the Memory Board from this board's Clock Qualifier Gate (described in the foregoing subsection).

As the counters count from 00 through FF, the ripple-carry out of U49-13 (occuring at count FF) is fed to the two flip-flops, U38A and U14B. This circuitry generates signal ROLLOVER1+ the first time address FF is reached and

signal ROLLOVER2+ the second time. These two signals are fed to Interface Status Port U46 for use by the Control Program.

The counter continues to sequence through the RAM address range, rolling over again and again, until the trigger conditions are met and the BWE+ clock is subsequently stopped by signal BCLKINH+ (to be discussed in the following subsection). Of course, in some instances this clock interruption may occur before even the first rollover. In other instances, the interruption may not occur until manual intervention, such as a FORCE DISPLAY or a menu call.

8.2.5 Posttrigger Counter

The Posttrigger Counter (see schematic sheet 3) comprises the Variable Counter, the Fixed Counter, and the Clock Inhibit circuits. This circuitry causes data collection to continue for the menu-specified number of data words after the trigger conditions have been met. Actually, the menu expresses this parameter as pretrigger count, but the Control Program converts the number to posttrigger count for more efficient circuit implementation.

The menu allows a pretrigger count range of 0 to 250 words. In the 32-bit x 250-word State mode, this translates into a posttrigger count range of 250 to 0 words. And in the 16-bit x 500-word State mode, it translates into a posttrigger count range of 500 to 250 words. Note that while there can be 0 posttrigger words in the 32-bit mode, but there will always be at least 250 posttrigger words in the 16-bit mode.

The Variable Counter consists of U10 and U12, 74LS161 synchronous 4-bit binary counters. They are combined to form an 8-bit counter with a maximum count of FFh (255d). This counter serves to count the variable portion of the posttrigger count in the 16-bit mode and all of the posttrigger count in the 32-bit mode.

At setup time, the Control Program presets the counter to the proper calculated value. The value loaded is FF - c, where c is the posttrigger count. This transformation is done so the ripple-carry ouput can be used as an indication that the count has been completed. (The actual loaded value may vary by one or two counts from FF - c to compensate for propagation delays in associated circuitry.)

When the trigger conditions have been met, signal PTENB+ (PostTrigger Enable) goes high, disabling the load inputs and enabling the count function. The counter advances at each pulse of BWE+, the qualified data-collection clock. Count completion is announced, as just mentioned, by the ripple-carry output at U12-15.

The Fixed Counter consists of U22 and U23, also 74LS161s connected as an 8-bit counter with a maximum count of FF. The parallel inputs to this counter are hard-wired to load the count of 6, thus leaving 249d as the upward count to produce the ripple-carry (the missing count is a propagation time correction). If the 16-bit x 500-word mode has been selected, this counter serves as the posttrigger counter for the B Memory Board. (Recall that in the 16-bit mode, the 250 words of the B Memory must always be allocated to posttrigger data.)

The Clock Inhibit circuit consists of: U33B,C,D, each 1/4 of a 74S00 quad NAND gate (B and C are here used as negative-input OR gates); U21C, 1/4 of a 74LS32 quad OR gate; U32, a 74S74 dual D flip-flop; and U13B, 1/2 of a 74S51 dual AND-NOR gate. When the posttrigger count has been reached, this circuitry generates clock-inhibit signals as follows.

When the Variable Counter reaches its terminal count, the ripple-carry output at U12-15 goes high, producing signal ACTDN+ (A Countdown +). This signal goes through U21C to set flip-flop U32B, whose Q- output in turn goes through U33C to produce signal ACLKINH+ (A Clock Inhibit +). This signal goes to the A Memory Board and inhibits any further clocking of collected data into the A Memory. (The Q output of U32B is fed back through U21C to latch the set condition of U32B past the duration of the ripple-carry pulse.)

If the 32-bit mode is in effect, signal SEL32+ is high and lets signal ACTDN+ through multiplexer U13B to reset flip-flop U32A. The Q output of U32A in turn goes through U33B to produce signal BCLKINH+ (B Clock Inhibit +) which is sent to the B Memory Board. There, BCLKINH+ stops the generation of the BWE+ clock pulse fed to this board, and this stops all posttrigger counting.

The Q- output of flip-flop U32A produces the signal PTCTDN+ (Posttrigger Countdown +) which is fed to Interface Status Port U46 to let the Control Program know that the posttrigger countdown has been completed.

If the 16-bit mode is in effect, ACTDN+ does not get through U13B to reset U32A, and BCLKINH+ is not then produced. However, output Q of flip-flop U32B (which has been latched in the set condition) is fed to the load inputs of the Fixed Counter. This signal disables the load mode and allows the counter to begin counting BWE+ clock pulses. Recall that this counter has been preset to 6 and must count 249d more clocks to terminal count. When terminal count is reached, the ripple-carry output, BCTDN+ (B Countdown +), goes through U13B to reset flip-flop U32A and produce signals BCLKINH+ and PTCTDN+ as previously described.

If the posttrigger count is 0, the signals PSTTG0+ (Posttrigger 0) and PTENB+ are high at the inputs of NAND gate U33D. The resulting low output from U33D then presets flip-flop U32A and clears flip-flop U32B, thereby producing ACLKINH+, BCLKINH+, and PTCTDN+ without any counting having occured.

The Control Program can also produce signals ACLKINH+ and BCLKINH+ by sending signal SWCLKINH- (Software Clock Inhibit -) to the inputs of negative OR gates U33B and U33C.

8.2.6 Restart Generator

The Restart Generator (see schematic sheet 3) consists of: U35A,B, two sections of a 74S02 quad NOR gate (here used as negative input AND gates); and U34, a 74S64 4-2-3-2 AND-NOR gate. This circuit generates the RST- (Restart) signal, which is used by Stack Management to reload the trigger Stack Address Counter with the address for level 0 (this address is still latched in Interface Shift Register section U30B) and start over again in the testing for a match of trigger conditions.

Signal RST- is produced under any of the following conditions:

a. the NNNNth clock is reached when the ON-NNNNth-CLOCK delay mode is in effect

b. the NNNNth clock is reached when the BEFORE-NNNNth-CLOCK delay mode is in effect

c. the menu-specified RESTART word is recognized

d. the Control Program outputs the signal LDSTKAD+ (Load Stack Address) from Interface Output Port U44-2

8.2.7 Trigger Delay Control

Trigger Delay Control (see schematic sheet 4) comprises the Delay Count RAM, the Delay Counter, the Delay-Mode RAM, and Delay-Mode Control. These circuits implement the various menu-selectable trigger-delay functions. When the specified delay conditions have been met, on a level-by-level bassis, the circuits produce signals that allow the search for trigger words to proceed to the next level. (NOTE: The trigger word at level 0 does not have a delay function.)

The Delay Count RAM consists of U15, U16, U17, and U18, all 74S189 16-word x 4-bit static RAMs. They are connected in cascade as a 16-word x 4 4-bit digit RAM. This RAM is loaded by the processor at setup time with the menu-selected delay count (with a count range of 0—9999d) for each of the 15 delayable trigger-word levels. The stored delay counts are then used to preset the Delay Counter as each trigger-word level is reached during the processing of incoming data.

The 4 address lines of each RAM are fed in parallel with signal NSA (Next Stack Address) which comes from the Stack Address Counter. (The 4 address bits decode into 16 stack addresses which correspond to the 16 trigger-word levels on the menu.) When loading the RAM at setup time, the Control Program addresses it through the transparent Stack Address Counter using section U30B of the Interface Shift Register. Delay-count data for the RAM is loaded using sections U25 and U26 of the Shift Register. After loading is completed, the Control Program presets the Stack Address Counter with the address count corresponding to the number of trigger levels specified on the menu.

After RESET, the RAM's addresses come from the counting Stack Address Counter and start with trigger-word level 0. (Although there can be no delay specified for trigger-word level 0, the level is stepped through for simplicity of logic. Also, note that trigger-word level 0 does not correspond to stack address 0 unless all 16 trigger-word levels are specified on the menu). As each trigger stack level is entered, the stored 4-digit delay count for that level is fed from the Delay Count RAM to the Delay Counter as four 4-bit sections in parallel.

The Delay Counter consists of: U2B,C,D, sections of a 74S08 quad AND gate; U19, also a 74S08; U4, U5, U6, and U7, all 74S162 synchronous 4-bit decade counters; and U24A, 1/4 of a 74S00 quad NAND gate. At the start of

processing for each stack level, signal POPEN- (from Stack Control) is brought low. This loads the Delay Counter with the count stored in the Delay Count RAM for that stack level. The count value stored and loaded is 9999d - c, where c is the menu-specified count. This conversion is done so the ripple-carry out of U7-15 can be used to indicate terminal count. (The actual loaded value may vary by one or two counts from 9999d - c to compensate for propagation delays in associated circuitry.) When POPEN- returns high, the counter begins to count.

The count is advanced by DBCLK+ (Delayed B Clock +, derived from BWE+, the qualified data collection clock) when the count-enable inputs at P (pin 7 on U4,5,6,7) are high. (U2B,C,D and U19A,B provide carry look-ahead to speed up the counter.) The P inputs are fed with signal TRIGCTEN+ (Trigger Count Enable +) from Delay Mode Control. If the menu-specified delay mode calls for counting clocks, Delay Mode Control holds the P inputs continually high. If the delay mode calls for counting trigger-word recognitions, at each such recognition, Delay Mode Control pulses the P inputs high long enough for the counter to count one clock.

When the terminal count is reached, the resulting ripple-carry out of U7-15 goes through U19C,D and U24A to produce signals DLYCTDN+ and DLYCTDN- (Delay Countdown + and -).

The Delay-Mode RAM, U20, is a 74S189 16-word x 4-bit static RAM. As with the Delay Count RAM, the 16 word-addresses represent the 16 levels of the trigger stack. This RAM is loaded by the processor at setup time (using sections U30A and U30B of the Interface Shift Register) with the menu-selected delay mode for each of the 15 delayable trigger-word levels. The 4 data bits encode the mode information as follows. D2, D3, and D4 constitute a 3-bit code for the 5 available delay modes. D1 is high if triggering is to occur on, or be delayed from, the trigger word itself. D1 is low if triggering is to occur on, or be delayed from, all but the trigger word. (The mode encoded by D1 is not, strictly speaking, a delay mode; it applies to both delayed and undelayed trigger recognition.)

For reference, the available trigger-word delay modes and their stored codes are:

	Menu Delay Mode		D4	D3	D2
The trigger word	occurs	AFTER NNNNth CLOCK	0	0	0
	occurs	BEFORE NNNNth CLOCK	1	0	0
	occurs	ON NNNNth CLOCK	0	1	0
	occurs	NOT ON NNNNth CLOCK	1	1	0
		OCCURS NNNN TIMES	0	0	1

Delay-Mode Control consists of: U8 and U9, two 74S74 dual D flip-flops; U3, a 74S64 4-2-3-2 AND-NOR gate; U14A, 1/2 of a 74S74; and U13A, 1/2 of a 74S51 dual AND-NOR gate.

The U8 and U9 flip-flops latch the delay-mode code bits, read out of the Delay-Mode RAM at NSA time, for use during the processing of the current stack

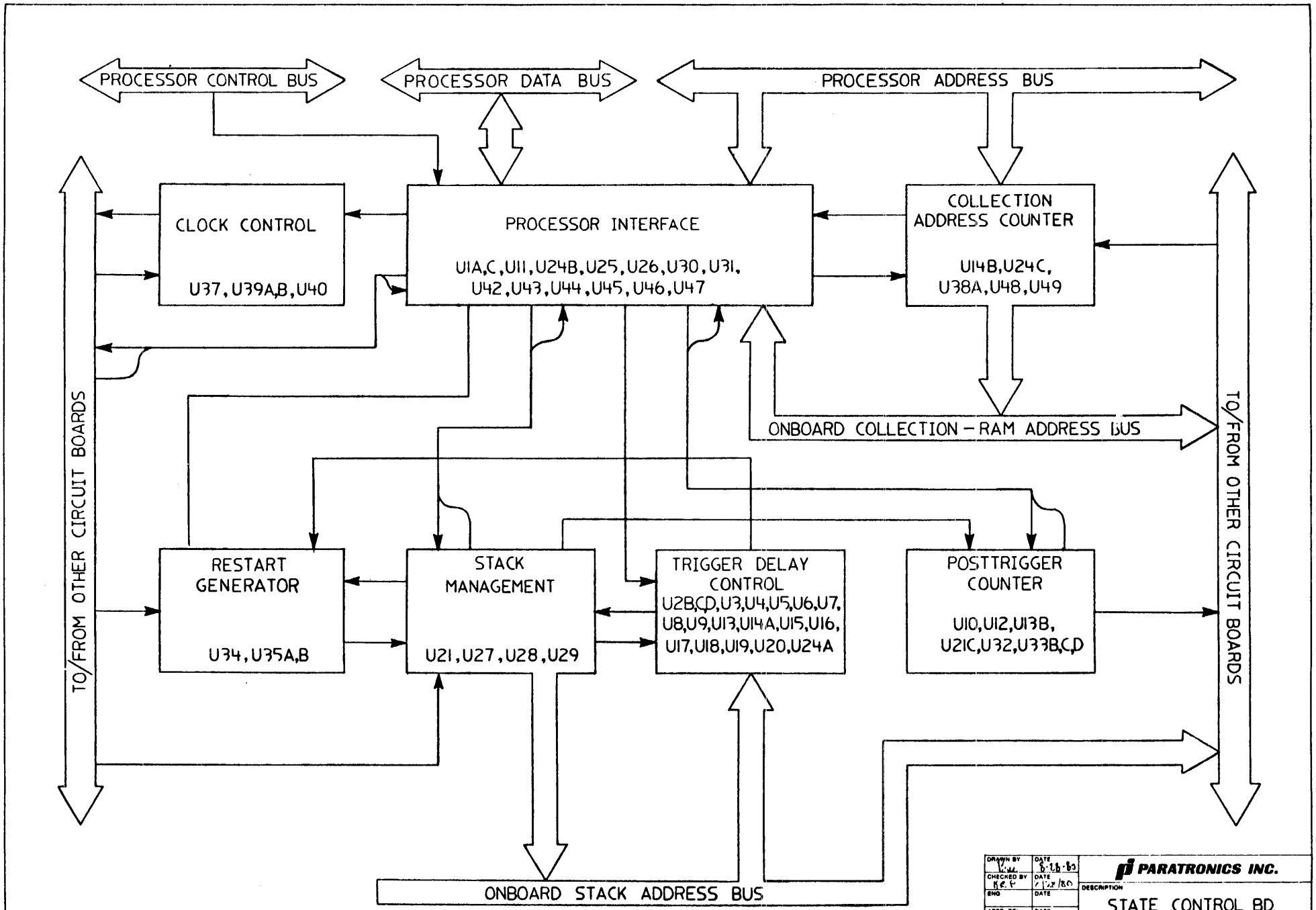
level. The U14A flip-flop generates a one-clock-interval pulse on the NNNNth clock for use by the U3 multiplexer.

The U13A AND-NOR gate uses TRIGCTSEL+ (Trigger Count Select +), the latched D2 mode-code bit, to determine the nature of output signal TRIGCTEN+ (Trigger Count Enable+) which is fed to the P enable inputs of the Delay Counter. If TRIGCTSEL+ is high, TRIGCTEN+ is held low except when TRIG- (Trigger-word recognized -) pulses it high at each trigger-word recognition long enough for the Delay Counter to count one clock. In this mode (D2 = 1), the Delay Counter counts trigger-word occurrances. If TRIGCTSEL+ is low, TRIGCTEN+ is held continuously high. In this mode (D2 = 0), the Delay Counter counts clocks.

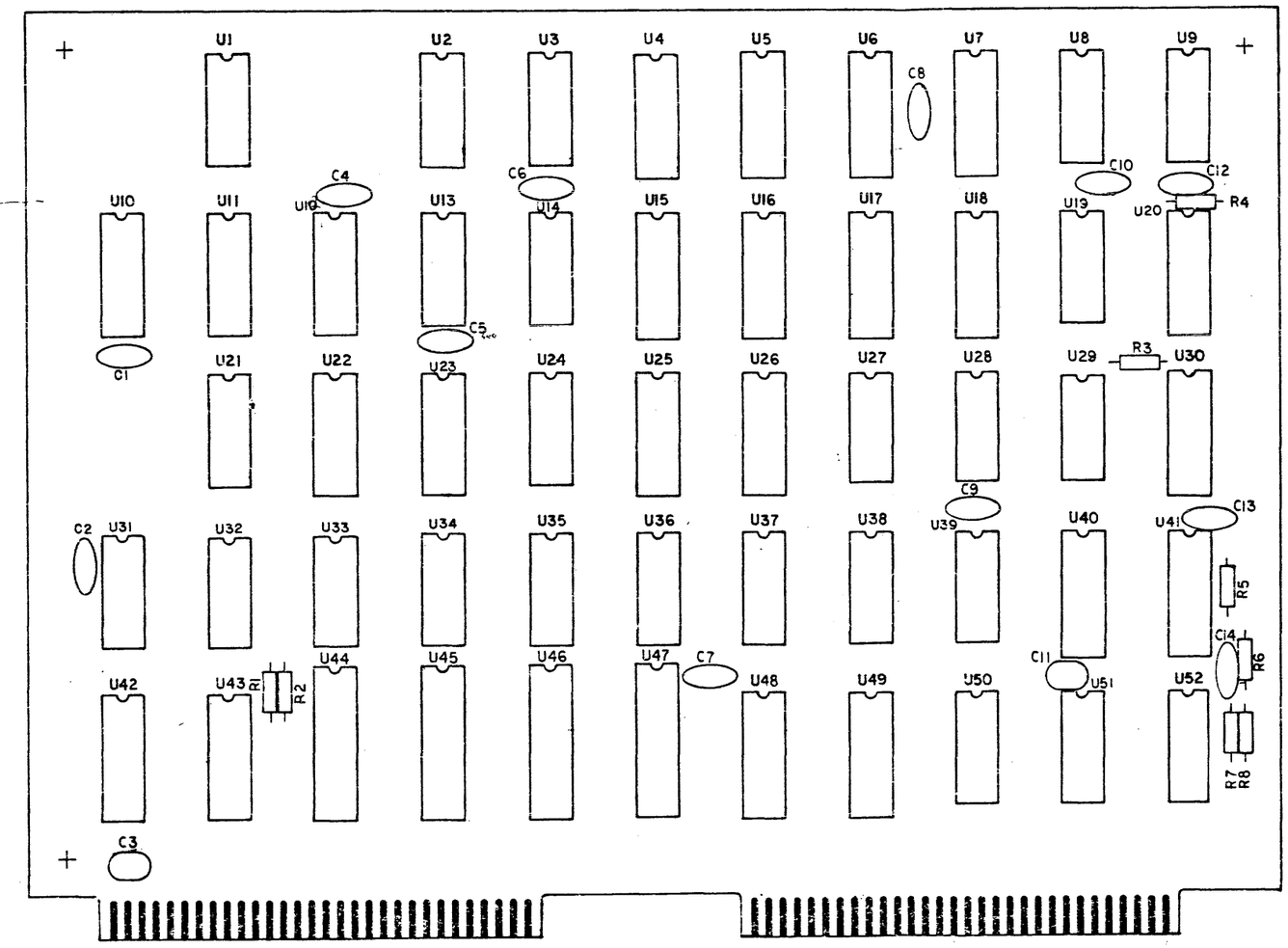
The U3 multiplexer combines the Delay Counter's terminal-count signals, DLYCTDN- and DLYCTDN+, with the current delay mode information and produces signal DLYTC+ (Delay Terminal Count +). This signal is fed to Stack Control multiplexer U27 (schematic sheet 2) where it enables the next trigger-word recognition (signal TRIG+) to generate POPEN-. If other affecting conditions are favorable, POPEN- advances the stack level. In some delay modes, DLYCTDN+ or DLYCTDN- will cause the Restart Generator to produce the RST- signal which overrides DLYTC+ and starts the whole trigger-word search process over again.

8.3 SCHEMATIC, BOARD LAYOUT, & PARTS LIST

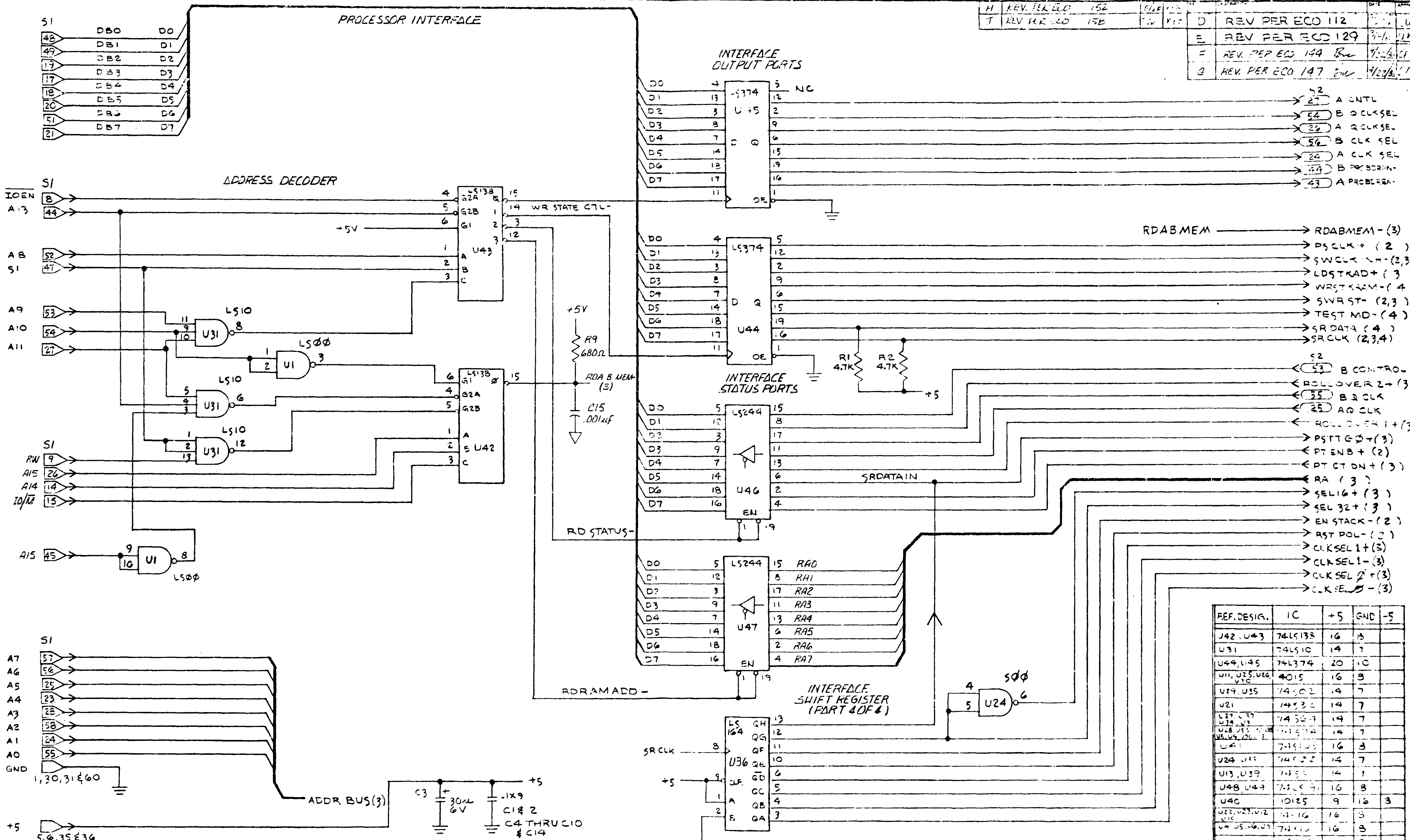
The schematic diagram, board layout, and parts list for the State Control Board are contained on the following pages.



DRAWN BY	DATE 8-26-80	PARATRONICS INC.
CHECKED BY	DATE 9/24/80	DESCRIPTION
ENG	DATE	STATE CONTROL BD. BLOCK DIAGRAM
APPR REL	DATE	
DECIMAL XXX = ± 005, XX = ± 02		C DRAWING NO 145-0069-001
FRACTIONAL ± 1/64		SCALE SHT OF REV
ANGULAR ± 0°30'		
BREAK ALL SHARP EDGES		
DO NOT SCALE DRAWING		



UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR G. S. 12-4-79	PARATRONICS INC.	
MAT'L	BREAK ALL SHARP EDGES DECIMAL ANGULAR .XX = ± .XXX = ±	LEGENDMASTER STATE CONTROL	
FINISH	DO NOT SCALE DRAWING	DRWG NO 126-0069-201 REV. A	
		D SCALE — SHT 1 OF 1	



REV	DESCRIPTION	DATE	APPROVED
H	REV. PER ECO 152		
I	REV PER ECO 158		
D	REV PER ECO 112		
E	REV PER ECO 129		
F	REV. PER ECO 144		
G	REV. PER ECO 147		

REF. DESIG.	IC	+5	GND	-5
U42, U43	74LS138	16	8	
U31	74LS10	14	7	
U44, U45	74LS374	20	10	
U11, U25, U26, U30	4015	16	8	
U29, U35	74S02	14	7	
U21	[illegible]	14	7	
U27, U37, U34, U3	[illegible]	14	7	
U28, U32, ... U8, U9, ...	[illegible]	14	7	
U41	[illegible]	16	8	
U24, U33	74S00	14	7	
U13, U39	74S...	14	7	
U48, U49	[illegible]	16	8	
U40	10125	9	16	3
U22, U23, U12, U16	...16	16	8	
U4, U5, U6, U7	74...	16	8	
U5, U6, U7, U8...	[illegible]	16	2	
U1	[illegible]	14	3	
U2, U19	74...	14	7	

REF. DESIG.	I.C.	+5	GND	-5
U36	74LS164	14	7	
U50	74S64	14	7	
U46, U47	74LS244	20	10	

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES

MAT'L

FINISH

BREAK ALL SHARP EDGES — DECIMAL — ANGULAR

DO NOT SCALE DRAWING

PARATRONICS INC.

SCHEMATIC MODEL 540 STATE CONTROL BOARD

DRWG NO 127-0069-001 REV. J

D — SHT 1 OF 4

CORRECTIONS 8-18-80

STACK MANAGEMENT

STACK ADDRESS COUNTER

INTERFACE SHIFT REGISTER (PART 2 OF 4)

STACK ADDRESS LATCHES

STACK CONTROL

CLOCK CONTROL PART 1 OF 2

CLOCK MUX

(3) SRD2

(1) SR CLK +

(4) SRDI +

(1) SWCLK IN H

(4) DLY TC +

(1) ENSTACK

ENSTACK-

RSTL+

SWRST-

PTENB-

TRIG +

(1) SWRST-

(3) RST-

BWE+

BWE+ 35

(1) PSCLK +

BTAPCLK- 37

ATRIG 45

BTRIG 46

(4) TRIGPOL +

(4) TRIGPOL -

ARST 47

BRST 48

(1) RSTPOL -

CT 36

APROBCLK 23

(1) CLKSEL0 -

(1) CLKSEL1 -

(1) CLKSEL0 +

(1) CLKSEL1 +

BPROBCLK 57

NSA (4)

STKE-

NSA3

NSA2

NSA1

NSA0

ENSTACK (1)

DBCLK+

POPEN-

STKCLK+

PTENB-

POPSTK+

TRIG-

TRIG+

BCLK-

DBCLK+(3)

DB CLK+

RSTL-

8 RSTL+

SWRST-

PTENB-

PTENB+(1,3)

S2 42 FS

S2 17 TSA3

S2 18 TSA2

S2 19 TSA1

S2 20 TSA0

TRIGGER RAM STACK ADDRESS

DBCLK+ → DBCLK+(4)

BWE+ → BWE+(3)

RSTL- → RSTL-(3)

POPEN-(2)

POPSTK+(4)

TRIG-(4)

TRIG+(3)

RESTART+(3)

S2 4 A LATCH CLK

S2 34 B LATCH CLK

U30 SRD2

U41 S169

U27 S64

U38 S74

U23A S74

U21B S32

U29B S74

U52 S74

U51 S74

U29 S02

U35C S02

U29C S02

U35D S02

U50A S86

U50B S86

U50C

U40A 1 1012S

U39 S51

U37 S64

R5 330Ω

R6 330Ω

C14 100pf

R7 330Ω

R8 330Ω

R3 330Ω

R4 330Ω

C12 100pf

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR		PARATRONICS INC.
	CK LKS	12/21/79	
MAT'L	APPR		
FINISH	BREAK ALL SHARP EDGES: DECIMAL ANGULAR .XX ± .1 ± .XXX ± .1 DO NOT SCALE DRAWING		DRWG NO 127-0069-001 REV J SHT 2 OF 4 SCALE D

ACQ1 (21)
ECQ1 (51)
ACQ2 (22)
BCQ2 (52)

CLOCK CONTROL PART 2 OF 2

CLOCK QUALIFIER GATE

U39 — S51

S2 (39) BCLKQUALIN-
S2 (6) ACLKQUALIN-

COLLECTION ADDRESS COUNTER

RA7 (9)
RA6 (10)
RA5 (11)
RA4 (12)
RA3 (13)
RA2 (14)
RA1 (15)
RA0 (6)
RAM ADDR B-7 TO MEMORY BOARDS

RA(1)
ROLLOVER2+(1)
ROLLOVER1+(1)

ADDR COUNTERS

(1) ADDR BUS

A7 A6 A5 A4 A3 A2 A1 A0

U49 LS191 — RA7 RA6 RA5 RA4
U48 LS191 — RA3 RA2 RA1 RA0

ROLLOVER LATCHES

U24C — S00 — +5 — U38A — BWE+

S74 — U14B

FIXED COUNTER

BCTDN+

U22 LS161 74 — +5

SWRST- 1/2 74S74 — U32A — CLOCK INHIBIT

U33B — S00 — S2 (38) BCLKINH+

PTCTDN+(1)

(1) RDABMEM-
(2) BWE+

POSTTRIGGER COUNTER

PTØCTDN-

ACTDN+

U21C LS32

(1) PSTTGØ+

U33D — S00 — PTENB+

(1) SWRST-
(1) SRD3
(1) SRCLK

SWRST-

1/2 74S74 — U32B

VARIABLE COUNTER

4015 — U11

U12 LS161 — +5
U10 LS161 — +5

U23 LS161 74

U13B — S51

BWE+

INTERFACE SHIFT REGISTER (PART 3 OF 4)

SEL16+
SEL32+
SWCLKINH-

U33A — S00 — S2 (7) ACLKINH+

RESTART GENERATOR

DLYCTDN
TRIG+

U35A — S02

ON NTH CLOCK
BEFORE NTH CLOCK

U34 — S04 — RST-(2)

MI-
MØ+

U35B — S02

(2) BWE+
(1) SEL16+
(1) SEL32+
(1) SWCLKINH-
(4) DLYCTDN-
(2) TRIG+
(4) MI-
(4) MØ+
(4) DLYCTDN+
(2) RESTART+
(1) LDSTKAD+
RSTL-(2)

DLYCTDN+
RESTART+
LDSTKAD+
RSTL-

(2) SRD2
(2) PTENB+

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR		PARATRONICS INC.
	CK LLOS	4/26/77	
	APPR		
MAT'L	BREAK ALL SHARP EDGES		
	DECIMAL ANGULAR		
	XX ± .2 ± 1		
	XXX ± .2		
FINISH	DO NOT SCALE DRAWING	DRWG NO 127-0069-001	REV G
		D SCALE —	SHT 3 OF 4

TRIGGER DELAY CONTROL

INTERFACE SHIFT REGISTER PART 1 OF 4

DELAY MODE CONTROL PART 1 OF 2

DELAY MODE CONTROL PART 2 OF 2

DELAY-MODE RAM

DELAY COUNT RAMS

DELAY COUNTERS

(1) TEST MD- →

(2) POPSTK+ →

(1) SR CLK →

(1) SR DATA →

(1) WRSTK RAM- →

(2) NSA →

(2) POPEN - →

(2) DB CLK+ →

(2) TRIG- →

SRD1+ → SRD1+ (2)

M1- (3)

MØ+ (3)

DLYTC+ (2)

BEFORE NTH CLOCK

NOT ON NTH CLOCK

TRIG POL+(2)

TRIG POL-(2)

DLYCTDN- (3)

DLYCTDN+ (3)

DBCLK+

TRIG-

TRIG CT SEL+

TRIG CT EN+

U30A ½ 4015 C

U26 4015 D

U25 4015 D

U20 S189

U18 S189

U17 S189

U16 S189

U15 S189

U9 S74

U8 S74

U14A ½ S74

U3 S64

U19A U19B U19C U19D S08

U24A S00

U2D U2C U2B S08

U7 U6 U5 U4 74S162

U13A S51

SRD1+

NSA3 NSA2 NSA1 NSAØ

WR ADD ADC ADB ADA

M1- MØ+ MØ-

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR		PARATRONICS INC.
	CK LIOS	12/26/79	
	APPR		
MAT'L	BREAK ALL SHARP EDGES		
	DECIMAL	ANGULAR	
	XX ±	°	
	XXX ±		
FINISH	DO NOT SCALE DRAWING		DRWG NO 127-0069-001 REV G
			D SCALE SHT 4 OF 4

S I N G L E L E V E L E X P L O S I O N

09/04/80

PAR143-0069-0090-00 DESCRIPTION : STATE CONTROL PCB ASSY-OUTSIDEECO#: 168 REV.CU.: F

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
111-0207-0103-00	D	22 UF 16V CAP. ELECTRO.,RAD.	2	1	0	08/21/80	OPEN	0	C11 C3
111-0012-0039-00	D	330 PF 1KV CAP. CD	1	1	0	07/11/80	OPEN	0	C15
110-0005-0051-00	D	330 OHM 1/4W 5% CF RES	6	1	0	OPEN	OPEN	0	R3 R4 R5 R6 R7 R8
111-0012-0030-00	D	100 PF 1KV CAP. CD	2	1	0	OPEN	OPEN	0	C12 C14
110-0005-0079-00	D	4.7 K OHM 1/4 W CF RES	2	1	0	OPEN	OPEN	0	R1 R2 R9
111-0004-0072-00	D	.1 UF 25V CAP. CD	10	1	0	OPEN	OPEN	0	C1 C10 C13 C2 C4 C5 C6 C7 C8 C9
115-0003-0001-00	D	SOCKET,14PIN	25	1	0	OPEN	OPEN	0	U1 U13 U14 U19 U2 U21 U24 U27 U28 U29 U3 U31 U32 U33 U34 U35 U36 U37 U38 U39 U50 U51 U52 U8 U9
115-0005-0001-00	D	SOCKET,16PIN	23	1	0	OPEN	OPEN	0	U10 U11 U12 U15 U16 U18 U19 U20 U22 U23 U25 U26 U30 U4 U40 U41 U42 U43 U48 U49 U5 U6 U7
115-0009-0001-00	D	SOCKET,20PIN	4	1	0	OPEN	OPEN	0	U44 U45 U46 U47
126-0069-0001-00	D	STATE CONTROL PC FAB	1	1	0	OPEN	OPEN	0	

LEGEND UM : 01=EACH 02=INCH 03=FEET 04=BULK 05=AS REQUIRED 06=OTHER
LEGEND KEY: A=W/PARTS LIST D=W/O PARTS LIST R=REFERENCE DOCUMENT S=SPECIFICATION

****

BM301A

PARATRONICS INC.

SINGLE LEVEL EXPLOSION

09/04/80

PAR143-0069-0001-00 DESCRIPTION : STATE CONTROL PC ASSY ECO#: 168 REV.CU.: F

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
113-0002-0086-00	D	I.C., 74S86	1	1	0	OPEN	OPEN	0	U50
113-0003-0000-00	D	I.C., 74LS00	1	1	0	OPEN	OPEN	0	U1
113-0003-0032-00	D	I.C., 74LS32	1	1	0	OPEN	OPEN	0	U21
113-0002-0169-00	D	74S169 IC. T.I.	1	1	0	OPEN	OPEN	0	U41
113-0002-0008-00	D	74S08 I.C.	2	1	0	OPEN	OPEN	0	U19
U2									
113-0003-0164-00	D	I.C., 74LS164	1	01	0	OPEN	OPEN	0	U36
113-0002-0000-00	D	I.C., N74S00N	2	1	0	OPEN	OPEN	0	U24
U33									
113-0002-0002-00	D	I.C., 74S02	2	1	0	OPEN	OPEN	0	U29
U35									
113-0002-0051-00	D	I.C., 74S51	2	1	0	OPEN	OPEN	0	U13
U39									
113-0002-0064-00	D	I.C., 74S64	4	1	0	OPEN	OPEN	0	U27
U3 U34 U37									
113-0002-0074-00	D	I.C., 74S74	8	1	0	OPEN	OPEN	0	U14
U28 U32 U38 U51 U52 U8 U9									
113-0002-0162-00	D	I.C., 74S162	4	1	0	OPEN	OPEN	0	U4
U5 U6 U7									
113-0002-0189-00	D	I.C., 74S189	5	1	0	OPEN	OPEN	0	U15
U16 U17 U18 U20									
113-0003-0010-00	D	I.C., 74LS10	1	1	0	OPEN	OPEN	0	U31
113-0003-0138-00	D	I.C., 74LS138	2	1	0	OPEN	OPEN	0	U42
U43									
113-0003-0161-00	D	I.C., 74LS161	4	1	0	OPEN	OPEN	0	U10
U12 U22 U23									
113-0003-0191-00	D	I.C., 74LS191	2	1	0	OPEN	OPEN	0	U48
U49									
113-0003-0244-00	D	I.C., 74LS244	2	1	0	OPEN	OPEN	0	U46
U47									
113-0003-0374-00	D	I.C., 74LS374	2	1	0	OPEN	OPEN	0	U44
U45									
113-0042-0001-00	D	SCL4015BE	4	1	0	OPEN	OPEN	0	U11
U25 U26 U30									
113-0200-0125-00	D	I.C., MC10125	1	1	0	OPEN	OPEN	0	U40
143-0069-0090-00	D	STATE CONTROL PCB ASSY-OUTSIDE	1	1	0	OPEN	OPEN	168	

LEGEND UM : 01=EACH 02=INCH 03=FEET 04=BULK 05=AS REQUIRED 06=OTHER
LEGEND KEY: A=W/PARTS LIST D=W/O PARTS LIST R=REFERENCE DOCUMENT S=SPECIFICATION

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9.0 STATE MEMORY BOARD

9.0 STATE MEMORY BOARD

9.1 INTRODUCTION

The State Memory Board accepts data from 16 incoming data lines and, if so directed by State Control, stores it for later analysis and display. The PI 540 has two State Memory Boards; one for the 16 data lines from Probe Pod A, and one for the 16 data lines from Probe Pod B. They are called State Memory Board A and State Memory Board B, respectively. The two boards are identical and interchangeable. However, certain connections to the Function Motherboard sockets cause the board plugged into the socket allocated to Board A to operate somewhat differently than the one plugged into the socket allocated to Board B. The following discussion will present the State Memory Board without regard to whether it is an A board or a B board except in the few places where it is appropriate to make a distinction.

9.2 FUNCTIONAL DESCRIPTION

A block diagram of the State Memory Board is shown in figure 9-1. When appropriate during the following discussion, please refer to this figure and to the schematic diagram, board layout, and parts list which are included at the end of this section. Also, tables of connector pins versus signal names for all motherboard connectors are provided in section 15 along with an alphabetical list of all interboard signals. And, should the need arise, a Glossary in section 16 offers explanations for acronyms or terms that may be unfamiliar.

As shown in the block diagram, the major functional units of the State Memory Board circuitry are the Qualifier-Word RAM, the Trigger-Word RAM, the Data Collection RAM, the Address Decoder, the Clock Generator, and a number of I/O buffers.

When considering the three memory systems of the State Memory Board, the qualifier-word memory and trigger-word memory can be thought of as comparison devices, whereas the data-collection memory is the more usual storage device. Broadly speaking, these memories operate as follows.

At setup time, the Control Program stores the two menu-specified clock-qualifier words in the Qualifier-Word RAM. It also stores all the specified trigger words, level by level, in the Trigger-Word RAM. At run time, an incoming data word is clocked into the Probe Input Buffer by the primary external clock. (A data word consists of the 18 parallel bits existing at clock time on the 16 incoming data lines and 2 incoming qualifier lines.) From the buffer, the data is fed to the Qualifier-Word RAM and the Trigger-Word RAM, but not yet to the Data Collection RAM.

The Qualifier-Word RAM compares the incoming data word with the two clock-qualifier words; and the Trigger-Word RAM compares the incoming data word with the trigger word at the current trigger stack level. If the data word is found to match either of the two menu-specified clock-qualifier words, the current clock period is considered qualified for data collection. As a result, the data in the Probe Input Buffer is stored in the Data Collection

RAM and the outcome of the trigger-word comparison (which has taken place concurrently with the qualifier-word comparison) is processed.

However, if the qualifier-word comparison does not qualify the current clock period, the data word is not stored in the Data Collection RAM and the outcome of the trigger-word comparison is ignored. (Of course, the menu may have specified all bits in the clock-qualifier words as "dont care" Xs, in which case all clock periods qualify.)

This operation is described in more detail in the following subsections.

9.2.1 Input/Output Buffers

The Input/Output Buffers comprise the Probe Input Buffer, the Probe Output Buffer, the Setup Data Buffer, the Read-TSA (Trigger Stack Address) Buffer, the Collection Address Buffer, the Collection Input Buffer, and the Collection Output Buffer.

The Probe Input Buffer consists of: U15 and U16, both 74S374 octal D flip-flops; and U26A, 1/2 of a 74S374. The 16 data inputs of U15 and U16 are connected through P2 to the 16 incomming data lines from the probe pod. The 16 data outputs are fed to the Collection Input Buffer and to address inputs on both the Qualifier-Word RAM and the Trigger-Word RAM. (The reason for connecting these data lines to the address lines of the two RAMs will be discussed later.)

Two of the four inputs of U26A are connected through P2 to the two qualifier lines, Q1 and Q2, from the probe pod. One of the remaining two inputs of U26A is connected through P2 to the trigger output, FT, of the timing analyzer section. The other is connected through P2 to the external input, EXT, from the BNC connector on the rear panel. The four outputs of U26A are connected to address inputs on both the Qualifier-Word RAM and the Trigger-Word RAM.

U15, U16, and U26A are all clocked by the menu-selected primary external clock, LATCHCLK, which is fed from the State Control Board through P2. The outputs of all three devices are enabled by signal DATEN- (Data Enable -) from the Address Decoder.

The Probe Output Buffer consists of U17 and U24, both 74S374 octal D flip-flops. This buffer is used to send data from the processor to optional or custom probes designed to accommodate data output.

The 8 inputs of U17 are connected in parallel with those of U24 to the 8-bit Processor Data Bus. The outputs of U17 and U24 are connected in cascade through P2 to the 16 probe data lines. Demultiplexing of the 8-bit input to the 16-bit output is accomplished by the Control Program with the aid of the buffer's two input strobe signals, W6- and W7- (Write 6 -, and Write 7 -). The 3-state outputs are enabled by PROBDREN- (Probe Data Remote Enable -) from State Control.

The Setup Data Buffer consists of: U10 and U11, both 74LS244 octal buffers; and U28B, 1/2 of a 74LS244. This buffer is used by the processor for

loading setup information (obtained from the menu) into the Qualifier-Word and Trigger-Word RAMs in a manner that will be described in later paragraphs.

The 20 output lines are connected in cascade through the Onboard Data-In Bus to 20 address inputs of the RAMs just mentioned. The 20 inputs are connected in 5 paralleled sets of 4 lines to 4 lines of the Processor Address Bus. In the case of the Qualifier-Word RAM, demultiplexing of the 4 input lines to the 20 output lines is accomplished by the Control Program with the aid of the 5 write signals, WO- through W4-. In the case of the Trigger-Word RAM, the demultiplexing is accomplished by the Control Program with the aid of the RAM organization. The buffer's 3-state outputs are enabled by signal SDBUFEN- (Setup Data Buffer Enable -) from the Address Decoder.

The Read-TSA Buffer (TSA = Trigger Stack Address) consists of U28A, 1/2 of a 74LS244 octal buffer. It is used by the processor to read the trigger stack address supplied to the Trigger-Word RAM by State Control. The 4 input lines are fed from the State Control Board through P2, and the 4 output lines are connected to the Processor Data Bus. The outputs are enabled by signal RDSTKADD (Read Stack Address) from the Address Decoder.

The Collection Address Buffer consists of U36, a 74LS373 octal D latch. Its 8 input lines are connected through P2 to the RA (RAM Address) signal from State Control, and its 8 output lines are connected to the 8 address inputs of the Data Collecation RAM. If the current clock period is qualified for data collection, the RA signal from State Control is latched into the buffer by the negative-going WE- (Write Enable -) pulse from the Clock Generator. This data collection address is held stable at the outputs of the Collection Address Buffer for the duration of the WE- pulse, which is also the write pulse for the Data Collection RAM.

The Collection Input Buffer consists of U6 and U14, both 74S373 octal D latches. The buffer's 16 inputs are fed from the 16 outputs of the Probe Input Buffer. The buffer's 16 outputs are connected to the 16 data inputs of the Data Collection RAM. If the current clock period is qualified for data collection, the incoming data from the Probe Input Buffer is latched into the Collection Input Buffer by the negative-going WE- pulse from the Clock Generator. The data is held stable at the outputs of the Collection Input Buffer for the duration of the WE- pulse.

(The two stabilizing buffers just discussed are necessary because of propagation delays and delays introduced by the Clock Generator to allow time for the qualification comparison. At high clock rates these delays may result in the next RAM address and the next probe data word arriving at the Memory Board before the current write to the Data Collection RAM has been completed.)

The Collection Output Buffer consists of U27, a 74LS244 octal buffer. It is used by the processor to read collected data from the Data Collection RAM for purposes of data analysis and display. The buffer's 8 input lines are connected in parallel to two sets of 8 output lines on the RAM. The buffer's 8 output lines are connected to the 8-bit Processor Data Bus. Multiplexing of the RAM's 16 output lines to the buffer's 8 input lines is accomplished by the Control Program with the aid of two RAM output enable signals, RAMHI- and RAMLO-, from the Address Decoder. The buffer's outputs to the bus are enabled by signal RBUFEN- (Read Buffer Enable -) from the Address Decoder.

9.2.2 Qualifier-Word RAM

The Qualifier-Word RAM consists of U4, U5, U12, U13, and U23, all 74S289 16-word x 4-bit static RAMs. These RAMs are connected as follows. The 16 data lines from the output of the Probe Input Buffer are divided into 4 sets of 4 lines. A set of 4 lines is fed to the 4 address inputs of each of the 4 RAMs, U12, U13, U5, and U4, starting with the 4 most significant bits fed to the 4 address inputs of U12. The 4 qualifier lines from the output of the Probe Input Buffer are fed to the 4 address lines of RAM U23.

For each of the 5 RAMs, the 16 possible combinations of the 4 bits on the address lines address the 16 word locations in the RAM. This means that any given combination of values of the 4 probe input bits in a set will address a unique word location in that set's RAM. Each word location contains 4 storage bits. Of these 4 bits, bit 0 is assigned to the ARM word, bit 1 is assigned to the CQ1 clock-qualifier word, bit 2 is assigned to the CQ2 clock-qualifier word, and bit 3 is assigned to the RESTART word.

> NOTE: The ARM word is only used in the 40-Channel State mode, in which it is the first of the two trigger words shown on the 8-Channel Timing/State menu. For further details, please refer to the discussion of the 40-Channel State mode in sub-section 1.2 of the Introduction.)

An example will serve to demonstrate how this arrangement allows the Qualifier-Word RAM to perform a comparison function. Assume that a menu for the 16-channel mode has specified, in binary format, the following first clock-qualifier word:

0110 001X XXXX XXXX -1XXX XX

At setup time, the Control Program places this menu word's 4 most significant bits, 0110, on the address inputs of RAM U12 through the Setup Data Buffer. Into the second bit position (the CQ1-word bit position) of the 4-bit word thus addressed, the Control Program then writes a 1 (through the DI1 input of the RAM and using write enable W3- from the Address Decoder). (It also writes into the other three bit positions for the ARM, CQ2, and RESTART words, but we are not concerned with those words at the moment.)

The 1 that is written into this 0110, bit-1 location means match. The Control Program writes a 0, for no match, into bit 1 of the other 15 words in RAM U12 because these other locations will be addressed by "no-match" bit combinations of the input data. Now, whenever the 4 MSBs of the incoming data are 0110, RAM U12 will output a 1 from DO1; for all other bit combinations, it will output a 0 from DO1.

For RAM U13, addressed by the next set of 4 bits, 001X, the Control Program writes a 1 into bit 1 of the words at addresses 0010 and 0011 (the LSB of this set is a "don't care" X) and a 0 into bit 1 of the remaining 14 words. For RAMs U5 and U4, the Control Program writes a 1 into bit 1 of all 16 words, since all 4 address bits are Xs. For RAM U23, addressed by the qualifier-bit group, 1XXX, the Control Program writes a 0 into bit 1 of the 8 word locations addressed by 0000 through 0111. And it writes a 1 into bit 1 of the 8 word locations addressed by 1000 through 1111.

Assume that at run time the following data word is clocked into the Probe Input Buffer by LATCHCLK and is placed, in 4-bit groups, on the address inputs of the 5 RAMs in the Qualifier-Word RAM.

	U12	U13	U5	U4	U23
data word	0110	0011	1010	0001	0000
menu word	0110	001X	XXXX	XXXX	1XXX

For RAM U12, output DO1 (from bit 1) of the word thus addressed is a 1 (match) because the Control Program loaded a 1 in bit 1 at address 0110. Similarly, output DO1 is a 1 for U13, U5, and U4, but a 0 (no match) for U23.

The 74S289 RAMs have open collector outputs; and all five DO1 outputs are tied together, have a pullup resistor in U3, and are fed to P2-19 as signal CQ1. This amounts to a wired AND for the 5 DO1 outputs. The DO0, DO2, and DO3 outputs are connected in a like manner. For the input data word in our example, signal CQ1 is low (logic 0) because the U23 DO1 output pulls the line low.

Now assume that a little later on, the following data word comes along:

	U12	U13	U5	U4	U23
data word	0110	0010	0000	1111	1100
menu word	0110	001X	XXXX	XXXX	1XXX

This word produces a 1 at the DO1 outputs of all 5 RAMs, and signal CQ1 goes high.

The Qualifier-Word RAM's four output signals, ARM, CQ1, CQ2, and RESTART, are fed to connector pins S2-20, 19, 18, and 17, respectively. Signals CQ1 and CQ2 are used by Clock Control on the State Control Board (ref. schematic sheet 3), and signal RESTART is used by the Restart Generator on the State Control board (ref. schematic sheet 3). The ARM signal at pin S2-20 is not used. However, ARM is also fed to U22A where it is translated to ECL level, inverted, and fed to pin S2-9 as signal SA- (State ARM -). This signal is used by the Arm Linker on the Timing Control Board when the analyzer is in the 40-Channel State mode. In fact, in the 40-Channel State mode, SA- is the only one of the Qualifier-Word RAM signals that is used because data-word clock qualification (CQ1 and CQ2) is not available in this mode and neither is RESTART. Furthermore, in the 40-Channel mode the EXT link is implemented in Timing Control and the FT link is not available (the Timing analyzer is acting as one of the State sections). Therefore, in the Qualifier-Word RAM's ARM word, the Control Program automatically treats both of these link bits as Xs.

9.2.3 Trigger-Word RAM

The Trigger-Word RAM consists of U19, U20, U21, U25, and U30, all of which are Signetics 82S117 256-word x 1-bit static RAMs. The 256 1-bit word locations in each RAM are addressed by 8 address inputs, A7—A0.

As with the Qualifier-Word RAM, the 16 data lines from the output of the Probe Input Buffer are divided into four sets of 4 lines. One set is fed to address inputs A3—A0 of each of the four RAMs, U21, U20, U30, and U19. The 4 qualifier lines from the output of the Probe Input Buffer are fed to address inputs A3—A0 of U25.

Address inputs A7—A4 of the five RAMs are connected to Trigger Stack Address lines TSA3—TSA0 from the State Control Board. These 4 address bits to each RAM decode into 16 blocks of 16 locations each, and each block represents one of the 16 trigger stack levels on the menu.

The Trigger-Word RAM performs the comparison function in much the same way as the Qualifier-Word RAM, but with a difference in the bit organization. First, assume we are at level 0 of the trigger stack. As before, the incoming 20-bit data word is divided into five 4-bit groups, and each group feeds 4 address inputs of one of the five RAMs. These 4 address bits address 16 locations, and, just as in the Qualifier-Word RAM, each location represents one of the 16 possible combinations of 1s and 0s for the 4 input data bits.

Just as with the Qualifier-Word RAM, each location is loaded at setup time with a 1 or a 0, for "match" or "no match", according to the bit configuration of the menu-specified trigger word at stack-level 0. And as before, the five RAM outputs are connected in a wired AND so there must be a "match" for all five 4-bit groups of the incoming data word to produce a TRUE output from the Trigger-Word RAM.

In the Qualifier-Word RAM, the four search words (ARM, CQ1, CQ2, and RESTART) all have to be compared with the incoming data word simultaneously. Each search word is therefore assigned a bit in the RAM output word. But in the Trigger-Word RAM, the sixteen search words (the menu-specified trigger words at stack levels 0—15) do not have to be compared simultaneously. In fact, only the trigger word at the current trigger stack level has to be compared. Each of the 16 search words is therefore assigned a block of 1-bit RAM words, and the proper block is selected by the 4-bit Trigger Stack Address fed to the A7—A4 inputs of each RAM.

As the Trigger Stack Address at each RAM's A7—A4 inputs advances to the next higher stack level, the comparison activity of the 4 input data bits at the RAM's A3—A0 inputs is shifted to the next higher block of 16 stored bits (one bit for each of the 16 possible combinations of the 4 input data bits). At any given stack level, the five RAMs look exactly like a Qualifier-Word RAM having only one qualifier word, say CQ1.

The 82S117 RAMs have open collector outputs, and all five single-bit outputs are connected together in a wired AND to produce the output signal TRIG+ (Trigger +) at connector pin S2-16. This TRIG+ signal is used by Stack Management on the State Control Board. (The pullup resistor for the wired AND is on the State Control Board). The RAM output is also fed to U22B where is is translated to ECL level, inverted, and fed to pin S2-10 as signal ST- (State Trigger -). This ST- signal is used by the Trigger Linker on the Timing Control Board when the analyzer is in the 40-Channel State mode. Also, in the 40-Channel mode the EXT link is implemented in Timing Control and the FT link is not available (the Timing analyzer is acting as one of the State

sections). Therefore, for the trigger word at each level in the Trigger-Word RAM, the Control Program automatically treats both of these link bits as Xs.

9.2.4 Clock Generator

The Clock Generator consists of: U31 and U35, both 50ns delay lines with selectable delay outputs; U32A,B,C,D,E, sections of a 74S04 hex inverter; U33, a 74S02 quad NOR gate (section B is here used as a negative input AND gate); and U34A, 1/2 of a 74S74 dual D flip-flop. Upon receipt of a low CLKQUALIN- signal from State Control (which signifies that the current input data word is approved for data collection), this circuitry produces the delayed data collection clock WE- (Write Enable -). It also produces WE+ (an inverted WE-) and DLYWE- (a WE- clock with additional delay), both used by State Control.

The menu-selected primary external clock, LATCHCLK, which is fed from State Control to clock the Probe Input Buffer, is also fed through U32E to the delay line U31. After a delay of about 40 ns, the clock is fed from the delay line through U32D to the clock input of flip-flop U34A. If the output of U33B has been brought high by a low CLKQUALIN- at the input, the flip-flop is set by the delayed clock. The flip-flop is reset, after about 40ns delay, by the feedback chain through delay line U35. The resulting 40ns pulses from the Q and Q- outputs of the flip-flop are fed to inverters U33C and D and supplied as clock signals WE- and WE+. The flip-flop's Q output is further delayed in U35 and supplied through inverter U32A as clock signal DLYWE- (Delayed Write Enable -).

Generation of all three clock outputs is stopped when flip-flop U34A is held reset by a high CLKINH+ signal at the input of U33A. This condition obtains when data collection has been completed or when the FORCE DISPLAY keyboard key is depressed.

9.2.5 Address Decoder

The Address Decoder consists of: U1 and U29, 74LS138 3-to-8 decoders; U2, a Monolithic Memories 6330-1 32-word x 8-bit PROM; and U32F, one section of a 74S04 hex inverter. This circuitry provides the processor with I/O port addressing of certain I/O buffers, with read addressing of the Data Collection RAM, and with write addressing of the Qualifier-Word RAM and Trigger-Word RAM.

The U1 decoder and the U2 PROM use Processor Address Bus bits A7—A15 and processor control signal RW (Read/Write) to generate the following enable signals:

RAMHI- (RAM High -, decoded from RW .AND. address HHHh), which enables the outputs of data collection RAMs U7 and U8 for a processor read of collected data

RAMLO- (RAM Low -, decoded from RW .AND. address HHHh), which enables the outputs of data collection RAMs U9 and U18 for a processor read of collected data

RBUFEN- (Read-Buffer Enable -, decoded from RW .AND. address HHHh), which enables the outputs of the Collection Output Buffer for a processor read of collected data from the Data Collection RAM

RDSTKADD- (Read Stack Address -, decoded from RW .AND. address HHHh), which enables the outputs of the Read TSA Buffer for a processor read of the trigger stack address signals from State Control

DATEN- (Data Enable -, decoded from RW .AND. address HHHh), which enables the outputs of the Probe Input Buffer for a transfer of probe input data to the Qualifier-Word RAM, Trigger-Word RAM, and Collection Input Buffer

SDBUFEN- (Setup Data Buffer Enable -, decoded from RW .AND. address HHHh), which enables the outputs of the Setup Data Buffer for processor addressing of the Qualifier-Word RAM and Trigger-Word RAM

The U29 decoder is enabled by signal SDBUFEN- from the U2 PROM. When thus enabled, it uses processor control signal WR- and bits A4—A6 from the Processor Address Bus to generate the following signals:

W0-—W4- (Write 0—4, decoded from WR- .AND. addresses HHHh—HHHh), which enable processor writes to the 5 RAMs in the Qualifier-Word RAM

W5- (Write 5 -, decoded from WR- .AND. address HHHh), which enables processor writes to all sections of the Trigger-Word RAM

W6- and W7- (Write 6 -, 7 -, decoded from WR- .AND. address HHHh), which enable the outputs of the two sections of the Probe Output Buffer for processor writes to the probe pod

9.2.6 Data Collection RAM

The Data Collection RAM consists of U7, U8, U9, and U18, all Fairchild 93422 (or equivalent) 256-word x 4-bit static RAMs. The 8 address lines of the 4 RAMs are connected in parallel to the outputs of the 8-bit Collection Address Buffer. The 4 data-in lines of the 4 RAMs are connected in cascade (with U8 at the high order end) to the 16 output lines of the Collection Input Buffer.

The write-enable inputs of the 4 RAMs are connected in parallel to signal WE- from the Clock Generator. Therefore, in the write (or data collection) mode, the 4 RAMs act as a single 256-word x 16-bit RAM. Incoming 16-bit data words from the Collection Input Buffer are written into the Data Collection RAM by WE- write pulses from the Clock Generator. Sequential addresses are supplied through the Collection Address Buffer from the Collection Address Counter on the State Control Board.

However, the arrangement is different for the read mode. The output-enable inputs of U8 and U7 are tied together and connected to signal RAMHI- from the Address Decoder, and the output-enable inputs of U18 and U9 are tied together and connected to signal RAMLO- from the Address Decoder. The 4 data-out lines of U8 and of U7 are connected in cascade to the 8 inputs of the

Collection Output Buffer. The 4 data-out lines of U18 and of U9 are similarly cascaded and connected in parallel with the U8-U7 set.

In the post-collection read mode, the Control Program multiplexes the 16-bit data word into the 8-bit Collection Output Buffer by placing the word address on the RAM address inputs twice; once with the RAMHI- output-enable signal active, and once with the RAMLO- output-enable signal active. In both instances buffer-enable signal RBUFEN- is active. As they arrive in main memory, the two 8-bit sections of the data word are combined by the Control Program into the 16-bit data word.

9.3 BOARD A VERSUS BOARD B

Now that we have examined the operation of an individual State Memory Board, we are in a position to take up the differences in function between a board plugged into the A slot and a board plugged into the B slot.

9.3.1 Qualifier Bits

First, there is the matter of the two qualifier lines coming from each of the two probe pods. Those coming from Pod A connect to Board A, and those coming from Pod B connect to Board B. The EXT qualifier and the Timing link connect to both Board A and Board B. These 4 qualifier lines connect to each board at the inputs to U26A in the Probe Input Buffer, and they carry signal identifications Q1, Q2, EXT, and FT.

On the menu, the qualifier bits show at the end of a clock-qualifier word line or a trigger word line as:

```
-XXXX XX
```

The formatting is shown on the menu Clock Select line as:

```
QUALIFIERS: -AABB ET
```

With the additional identification of our signal names, the menu formatting would be:

```
QUALIFIERS: -AQ1,AQ2,BQ1,BQ2  EXT,FT
```

At the inputs to the Probe Input Buffer, and therefore also at the address inputs to the Qualifier-Word and Trigger-Word RAMs, the signals are:

```
AQ2,AQ1,FT,EXT      (for Board A)
BQ2,BQ1,FT,EXT      (for Board B)
```

The input qualifier lines, Q1 and Q2, must not be confused with the outputs of the Qualifier-Word RAM, CQ1 and CQ2! For either the A or B Board,

the CQ1 output represents the result of the comparison of an entire input data word with the entire menu-specified first clock-qualifier word, including both the Q1 and Q2 bits. Similarly, the CQ2 output represents the result of the comparison of an entire input data word with the entire menu-specified second clock-qualifier word, including both the Q1 and Q2 bits.

9.3.2 Signal CLKQUALIN

CLKQUALIN- (Clock Qualifier In -) is the signal that enables the Clock Generator and thereby turns on the WE- (Write Enable -) pulse for the State Memory Board and the WE+ and DLYWE- clock pulses for the State Control Board. Signal WE- is, of course, the pulse that causes the current 16-bit input data word to be stored in the Data Collection RAM.

Recall that ACLKQUALIN (the CLKQUALIN- signal to State Memory Board A) is hard-wired to a constant low (true) level (refer to the Clk Qual Gate at the top of sheet 3 on the State Control Board schematic). This means that the State Memory Board plugged into the A socket will collect a 16-bit data word at every LATCHCLK, no matter what the outcome of the clock-qualifier comparison. However, the BWE+ and BDLYWE- clocks that drive State Control (in particular, the Collection Address Counter, which feeds both Memory Boards) come from Board B. And these clocks are not generated unless BCLKQUALIN- is low. Further, from the logic of the Clk Qual Gate, BCLKQUALIN- is not low unless ACQ1 .AND. BCQ1 are high (true) .OR. ACQ2 .AND. BCQ2 are high. (ACQ1 is CQ1, the first clock-qualifier word signal, from Board A, etc.)

This means that the data words collected by Board A are written one on top of the other into the same address in the Data Collection RAM until the clock qualification requirements set up in the Qualifier-Word RAM on both Board A and Board B are met. At that point, BCLKQUALIN- causes BWE- to be generated so that the B data word is collected as well as the A data word. BWE+ and BDLYWE- are also generated so that the data collection address is advanced. The next A data word (qualified or not) goes into the new address, thus preserving the qualified A data word in the previous address.

9.3.3 Signal CLKINH

The Clock Generator on the State Memory Board can be inhibited from producing the WE family of clocks by signal CLKINH+ (Clock Inhibit +) from State Control. State Control generates two such signals; ACLKINH+ for Board A, and BCLKINH+ for Board B.

When the analyzer is in the 32-channel x 250-word mode, Board A and Board B finish collecting at the same time, stopped by concurrent signals ACLKINH+ and BCLKINH+ from State Control. When processing the collected data, the Control Program reads 16-bit words from equivalent addresses in Board A and Board B and lays them side by side in main memory as one 32-bit word.

When the analyzer is in the 16-channel x 500-word mode, the inputs to Board A and Board B are connected in parallel. The two boards are collecting identical data up until the time that data collection on Board A is stopped by ACLKINH+ at the menu-specified posttrigger count less 250. Board B continues

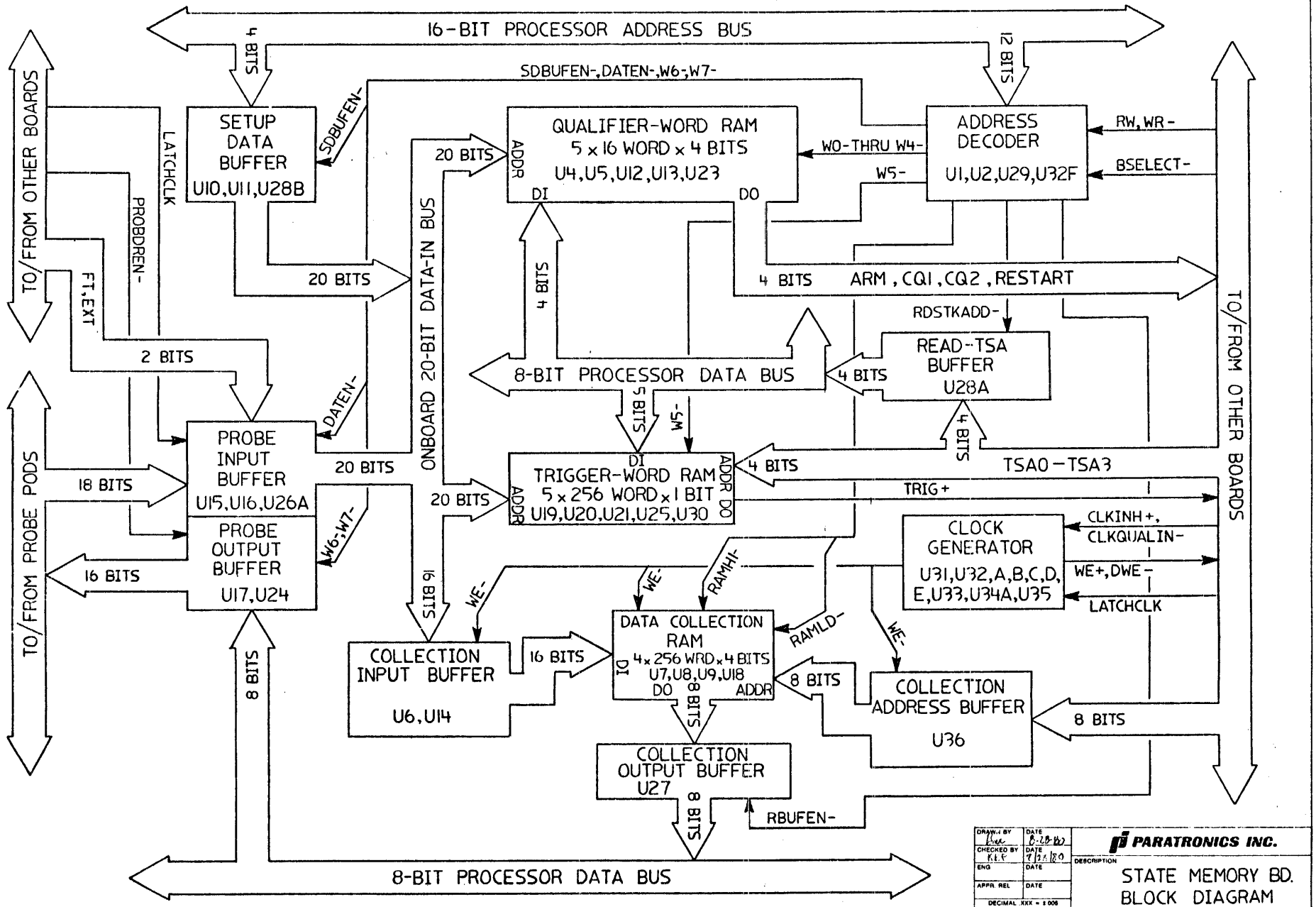
to collect for 250 more words and then is stopped by BCLKINH+. (Recall that the user is constrained to allocate at least 250 words, the full Board B memory capacity, to posttrigger data.)

9.3.4 Signal BSELECT-

The Control Program must be able to read from one State Memory Board at a time. It must also be able to write setup data into the Qualifier-Word RAM and Trigger-Word RAM one board at a time. This facility is provided by signal BSELECT-, which is fed from connector pin S2-15 to Address Decoder pin U2-14, with a pullup resistor at U3-11. Connector pin S2-15 is hard-wired low at the B socket but left open (to be pulled high) at the A socket. The Address Decoder responds to Board B addresses when the signal is low, and to Board A addresses when the signal is high.

9.4 SCHEMATIC, BOARD LAYOUT, & PARTS LIST

The schematic diagram, board layout, and parts list for the State Memory Board are contained on the following pages.



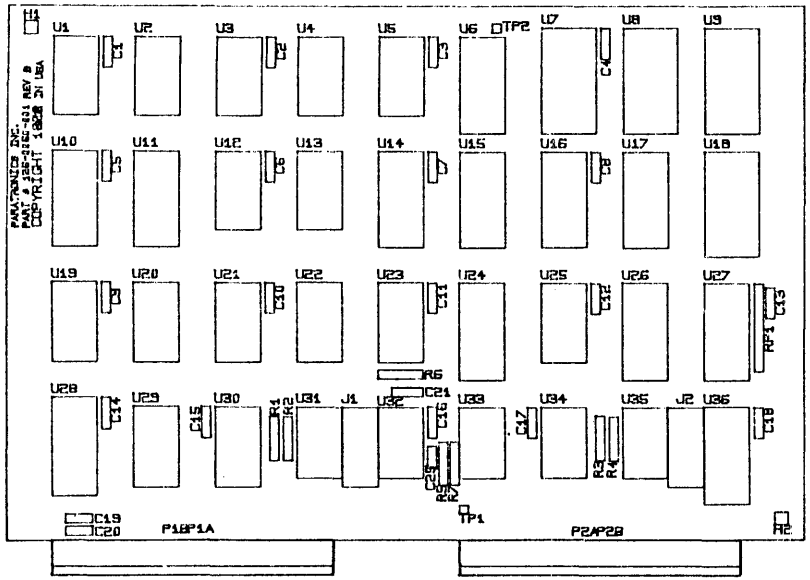
DRAWN BY / DATE	B-28-80
CHECKED BY / DATE	9/25/80
ENG / DATE	
APPR. REL / DATE	
DECIMAL XXX = ± 005, XX = ± 02	
FRACTIONAL ± 1/64	
ANGULAR ± 0°30'	
BREAK ALL SHARP EDGES	
DO NOT SCALE DRAWING	

PARATRONICS INC.

DESCRIPTION: STATE MEMORY BD. BLOCK DIAGRAM

C | DRAWING NO 145-0060-001 | SCALE | SHT | OF | REV.

REV	DESCRIPTION	DATE	APPROVED



DRAWN BY GS	DATE	PARATRONICS INC.	
CHECKED BY	DATE	DESCRIPTION	LEGEND MASTER
ENG	DATE		540 STATE MEMORY
APPR REL	DATE		
DECIMAL XXX = ±.005 XX = ±.02 FRACTIONAL ± 1/64 ANGULAR ± 0°30'		DRAWING NO.	126-0060-201 B
BREAK ALL SHARP EDGES		SCALE ——	SHT 1 OF 1 REV.
DO NOT SCALE DRAWING			

REV	DESCRIPTION	DATE	APPROVED
C	REV PER ECO 103		
D	REV PER ECO 155	4/26/84	

DATA COLLECTION RAM

PROBE OUTPUT BUFFER

U24, 74LS374

U17, 74LS374

U36, 74LS374 COLLECTION ADDRESS BUFFER

INPUT/OUTPUT BUFFERS (PART 1 OF 2)

INPUT OUTPUT BUFFERS PART 2 OF 2

U8 93 412 / 93 422

U17 93412 / 93422

U18 93412 / 93422

U9 93412 / 93422

RAMLO

RAMHI

COLLECTION OUTPUT BUFFER

U27, 74LS244

ADDRESS DECODER U1 74LS138

LOCK GENERATOR

U35 SOnS D.L.

U31 SONS D.L.

U34A S74

U32A 74SO4

U32B 74SO4

U32C 74SO2

U32F 74SO4

U33D 74SO2

U33C 74SO2

U33A 74SO2

U32E 74SO4

U16, 74LS374

U15, 74LS374

U26 74S374

U14, 74S373 COLLECTION U16, 74S373 INPUT BUFFER

U11, 74LS244 SET-UP DATA BUFFER

U10, 74LS244

U28, 74LS244 READ TSA BUFFER

U29, 74LS138

PROBE OR SET UP DATA BITS

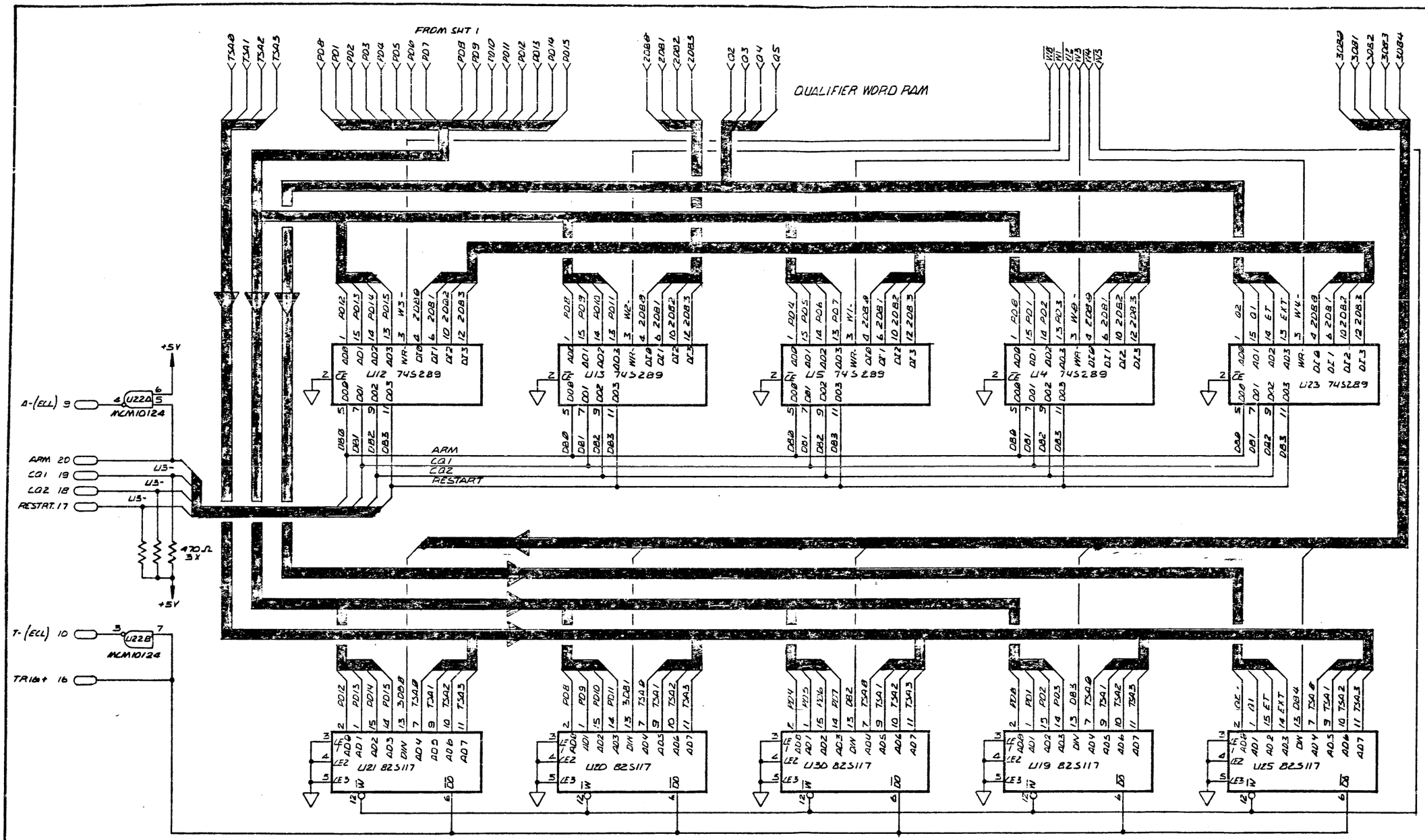
PROBE OR SET-UP QUAL BITS

TRIGGER STACK ADDRESS

QUALIFIER SET-UP MATCH/NO MATCH BITS

TRIGGER SET-UP MATCH/NO MATCH BITS.

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DRAWN	SD	PARATRONICS INC.
MAT'L	CK		SCHEMATIC DIAGRAM 540 STATE MEMORY
FINISH	APPR		
	BREAK ALL SHARP EDGES		DRWG NO 127 0060-001 REV D
	DECIMAL ANGULAR		D SCALE SHT 1 OF 2
	DO NOT SCALE DRAWING		



IC. TYPE	"U" NO PEF	+5V	-5V	GND
7402	33	14	—	8
7404	32	14	—	8
74S288	4,5,12,13,23		—	
74S373	6,14	20	—	10
74S374	11,24	20	—	10
7474	34	14	—	7
74LS138	1,23	16	—	8
74LS244	10,11,21,23	20	—	10
74LS373	36	20	—	10
74LS374	17,24	20	—	10
93412/22	7,8,9,12		—	
10124	22			
6330-1	2	16	—	8

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES

MAT'L

FINISH

CK 8/26/80

APPR

BREAK ALL SHARP EDGES

DECIMAL ANGULAR

XX = ± 1

XXX = ± 2

DO NOT SCALE DRAWING

PARATRONICS INC.

SCHEMATIC DIAGRAM 540 STATE MEMORY

DRWG NO 127-0060-001 REV. D

SCALE

SHT 2 OF 2

SINGLE LEVEL EXPLOSION

09/04/80

PAR143-0060-0090-00 DESCRIPTION : STATE MEMORY PCB ASSY-OUTSIDEECO#: 151 REV.CU.: D

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
111-0207-0103-00	D	22 UF 16V CAP. ELECTRO.,RAD.	2	1	0	08/21/80	OPEN	0	C19 C20
110-0005-0051-00	D	330 OHM 1/4W 5% CF RES	2	1	0	01/08/80	OPEN	0	R5 R6
110-0005-0063-00	D	1K OHM 1/4W 5% CF RES	1	1	0	01/08/80	OPEN	0	R7
111-0012-0030-00	D	100 PF 1KV CAP. CD	1	1	0	01/08/80	OPEN	0	C25
110-0300-0001-00	D	RES. NETWORK,STKPOLE S10-9-1	1	1	0	OPEN	OPEN	0	RP1
113-0046-0001-00	D	21185 DELAY LINE	2	1	0	OPEN	OPEN	0	U31 U35
110-0005-0045-00	D	180 OHM 1/4W 5% CF RES	2	1	0	OPEN	OPEN	0	R1 R3
110-0005-0047-00	D	220 OHM 1/4W 5% CF RES	2	1	0	OPEN	OPEN	0	R2 R4
110-0304-0001-00	D	470 OHM RES. NETWORK	1	1	0	OPEN	OPEN	0	U3
111-0004-0072-00	D	.1 UF 25V CAP. CD	18	1	0	OPEN	OPEN	0	C1 C10 C11 C12 C13 C14 C15 C16 C17 C18 C2 C3 C4 C5 C6 C7 C8 C9
115-0003-0001-00	D	SOCKET,14PIN	3	1	0	OPEN	OPEN	0	U32 U33 U34
115-0005-0001-00	D	SOCKET,16PIN	14	1	0	OPEN	OPEN	0	U1 U12 U13 U19 U2 U20 U21 U22 U23 U25 U29 U30 U4 U5
115-0009-0001-00	D	SOCKET,20PIN	12	1	0	OPEN	OPEN	0	U10 U11 U14 U15 U16 U17 U24 U26 U27 U28 U36 U6
115-0010-0001-00	D	SOCKET,22PIN	4	1	0	OPEN	OPEN	0	U18 U7 U8 U9
117-0030-0001-00	D	TERMINAL, 120-1032-04, CAMBION	2	1	0	OPEN	OPEN	0	TP1 TP2
126-0060-0001-00	D	STATE MEMORY PC FAB	1	1	0	OPEN	OPEN	0	

LEGEND UM : 01=EACH 02=INCH 03=FEET 04=BULK 05=AS REQUIRED 06=OTHER
LEGEND KEY: A=W/PARTS LIST D=W/O PARTS LIST R=REFERENCE DOCUMENT S=SPECIFICATION

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SINGLE LEVEL EXPLOSION

09/04/80

PAR143-0060-0001-00 DESCRIPTION : STATE MEMORY PC ASSY ECO#: 151 REV.CU.: D

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
113-0002-0002-00	D	I.C., 74S02	1	1	0	OPEN	OPEN	0	U33
113-0053-0001-00	D	27S02, 74S289	5	1	0	OPEN	OPEN	0	U12
U13 U23 U4 U5									
113-0002-0004-00	D	I.C., 74S04	1	1	0	OPEN	OPEN	0	U32
113-0002-0074-00	D	I.C., 74S74	1	1	0	OPEN	OPEN	0	U34
113-0002-0373-00	D	I.C., N74S373N	1	1	0	04/28/80	OPEN	0	U36
113-0002-0374-00	D	I.C., 74S374	5	1	0	04/28/80	OPEN	0	U14
U15 U16 U26 U6									
113-0003-0138-00	D	I.C., 74LS138	2	1	0	OPEN	OPEN	0	U1
U29									
113-0003-0244-00	D	I.C., 74LS244	4	1	0	OPEN	OPEN	0	U10
U11 U27 U28									
113-0003-0374-00	D	I.C., 74LS374	2	1	0	OPEN	OPEN	0	U17
U24									
113-0200-0124-00	D	I.C., MC10124	1	1	0	OPEN	OPEN	0	U22
113-0010-0003-00	D	6330-1 PROM	1	1	0	OPEN	OPEN	0	U2
113-0017-0002-00	D	I.C., 93L422, 93422, 93412	4	1	0	OPEN	OPEN	0	U18
U7 U8 U9									
113-0045-0001-00	D	82S117, AM27LS01C, 93411 IC	5	1	0	OPEN	OPEN	0	U19
U20 U21 U25 U30									
143-0060-0090-00	D	STATE MEMORY PCB ASSY-OUTSIDE	1	1	1	OPEN	OPEN	151	

LEGEND UM : 01=EACH 02=INCH 03=FEET 04=BULK 05=AS REQUIRED 06=OTHER
LEGEND KEY: A=W/PARTS LIST D=W/O PARTS LIST R=REFERENCE DOCUMENT S=SPECIFICATION

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10.0 TIMING CONTROL BOARD

10.0 TIMING CONTROL BOARD

10.1 INTRODUCTION

Hardware registers, counters, and RAMs on the Timing Control Board are loaded by the Control Program in accordance with information entered from the keyboad under the guidance of the timing menu. Using the parameters and modes thus specified, the Timing Control Board directs the collection of timing data in the Timing Memory.

10.2 FUNCTIONAL DESCRIPTION

A block diagram of the Timing Control Board is shown in figure 10-1. When appropriate during the following discussion, please refer to this figure and to the schematic diagram, board layout, and parts list which are included at the end of this section. Also, tables of connector pins versus signal names for all motherboard connectors are provided in section 15 along with an alphabetical list of all interboard signals. And, should the need arise, a Glossary in section 16 offers explanations of acronyms or terms that may be unfamiliar.

As shown in the block diagram, the major functional units of the Timing Control Board circuitry are the Processor Interface, the Clock Generator, Clock Control, Trigger Control, Arm Control, Sequencer, and the Posttrigger and Delay Counters. These units are discussed in detail in the following subsections.

10.2.1 Processor Interface

The Processor Interface (see schematic sheet 4) comprises the Address Decoder, the Master Control Register, the Control Shift Register, and the Status Port. This circuitry allows the processor to load registers, counters, and RAMs on the Timing Control Board with user-supplied information in order to prepare the Timing Analyzer for the intended application. Also, this circuitry allows the processor to interrogate various status and signal lines and to send various control signals when appropriate.

The Address Decoder consists of U50, a 74LS138 3-to-8 decoder. This circuit allows the processor to clock the Master Control Register (with signal MCRCLK), to address the Status Port (with signal RDSTAT-), to send write enable signal WRRAM- to the Sequencer RAM, and to send reset signal RESET- to the Sequencer Latch.

The Master Control Register consists of U49, a 74LS374 octal D flip-flop, and Q1 and Q2, both 2N3905 transistors. U49 latches control signals from the Processor Data Bus when clocked by MCRCLK from the Address Decoder. These signals include: SRCLK, the clock for the Control Shift Register; SRDATA, serial data for the Control Shift Register; and SWCLKINH, a software-generated clock-inhibit signal that allows the Control Program to stop all clocks from Clock Control when appropriate. The remaining signals from the Master Control Register are high-speed control signals to the Clock Generator that cannot be handled by the slower Control Shift Register. (Also, when the Control Shift

Register is not being loaded, the shift register data line, U49-5, doubles as a clock-select signal line to the Clock Generator.) The two transistors, Q1 and Q2, shift the signal levels from TTL to CMOS on the two lines that feed the Control Shift Register (which is made up of CMOS devices).

The Control Shift Register consists of 8 CMOS 4015 dual 4-bit static shift registers, U26 through U33. These registers supply 63 software generated control signals to other circuits on the Timing Control Board. The registers are loaded in series through the SRDATA line from the Master Control Register, and their 63 parallel outputs are supplied at ECL-compatible levels. (This scheme saves the circuit board space that would have been required for 62 parallel input lines and 62 level-shifting transistor circuits.)

The Status Port consists of U48, a 74LS373 octal D latch, and U53A,D, sections of a quad ECL-to-TTL translator. The U48 latch acts as an input port that allows the processor to read the status of certain critical signals when appropriate. U53A and D translate the levels of two ECL signal lines feeding the TTL latch.

10.2.2 Clock Generator

The Clock Generator (schematic sheet 6) comprises the Clock Oscillator, the First Stage Divider, the First Stage Selector, the Second Stage Divider, and the Second Stage Selector. This circuitry generates internal clock pulses in the full complement of available discrete clock periods, from 20 ns through 10 ms. It also provides the means for the Control Program to select the keyboard-specified clock period from this complement.

The Clock Oscillator consists of: U10D, a section of a 10102 quad NOR gate; discrete components Y1, L1, C1, R1, and R2; U9, a 10138 biquinary counter; and U53C, a section of a 10125 ECL-to-TTL translator. U10D and its associated discrete components form an oscillator with a 100-MHz output. This 100-MHz signal is fed to both clock inputs of counter U9 which produces a 50-MHz signal at pin 15 and a 20-MHz signal at pin 4. The 50-MHz (20-ns) signal, the fastest clock in the complement, is fed directly to Clock Control (on schematic sheet 8) as signal INT50 (Internal 50 MHz). The 20-MHz (50-ns) signal is translated to TTL level by U53C and fed to the First Stage Divider for further processing. It is also fed directly to the Second Stage Selector for possible selection by the Control Program.

The tuning slug in inductor L1 is adjusted for a signal frequency, as measured at pin U9-15, of 50 MHz $\pm$ 0.005%.

The First Stage Divider consists of: U1, a 74LS74 dual D flip-flop; and U8, a 74LS90 biquinary counter. By successively dividing the 50-ns input signal, this circuitry produces signals with periods of 100 ns (at U1-5), 200 ns (at U1-9), 500 ns (at U8-8), and 1000 ns (at U8-12). These signals are fed to the First Stage Selector.

The First Stage Selector consists of U2, a 74LS151 1-of-8 data selector. This circuit uses 2 software-generated clock-select signals (CLKSELD and CLKSELE from the Procesor Interface) to select the pin 6 output from one of the 4 inputs coming from the First Stage Divider. The selected output is fed

to the Second Stage Divider for further processing. It is also fed directly to the Second Stage Selector for possible selection by the Control Program.

The Second Stage Divider consists of 4 74LS90 biquinary counters, U4, U5, U6, and U7. Each of these counters is connected to divide by 10. The four-divider chain provides four output clock signals with periods equal to the input period multiplied by 10 (at U4-12), 100 (at U5-12), 1000 (at U6-12), and 10,000 (at U7-12). (For example, with 100 ns selected as the input, the output signals would have periods of 1 us, 10 us, 100 us, and 1 ms.) The four output lines are fed to the Second Stage Selector.

The Second Stage Selector consists of U3, a 74LS151 1-of-8 data selector, and U55B, a section of a 10124 quad TTL-to-ECL translator. The U3 selector has a software-generated pseudo clock (PSEUDOCLK) on input pin 12; the 50-ns clock on input pin 14; the output of the First Stage Selector on input pin 15; and the outputs of the Second Stage Divider on input pins 1, 2, 3, and 4. The Processor Interface feeds the U3 select inputs (pins 9, 10, and 11) with the software-generated clock-select signals CLKSELA, CLKSELB, and CLKSELC.

By manipulating these three select signals and the two select signals CLKSELD and CLKSELE to the First Stage Selector, the Control Program can select either the pseudo clock or any one of 17 internal clocks whose periods range from 50 ns through 10 ms in cascading 1-2-5 ratios. (The 20-ns highest-speed clock is selectable in Clock Control.) The selected clock output from pin 6 is fed through the U55B translator to Clock Control as ECL-level signal INT<50 (Internal Less Than 50 MHz).

10.2.3 Clock Control

Clock Control (see schematic sheet 8) is made up of Qualifier Control, the Final Clock Selector, and Clock Delay. This circuitry implements (under the direction of the Control Program) the following keyboard-entered clock choices:

a. The choice of internal or external clock

b. If internal, the choice of a 50-MHz or less-than-50-MHz clock (the particular specified value of the less-than-50-MHz clock having been preselected in the Clock Generator)

c. If external, the choice of the positive- or negative-going edge

d. If external, the choice of 0, 1, or X for clock-qualifier polarity

Internal to the Timing Analyzer, data is always clocked with a positive-going clock edge. Therefore, if the keyboard-entered choice is for an external negative-going clock edge, that negative-going edge must be converted to a positive-going edge for the working clock used within the analyzer. This conversion, if required, is performed by Clock Control. Also, using clock inhibit signals from the Posttrigger Counter, Clock Control shuts off all Timing Analyzer working clocks at posttrigger terminal count.

Qualifier Control consists of: U10A,B,C, sections of a 10102 quad NOR gate (however, section C has an OR output, and sections A and B are used here as negative-input AND gates); and U47, a 10130 dual latch. The clock qualifier signal, QCLK+ from the Model 80 Probe, is connected to one input of gate U10A; and the inverted clock qualifier signal, QCLK- from the Model 80 Probe, is connected to one input of gate U10B. Gates U10A and U10B are enabled by the software-generated control signals SWQCLK0- (Software Clock Qualifier 0 -) and SWQCLK1-, respectively.

The use of these two signals is based on the keyboard-entered choice of 0, 1, or X for clock qualifier polarity.

a. If the choice was 0, the Control Program brings SWQCLK0- low, and a low level of QCLK+ will produce a high (TRUE) qualifier signal, QUAL, at U10C-14

b. If the choice was 1, the Control Program brings SWQCLK1- low, and a low level of QCLK- (which corresponds to a high level of QCLK+) will produce a high QUAL signal at U10C-14

c. If the choice was X, the Control Program brings both SWQCLK0- and SWQCLK1- LOW, and either level of QCLK+ will produce a high QUAL

This QUAL signal is fed to the D inputs of latches U47A and U47B. The latch's common clock input (pin 9) is left unconnected so that it is pulled low internally. This allows the latches to be clocked separately at the clock-enable inputs, pins 6 and 11. The two polarities of the external clock signal, CLK+ and CLK- from the Model 80 Probe, are fed to these two pins, with CLK+ going to pin 6 and CLK- going to pin 11. The latches are transparent while these clock inputs are low, but latch on the positive-going clock transition. The Q- output of U47A, which is clocked by the leading edge of CLK+, is used to enable gate U35A, which is the control gate for the working clock that represents an external positive-going clock edge. The Q- output of U47B, which is clocked by the trailing edge of CLK-, is used to enable gate U35B, which is the control gate for the working clock that represents an external negative-going clock edge.

If signal QUAL is high at the time of the positive-going clock edge at the CE- input of either or both latches, a clock-enabling low level is fed (for the duration of the clock period) from the Q- output of the set latch(s) to the corresponding U35 gate. These enabling levels from the two latches establish that the corresponding clock edge meets the qualifier conditions and may be further selected by the Final Clock Selector.

The Final Clock Selector consists of U34 and U35, both 10211 dual 3-input, 3-output NOR gates (used here as negative-input AND gates). By means of enabling signals, the Control Program uses these gates to select the data clock for the Timing Analyzer in accordance with keyboard-entered choices. The following choices are implemented:

a. The choice of external or internal clock—the external clock is handled by gates U35A (for CLK-) and U35B (for CLK+); the internal clock is handled by gates U34A (for INT50) and U34B (for INT<50)

b. The choice of the positive- or negative-going edge if the clock is external—this choice is implemented by software-generated signals SWPE- (Software Positive Edge -) and SWNE- at gates U35A and U35B, respectively

NOTE: As mentioned earlier, the Timing Analyzer always uses the positive-going edge of the working clock. Therefore, a keyboard-selected negative-going edge must be converted to an equivalent positive-going edge. This conversion is made in gate U35B. Because these 10211 AND gates have negative inputs, the U35B gate is enabled by SWNE- and fed by CLK+ whose trailing edge is negative going, thereby producing a working clock with the desired positive-going trailing edge. Similarly, the U35A gate is enabled by SWPE- and fed by CLK- whose leading edge is negative going, thereby producing a working clock with the desired positive-going leading edge.

c. The choice of a 50-MHz or less-than-50-MHz clock frequency if the clock is internal (the particular specified value of the less-than-50-MHz clock having been preselected in the Clock Generator)—this choice is implemented by software-generated signals SW50- (Software 50 MHz -) and SW<50- at gates U34A and U34B, respectively

By means of clock-inhibit signals CLKINHA+, CLKINHB+, and CLKINHC+ from the Posttrigger Counter, the U34 and U35 gates also implement clock shutoff at the end of posttrigger data collection. CLKINHA+ to U35A and CLKINHB+ to U35B are wire OR'd with the respective clock qualifier signals from the Qualifier Control latches, and CLKINHC+ is fed to both U34A and U34B. At posttrigger terminal count, all three clock inhibit signals go high simultaneously, thus the working clock is shut off no matter which of the four gates is active.

A wired OR consisting of one output from each of the four gates in the Final Clock Selector produces the final working clock, which is fed to the Clock Delay circuit. (Within the logic of the Control Program, the four selecting signals are mutually exclusive. Therefore, only one of the four gates is enabled at any given time. If either SW50- or SW<50- is low, both SWPE- and SWNE- are held high. Or, if either SWPE- or SWNE- is low, both SW50- and SW<50- are held high.)

An identical clock from a separate wired-OR set of the gate outputs is fed to connector pin S2-6 as signal CT (Clock, Timing). This signal is one of the two clocks sent to the Timing Memory Board (CLKTTL, to be discussed in a momet, is the other). CT is also the clock for the Waveform Control Board. (CT is fed to the Clock Conditioning circuit shown on sheet 5 of the Waveform Control Board schematic.) Also, when the PI 540 is in the 40-bit State mode, the CT clock is used as the selected clock by the State Control Board. (CT is fed to the Clock Control circuit shown on State Control schematic sheet 2.)

The Clock Delay circuit consists of: U23, a delay line; U53B, a section of a 10125 quad ECL-to-TTL translator; and U56D, a section of a 10101 quad OR/NOR gate (used here as a buffer/driver). This circuitry produces the following two working clocks:

a. CLKECL, an ECL-level clock that is identical to the CT clock except for being delayed from it by about 2.5 ns

b. CLKTTL, a TTL-level clock that is identical to the CT clock except for being delayed from it by about 15 ns

CLKECL is used throughout the Timing Control Board. CLKTTL is used by the Timing Memory Board. (CLKTTL is fed to the Clock Generator shown on sheet 1 of the Timing Memory Board schematic.)

10.2.4 Trigger Control

Trigger Control (see schematic sheet 3) comprises the Trigger Linker and the Trigger Filter. This circuitry allows the Control Program to set up any keyboard-specified trigger linkages with State, Waveform, or External trigger signals. It also implements the keyboard-selected degree of trigger filtering. (Trigger filtering is the requirement that the trigger signal be TRUE longer than a specified number of clock periods in order to be considered valid). In addition, when the 40-bit State mode has been selected, this circuitry allows the Control Program to combine the State and Timing trigger comparator memories so that they test for 40-bit trigger words.

The Trigger Linker consists of: U56A,B,C, sections of a 10101 quad OR/NOR gate (used here as buffer/inverters); U55C,D, sections of a 10124 quad TTL-to-ECL translator; and U42B, U45, and U46, all 10117 dual 2-wide OR-NAND gates.

NOTE: The upper OR gates in U45A,B and U46A are not used in this configuration of the PI 540. The software-generated enabling levels to these OR gates (signals SWTT0-, SWSTA0-, and SWSTB0- from the Processor Interface) are held always high so the outputs of the three NAND gates are controlled by their lower OR gates.

U56A, B, and C are used to provide both TRUE and inverted signals to the OR-NAND gates U45A, U45B, and U46A. However, as noted above, only the inverted outputs are used. U55C and D convert TTL level signals to ECL level for gates U46B and U42B and for their counterpart gates in the Arm Linker.

The outputs of the five 2-wide OR-NAND gates are connected in a wired AND (all outputs must be low to produce the active-low trigger signal) and fed to the Trigger Filter. In this configuration of the PI 540, the enabling signal SWTT1- is held always low by the Control Program so that the Timing trigger signal TT- controls the output of U45A.

The OR-NAND gates U45B and U46A are only active when the 40-bit State mode is in effect, at which time they, along with U45A, act to AND the TT- trigger signal from the Trigger-Word RAM on the Timing Memory Board with the STA- and STB- trigger signals from the Trigger-Word RAMs on State Memory

Boards A and B. (In effect, the trigger comparator memories on the three boards perform as one long comparator memory for a 40-bit trigger word.)

When the 40-bit State mode has been selected from the keyboard, this trigger AND function is enabled by the software-generated signals SWTT1-, SWSTA1-, and SWSTB1- from the Processor Interface. When the 40-bit State mode is not in effect, the Control Program holds SWSTA1- and SWSTB1- high so that the outputs of U45B and U46A are held low and do not interfere with the wired AND of the remaining three OR-NAND gates.

Gates U46B and U42B implement the trigger linkage function for the Timing Analyzer and for the 40-Channel State Analyzer. If keyboard input has called for a trigger link to the External signal, EXTECL+, the Control Program brings SWEXT- low so that EXTECL+ affects the output of U46B. Otherwise, SWEXT- is held high and EXTECL+ has no effect. Similarly, if a trigger link to the State trigger has been specified, SWFS- is brought low so that input signal FSECL+ (Function of State) affects the output of U46B. And if a link to the Waveform trigger has been specified, SWWT- is brought low so that input signal WTRIG+ controls the output of U42B.

Because of the wired AND connection of the OR-NAND gate outputs, all enabled linkages must be TRUE simultaneously with the Timing trigger TT- (or the 40-bit trigger output if the 40-bit State mode is in effect) in order to produce a low (TRUE) trigger output, TRIG-, to the Trigger Filter. Of course, the State link signal, FSECL+, will not be enabled in the 40-bit State mode.

The Trigger Filter consists of: U41A,B,C, sections of a 10102 quad NOR gate (section A is used here as a negative-input AND gate, and sections B and C are used here as inverters); and U52, a 10137 decade counter.

U41B inverts TRIG- and feeds it to the U52 decade counter at pin 9. At setup time, the S1 and S2 inputs to the decade counter are both low, putting the counter in the load mode. The Control Program, using the signals TF0 (Trigger Filter 0) through TF3 from the Processor Interface, presets the counter to the keyboard-specified filter value. This value may range from the default value of 0 to a maximum of 9.

When the trigger signal goes TRUE, S1 goes high, putting the counter in the count down mode. Clocked by CLKECL from Clock Control, the counter counts down from the preset filter value. The counter outputs are connected in wired AND, so when the count reaches 0, the pin-5 input to AND gate U41A is brought low. (The 0-count low level is inverted by U41C and fed back to the counter's Carry-In input, U52-10, to stop the count.) If the trigger signal on U41A-4 is still TRUE (low) at 0 count, the trigger signal TRIG+ goes TRUE at the output of U41A. TRIG+ is fed to the Sequencer Latch (schematic sheet 5).

10.2.5 Arm Control

Arm Control (see schematic sheet 2) comprises the Arm Linker and the Arm Filter. This circuitry allows the Control Program to set up any keyboard-specified linkages with External, State, or Waveform arm signals; and it implements the keyboard-selected degree of arm filtering. (Arm filtering is the requirement that the arm signal be TRUE for a specified number of clock

periods in order to be considered valid). Also, when the 40-bit State mode has been selected, this circuitry allows the Control Program to combine the State and Timing arm comparator memories so that they test for 40-bit arm words.

The Arm Linker consists of: U54B,C,D, sections of a 10101 quad OR/NOR gate (here used as buffer/inverters); and U42A, U43, and U44, all 10117 dual 2-wide OR-NAND gates. The operation of this circuitry is analogous in every respect to the operation of the Trigger Linker. Note that ECL-level EXT and FS signals are taken from the U55 translators in the Trigger Linker.

The Arm Filter consists of: U40A,B,C, sections of a 10102 quad NOR gate (section A is used here as a negative-input AND gate, and sections B and C are used here as inverters); and U51, a 10137 decade counter. The operation of this circuitry is analogous in every respect to the operation of the Trigger Filter.

10.2.6 Sequencer

The Sequencer (schematic sheet 5) comprises Load Control, the Sequencer Latch, the Sequencer RAM, and Sequencer Output. This circuitry allows the Control Program to set up (in accordance with the keyboard-entered instructions) the proper sequence of operation for the Delay Counter and Posttrigger Counter in relation to the occurance of arm and trigger events. (Although the circuit details differ, the Sequencer's counterpart on the State Control Board is the combined Delay Count RAM, Delay Mode RAM, and Delay Mode Control circuits. But in the Timing Analyzer, there is only one level of trigger word to which delay may be applied, compared with 15 in the State Analyzer. Thus the somewhat simpler circuit in the Timing Analyzer.)

Load Control consists of: U39A,B, sections of a quad TTL-to-ECL translator; and U20C,D, and U38, quad AND gates. Circuits U39A and B provide level translation for the RESET- signal to the Sequencer Latch and for the WRRAM- (Write RAM) write-enable signal to the Sequencer RAM. Both of these signals come from the Address Decoder in the Processor Interface. Gates U20C and D and U38 are enabled by the LDSEQ+ (Load Sequencer +) signal from the Control Shift Register in the Processor Interface. When enabled, these gates feed setup address signals, PTCTR03 (Posttrigger Counter 03) through PTCTR08, to the Sequencer RAM.

The Sequencer Latch consists of U12, a 10186 hex D flip-flop. Inputs to the latch are the ARM+ and TRIG+ signals from Arm Control and Trigger Control; the DLYTC- (Delay Terminal Count -) signal from the Delay Counter; and the three data output lines from the Sequencer RAM. The six outputs of the latch are fed to the six address inputs of the Sequencer RAM. Output Q0 also feeds the ARML+ (Arm Latch +) signal to the Count Mode Selector (schematic sheet 7); and outputs Q3, 4, and 5 also feed signals S0 (Sequence 0), S1, and S2 to Sequencer Output.

Sequencer Output consists of: U36, a 10125 quad ECL-to-TTL translator; and U24, a 10162 1-of-8 decoder. Translators U36B, C, and D translate the Sequencer Latch outputs S0, S1, and S2 to TTL level and feed them to the Status Port in the Processor Interface. Sequencer Latch outputs S0, S1, and

S2 also go to the three decoder inputs. The two decoder output signals, DLYCNT+/LD- (Delay Count + / Load -) and PTCNT+/LD- (Posttrigger Count + / Load -), are fed to the Delay Counter and Posttrigger Counter, respectively. PTCNT+/LD- is also fed through translator U36A as the signal FT (Function of Timing). This signal goes to the Status Port in the Processor Interface and also, through connector pin S2-11, to the State Memory Boards for possible linking. (PTCNT+/LD- and FT go high when Timing arm and trigger conditions have been met.)

The Sequencer RAM consists of U13, U25, and U37, all 10148 64-word x 1-bit static RAMs. The RAM data inputs are fed from the Processor Interface with signals PTCTR00 (Posttrigger Counter 00), PTCTR01, and PTCTR02. The RAM address inputs are fed by a wired OR connection from both the Sequencer Latch and the Load Control gates.

At setup time, the processor brings the RAM WE- inputs low with signal WRRAM- and resets the Sequencer Latch so that all latch outputs are low. The RAM address inputs are therefore under processor control through the Load Control gates. This allows the Control Program to load the RAMS with sequencing data in accordance with the keyboard-entered delay mode information. Further, because Sequencer Latch output signals S0, S1, and S2 to the decoder inputs are all low, both decoder output signals, DLYCNT+/LD- and PTCNT+/LD-, are in the load state (low). This allows the Control Program to preset the Delay Counter and Posttrigger Counter to appropriate values.

At run time, the Control Program brings the Load Control gate outputs low with a low LDSEQ+. This leaves the RAM address inputs under control of the Sequencer Latch. The Sequencer Latch is clocked by CLKECL and, starting with address 00, steps through the control sequence stored in the RAM. The high-order 3 bits of each successive RAM address are determined by the three RAM outputs from the previous address. The low-order three address bits only change when an arm- or trigger-word match occurs or when delay terminal count is reached. At the proper point in the delay control sequence, S0, S1, and S2 decode to bring DLYCNT+/LD- high, thus starting the delay count. Similarly, at the proper time, PTCNT+/LD- is brought high, thus starting the posttrigger count.

10.2.7 Posttrigger and Delay Counters

The Posttrigger and Delay Counters comprise the Count Mode Selector, the Delay Counter, and the Posttrigger Counter. These circuits allow the Control Program to implement the keyboard-selected delay function and the specified pretrigger-posttrigger division of collected data.

The Count Mode Selector consists of U20A,B, sections of a 10104 quad AND gate, and U41D, a section of a 10102 quad NOR gate (used here as an inverter). The wired OR outputs of U20A and B produce signal DLYCLK (Delay Clock) which occurs either at every ARML+ occurance or at every CLKECL clock, depending on the polarity of software-generated signal DLYARM+/CLK- (which in turn is dependent on a keyboard entry). DLYCLK is used to clock the Delay Counter.

The Delay Counter consists of: U17, U18, U19, and U21, all 10137 decade counters; and U22A, B, and D, sections of a 10103 quad OR gate (used here as

negative-logic AND gates). The counters are operated in the countdown mode and, using the U22 AND gates, are connected in cascade in such a way that a terminal count of 0000 produces a low signal, DLYTC- (Delay Terminal Count -), at the wired AND junction of the U21 and U22D outputs. The maximum preset count value is 9999.

At setup time, the counters are placed in the load mode by a low level on the DLYCNT+/LD- signal line from the Sequencer to the S1 mode-select inputs of the counters. This allows the Control Program to load the keyboard-specified delay count in the counters using signals DLYCTR00 (Delay Counter 00) through DLYCTR15 from the Control Shift Register in the Processor Interface.

At run time, if and when the conditions specified in the selected delay mode are met, the Sequencer brings DLYCNT+/LD- high. This puts the Delay Counter in the countdown mode and allows the preset count to be decremented by each pulse on the DLYCLK line from the Count Mode Selector. This line may carry either CLKECL clocks or ARML+ pulses, depending on whether the selected delay mode specifies the delay in terms of clocks or in terms of arm-word occurances. If and when the countdown reaches 0000, signal DLYTC- goes low. DLYTC- is fed to one input of the Sequencer Latch.

The Posttrigger Counter consists of: U14, U15, and U16, all 10137 decade counters; U22C, a section of a 10103 quad OR gate (used here as a negative-logic AND gate); U11, a 10211 dual 3-input, 3-output NOR gate; and U39C, a section of a 10124 quad TTL-to-ECL translator. The counters are operated in the countdown mode and, using the U22C AND gate, are connected in cascade in such a way that a terminal count of 000 produces low levels at input pins 5 and 7 of AND gate U11A. The maximum preset count value is 999.

At setup time, the counters are placed in the load mode by a low level on the PTCNT+/LD- signal line from the Sequencer to the counters' S1 mode-select inputs. This allows the Control Program to load the counters with the post-trigger count using signals PTCTR00 (Posttrigger Counter 00) through PTCTR11 from the Control Shift Register in the Processor Interface. (The Control Program derives the posttrigger count from 1000 minus the keyboard-specified pretrigger count.)

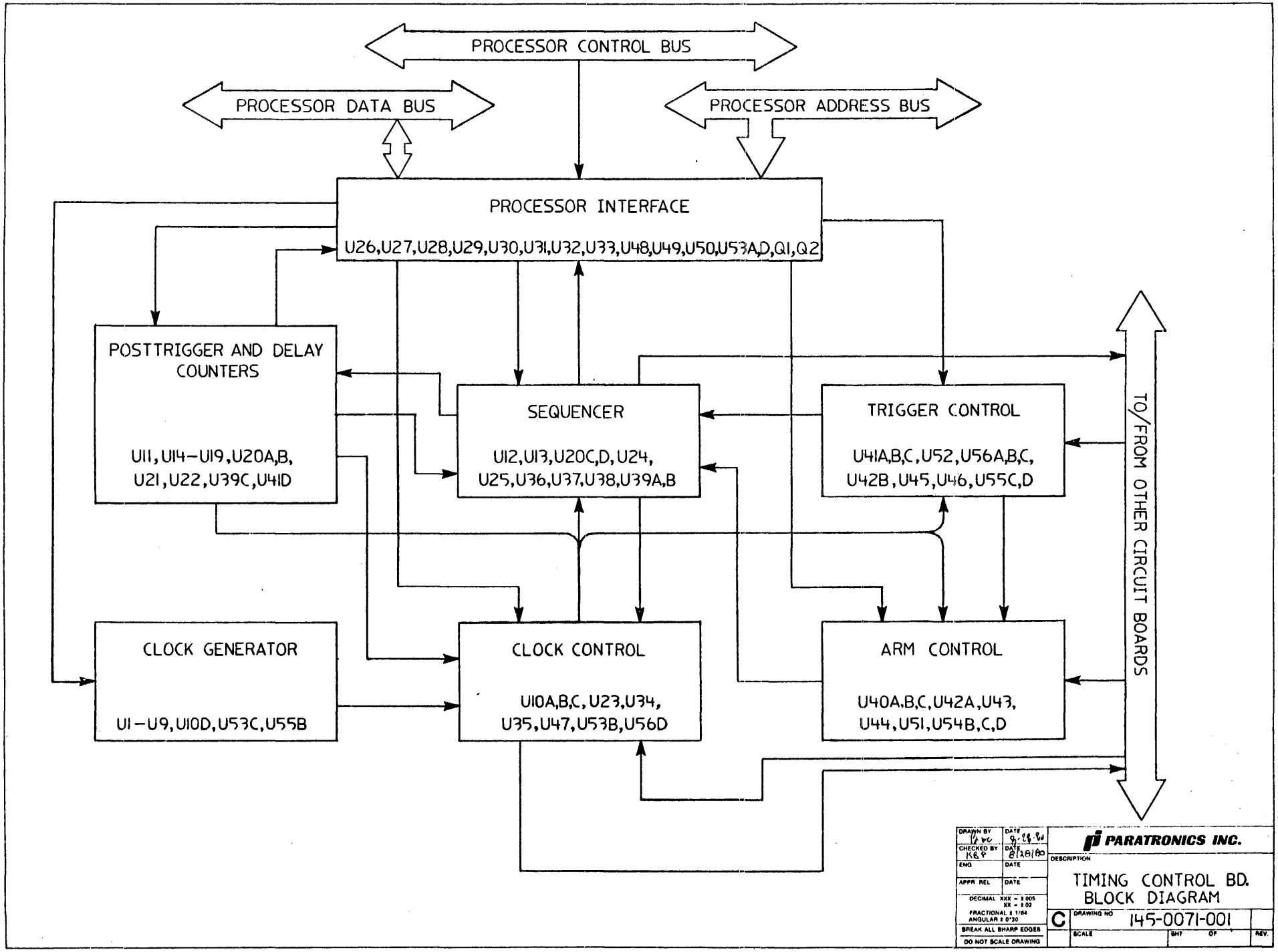
At run time, if and when the specified arm, delay, and trigger conditions are met, the Sequencer brings PTCNT+/LD- high. This puts the Posttrigger Counter in the countdown mode and allows the preset count to be decremented by CLKECL from Clock Control. A terminal count of 000 produces high outputs from AND gate U11A if the software-generated enable signal, ENCLKINH- (Enable Clock Inhibits -), is low. (ENCLKINH- comes from Control Shift Register in the Processor Interface and is normally brought low by the Control Program at run time.)

The three outputs of U11A are connected in wired OR with those of U11B and produce three identical signals, CLKINHA+ (Clock Inhibit A+), CLKINHB+, and CLKINHC+. These signals are produced either by the posttrigger terminal count through U11A or by SWCLKINH- (Software Clock Inhibit -) through U11B. (SWCLKINH- comes from the Master Control Register in the Processor Interface and is used by the Control Program during setup.) The three clock inhibit signals are fed to Clock Control and shut off all working clocks (CT, CLKECL, and CLKTTL) when the posttrigger terminal count has been reached. (Three

identical clock inhibit signals are needed because two must be separately wire OR'd with the two Qualifier Control latch outputs shown on schematic sheet 8.)

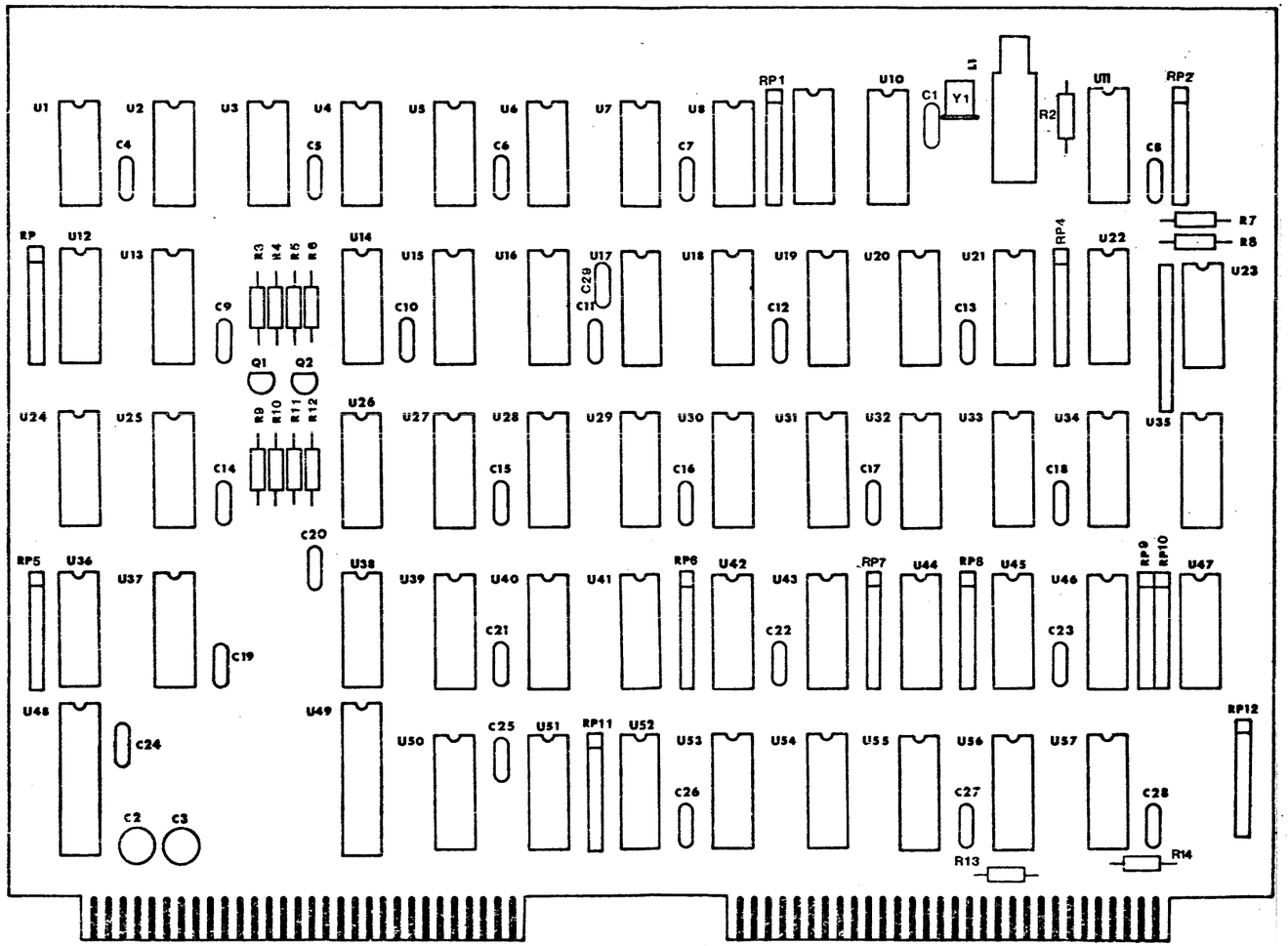
10.3 SCHEMATIC, BOARD LAYOUT, & PARTS LIST

The schematic diagram, board layout, and parts list for the Timing Control Board are contained on the following pages.



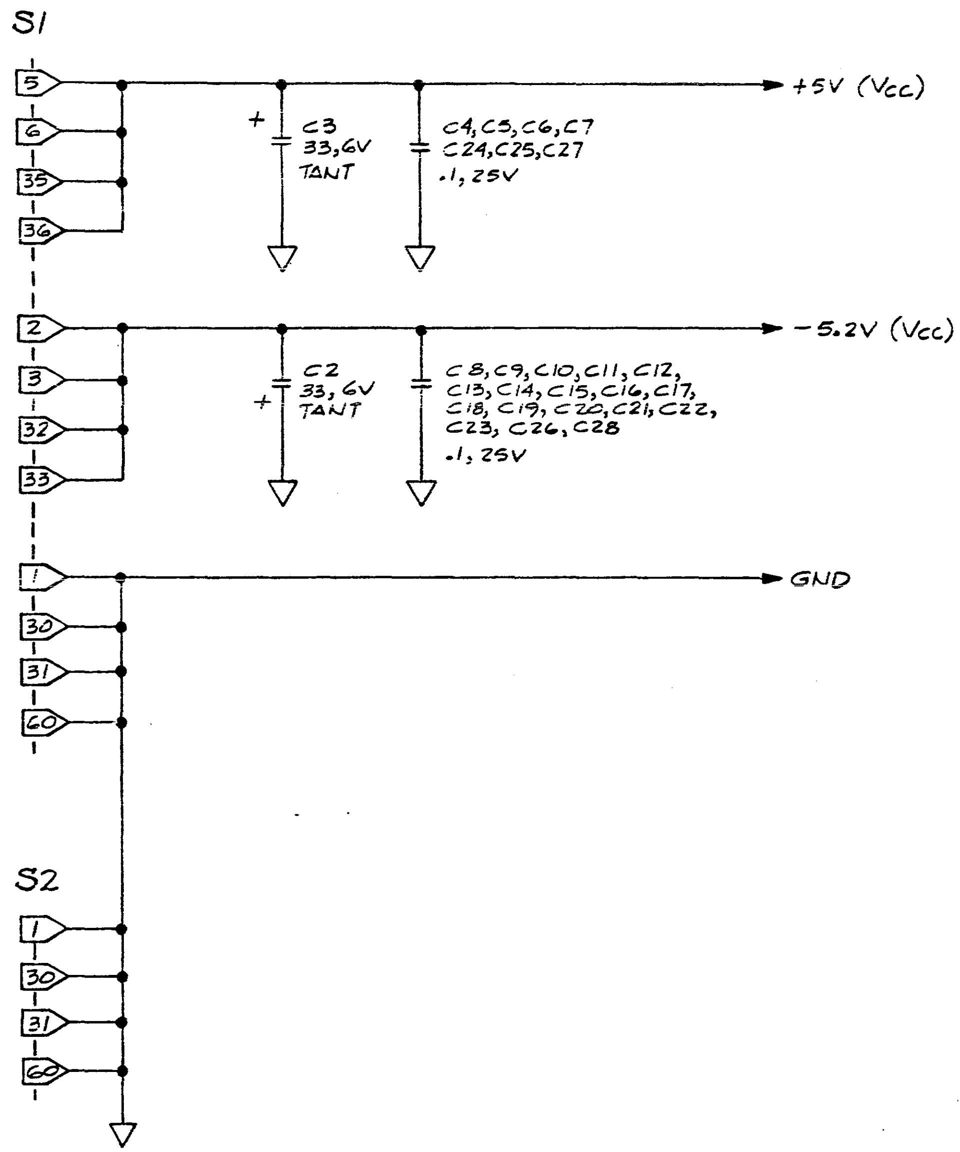
DRAWN BY	DATE	PARATRONICS INC.
CHECKED BY KRP	DATE 8/20/80	DESCRIPTION
ENG	DATE	TIMING CONTROL BD. BLOCK DIAGRAM
APPR REL	DATE	
DECIMAL XXX = ± 005 XX = ± 02		C DRAWING NO 145-0071-001
FRACTIONAL ± 1/64 ANGULAR ± 0°30		SCALE SHT OF REV.
BREAK ALL SHARP EDGES		
DO NOT SCALE DRAWING		

REV	DESCRIPTION	DATE	APPROVED
B	REV PER ECO 066	11-1-79	
C	REV PER ECO 106		
D	REV PER ECO 133A		



DRAWN BY: [illegible]	DATE: 8-28-79	PARATRONICS INC.	
CHECKED BY: [illegible]	DATE: 12-4-79	DESCRIPTION: LEGENDMASTER	
ENG: [illegible]	DATE: 12-4-79	TIMING CONTROL	
APPR. REL: [illegible]	DATE: 12-20-79		
DECIMAL .XXX ± .005 .XX ± .02		D	DRAWING NO: 126-0071-201 D
FRACTIONAL ± 1/64			SCALE: 2/1 SHT 1 OF 1 REV.
ANGULAR ± 0°30'			
BREAK ALL SHARP EDGES			
DO NOT SCALE DRAWING			

REV	DESCRIPTION	DATE	APPROVED
C	REV PER ECO 106	3/4/80	WOS
D	REV PER ECO's 130,133A		GDM
E	REV PER ECO	9/26/80	ES



POWER DISTRIBUTION

"U" NUMBER'S	DEVICE	+5V (VCC)	-5.2V (VCC)	GND	PACKAGE
54,55,56	10101	—	8	1, 16	16 DIP
42,43,44,45,46	10117	—	8	1, 16	↕
40, 41, 10	10102	—	8	1, 16	
51,52,16,15,14,21,19,18,17	10137	—	8	1, 16	
55, 39	10124	9	8	16	
50	74LS138	16	—	8	16 DIP
49	74LS374	20	—	10	20 DIP
53, 36	10125	9	8	16	16 DIP
48	74LS373	20	—	10	20 DIP
26,27,28,30,31,32,33,29	CD4015	—	8	16	16 DIP
20, 28	10104	—	8	1,16	↕
12	10186		8	1,16	
37,25,13	10148		8	1, 16	
24	10162		8	1,16	
2, 3	74LS151	16	—	8	16 DIP
4,5, 6, 7, 8	74LS90	5	—	10	14 DIP
1	74LS74	14	—	7	14 DIP
9	10138	—	8	1,16	16 DIP
22	10103	—	8	1, 16	↕
11, 35, 34	10211	—	8	1, 15, 16	
47	10130	—	8	1, 16	16 DIP

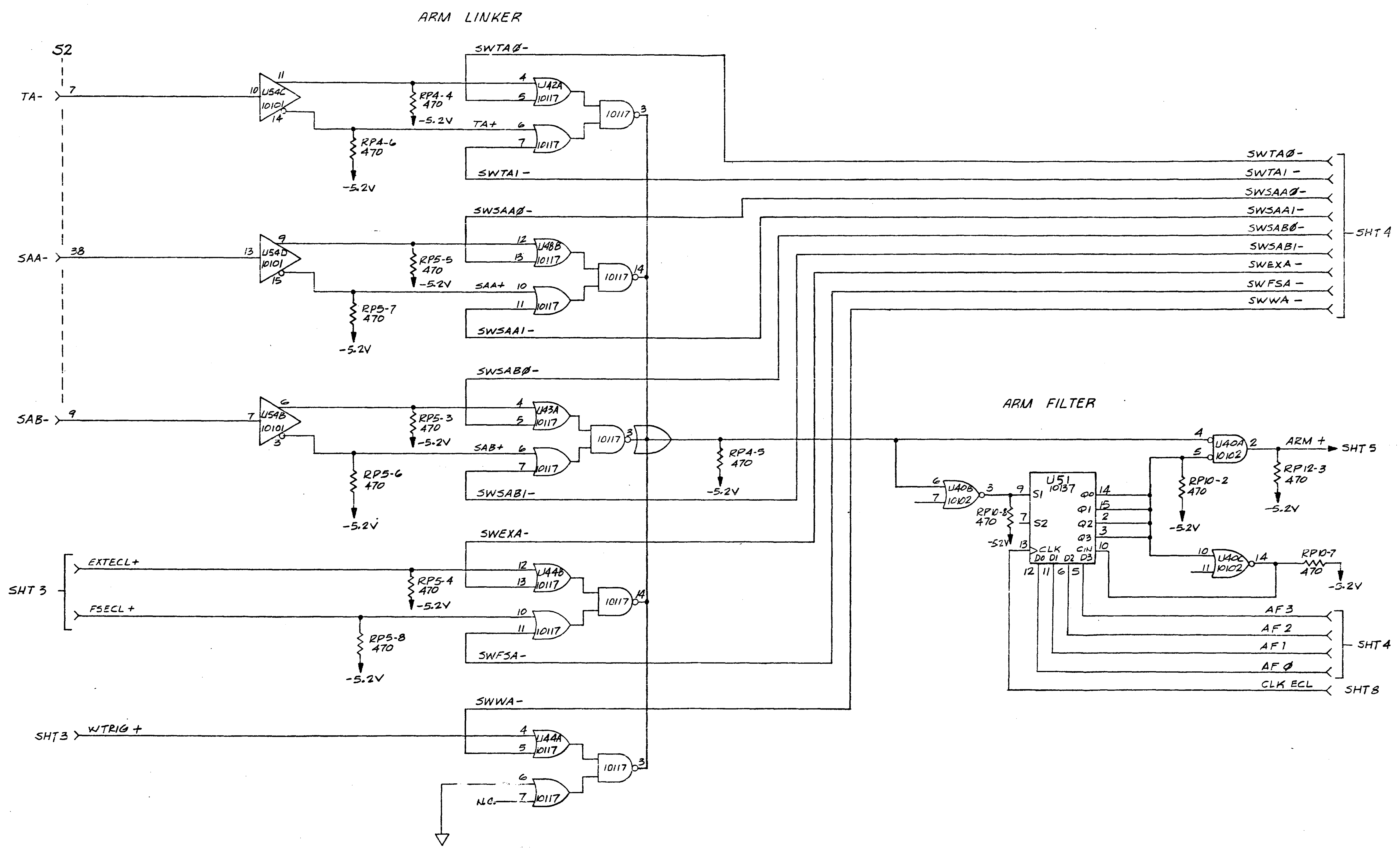
2. ALL CAPACITORS ARE IN MICROFARADS, DISC CERAMIC
1. ALL DISCRETE RESISTORS ARE 1/4W, 5%
NOTES: UNLESS OTHERWISE SPECIFIED:

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	
MAT'L —	
FINISH —	
DR	1-3-80
CK	1-7-80
APPR	1-7-80
BREAK ALL SHARP EDGES; DECIMAL .XX ± .XXX ±; ANGULAR ±	DO NOT SCALE DRAWING

PARATRONICS INC.

MODEL 540 TIMING CONTROL
ELECTRICAL SCHEMATIC
PWR & GND DISTRIBUTION

DRWG NO 127-0071-001 REV E
D | SCALE | SHT 1 OF 8



UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES

PARATRONICS INC.

MODEL 540 TIMING CONTROL
ELECTRICAL SCHEMATIC
ARM CONTROL

DRWG NO 127-0071-001 REV E
SHT 2 OF 3

TRIGGER LINKER

S2

TT- 8 — U56A 10101 (4, 2; 5) — RPG-4 470 — -5.2V — TT+
RPG-6 470 — -5.2V

STA- 39 — U56B 10101 (7, 3; 6) — RPG-5 470 — -5.2V — STA+
RPG-8 470 — -5.2V

STB- 10 — U56C 10101 (10, 14; 11) — RPG-3 470 — -5.2V — STB+
RPG-7 470 — -5.2V

EXT(TTL) 12 — U55C 10124 (10, 12; 15) — EXTECL+ 12
SHT 2 ← EXTECL+

SHT 2 ← FSECL
FS(TTL) 42 — U55D 10124 (11, 13; 14)

WTRIG+ 40
SHT 4 ← WTRIG+

SWTT0-, SWTT1-, SWSTA0-, SWSTA1-, SWSTB0-, SWSTB1-, SWEXT-, SWFST-, SWWT-

U45A 10117 (4, 5; 3) — 10117 (3, 6; 7) — 10117 (3)
U45B 10117 (12, 13; 14) — 10117 (14, 10; 11) — 10117 (14)
U46A 10117 (4, 5; 3) — 10117 (3, 6; 7) — 10117 (3)
U46B 10117 (12, 13; 14) — 10117 (14, FSECL+ 10; 11) — 10117 (14)
U42B 10117 (12, 13; 14) — 10117 (14, N.C. 10; 11) — 10117 (14)

RP4-7 470 — -5.2V

SWTT0-, SWTT1-, SWSTA0-, SWSTA1-, SWSTB0-, SWSTB1-, SWEXT-, SWFST-, SWWT- → SHT4

TRIGGER FILTER

U41B 10102 (6, 7; 3) — RP10-5 470 — -5.2V

10137 U52 (9, 7, 13; 14, 15, 2, 3, 10; 12, 11, 6, 5)
S1 S2 CLK CIN — Q0 Q1 Q2 Q3 — D0 D1 D2 D3

U41A 10102 (4, 5; 2) — TRG+ → SHT5
RP4-8 470 — -5.2V
RP12-5 470 — -5.2V

U41C 10102 (10, 11; 14)
RP10-6 470 — -5.2V

TF3, TF2, TF1, TF0 → SHT4

CLK ECL ← SHT 8

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR Bo Cornell	12-20-79	PARATRONICS INC.
	CK G Fm	1-7-80	MODEL 540 TIMING CONTROL
MAT'L —	APPR G F M	1-7-80	ELECTRICAL SCHEMATIC
FINISH —	BREAK ALL SHARP EDGES; DECIMAL XX ± .1, XXX ± .1; ANGULAR 1; DO NOT SCALE DRAWING		TRIGGER CONTROL
			DWG NO 127-0071-001 REV E
			SCALE — SHT 3 OF 8

SHT 5 RESET-
SHT 5 WR RAM-
D0 48
D1 49
D2 19
D3 17
D4 18
D5 20
D5 51
D7 21
SI
SI
ADDRESS DECODER
A0 55
A1 24
A2 58
A13 44
I/O EN- 8
A11 27
U50 74LS138
WRRAM-
RDSTAT-
RESET-
+5V
MCRCLK
R12 1K
R11 1K
-5.2V
Q2 2N3905
R5 3.3K
MASTER CONTROL REGISTER
SRDATA
U49 74LS374
CLKSELE
CLKSELA
CLKSELB
CLKSELC
CLKSELD
SWCLKINH-
PSEUDOCLK
SRCLK
+5V
R4 1K
R10 1K
R9 1K
-5.2V
Q1 2N3905
R3 3.3K
STATUS PORT
U53 10125
U48 74LS373
RDSTAT-
FTTTL
S2TTL
S1TTL
S0TTL
CLKINHC+
SHT 5
SHT 7
CONTROL SHIFT REGISTER
U26 CD4015
U27 CD4015
U28 CD4015
U33 CD4015
U30 CD4015
U31 CD4015
U32 CD4015
U29 CD4015
-5.2V
TF3
TF2
TF1
TF0
AF3
AF2
AF1
AF0
SHT 3
SHT 2
SW<50
SW50-
LED5EQ
SHT 8
SHT 5
SWNE-
SWPE-
SWQCLK0
SWQCLK1
SHT 8
SWWA-
SWFSA-
SWEXA-
SW5AB1-
SW5AB0-
SW5AA1-
SW5AA0-
SWTA1-
SWTA0-
SHT 2
SWWT-
SWFST-
SWEXT-
SW5TB1-
SW5TB0-
SW5TA1-
SW5TA0-
SHT 3
SHT 5 & 7
PTCTR00
PTCTR01
PTCTR02
PTCTR03
PTCTR04
PTCTR05
PTCTR06
PTCTR07
PTCTR08
SHT 7
PTCTR09
PTCTR10
PTCTR11
DLYCTR00
DLYCTR01
DLYCTR02
DLYCTR03
DLYCTR04
DLYCTR05
DLYCTR06
DLYCTR07
DLYCTR08
DLYCTR09
DLYCTR10
DLYCTR11
DLYCTR12
DLYCTR13
DLYCTR14
DLYCTR15
SHT 8 DLYARM+/CLK-
SHT 7 ENCLKINH-
SHT 3 SWTT0-
SWTT1-

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR K.D.Sarell	1-20-9	PARATRONICS INC.
	CH GFM	1-7-80	
	APPR GFM	1-7-80	MODEL 540 TIMING CONTROL
MAT'L —	BREAK ALL SHARP EDGES		ELECTRICAL SCHEMATIC
FINISH —	DECIMAL ANGULAR		PROCESSOR INTERFACE
	DO NOT SCALE DRAWING		DRWG NO 127-0071-001 REV E
	D	SCALE —	SHT 4 OF 8

SHT 4 — PTCTRØØ, PTCTRØ1, PTCTRØ2
SHT 2 — ARM+
SHT 3 — TRIG+
SHT 7 — DLYTC−
SHT 8 — CLKECL

LOAD CONTROL

+5V

RESET− → U39B 10124 (7, 6 → 3) → RP12-4 470 → −5.2V

WRRAM− → U39A 10124 (5, 6 → 2) → RP2-5 470 → −5.2V

PTCTRØ3 → U20C 10104 (10, 11 → 14) → RP2-2 470 → −5.2V

PTCTRØ4 → U20D 10104 (12, 13 → 15) → RP2-3 470 → −5.2V

PTCTRØ5 → U38C 10104 (10, 11 → 14) → RP2-4 470 → −5.2V

PTCTRØ6 → U38B 10104 (7, 6 → 3) → RP12-2 470 → −5.2V

PTCTRØ7 → U38D 10104 (12, 13 → 15) → RP12-6 470 → −5.2V

PTCTRØ8 → U38A 10104 (5, 4 → 2) → RP12-7 470 → −5.2V

LDSEQ+

SHT 4 ←

SEQUENCER LATCH

U12 10186 (D0–D5, R; Q0–Q5)

ARML+ → SHT 8

SØ
S1
S2

SEQUENCER RAM

U37 10148 (A0–A5, DIN, WE; DOUT) → RP2-8 470 → −5.2V

U25 10148 (A0–A5, DIN, WE; DOUT) → RP2-7 470 → −5.2V

U13 10148 (A0–A5, DIN, WE; DOUT) → RP2-6 470 → −5.2V

SEQUENCER OUTPUT

U24 10162 (A, B, C; Q3–Q7)

DLYCNT+/LD− → RP3-8 470 → −5.2V → SHT 7

PTCNT+/LD− → RP4-2 470 → −5.2V → SHT 7

S2

U36A 10125 (3 → 4): FT, FTTTL

U36D 10125 (15 → 13): SØTTL

U36C 10125 (11 → 12): S1TTL

U36B 10125 (7 → 5): S2TTL

→ SHT 4

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES	DR E.Williamson	12-20-7	PARATRONICS INC.
	CK G.F.M	1-7-8	MODEL 540 TIMING CONTROL
	APPR G.F.M	1-8-8	ELECTRICAL SCHEMATIC SEQUENCER
MAT'L —	BREAK ALL SHARP EDGES		DRWG NO 127-0071-001 REV E
FINISH —	DECIMAL ANGULAR .XX ± .3 ± .XXX ± .2		D SCALE — SHT 5 OF 8
	DO NOT SCALE DRAWING		

SECOND STAGE DIVIDER

FIRST STAGE SELECTOR

1ns

10ns

100ns

1000ns

10,000 ns

74LS151 U2

100ns 200ns 500ns 1000ns

D4 D5 D6 D7 D2 D1 D0 C B A

W S

-5.2V Vcc

U4 74LS90 U5 74LS90 U6 74LS90 U7 74LS90

B QA QD A

Vcc

SHT 4 CLKSELD CLKSELE

FIRST STAGE DIVIDER

CLOCK OSCILLATOR

U9 10138

10ns 50ns 20ns

RP9-7 470 -5.2V

U1 74LS74

50ns 100ns 200ns

U1OD 10102

R2 2K -5.2V

Y1 100 MHZ

L1 4 1/2 TURNS ON TUNEABLE FERRITE FORM

C1 2.2Pf

U53C 10125

RP10-4 470 -5.2V

U8 74LS90

500ns 1000ns

SECOND STAGE SELECTOR

50ns

U3 74LS151

D5 D4 D3 D2 D1 D0 D7

PSEUDOCLK

CLKSELA CLKSELB CLKSELC

SHT 4

+5V

U55B 10124

INT< 50

INT50

SHT 8

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR Ron Gowell 12-20-79	PARATRONICS INC.
	CK G.F.M 1-3-80	
	APPR G.F.M 1-8-80	MODEL 540 TIMING CONTROL
MAT'L —	BREAK ALL SHARP EDGES	ELECTRICAL SCHEMATIC
FINISH —	DECIMAL ANGULAR	CLOCK GENERATOR
	XX = ± ±	DRWG NO 127-0071-001 REV E
	XXX = ± DO NOT SCALE DRAWING	D SCALE — SHT 6 OF 8

COUNT MODE SELECTOR

ARML+ → U20A 10104 (4, 5 → 2)

DLYARM+/CLK- → U20A 10104 (5)

U41D 10102 (13 → 15): DLYARM-/CLK+ → U20B 10104 (6, 7 → 3)

CLKECL → U20B 10104 (7)

RPS-2 → -5.2V

ARML+ → SHT 5

CLKECL → SHT 2,3 & 5

DLYARM+ CLK- → SHT 4

POST TRIGGER COUNTER

SHT 4 →

PTCTR00
PTCTR01
PTCTR02
PTCTR03
PTCTR04
PTCTR05
PTCTR06
PTCTR07
PTCTR08
PTCTR09
PTCTR10
PTCTR11

U16 10137 (D3 D2 D1 D0; C1; C S1 S2) — RP3-2 → -5.2V

U15 10137 (D3 D2 D1 D0; C1; C S1 S2) — RP3-4 → -5.2V

U14 10137 (D3 D2 D1 D0; C1 → NC; C Q3 Q2 Q1 Q0 S1 S2)

SHT 5 PTCNT+/LD

SHT 8 CLKECL

C29 .100 PF — RP1-6 → -5.2V — RP3-5 → -5.2V

U22C 10103 (12, 13 → 15)

SHT 4 ENCLKINH-

SHT 8 CLKINHC+
CLKINHB+
CLKINHA+

U11A 10211 (5, 6, 7 → 2, 3, 4)

U11B 10211 (9, 10, 11 → 12, 13, 14)

SHT 4 SWCLKINH-

U39C 10124 (10 → 15) — RP1-7 470

SHT 5 DLYTC-

RP12-5 → -5.2V
RP12-4 → -5.2V
RP4-6 → -5.2V
RP12-8 → -5.2V

DELAY COUNTER

DLYCTR15
DLYCTR14
DLYCTR13
DLYCTR12
DLYCTR11
DLYCTR10
DLYCTR9
DLYCTR8
DLYCTR7
DLYCTR6
DLYCTR5
DLYCTR4
DLYCTR3
DLYCTR2
DLYCTR01
DLYCTR00

→ SHT 4

U21 10137 (D3 D2 D1 D0; C1; C Q3 Q2 Q1 Q0 S1 S2)

U19 10137 (D3 D2 D1 D0; C1; C Q3 Q2 Q1 Q0 S1 S2)

U18 10137 (D3 D2 D1 D0; C1; C Q3 Q2 Q1 Q0 S1 S2) — RP3-7 470 → -5.2V

U17 10137 (D3 D2 D1 D0; C1 → NC; C Q3 Q2 Q1 Q0 S1 S2)

DLYCLK

RP4-3 → -5.2V

DLYCNT+/LD → SHT 5

U22D 10103 (10, 11 → 14)

U22A 10103 (4, 5 → 2) — RPi-8 → -5.2V — RP1-4 470 → -5.2V

U22B 10103 (7, 6 → 3) — RP3-3 470 → -5.2V — RP1-5 470 → -5.2V

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR Eric Lance	12-20-79	PARATRONICS INC.
	CK FM	1-7-80	MODEL 540 TIMING CONTROL
	APPR FM	1-7-80	ELECTRICAL SCHEMATIC
MAT'L	BREAK ALL SHARP EDGES		POST TRIGGER & DELAY COUNTERS
FINISH	DECIMAL .XX = ± .XXX = ±	ANGULAR :	DRWG NO 127-0071-001 REV E
	DO NOT SCALE DRAWING		D SCALE — SHT 7 OF 8

QUALIFIER CONTROL

S2-58 QCLK+ — RP8-9 100, RP7-7 160 → -5.2V; U10A 10102 (4, 5 → 2)
SHT 4 SWQCLKØ- (Q CLK SEL) — RP7-7 160 → -5.2V
RP11-7 → -5.2V
U10C 10102 (10, 11 → 14 QUAL+)
S2-57 QCLK- — RP8-8 100, RP7-8 160 → -5.2V
SHT 4 SWQCLK1- — U10B 10102 (6, 7 → 3)
RP11-6 470 → -5.2V
S2-56 CLK+ — 160 → -5.2V; 100
SHT 4 SWNE-
EXT CLK
RP11-3 470 → -5.2V
S2-55 CLK- — RP7-6 160 → -5.2V; RP8-6 100
SHT 7 CLKINHB+
SHT 4 SW50-

FINAL CLOCK SELECTOR

QUAL+ 7 → U47A 10130 D; CLK+ 6 → CE; Q → 3 QUAL.
U47B 10130 (QUAL+ 10; CLK- 11 → CE; Q → 14 QUAL)
CLKSEL
CLKINHA+
SWPE-
U35A 10211 (5, 6 → 2; CLK- 7 → 3)
SWNE- 9; CLK+ 10 → U35B 10211 (11 → 12)
CLK+
CLK ECL — SHT 2,3,5 & 7
CLK INH +A — SHT 7
SWPE- — SHT 4
LLOCK → 6 CT
SW50- → U34A 10211 (5, 6 → 2)
INT50 → RP11-8 470 → -5.2V
INT<50 → RP1-3 470 → -5.2V
SHT 6 — INT CLOCK
SHT 7 CLKINHC+ — INT CLOCK SELECT (-) → U34B 10211 (9, 10 → 12)
SHT 4 SW<50- → RP11-2 470 → -5.2V

CLOCK DELAY

U23 20 NS D.L. (1 IN → C 14)
C 2 4 6 8 10 12 14 16 18 20
7 13 2 12 3 11 4 10 5 9 6
JUMPER AREA
RB 180Ω
R7 270Ω → -5.2V
U53B 10125 (7, 6 → 5) → 43 CLKTTL → S2
U56D 10101 (13 → 9)

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR E.M. Caldwell 12-20-9	PARATRONICS INC.	
MAT'L	APPR	MODEL 540 TIMING CONTROL	
FINISH	BREAK ALL SHARP EDGES DECIMAL XX = ± XXX = ± ANGULAR ±	ELECTRICAL SCHEMATIC CLOCK CONTROL	
	DO NOT SCALE DRAWING	DRWG NO 127-0071-001	REV E
		D SCALE —	SHT 8 OF 8

SINGLE LEVEL EXPLOSION

09/04/80

PAR143-0071-0090-00 DESCRIPTION : TIMING CONTROL PC ASSY-OUTSIDEECO#: 133 REV.CU.: D

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
111-0207-0103-00	D	22 UF 16V CAP. ELECTRO.,RAD.	2	1	0	08/21/80	OPEN	0	C2 C3
111-0012-0003-00		2.2 PF 1KV CAP. CD	1	1	0	OPEN	OPEN	0	C1
113-0046-0003-00	D	DELAY LINE,LC0202100B,PE21182	1	1	0	05/05/80	OPEN	0	U23
110-0005-0070-00	D	2 K OHM 1/4W 5% CF RES	1	1	0	03/06/80	OPEN	0	R2
110-0005-0047-00	D	220 OHM 1/4W 5% CF RES	2	1	0	OPEN	OPEN	0	R13 R14
111-0012-0030-00	D	100 PF 1KV CAP. CD	1	1	0	OPEN	OPEN	0	C29
126-0071-0001-00	D	TIMING CONTROL PC FAB	1	1	0	OPEN	OPEN	0	
115-0009-0001-00	D	SOCKET,20PIN	2	1	0	OPEN	OPEN	0	U48 U49
115-0005-0001-00	D	SOCKET,16PIN	47	1	0	OPEN	OPEN	0	U10
U11 U12 U13 U14 U15 U16 U17 U18 U19 U2 U20 U21 U22 U24 U25 U26									
U27 U28 U29 U3 U30 U31 U32 U33 U34 U35 U36 U37 U38 U39 U40 U41									
U42 U43 U44 U45 U46 U47 U50 U51 U52 U53 U54 U55 U56 U9									
115-0003-0001-00	D	SOCKET,14PIN	6	1	0	OPEN	OPEN	0	U1
U4 U5 U6 U7 U8									
121-0013-0001-00	D	UNICOIL,T7-116,4 1/2 TURNS	1	01	0	OPEN	OPEN	0	L1
110-0308-0001-00	D	4700HM X 7 RESISTOR NETWORK	10	1	0	OPEN	OPEN	0	RP1
RP11 RP12 RP2 RP3 RP4 RP5 RP6 RP7 RP8									
110-0307-0001-00	D	1600HM X 7 RESISTOR NETWORK	1	1	0	OPEN	OPEN	0	RP9
110-0306-0001-00	D	1000HM X 7 RESISTOR NETWORK	1	1	0	OPEN	OPEN	0	RP10
110-0005-0045-00	D	180 OHM 1/4W 5% CF RES	1	1	0	OPEN	OPEN	0	R8
110-0005-0049-00	D	270 OHM 1/4W 5% RES	1	1	0	OPEN	OPEN	0	R7
110-0005-0063-00	D	1K OHM 1/4W 5% CF RES	6	1	0	OPEN	OPEN	0	R10
R11 R12 R4 R6 R9									
110-0005-0075-00	D	3.3 K OHM 1/4 W CF RES	2	1	0	OPEN	OPEN	0	R3 R5
111-0004-0072-00	D	.1 UF 25V CAP. CD	25	1	0	OPEN	OPEN	0	C10
C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26									
C27 C28 C4 C5 C6 C7 C8 C9									
112-0101-0001-00	D	TRANSISTOR, 2N3905	2	1	0	OPEN	OPEN	0	Q1 Q2

LEGEND UM : 01=EACH 02=INCH 03=FEET 04=BULK 05=AS REQUIRED 06=OTHER
LEGEND KEY: A=W/PARTS LIST D=W/O PARTS LIST R=REFERENCE DOCUMENT S=SPECIFICATION

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SINGLE LEVEL EXPLOSION

09/04/80

PAR143-0071-0001-00 DESCRIPTION : TIMING CONTROL PC ASSY ECO#: 133 REV.CU.: D

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
112-0305-0001-00	D	100 MHZ CRYSTAL	1	1	0	05/06/80	OPEN	0	Y1
113-0003-0151-00	D	I.C., 74LS151	2	1	0	OPEN	OPEN	0	U2
U3									
113-0200-0103-00	D	I.C.,MC10103	1	1	0	OPEN	OPEN	0	U22
113-0003-0374-00	D	I.C., 74LS374	1	1	0	OPEN	OPEN	0	U49
143-0071-0090-00	D	TIMING CONTROL PC ASSY-OUTSIDE	1	1	0	OPEN	OPEN	133	
113-0003-0074-00	D	IC, 74LS74	1	1	0	OPEN	OPEN	0	U1
113-0003-0090-00	D	I.C., 74LS90	5	1	0	OPEN	OPEN	0	U4
U5 U6 U7 U8									
113-0003-0138-00	D	I.C., 74LS138	1	1	0	OPEN	OPEN	0	U50
113-0003-0373-00	D	I.C., 74LS373	1	1	0	OPEN	OPEN	0	U48
113-0042-0001-00	D	SCL4015BE	8	1	0	OPEN	OPEN	0	U26
U27 U28 U29 U30 U31 U32 U33									
113-0200-0101-00	D	I.C.,MC10101	2	1	0	OPEN	OPEN	0	U54
U56									
113-0200-0102-00	D	I.C.,MC10102	3	1	0	OPEN	OPEN	0	U10
U40 U41									
113-0200-0104-00	D	I.C., 10104N	2	1	0	OPEN	OPEN	0	U20
U38									
113-0200-0117-00	D	I.C., 10117N	5	1	0	OPEN	OPEN	0	U42
U43 U44 U45 U46									
113-0200-0124-00	D	I.C., MC10124	2	1	0	OPEN	OPEN	0	U39
U55									
113-0200-0125-00	D	I.C., MC10125	2	1	0	OPEN	OPEN	0	U36
U53									
113-0200-0130-00	D	I.C., M10130	1	1	0	OPEN	OPEN	0	U47
113-0200-0137-00	D	I.C., MC10137	9	1	0	OPEN	OPEN	0	U14
U15 U16 U17 U18 U19 U21 U51 U52									
113-0200-0138-00	D	I.C., MC10138	1	1	0	OPEN	OPEN	0	U9
113-0200-0148-00	D	I.C., MC10148	3	1	0	OPEN	OPEN	0	U13
U25 U37									
113-0200-0162-00	D	I.C., 10162N	1	1	0	OPEN	OPEN	0	U24
113-0200-0186-00	D	I.C., MC10186	1	1	0	OPEN	OPEN	0	U12
113-0200-0211-00	D	I.C., MC10211	3	1	0	OPEN	OPEN	0	U11
U34 U35									

LEGEND UM : 01=EACH 02=INCH 03=FEET 04=BULK 05=AS REQUIRED 06=OTHER
LEGEND KEY: A=W/PARTS LIST D=W/O PARTS LIST R=REFERENCE DOCUMENT S=SPECIFICATION

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11.0 TIMING MEMORY BOARD

11.0 TIMING MEMORY BOARD

11.1 INTRODUCTION

The Timing Memory Board stores high-speed incoming data in a multiplexed static RAM when so directed by the Timing Control Board. Also, using logic-gate comparators, it detects matches of incoming data with keyboard-specified arm and trigger words. Further, when so instructed from the keyboard, it detects and pulse-stretches data glitches for storage and display.

11.2 FUNCTIONAL DESCRIPTION

A block diagram of the Timing Memory Board is shown in figure 11-1. When appropriate during the following discussion, please refer to this figure and to the schematic diagram, board layout, and parts list which are included at the end of this section. Also, tables of connector pins versus signal names for all motherboard connectors are provided in section 15 along with an alphabetical list of all interboard signals. And, should the need arise, a Glossary in section 16 offers explanations for acronyms or terms that may be unfamiliar.

As shown in the block diagram, the major functional units of the Timing Memory Board circuitry are the Processor Interface, the Clock Generator, the Timing RAM, and the Data Comparators. These units are discussed in detail in the following subsections.

11.2.1 Processor Interface

The Processor Interface comprises the Address Decoder, Probe Threshold Control, the Control Port, the Status Port, the Last-Word Address Port, and the Control Shift Register. (Except for the Last-Word Address Port and the Control Shift Register, the Processor Interface is shown on schematic sheet 1. The Last-Word Address Port is shown on sheet 2; and the Control Shift Register is shown partly on sheet 3 and partly on sheet 4.) This circuitry allows the Control Program to set up certain Probe parameters according to keyboard-entered instructions, to send certain control signals when appropriate, and to interrogate various status and signal lines as the need arises.

The Address Decoder consists of: U52, an MMI 6301-1 256-word x 4-bit PROM; U43B, a section of a 74S10 triple 3-input NAND gate (used here as an inverter); and U51, a 74LS138 3-to-8 decoder. When the U52 PROM is enabled by processor control signal RW (Read OR Write), it accepts Processor Address Bus signals A10 through A15 and processor control signals S1 (Read) and IO+/M- (I/O + Memory -) and decodes them to produce the following control signals:

a. RDLAST- (Read Last -), which enables the Last-Word Address Port, U5 on sheet 2

b. RDRAM- (Read RAM-), which places the RAM Address Counter (U54 and U55 on sheet 2) in the load mode so that the processor can preset the counter or address the RAM

c. EN51- (Enable U51 -), which enables the second stage address decoder, U51

When the U51 decoder is enabled by EN51-, it accepts Processor Address Bus signals A0 and A1 and processor control signals IO+/M- and RW and decodes them to produce the following control signals:

d. EORAM0 (Enable Output, RAM 0), EORAM1, EORAM2, and EORAM3, which enable the outputs of RAM sections 0, 1, 2, and 3, respectively

e. LDTHRESHA- (Load Threshold A -) and LDTHRESHB-, which enable the CS- inputs of the U56 and U57 D/A converters in Threshold Control

f. ENSTAT- (Enable Status -), which enables the Status Port, U50

g. ENCTRL- (Enable Control -), which enables the Control Port, U42

The Probe Threshold Control consists of: U56 and U57, AM 6080 8-bit D/A converters; and U58, an LM747 dual operational amplifier. When enabled by LDTHRESHA- from the Address Decoder and WR- from the processor, D/A converter U57 converts a digital value (fed to it from the Processor Data Bus by the Control Program in accordance with keyboard-entered instructions) to an analog voltage. This voltage is fed through operational amplifier U58A to the Model 80 Probe as THRESHA, a threshold reference voltage for the external clock, the qualifier, and data channels 0, 1, 2, and 3. Similarly, U56 and U58B supply THRESHB to the Model 80 Probe for data channels 4, 5, 6, and 7.

Potentiometer R19 is used to set the reference voltage fed to pin 14 of D/A converters U56 and U57. This voltage, as measured at test point TP1, should be 10.0 V, ± 0.05 V.

The Control Port consists of: U42, a 74LS174 hex D flip-flop; Q3, a 2N3905 transistor; and Q7, a 2N3904 transistor. When U42 is enabled by signal ENCTRL-, the following signals are clocked into the flip-flops from the Processor Data Bus:

a. PRSCLKG- (Preset Clock Generator), which presets the four flip-flops in the Clock Generator

b. CLRCLKG- (Clear Clock Generator), which clears the four flip-flops in the Clock Generator

c. SRDATA (Shift Register Data), serial data to be loaded into the Control Shift Register

d. CLKSR (Clock, Shift Register), the clock that loads the Control Shift Register

e. HYSTCTRL (Hysteresis Control), which, when high, adds hysteresis to the comparators in the Model 80 Probe (the transistors Q3 and Q7 supply signal HYST as a nominal level, measured with Probe connected, of +1.7 V when hysteresis is ON or -5.1 V when hysteresis is OFF)

f. DSELT+/W- (Data Select Timing + / Waveform -), fed to the Data Comparator circuits where it is used to select either Timing data from the Model 80 Probe or Waveform data from the Waveform Control Board

The Status Port consists of: U50, a 74LS367 hex bus driver with 3-state outputs; and Q4, a 2N3904 transistor. When the U50 outputs are enabled by ENSTAT-, this circuitry allows the processor to read the following signals:

a. CLKPH0-—CLKPH3- (Clock, Phase 0—3), which, when read at clock shutoff time, permit the Control Program to determine which of the four RAM sections contains the last data word collected

b. ROLLOVER, which indicates that the memory has been filled (at least once) and has started overwriting prior collected data with new

c. ENDSRD (End Shift Register Data), which is the content of the last bit in the Control Shift Register chain, permitting the Control Program to determine the status of serial data SRDATA as it is shifted through the registers (Q4 translates the level from CMOS to TTL)

The Last-Word Address Port (see schematic sheet 2) consists of U5, a 74LS244 octal buffer with 3-state outputs. The inputs of this buffer are connected to the Address Counter, and the outputs are connected to the Processor Data Bus. The outputs are enabled by RDLAST-, which is sent from the Address Decoder after clock shutoff. When thus enabled, this port allows the Control Program to read the contents of the Address Counter, which still contains the last memory address into which collected data was stored. This address, in conjunction with the status of the 4-phase clock, provides the orientation point for the Control Program's processing of the collected data. (For example, counting back from this point by the posttrigger count establishes the location of the stored trigger word.)

The Control Shift Register consists of: U7, U8, and U23 (on schematic sheet 4), and U10 and U12 (on sheet 3), all CMOS 4015 dual 4-bit static shift registers; and Q1 and Q2 (on sheet 3), both 2N3905 transistors. Q1 and Q2 translate Control Port signals CLKSR and SRDATA from TTL level to CMOS level. Shift Register sections U7, U8, U10, and U12 transmit software-generated control signals to the Arm- and Trigger-Bit Comparators, which detect data match with keyboard-specified arm and trigger words. Shift Register section U23 transmits software-generated control signals to the Data Selectors, which select either Timing data or Waveform data for storage in the Timing RAM.

11.2.2 Clock Generator

The Clock Generator (see schematic sheet 1) consists of: U59 and U60, both 74S74 dual D flip-flops; and U43C, a section of a 74S10 triple 3-input NAND gate. This circuitry provides a 4-phase clock to the Timing RAM.

The four flip-flops are connected in cascade, with all preset inputs fed in parallel by PRSCLKG- and all clear inputs fed in parallel by CLRCLKG- (the preset and clear signals both come from the Control Port). The flip-flops are

all clocked by CLKTTL from the Timing Control Board. The 4-phase clock outputs are taken from the Q- side of the flip-flops.

The Clock Generator is started in the preset condition, with the D input of the first flip-flop held low by the output of gate U43C. Feedback around the first flip-flop, U59A, would normally produce a divide-by-two. But the feedback is held off by the 3-input NAND gate, U43C, for three CLKTTL clock periods until the Q-low pulse has rippled down to the third flip-flop, U60A. (Please refer to figure 11-2.) The result is an asymetrical divide-by-four operation for each flip-flop, producing the set of output clock signals shown in the figure. The clock pulse from the Q- output of each succesive flip-flop is delayed from that of the preceding flip-flop by one CLKTTL period.

This 4-phase clock is fed to the Timing RAM sections as CLKPH0-, CLKPH1-, CLKPH2-, and CLKPH3-, with one clock phase going to each of the four sections. An additional clock, CLKPH0+, is taken from the Q output of U59A and fed to the Address Counter. (The application of these clocks will be discussed in the next subsection.)

11.2.3 Timing RAM

The Timing RAM (see schematic sheet 2) comprises the Address Counter, the Rollover Detector, and Timing RAM Sections 0, 1, 2, and 3. Each of the four RAM sections can store 256 8-bit words, thus the total storage capacity is 1024 8-bit words. (The memory is arranged in sections in a strategy that allows 45-ns RAMs to store data that is being clocked into the analyzer at intervals as short as 20 ns.)

Under the direction of the Control Program, the Timing RAM is used to store 1000 8-bit words of data sent from the Data Comparators. (Although the full memory capacity is 1024 words, the posttrigger count is adjusted so that only 1000 words are collected.) The data from the Comparators may have come from either the Model 80 Probe (as Timing data) or the Wavefrom Control Board (as Waveform data). After collection, data stored in the Timing RAM may be read by the Control Program for analysis and display.

The Address Counter consists of: U54 and U55, both 74LS191 4-bit binary counters; and U43A, a section of a 74S10 triple 3-input NAND gate (used here as an inverter). The two counters are wired to count up and are connected in cascade (through U43A) so as to produce an 8-bit output. This output is fed to the input of the U4 Address Latch of Timing RAM Section 0 and to the Last-Word Address Port.

The counter's load-control inputs are fed by RDRAM- from the Address Decoder. When RDRAM- is low, the counter outputs follow the inputs. This mode is used by the Control Program to preset the counter to 000 before data collection starts and to address the Timing RAM when reading data after collection stops. The counter's clock inputs are fed by CLKPH0+ from the Clock Generator, and clocking occurs on the positive-going edge of this signal. When data collection begins, the Address Counter starts counting from 000 and advances the address one count with each CLKPH0+ clock. The maximum count is 256 (including 000 as a count), the memory capacity of one section of the Timing RAM. If clocking continues beyond this point, the counter overflows

and starts over again from 000. Counting stops when the CLKTTL input clock to the Clock Generator is stopped by the Timing Control Board.

The Rollover Detector consists of U53B, 1/2 of a 74LS73 dual J-K flip-flop. This circuit detects the first occurrence of overflow of the Address Counter.

The J input of the flip-flop is wired high, and the K input is wired low. Therefore, once set, the flip-flop will not change state again until reset by a low signal to the clear input, pin 6. The flip-flop is clocked by the MSB, RA7, of the Address Counter, and clocking occurs on the negative-going edge of this signal. As maximum address count is approached, the MSB of the counter goes high. At counter overflow, the MSB goes low again, and this transition clocks the flip-flop. The signal used to clear the flip-flop is PRSCLKG- from the Control Port, the same signal that is used to preset the Clock Generator. Thus, before the start of data collection, the Rollover Detector is automatically cleared at the same time the Clock Generator is initialized.

The output of the flip-flop, signal ROLLOVER, is fed to the Status Port where it can be accessed by the Control Program. The state of the Rollover Detector after data collection has stopped is used by the Control Program in determining the exact location of the trigger word in the Timing RAM.

Timing RAM Section 0 consists of: U16 and U29, both Fairchild 93422 256-word x 4-bit static RAMs with 3-state outputs; Address Latch U4, a 74S373 octal D latch; and Data Flip-Flop U41, a 74S374 octal D flip-flop. This circuitry stores 256 8-bit words of collected data.

The address inputs of the two RAMs are connected in parallel to the outputs of the U4 Address Latch. The inputs of the Address Latch are connected to the outputs of the Address Counter, signals RA0 (RAM Address bit 0) through RA7. The 4-bit data inputs of the two RAMs are connected in cascade to the 8-bit output of the U41 Data Flip-Flop. The inputs of the Data Flip-Flop are connected to the onboard Timing Data Bus, signals TDB0 (Timing Data Bus bit 0) through TDB7. The 4-bit data outputs of the two RAMs are connected in cascade to the 8-bit Processor Data Bus, signals DB0 (Data Bus bit 0) through DB7. The output-enable inputs of the two RAMs are fed in parallel by signal EORAM0- from the Address Decoder. The phase-0 clock signal, CLKPH0- from the Clock Generator, is fed to the following points: The two RAM write-enable inputs, U16-20 and U29-20; the Address Latch enable, U4-11; and the Data Flip-Flop clock input, U41-11.

Timing RAM Section 1 consists of RAMs U15 and U28, Address Latch U3, and Data Flip-Flop U40. (Integrated circuit types are the same for all four RAM sections.) The address inputs of the two RAMs are connected in parallel to the outputs of the U3 Address Latch. The inputs of the Address Latch are connected, not to the outputs of the Address Counter, but to the outputs of the U4 Address Latch in Section 0. The other connections of this section are similar to those of Section 0, except that the enable signal from the Address Decoder is EORAM1- and the clock signal from the Clock Generator is CLKPH1-.

Timing RAM Section 2 consists of RAMs U14 and U27, Address Latch U2, and Data Flip-Flop U39. The connections of this section are similar to those of Section 1, except that the inputs of the U2 Address Latch are connected to the

outputs of the U3 Address Latch in Section 1, the enable signal is EORAM2-, and the clock signal is CLKPH2-.

Timing RAM Section 3 consists of RAMs U13 and U26, Address Latch U1, and Data Flip-Flop U38. The connections of this section are similar to those of Section 2, except that the inputs of the U1 Address Latch are connected to the outputs of the U2 Address Latch in Section 2, the enable signal is EORAM3-, and the clock signal is CLKPH3-.

As just described, the address inputs to the RAM sections are connected in an unclosed loop: from the Address Counter to the Section-0 Address Latch; from the Section-0 Address Latch to the Section-1 Address Latch; from the Section-1 Address Latch to the Section-2 Address Latch; and from the Section-2 Address Latch to the Section-3 Address Latch. The reason for making the connections in this way will become apparent as we proceed.

A typical data collection cycle occurs as follows (please refer to figure 11-2, the Clock Generator Timing Diagram). Data word AA on the Timing Data Bus (clock time marked at top of diagram) is clocked into the U41 Section-0 Data Flip-Flop by the positive-going edge of CLKPH0- (point A on the diagram). (This data is held in U41 until the next positive-going clock edge at point L.) Address AAA, the current address count, was set up in the Address Counter by CLKPH0+ at point J. This address is latched in the U4 Section-0 Address Latch by the low level occurring at the negative-going transition of CLKPH0- (point B on the diagram). (The address is held latched for the duration of the low level.)

The Address Counter is advanced one count by the positive-going edge of CLKPH0+ (point K on the diagram). Although this point coincides with the address-latch point, B, propagation times are such that the new address, LLL, does not reach the Section-0 Address Latch until after the current address, AAA, has been latched. The write enable inputs of the Section-0 RAMs are also brought low at point B. This write enable pulse lasts till the next positive-going transition of CLKPH0- at point L, and the data and address inputs are both held stable for the duration of this pulse.

(In regard to the timing specifications for the 93422 RAMs: The minimum write-pulse length, specified as 30 ns, is always exceeded. Even with the minimum CLKTTL period of 20 ns, the write-pulse width is 3 x 20 ns = 60 ns. Also, the data is clocked into the Data Flip-Flop one CLKTTL period ahead of the write pulse, so the data set-up time is at least 20 ns, four times the specified 5 ns minimum. And although the address is latched in the Address Latch on the same clock transition that starts the write pulse, the address has been stable as seen through the transparent latch for much longer than the required 10 ns; actually about 50 ns minimum in the Address Counter for the Section-0 RAMs, and 20 ns minimum in the preceding Address Latch for the RAMs in the other sections.)

At point C, the positive-going edge of CLKPH1- clocks data word CC into the Section-1 Data Flip-Flop, U40. (Data has changed since point A because the data is being fed to the Data Flip-Flops, connected in parallel to the onboard Timing Data Bus, at CLKTTL rate.) At point D, the AAA address being held in the Section-0 Address Latch is latched into the Section-1 Address Latch by the low level of CLKPH1-. (Note that although a count increment has

been started in the Address Counter, address AAA can still be used by Sections 1, 2, and 3 because of the series loop connection of the Address Latches.) The write enable inputs of the Section-1 RAMs are also brought low at point D, thus storing word CC.

We now have data word AA written into the Section-0 RAMs at address AAA and data word CC written into the Section-1 RAMs at address AAA. In the same way, with data clocked at point E and address latched at point F, data word EE is written into the Section-2 RAMs at address AAA. Similarly, data word GG is written into the Section-3 RAMs at address AAA.

At the next clock pulse of CLKPH0-, L-M, the next sequential address LLL is stable at the Address Counter output and is latched in Section-0 Address Latch, U4. The next set of four data words is written into the four RAM sections at address LLL, starting with data word LL in the Section-0 RAMs.

Each address therefore stores four consecutive data words, one in each RAM section. And each RAM section stores every fourth data word in consecutive addresses. When the Address Counter has reached maximum count, each RAM section contains 256 data words, for a total of 1024 data words interlaced in the four RAM sections. At the next CLKPH0+, the Address Counter overflows and starts over again at address 000. Of course, data collection may end at any address count and on any one of the 4-phase clock pulses.

At the end of data collection (posttrigger terminal count), CLKTTL stops, which in turn stops the Clock Generator. This stops the Address Counter and leaves all Timing RAM Address Latches and Data Flip-Flops in the state they were in at the last memory write. The Control Program reads the Last-Word Address Port to find the address of the last word stored. It also reads, from the Status Port, the state of the four flip-flops in the Clock Generator to find which RAM section stored the last word at that last address. It can then determine the address and RAM section for any desired stored data word.

At any time after the CLKTTL has stopped, the Control Program can read data words from the Timing RAM by bringing the Address Counter load control lines low with signal RDRAM- from the Address Decoder. In this load mode, the Address Counter passes incoming addresses from the Processor Address Bus straight through to the Section-0 Address Latch, U4. The Control Program also clears the Clock Generator flip-flops with CLRCLKG- from the Control Port. This brings all clock outputs to the RAM Address Latches high so that all four Address Latches are held in the transparent mode.

Therefore, when the Control Program places an address on the Processor Address Bus, that address goes through the Address Counter to all four Address Latches in the loop, and all four RAM sections are addressed simultaneously. Then the Control Program, knowing the RAM section that contains the word it wants to read, selects that RAM section by activating the proper RAM output-enable line (one of EORAM0- through EORAM3-) via the Address Decoder.

11.2.4 Data Comparators

There are 8 Data Comparators, one for each of 8 parallel incoming data lines. The incoming data may be from the Waveform Control Board or from the

Model 80 Probe. If it is from the Waveform Control board, the data only goes through the Data Selector (which selects Waveform or Timing data) and the ECL-to-TTL translator. On the other hand, if it is from the Model 80 Probe, the data is acted upon by two comparator functions. The first of these detects any glitch in the data; the second detects any match with a corresponding arm- or trigger-word bit.

> NOTE: A glitch is defined, from the viewpoint of the PI 540 Timing Analyzer, as a pulse on the data line that exceeds the selected voltage threshold but is shorter than the selected Timing Analyzer clock period. From the viewpoint of the user, a glitch might be defined as a pulse shorter than the normal data period or target-system clock period. But with the Timing Analyzer clock period usually 10 or more times shorter than the incoming data period, many such user-defined glitches are simply processed as data and are therefore displayed to the user without requiring the use of the Timing Analyzer's glitch-capture mode.

The selection of either the glitch-capture mode or sample mode of data input is made on a line-by-line basis by menu-prompted keyboard entries. The Data Comparators make it possible for the Control Program to turn glitch capturing on or off for each incoming data line in accordance with these keyboard-entered selections.

Data Comparator 0 (schematic sheet 4) consists of: U48B,C, sections of a 10102 quad NOR gate; U47A, 1/2 of a 10130 dual latch; U36B, 1/2 of a 10131 dual master-slave, positive-edge clocked, type D flip-flop; U19, a 10117 dual 2-3-input OR-AND/OR-NOR gate (used here as a 2-wide OR-NOR gate); U31A, 1/4 of a 10158 quad 2-input multiplexer; and U30A, 1/4 of a 10125 quad ECL-to-TTL translator. This circuitry performs the data comparator and data selection functions for data bit 0.

Data Comparators 1 through 7 (schematic sheets 3 and 4) are identical to Data Comparator 0 in every respect except for the U-numbers of ICs and the signal names of incoming and outgoing signals.

The following description of the function of Data Comparator 3 can be applied to the other seven Comparators as well. (During the discussion, please refer to figure 11-3, an expanded schematic of Data Comparator 3, and to figure 11-4, a Data Comparator timing diagram that illustrates the operation of the sample and glitch-capture modes.)

Timing data from the Model 80 Probe comes in to the Comparator in differential form—that is, as two signals of opposite polarity, here labeled D3+ and D3- (figure 11-3). D3+ is fed to the D input of Data Latch U37B. The common clock input, C-, for the U37 dual latch is left unconnected and is pulled low internally. The two latches in U37 are therefore controlled independently by their individual CE- inputs. The CE- input of U37B is fed with signal D3G+/S- (Data Bit 3, Glitch + / Sample -) from the U23 section of the Control Shift Register (schematic sheet 4).

If the sample mode has been keyboard-selected for Data Bit 3, the Control Program holds the CE- input of latch U37B low with signal D3G+/S-.

When the CE- input is low, the set and reset inputs of U37B are inhibited and the Q output follows the D input. In the sample mode, therefore, Data Latch U37B has essentially no effect and the Timing data is fed straight through to the D input of Data Flip-Flop U32A. U32A is a master-slave, type D flip-flop which is clocked by the positive-going edge of the clock signal. The U32A clock input is fed with signal CT (Clock, Timing), which comes from Clock Control on the Timing Control Board (via U44A, 1/3 of a 10216 triple line receiver shown on schematic sheet 4).

The CT clock is keyboard-selected as either external or internal; and, if the clock is internal, the clock period is also keyboard-selected. For Timing analysis, the clock is usually selected as internal, and the clock period is usually selected to be shorter than that of the data by a factor of at least 10 in order to obtain adequate resolution.

Figure 11-4a shows the Q output of U32A with U37B in the sample mode and with hypothetical D3+ data and CT clock inputs. Due to space constraints, the clock period in figure 11-4 is only about 5 times the D3+ data period, which does not meet the rule-of-thumb that calls for a factor of 10. The offset of the data transitions in the U32A-Q output relative to those in the D3+ input illustrates the resolution problem. Also notice that in the sample mode the two glitches (at points A and B), which are shorter than the clock period and fall in between positive-going clock transitions, do not appear in the output.

If the glitch-capture mode has been keyboard-selected for Data Bit 3, the Control Program holds the CE- input to U37B high with signal D3G+/S-. When the CE- input is high (which is the latched mode), the D input has no effect and U37B responds only to the set and reset inputs. The outputs of Comparator Gates U49C and U49D are connected to the U37B set and reset inputs, respectively. D3- and the U32A Q output are connected to the inputs of gate U49C; while D3+ and the U32A Q- output are connected to the inputs of gate U49D.

With these connections, Comparator Gate U49C detects any positive-going transitions in D3+ (actually, U49C detects negative-going transitions in D3-) and Comparator Gate U49D detects any negative-going transitions in D3+. Thus, any positive-going transition in D3+ (whether by data or glitch) sets latch U37B; and any negative-going transition in D3+ resets latch U37B. The U37B Q output is clocked into flip-flop U32A the same as it was in the sample mode.

> NOTE: The ECL devices used in the Comparator circuits are fast enough so that any glitch pulse $\geq$5 ns long will be detected.

The hypothetical D3+ and CT inputs in figure 11-4a are used again in figure 11-4b to illustrate the glitch-capture mode. Notice that the set-reset action of the Comparator Gates produes a signal at the Q output of U37B that is almost identical to the D3+ signal except that the trailing edge of any glitch is stretched to the next positive-going clock edge. This stretching results in the glitch being clocked into the U32A flip-flop as intended. The response of U32A to this clocking causes termination of the stretched glitch pulse in U37B, which in turn causes the reproduced glitch pulse in U32A to be terminated after one clock period. If the clock period is qualified by Clock Control for data collection, the glitch will be stored in the Timing RAM as a signal that is one clock period long.

In the figure, the D3+ signal is redrawn just below the Q output of U32A for ease of comparison. Again notice how the resolution deficiency causes a marked offset of the U32A output data signal relative to the D3+ input data signal. Of course, regardless of resolution, a captured glitch will always be offset from the input glitch by the time interval from the leading edge of the input glitch to the next positive-going clock edge.

Now that we have established a clocked and stable data input signal (representing D3+) at the Q and Q- outputs of Data Flip-Flop U32A, we can take up the operation of the Arm- and Trigger-Bit Comparator Gates. The upper OR gate of the U9B Arm-Bit Comparator Gate is fed with the Q output of U32A and with software-generated signal AW3B1- (Arm Word 3-Bit selected as 1 -); and the lower OR gate of U9B is fed with the Q- output of U32A and with signal AW3B0-. (These AW3B signals are software generated in accordance with keyboard selection and come from the U8 section of the Control Shift Register in the Processor Interface.) The output of the NAND gate in U9B is connected in a wired AND with the outputs of the other seven Arm-Bit Comparator Gates (all seven Comparator Gate outputs must be low in order to produce a low TA- output signal).

If arm-word bit 3 was keyboard-specified as a 1 (high), the Control Program holds signal AW3B1- low (true) and signal AW3B0- high; but if arm bit 3 was specified as a 0, the Control Program holds AW3B1- high and AW3B0- low. If arm bit 3 was specified as X (don't care), the Control Program holds both AW3B1- and AW3B0- high.

Assume that arm bit 3 was specified as a 1. Signal AW3B0- will be high, and the lower OR gate of U9B will always have a high output regardless of the data input. This leaves the upper OR gate in control of the U9B NAND gate output. Signal AW3B1- will be low, and as long as U32A-Q (which reflects D3+) is low, the output of the upper OR gate will be low and U9B-14 will be high (false), thereby holding the wired AND for signal TA- high. But if U32A-Q goes high, thus satisfying the requirement for arm bit 3, the output of the upper OR gate will go high, causing U9B-14 to contribute a low to the wired AND for TA-. If the outputs of the Arm-Bit Comparator Gates for the other seven data bits are also low, TA- will be low, indicating that an arm-word match has occurred.

By the same reasoning, if arm bit 3 was specified as a 0 and U32A-Q- goes high (indicating that D3+ is low), U9B-14 will contribute a low to the wired AND for TA-. Finally, if arm bit 3 was specified as an X, the output of both OR gates will always be high (because both AW3B1- and AW3B0- are high) and U9B-14 will constantly contribute a low to TA-.

If the glitch-capture mode is in effect, captured glitches will have the same effect as data on the operation of the Arm-Bit Comparator Gate. For example, if arm bit 3 was specified as a 1, the glitch at point A in figure 11-4b will cause a low output at U9B-14 for one clock period. Such spurious bit matches can be prevented by a keyboard-specified arm-word filter setting of 2 (designating that the arm-word match must be present at least 2 clock periods in order to be acted upon).

However, filter settings greater than 2 must be used with caution when the signal period is less than 10 times the clock period. For instance,

consider the situation shown in the U32A-Q output in figure 11-4b if the arm bit was specified as 0 and the filter setting was 3. Under these conditions, the expected match of the bit containing glitch A is masked due to interruption of the bit's low level by the captured glitch. The low portions of the bit that are on either side of the high glitch are not 3 clock periods and are therefore filtered out. A filter setting of 2, however, would filter out the glitch and still let the remainder of the bit through.

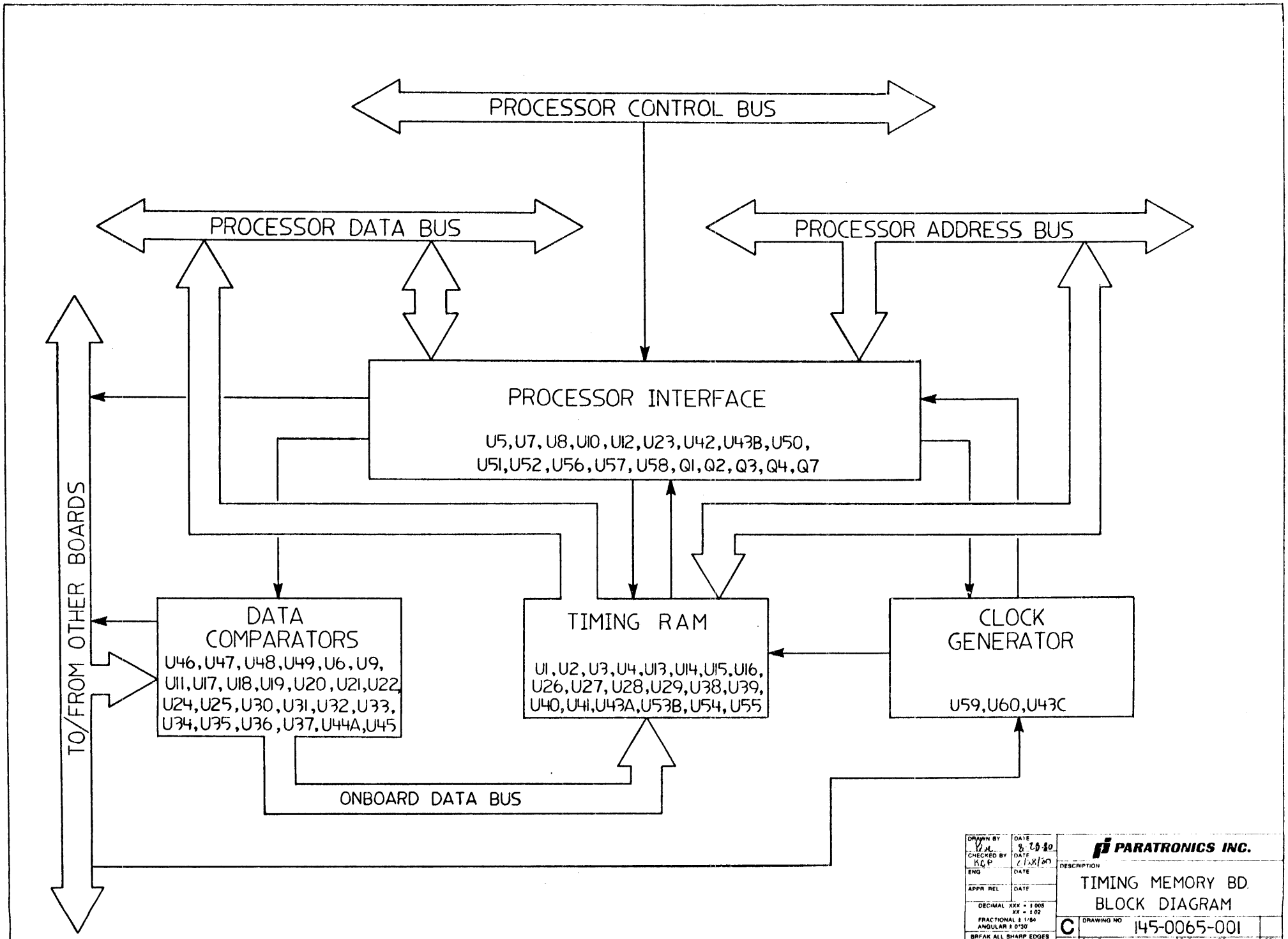
> NOTE: Keep in mind that the filtering action affects only the arm- and trigger-word match function, not the storage and display of collected data. (Refer to the Trigger Filter circuit shown on Timing Control schematic sheet 3.)

The Trigger-Bit Comparator Gate operates in exactly the same way as the Arm-Bit Comparator Gate; and the output of U9A is connected in a wired AND with the outputs of the other seven Trigger-Bit Comparator Gates.

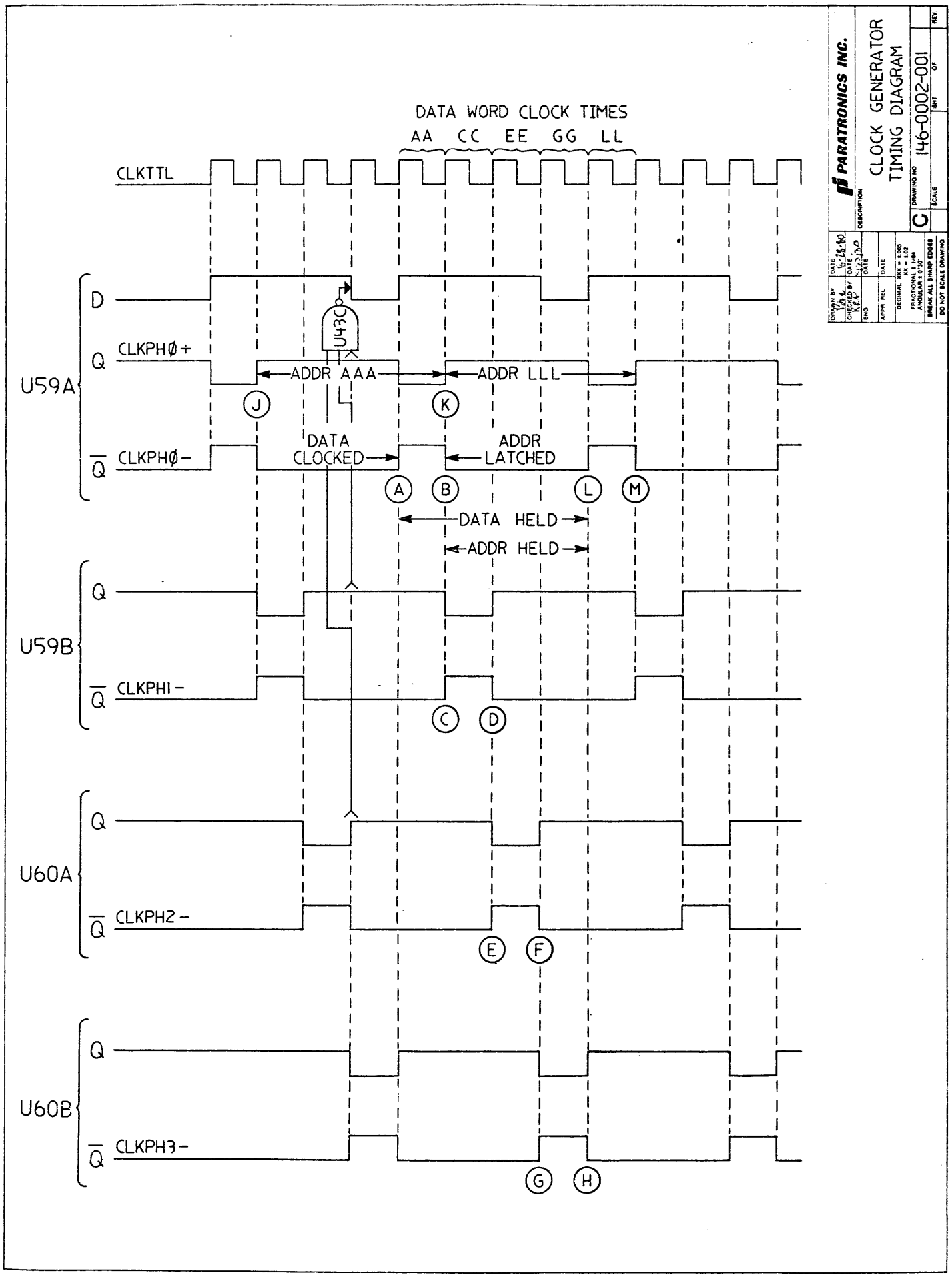
The Data Selector, U31D, is used by the Control Program to select either Timing data or Waveform data for storage in the Timing RAM. Bit-3 Timing data is fed from U32A-Q to input B of U31D; and bit-3 Waveform data (signal WD3) is fed from the Waveform Control Board through connector pin S2-50 to input A of U31D. Signal DSELT+/W- (Data Select Timing + / Waveform -) is used by the Control Program to select one input or the other as output to the level translator U17C. The output of U17C feeds the TDB3 (Timing Data Bus bit 3) line of the onboard Timing Data Bus that is connected to the inputs of the Data Latches in the Timing RAM sections.

11.3 SCHEMATIC, BOARD LAYOUT, & PARTS LIST

The schematic diagram, board layout, and parts list for the Timing Memory Board are contained on the following pages.



DRAWN BY	DATE 8 20 80	PARATRONICS INC.	
CHECKED BY KCP	DATE 8/28/80	DESCRIPTION	TIMING MEMORY BD. BLOCK DIAGRAM
ENG	DATE		
APPR REL	DATE		
DECIMAL XXX = ±.005 XX = ±.02		C	DRAWING NO 145-0065-001
FRACTIONAL ± 1/64 ANGULAR ± 0°30'			
BREAK ALL SHARP EDGES		SCALE	SHT OF REV
DO NOT SCALE DRAWING			


DATA WORD CLOCK TIMES
AA CC EE GG LL
CLKTTL
U59A
D
Q
CLKPHØ+
U43C
ADDR AAA
ADDR LLL
J
K
Q
CLKPHØ-
DATA CLOCKED
ADDR LATCHED
A
B
L
M
DATA HELD
ADDR HELD
U59B
Q
Q
CLKPHI-
C
D
U60A
Q
Q
CLKPH2-
E
F
U60B
Q
Q
CLKPH3-
G
H
PARATRONICS INC.
CLOCK GENERATOR TIMING DIAGRAM
DRAWING NO 146-0002-001
REV
SCALE
SHT OF
DRAWN BY
CHECKED BY
ENG
APPR MEL
DATE
DESCRIPTION
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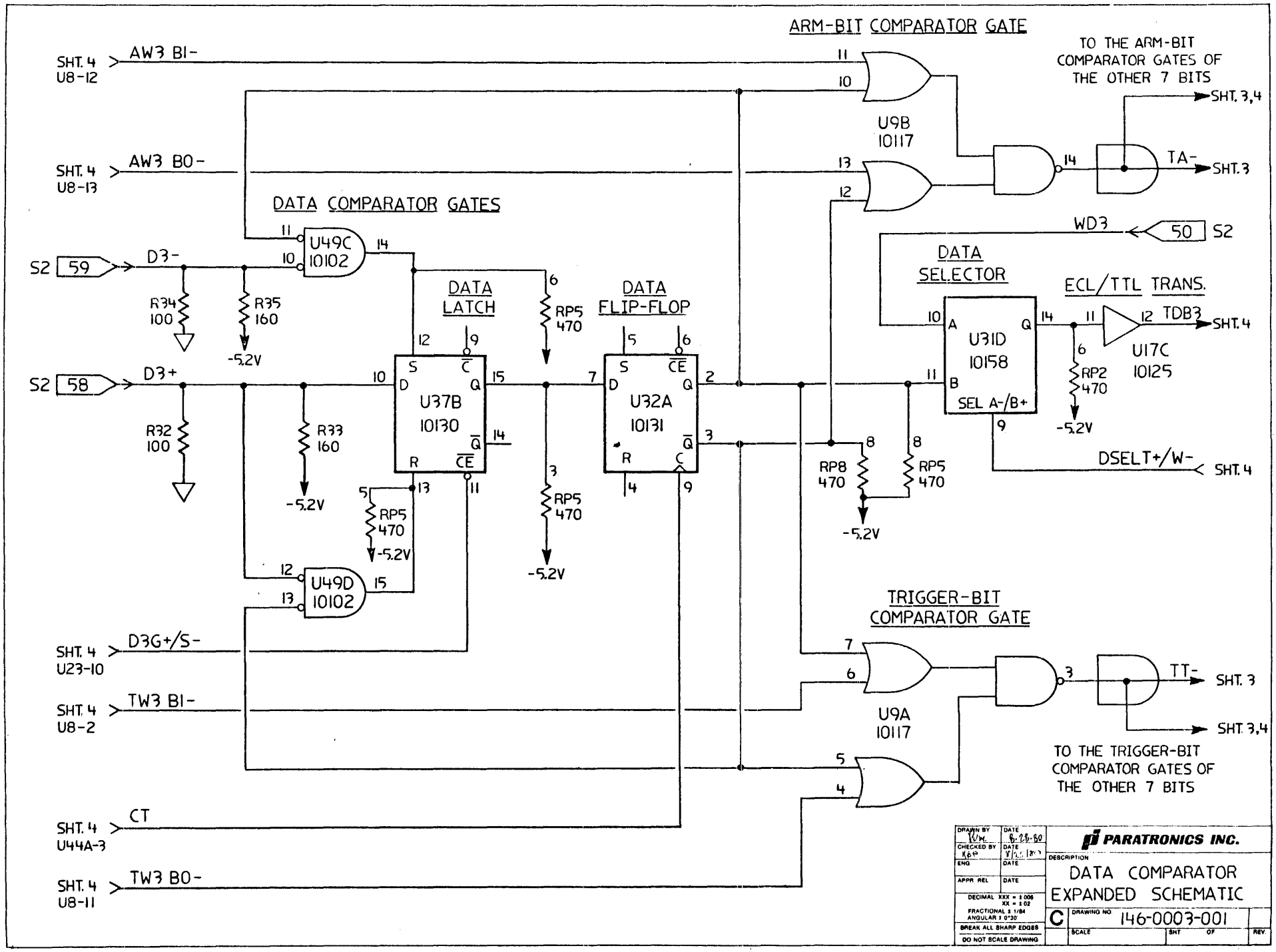
FRACTIONAL ± 1/64
ANGULAR ± 0°30'
BREAK ALL SHARP EDGES
DO NOT SCALE DRAWING



DRAWN BY	DATE	PARATRONICS INC.	
CHECKED BY	DATE	DESCRIPTION	
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APPR REL	DATE		
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FRACTIONAL ± 1/64 ANGULAR ± 0°30'			
BREAK ALL SHARP EDGES		SCALE	SHT OF REV.
DO NOT SCALE DRAWING			

PARATRONICS INC.

DESCRIPTION: DATA COMPARATOR TIMING DIAGRAM

DRAWING NO: 146-0001-001 REV

SCALE SHT OF

DRAWN BY DATE 8-28-86

CHECKED BY DATE

ENG DATE

APPR REL DATE

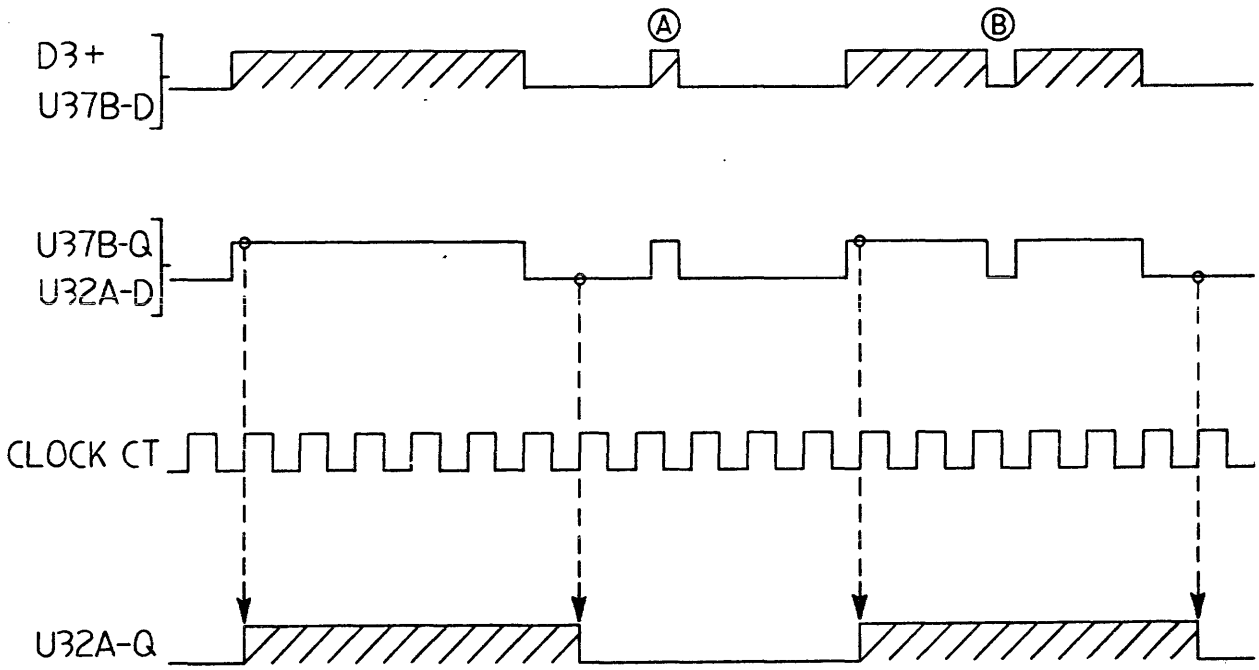
DECIMAL XX = ± .005, XXX = ± .002

FRACTIONAL ± 1/64

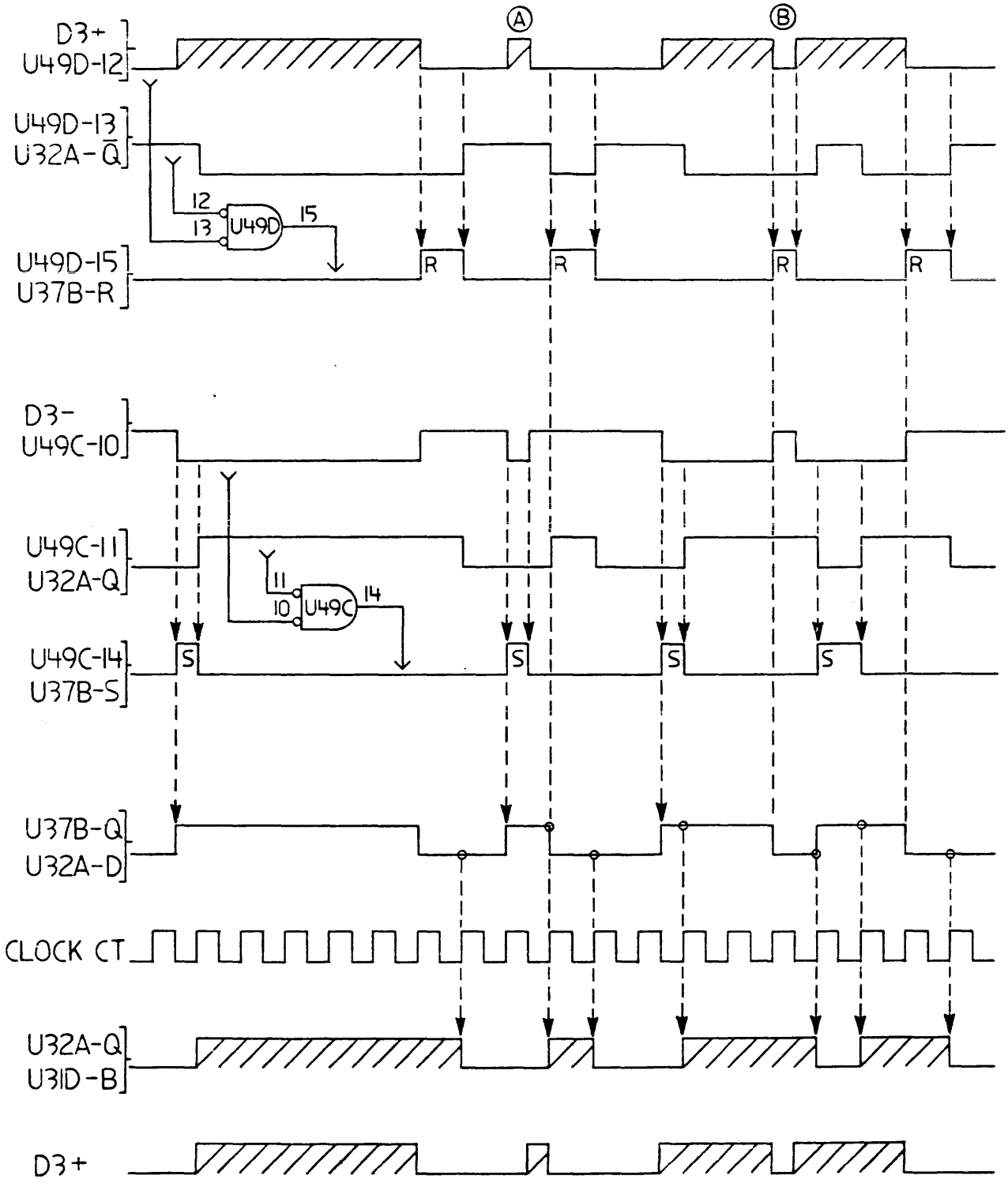
ANGULAR ± 0°30

BREAK ALL SHARP EDGES

DO NOT SCALE DRAWING



SAMPLE MODE



GLITCH-CAPTURE MODE

PARATRONICS INC.

DESCRIPTION: DATA COMPARATOR TIMING DIAGRAM

DRAWING NO: 146-0001-002

REV: C

SCALE

SHT 05

DRAWN BY: [illegible] DATE: 8-26-80

CHECKED BY: KLT DATE: 8/27/80

ENG

APPR MFG DATE

DECIMAL XXX = ±.005 XX = ±.02

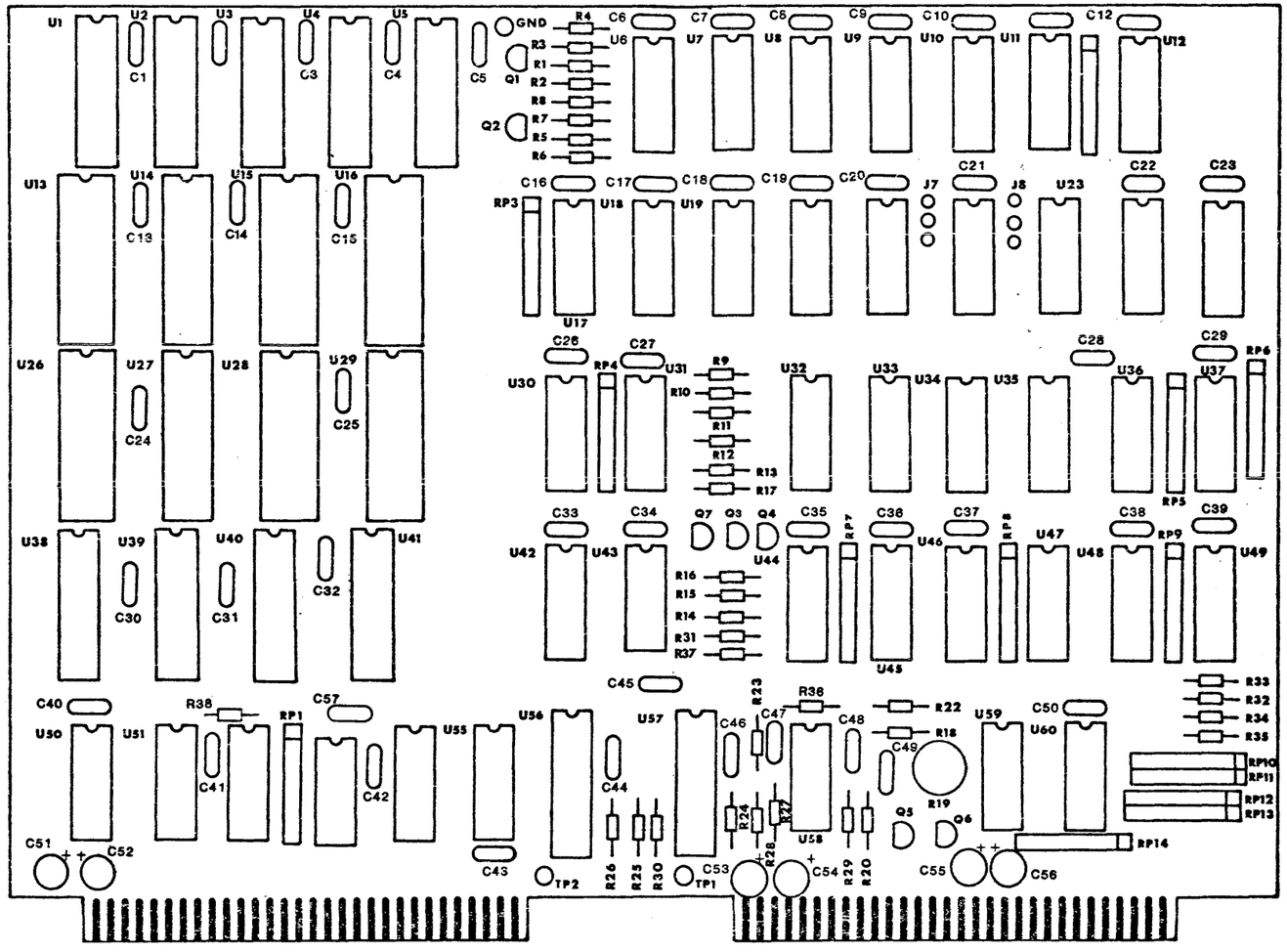
FRACTIONAL = 1/64

ANGULAR = ±1°

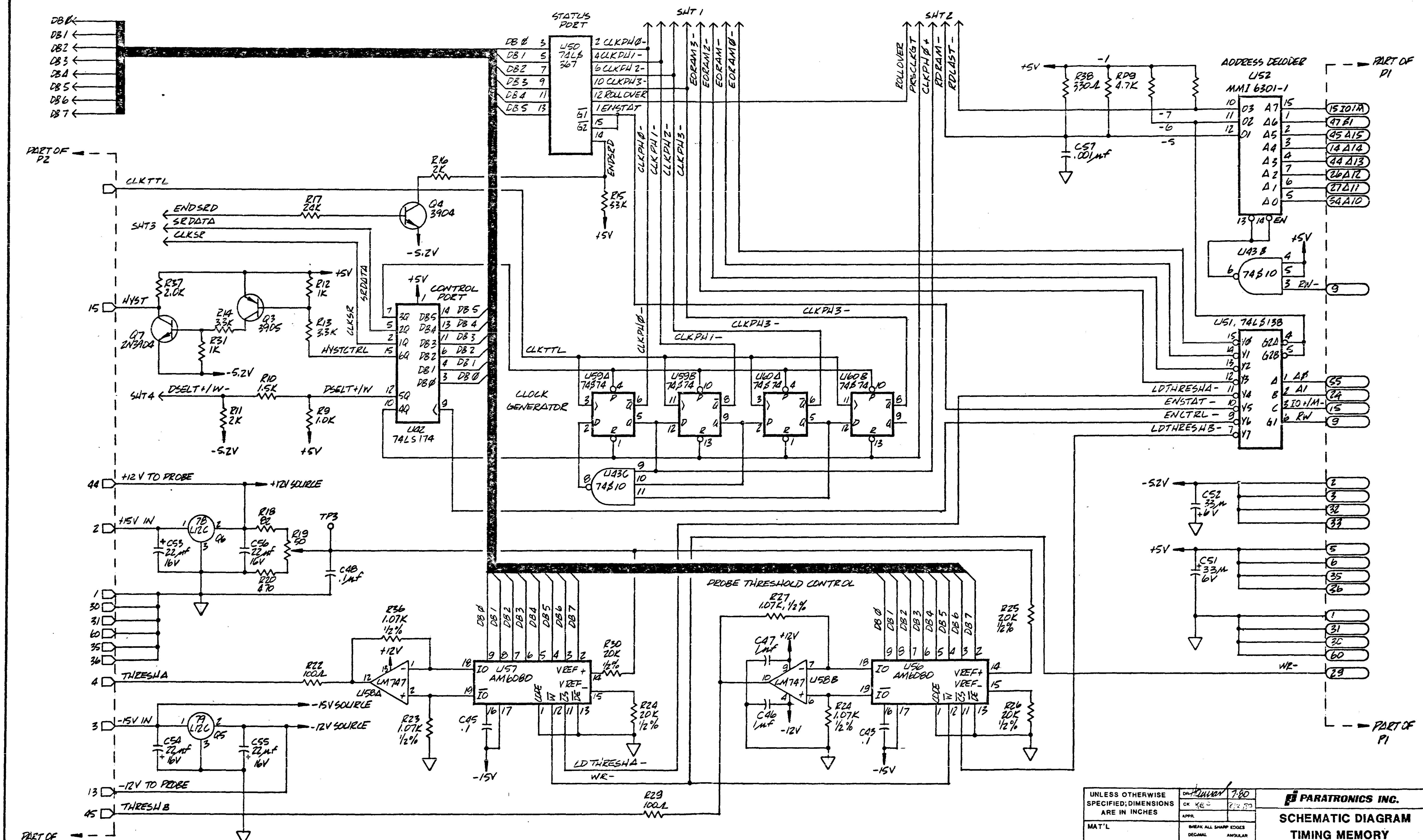
BREAK ALL SHARP EDGES

DO NOT SCALE DRAWING

REV	DESCRIPTION	DATE	APPROVED
B	REV PER ECO 095	2-14-85	



DRAWN BY	DATE 5-25-79	PARATRONICS INC.	
CHECKED BY	DATE	DESCRIPTION	
ENG	DATE	LEGENDMASTER	
APPR. REL	DATE	TIMING MEMORY	
DECIMAL .XXX = ±.005 .XX = ±.02			
FRACTIONAL ± 1/64 ANGULAR ± 0°30'		D	DRAWING NO 126-0065-201 B
BREAK ALL SHARP EDGES			SCALE 2/1 SHT 1 OF 1 REV.
DO NOT SCALE DRAWING			



UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR / CK / APPR. — 7-80	**PARATRONICS INC.**
MAT'L	BREAK ALL SHARP EDGES; DECIMAL / ANGULAR	SCHEMATIC DIAGRAM TIMING MEMORY
FINISH	DO NOT SCALE DRAWING	DRWG NO 127-0065-001 · REV. B · D · SHT 1 OF 4

TIMING RAM SECTION 2

TIMING RAM SECTION 1

TIMING RAM SECTION 3

TIMING RAM SECTION 8

TIMING DATA BUS

ROLLOVER DETECTOR

ADDRESS COUNTER

LAST WORD ADDRESS PORT

PART OF P1

PART OF P1

TO SHT 3

TO SHT 1

TO SHT 1

EDRAM3

EDRAM8

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR HAMMAN		PARATRONICS INC.
	CK [illegible]		SCHEMATIC DIAGRAM TIMING MEMORY
MAT'L	APPR.		
	BREAK ALL SHARP EDGES DECIMAL ANGULAR XX = ± XXX = ±		
FINISH	DO NOT SCALE DRAWING		DRWG NO 127-0065-001 REV. D SCALE SHT 2 OF 4

PART OF P2

WD2
D2-
D2+
WD8

DATA COMPARATOR Ø

DØ-
DØ-

WD3
D3-
D3+
WD-1

DATA COMPARATOR 1

D1-
D1+

CT

PART OF P2

N.C.

RP14 470 -5.2V
RP11 100
RP10 160 -5.2V
RP8 470 -5.2V
RP7 470 -5.2V
RP4 470 -5.2V

U46C 10102
U47A 10130
U36B 10131
U48B 10102
U19B 10117
U31B 10158
U19A 10117
U30A 10125
RP3 470 -5.2V
TDBØ
TA-
TT-
AW6B0
AW6B1
TW6B0
TW6B1
DØG+/S
DSELT+/W-

U46A 10102
U47B 10130
U36A 10131
U48D 10102
U6B 10117
U31C 10158
U6A 10117
U30B 10125
RP3 470 -5.2V
TDB1
TW1B0
TW1B1
AW1B0
AW1B1
D1G+/S

RP11,100
RP14 470
RP11 100
RP12 160 -5.2V
RP8 470 -5.2V
RP4 470 -5.2V
RP5 470 -5.2V
RP2 470 -5.2V

DATA COMPARATOR 2

U49A 10102
U37A 10130
U32B 10131
U49B 10102
U20B 10117
U31A 10158
U20A 10117
U17B 10125
RP2 470 -5.2V
TDB2
AW2B0
AW2B1
WD2

R35, 160 -5.2V
R34 160
R32 100
RP14 470 -5.2V

DATA COMPARATOR 3

U49C 10102
U37B 10130
U32A 10131
U49D 10102
U9B 10117
U31D 10158
U9A 10117
U17C 10125
RP2 470 -5.2V
TDB3
R33 360 -5.2V
RP5 470 -5.2V
RP8 470 -5.2V
AW3B0
AW3B1-
WD3

U7, CD4015
U23, CD4015
U8 CD4015
CLKSEL
CKT1
CT
TA-
TT-
DSELT1N-
SDATA1
SDATA0
TDB0
D1G+/S
D2G+/S
D3G+/S
D4G+/S
TW3B1-
TW3B0-
AW3B0-
AW3B1-
TW2B0-
TW2B1-

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR Hallman 6/80	PARATRONICS INC.	
	CK KLP 7/23/80	SCHEMATIC DIAGRAM TIMING MEMORY	
MAT'L	APPR		
	BREAK ALL SHARP EDGES DECIMAL ANGULAR XX = ± ± XXX = ±		
FINISH	DO NOT SCALE DRAWING	DRWG NO 127-0065-001	REV.
		D SCALE	SHT 3 OF 4

PART OF P2

DATA COMPARATOR 4

DATA COMPARATOR 5

DATA COMPARATOR 6

DATA COMPARATOR 7

U12, CD4015

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR HAUHAN
	CK KEF 5/21/80
	APPR
MAT'L	BREAK ALL SHARP EDGES
	DECIMAL ANGULAR
	XX = ± ±
FINISH	XXX = ±
	DO NOT SCALE DRAWING

PARATRONICS INC.

SCHEMATIC DIAGRAM
TIMING MEMORY

DRWG NO 127-0065-001 REV.

D SCALE SHT 4 OF 4

S I N G L E L E V E L E X P L O S I O N

09/04/80

PAR143-0065-0090-00 DESCRIPTION : TIMING MEMORY PCB ASSY-OUTSIDEECO#: 107 REV.CU.: C

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
111-0207-0103-00	D	22 UF 16V CAP. ELECTRO.,RAD.	6	1	0	08/21/80	OPEN	0	C51
C52 C53 C54	C55	C56							
110-0005-0051-00	D	330 OHM 1/4W 5% CF RES	1	1	0	07/10/80	OPEN	0	R38
111-0012-0050-00	D	.001UF 1KV, CD. CAP	1	1	0	07/10/80	OPEN	0	C57
110-0205-0001-00	D	3329H-50, 50 OHM POT, BOURNS	1	1	0	OPEN	OPEN	0	R18
110-0309-0001-00	D	4.7K X 7 RESISTOR NETWORK	1	1	0	OPEN	OPEN	0	RP1
110-0308-0001-00	D	470OHM X 7 RESISTOR NETWORK	9	1	0	OPEN	OPEN	0	RP14
RP2 RP3 RP4	RP5	RP6 RP7 RP8 RP9							
110-0307-0001-00	D	160OHM X 7 RESISTOR NETWORK	2	1	0	OPEN	OPEN	0	RP10
RP12									
110-0306-0001-00	D	100OHM X 7 RESISTOR NETWORK	2	1	0	OPEN	OPEN	0	RP11
RP13									
110-0051-2002-00	D	20K 1/2% ALLEN-BRADLEY	4	1	0	OPEN	OPEN	0	R24
R25 R26 R30									
110-0051-1071-00	D	1.07K 1/2%	4	1	0	OPEN	OPEN	0	R23
R27 R28 R36									
112-0116-0001-00	D	79L12C	1	1	0	OPEN	OPEN	0	Q5
112-0115-0001-00	D	78L12C	1	1	0	OPEN	OPEN	0	Q6
115-0010-0001-00	D	SOCKET,22PIN	8	1	0	OPEN	OPEN	0	U13
U14 U15 U16	U26	U27 U28 U29							
115-0009-0001-00	D	SOCKET,20PIN	11	1	0	OPEN	OPEN	0	U1
U2 U3 U38	U39	U4 U40 U41 U5	U56	U57					
115-0005-0001-00	D	SOCKET,16PIN	36	1	0	OPEN	OPEN	0	U10
U11 U12 U17	U18	U19 U20 U21 U22	U23	U24	U25	U30	U31	U32	U33 U34
U35 U36 U37	U42	U44 U45 U46 U47	U48	U49	U50	U51	U52	U54	U55 U6
U7 U8 U9									
115-0003-0001-00	D	SOCKET,14PIN	5	1	0	OPEN	OPEN	0	U43
U53 U58 U59	U60								
111-0004-0072-00	D	.1 UF 25V CAP. CD	50	1	0	OPEN	OPEN	0	C1
C10 C11 C12	C13	C14 C15 C16 C17	C18	C19	C2	C20	C21	C22	C23 C24
C25 C26 C27	C28	C29 C3 C30 C31	C32	C33	C34	C35	C36	C37	C38 C39
C4 C40 C41	C42	C43 C44 C45 C46	C47	C48	C49	C5	C50	C6	C7 C8
C9									
117-0030-0001-00	D	TERMINAL, 120-1032-04, CAMBION	3	1	0	OPEN	OPEN	0	TP1
TP2 TP3									
110-0005-0044-00	D	160 OHM 1/4W 5% RES. CF	2	1	0	OPEN	OPEN	0	R33
R35									
110-0005-0039-00	D	100 OHM 1/4W 5% CF RES	4	1	0	OPEN	OPEN	0	R22
R29 R32 R34									
110-0005-0055-00	D	470 OHM 1/4W 5% CF RES	1	1	0	OPEN	OPEN	0	R20
110-0005-0037-00	D	82 OHM 1/4 W 5% CF RES	1	1	0	OPEN	OPEN	0	R18
110-0005-0096-00	D	24K OHM 1/4 W CF RES	1	1	0	OPEN	OPEN	0	R17
110-0005-0070-00	D	2 K OHM 1/4W 5% CF RES	3	1	0	OPEN	OPEN	0	R11
R16 R30									
110-0005-0067-00	D	1.5KOHM 1/4W 5% CF RES	1	1	0	OPEN	OPEN	0	R10
110-0005-0075-00	D	3.3 K OHM 1/4 W CF RES	5	1	0	OPEN	OPEN	0	R13

S I N G L E L E V E L E X P L O S I O N

09/04/80

	PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
R14	R15 R2 R6									
	110-0005-0063-00	D	1K OHM 1/4W 5% CF RES	9	1	0	OPEN	OPEN	0	R1
R12	R3 R31 R4		R5 R7 R8 R9							
	112-0101-0001-00	D	TRANSISTOR, 2N3905	3	1	0	OPEN	OPEN	0	Q1
Q2	Q3									
	112-0100-0001-00	D	TRANSISTOR, 2N3904	2	1	0	OPEN	OPEN	0	Q4
Q7										
	126-0065-0001-00	D	TIMING MEMORY PC FAB	1	1	0	OPEN	OPEN	0	

LEGEND UM : 01=EACH 02=INCH 03=FEET 04=BULK 05=AS REQUIRED 06=OTHER
LEGEND KEY: A=W/PARTS LIST D=W/O PARTS LIST R=REFERENCE DOCUMENT S=SPECIFICATION

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PARATRONICS INC.

SINGLE LEVEL EXPLOSION

09/04/80

PAR143-0065-0001-00 DESCRIPTION : TIMING MEMORY PCB ASSY ECO#: 107 REV.CU.: C

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
113-0200-0116-00	D	IC,MC10116	1	1	0	OPEN	OPEN	0	U44
113-0003-0073-00	D	I.C., 74LS73	1	1	0	OPEN	OPEN	0	U53
113-0002-0074-00	D	I.C., 74S74	2	1	0	OPEN	OPEN	0	U59
U60									
113-0002-0010-00	D	I.C., 74S10	1	1	0	OPEN	OPEN	0	U43
143-0065-0090-00	D	TIMING MEMORY PCB ASSY-OUTSIDE	1	1	0	OPEN	OPEN	107	
112-0113-0001-00	D	LM747C OP AMP	1	1	0	OPEN	OPEN	0	U58
113-0002-0373-00	D	I.C., N74S373N	4	1	0	OPEN	OPEN	0	U1
U2 U3 U4									
113-0002-0374-00	D	I.C., 74S374	4	1	0	OPEN	OPEN	0	U38
U39 U40 U41									
113-0003-0138-00	D	I.C., 74LS138	1	1	0	OPEN	OPEN	0	U51
113-0003-0174-00	D	I.C., 74LS174	1	1	0	OPEN	OPEN	0	U42
113-0003-0191-00	D	I.C., 74LS191	2	1	0	OPEN	OPEN	0	U54
U55									
113-0003-0244-00	D	I.C., 74LS244	1	1	0	OPEN	OPEN	0	U5
113-0003-0367-00	D	I.C., 74LS367,	1	1	0	OPEN	OPEN	0	U50
113-0017-0002-00	D	I.C., 93L422, 93422, 93412	8	1	0	OPEN	OPEN	0	U13
U14 U15 U16 U26 U27 U28 U29									
113-0035-0003-00	D	82S129, 6301-1 PROM	1	1	0	OPEN	OPEN	0	U52
113-0042-0001-00	D	SCL4015BE	5	1	0	OPEN	OPEN	0	U10
U12 U23 U7 U8									
113-0043-0001-00	D	I.C., AM6080	2	1	0	OPEN	OPEN	0	U56
U57									
113-0200-0102-00	D	I.C.,MC10102	4	1	0	OPEN	OPEN	0	U35
U46 U48 U49									
113-0200-0117-00	D	I.C., 10117N	8	1	0	OPEN	OPEN	0	U11
U19 U20 U21 U24 U25 U6 U9									
113-0200-0125-00	D	I.C., MC10125	2	1	0	OPEN	OPEN	0	U17
U30									
113-0200-0130-00	D	I.C., M10130	4	1	0	OPEN	OPEN	0	U34
U37 U45 U47									
113-0200-0131-00	D	I.C.,MC10131	4	1	0	OPEN	OPEN	0	U22
U32 U33 U36									
113-0200-0158-00	D	I.C., MC10158	2	1	0	OPEN	OPEN	0	U18
U31									

LEGEND UM : 01=EACH 02=INCH 03=FEET 04=BULK 05=AS REQUIRED 06=OTHER
LEGEND KEY: A=W/PARTS LIST D=W/O PARTS LIST R=REFERENCE DOCUMENT S=SPECIFICATION

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12.0 WAVEFORM BOARD

12.0 WAVEFORM BOARD

12.1 INTRODUCTION

The Waveform Board provides a high speed analog interface for the PI 540 along with special display hardware used to represent the collected analcg signal on the CRT.

12.2 FUNCTIONAL DESCRIPTION

When appropriate during the following discussion, please refer to the schematic diagrams, board layout, and parts list which are included at the end of this section. Also, tables of connector pins versus signal names for all motherboard connectors are provided in Section 15 along with an alphabetical list of all interboard signals. And, should the need arise, a Glossary in section 16 offers explanations for acronyms or terms that may be unfamiliar.

Beginning with the analog section, the input signal enters the board via edge connector pin S2-29 which is connected to the back panel BNC connector mounted on the motherboard rear end plate. Relay K1 selects dc (closed) or ac input coupling. Relays K2—K5 and their associated components form a precision attenuator network with division ratios of 1, 10, 100, and 1000. Relay K6 provides a ground reference when closed.

FET Q1 is configured as a zero-offset source follower and is used for buffering and impedance transformation. This circuit drives a low-pass filter consisting of C16, C17, and L1 to bandwidth-limit the signal to be presented to the A/D converter. IC13, an LM733 Op Amp, in conjunction with relays K7 and K8, forms a programable-gain amplifier. IC9, an LH0024 Op Amp, and transistor Q2 provide high speed, low output-impedance buffering to drive the A/D converters and the triggering circuit. The offset, or "vertical position" voltage is added in at the input of U9. The offset voltage is generated under software control by D/A converter U11 and its associated buffer.

The triggering circuit consists of an AM687 high speed comparator, U8, which compares the input signal to a reference generated by D/A U10 under software control. The true or complement outputs of the AM687 are chosen by U7 to determine the slope of the triggering fed to the trigger latch U20, an MC10131 dual D flip-flop. The other half of the MC10131 is used to hold the trigger latch reset until the clocks start.

U6 is wired as output port "D5" (Hex) to control the circuit via relays K1-K8 and the trigger polarity select line.

The A/D converter is either one Siemens G508 or two TRW TDC1014Js. (The TRWs are slightly slower so that 2 are used and their outputs multiplexed.) The A/D converter output is sent to the Timing Memory Board for storage.

After collection in the Timing Memory, the data is operated on by the Control Program and sent to a 256-word x 8-bit display memory in the display section of the Waveform board. The display memory occupies address locations 2E00H through 2EFFH. (No provision is made for reading this memory.) Operation of the display section is briefly described as follows.

The CRT screen is mapped into the display memory as 256 vertical columns corresponding to 256 X values. Each X value has a memory location assigned to it. The 8-bit data value in each memory location determines the column "altitude", or Y value, of the video dot for that X value. The resulting string of 256 dots constitutes the waveform and is sent to the Video Display Board for display on the CRT.

If a dot in the string gaps up or down from the preceding dot by more than one raster scan line, the circuit has the ability to fill in the gap. This is done by adding a string of vertical dots in the new dot's column down or up to the scan line just above or below the preceding dot. The number of dots added may range from one to many, as required. This preserves the visual continuity of the display.

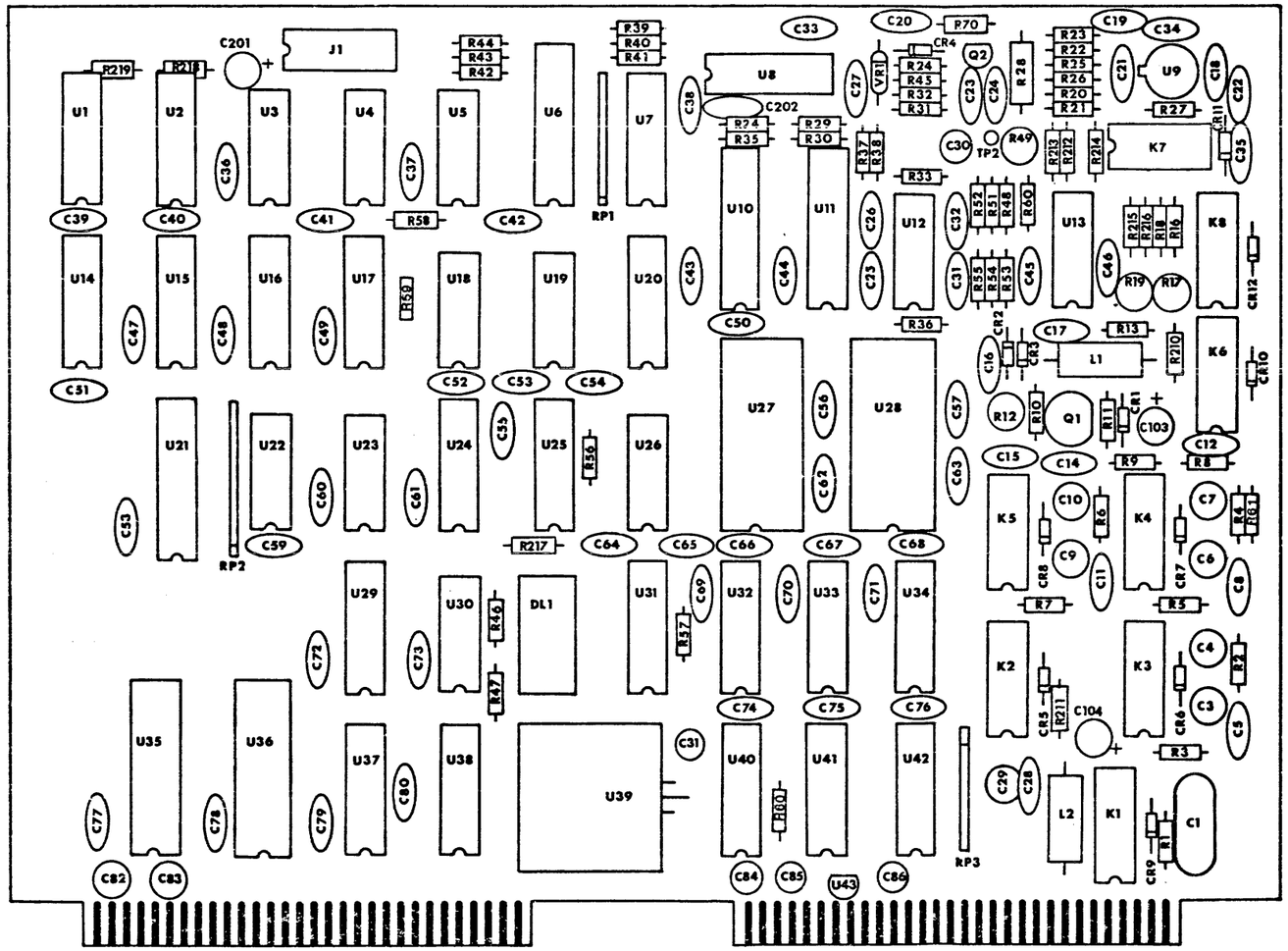
However, the line must be allowed to begin and end inside the screen boundaries so a scale and annotation may be included in the display. To accomplish this end, the gap-fill feature is inhibited for Y values of OFFH, and the Control Program places an FF-value dot at the beginning and end of the data string. No vertical line is drawn to or from the FF-value dot, and the dot itself is not displayed.

The display may be inhibited by writing a 00 to port 0D4H and enabled by writing a 01 to the same port. The display must be inhibited while the memory is being altered.

12.3 SCHEMATIC, BOARD LAYOUT, & PARTS LIST

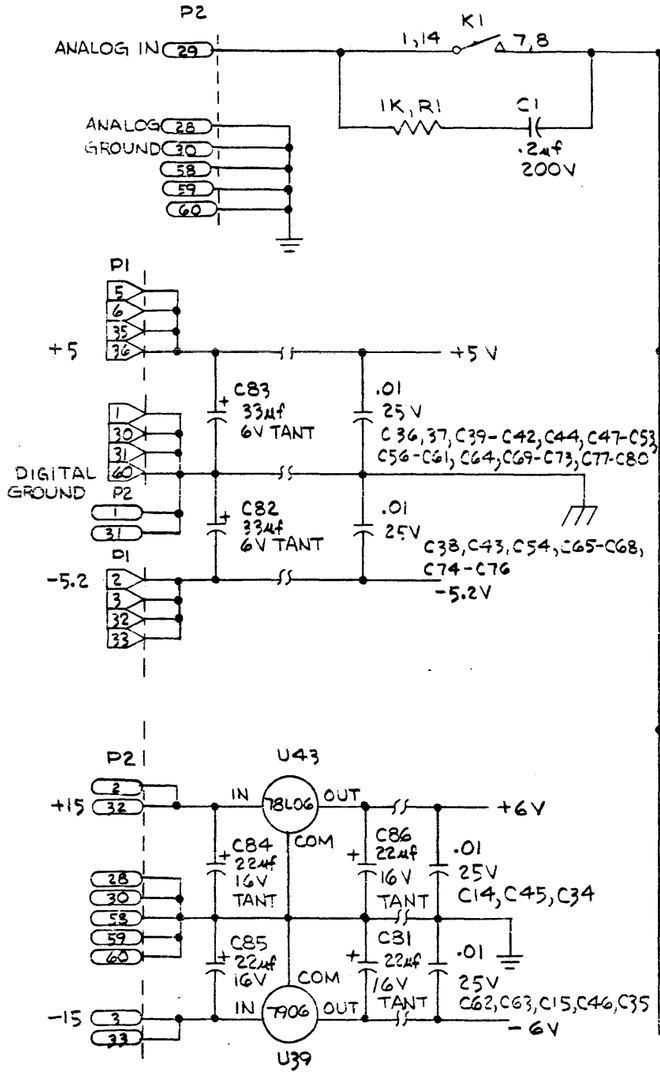
The schematic diagram, board layout, and parts list for the Waveform Board are contained on the following pages.

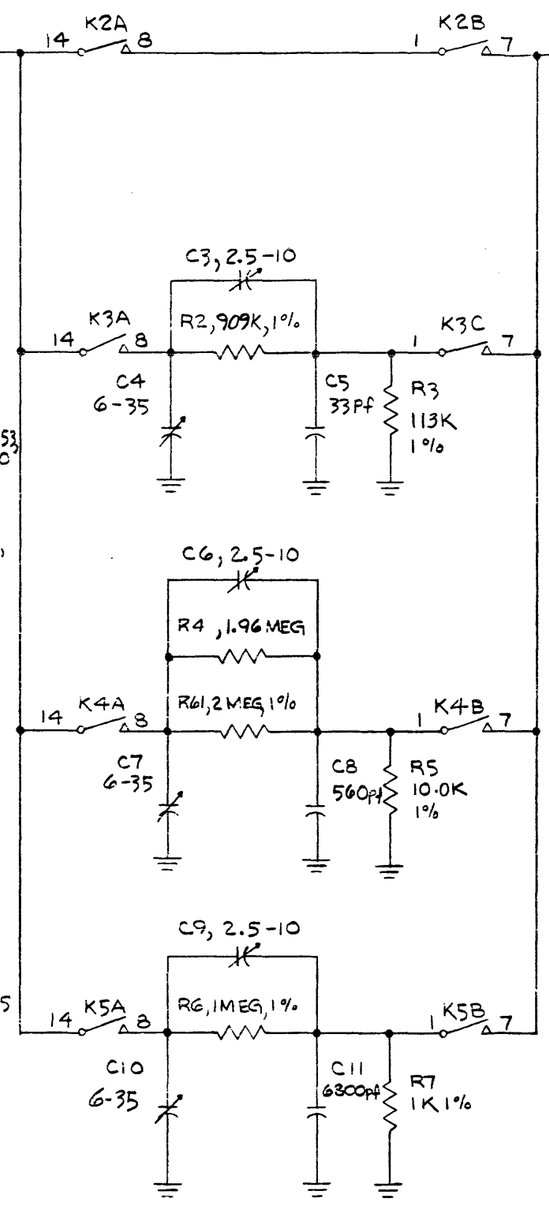
REV	DESCRIPTION	DATE	APPROVED
A	RELEASE 2-6-80	2-6-80	GM
B	REVISED PER ECO 137	7-10-80	MLP

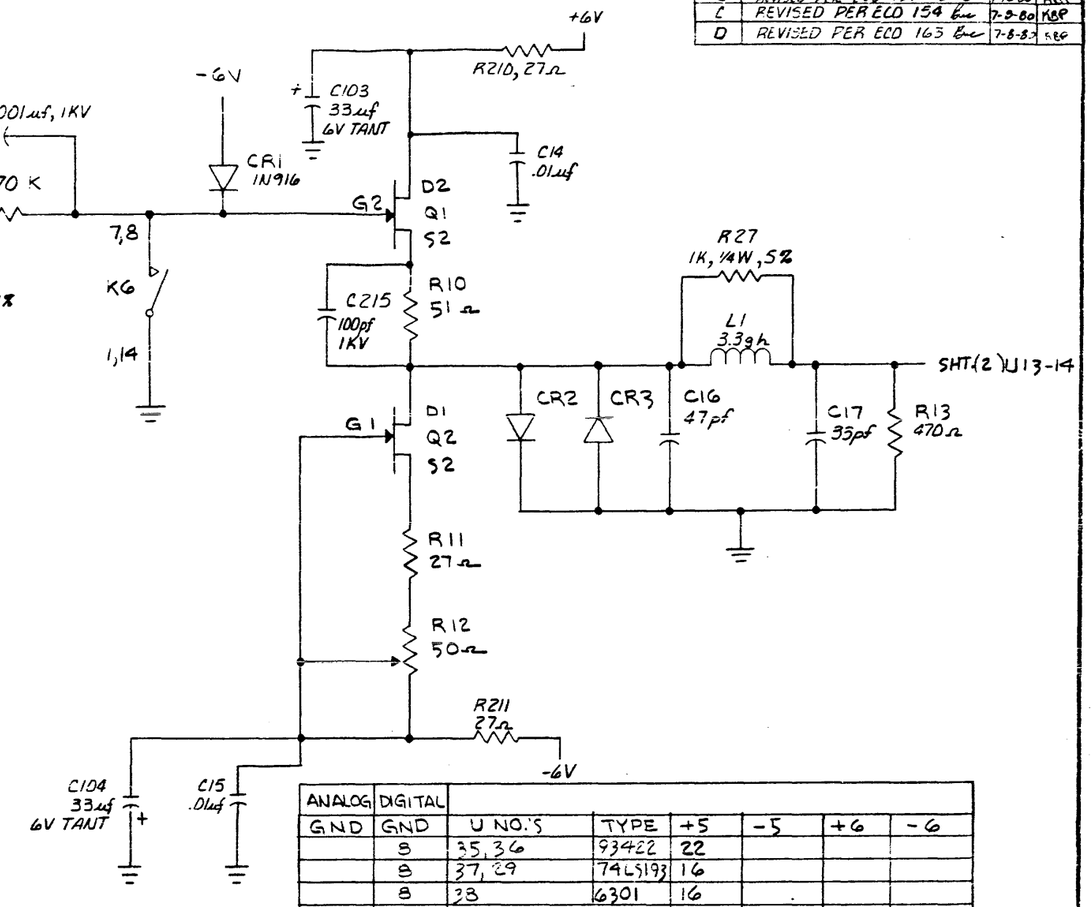


UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR G.S. 2-6-80	PARATRONICS INC.	
	CK [illegible] 2-6-80	LEGEND MASTER WAVEFORM BOARD	
	APPR G.M. 2-6-80		
MAT'L	BREAK ALL SHARP EDGES DECIMAL .XX ± .X .XXX ± .X ANGULAR ±		
FINISH	DO NOT SCALE DRAWING	DWG NO 126-0072-201 REV B	
		D SCALE SHT 1 OF 1	

REV	DESCRIPTION	DATE	APPROVED
6	REVISED PER ECO 137	4-12-80	KRP
C	REVISED PER ECO 154	7-3-80	KRP
D	REVISED PER ECO 163	7-8-80	KRP







ANALOG GND	DIGITAL GND	U NO.'S	TYPE	+5	-5	+6	-6
	8	35, 36	93422	22			
	8	37, 29	74LS193	16			
	8	28	6301	16			
	7	30	74S11	14			
	10	21, 6	LS374	20			
	7	22	LS30	14			
	7	23, 26, 4, 5	S74	14			
	8	24	S139	16	8		
	16	32, 33, 34, 40	10124	9	8		
1, 12	16	41	G508	7			
	8	14, 15, 16, 17	LS85	14			
	7	18	LS32	14			
	7	19	7407	9	8		
	16	25	10125	20			
	10	10, 11	6080	16			
	8	1, 2	LS161	14			
	7	3	S64	11	6		
	3, 14	5	AM637	7			
	8	27, 38	TDC1014J	3			
	1, 16	31	10116		8		
	1, 16	42	10176		3		
	1, 16	20	10131		3		
	1, 16	7	10102				

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR G.S.	2-14-80	PARATRONICS INC.
	CK		SCHEMATIC WAVEFORM BOARD
	APPR		
MAT'L	BREAK ALL SHARP EDGES		
FINISH	DECIMAL XX = ± XXX = ±	ANGULAR ±	
	DO NOT SCALE DRAWING		DRWG NO 127-0072-001 REV. D
			D SCALE SHT 1 OF 5

R16, 330Ω 1,14 K8 7,8 R17, 500Ω
R18, 470Ω R19, 500Ω
R215 82Ω R216 82Ω
+6
NE 592/733
R212, 475, 1% R20, 475, 1%
R214 475, 1%
K7
R213 475Ω 1%
R21 475Ω 1%
-6V
R13 SHT(1)
U13
R22 1.3K
C18 2.5-10pf TRIM
C19 33pf
LH0024
U9
C21 33pf
-6
+6V
R70 470Ω
R23 47Ω
+5.0V
R24 56Ω
C20
CR4
Q2
R28 100Ω 1/2W
-6.0V
R45 100Ω 1/4 W
VR2 1N702
+5V
R219 10K Ω
R218 68Ω
C201 33μf
C202 .01μf
AM687
U8
RP1-3 470
-5.2
10102
U7
RP1-2 470
-5
RP1-4 470
-5
VIN SHT.(5)
SET TRIG- SHT.(4) D7
SET OFF SET SHT.(4) D6
P1
DB7 21
DB6 51
DB5 20
DB4 18
DB3 17
DB2 19
DB1 49
DBØ 48
U11 AM6080
WE CS,DE CODE VR- VR+
R29 10K 1%
R30 10K 1%
VREF SHT(4)
U10 AM6080
R34 10K 1%
R35 10K 1%
VREF SHT(4)
+5
TL084 U12
C25 .01
R31 649Ω 1%
R32 27Ω
C202 .01μf
R33 649Ω, 1%
-.5V SHT.( )
R36 649 1%
C26 .01
R38, 27Ω
R37, 649Ω, 1%
R25 1.3K 1%
R26 680Ω
C23 33μf
C24 15pf
RP1-6 470
-5
P2
40 TW
U6 LS374
U24 74S139
7406 U19
CR5 K2
CR6 K3
CR7 K4
CR8 K5
CR9 K1
CR10 K6
CR11 K7
CR12 K8
L2 μH
C28 .01
C29 33μf 6V TANT
C27 .01
R39 1K
R40 1.5K
R41 2K
-5.2
10131 U20
CTINT
R42 1K
R43 1.5K
R44 2K
RP1-7 470
-5.2
RP1-5 470Ω
-5.2
LININH SHT.(3)
CTL REG SEL- SHT.(4&5) D5

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES
MAT'L
FINISH
BREAK ALL SHARP EDGES
DECIMAL ANGULAR
XX ± .1 ±
XXX ± .1
DO NOT SCALE DRAWING
PARATRONICS INC.
DRWG NO 127-0072-001 REV D
D SCALE NONE SHT 2 OF 5

-5
+5
U2 74LS161
U1 74LS161
R7
R6
R5
R4
R3
R2
R1
RØ
U15
U14
U16
U17
74LS85
DD7
DD6
DD5
DD4
DD3
DD2
DD1
DDØ
D7
D6
D5
D4
D3
D2
D1
DØ
74LS64
U3
U4 1/2 574
74LS32
U18
VIDEO OUT
J1
4
DOT CLK/2 SHT.(4)
EN VIDEO + SHT.(4)
U22
LS30
U30
S11
LIN INH SHT.(2)
DOT CLK / 2 SHT.(4)
J1
VRTC
3
HRTC
1
LS32
U18
U19, 74S06
EN VIDEO - SHT.(4)
U29 SHT.(4)
U21
74LS374
OE
R58 4.7K
RP2 4.7K
U35 & U36 SHT.(4)

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR		PARATRONICS INC.
	CK		
	APPR.		
MAT'L	BREAK ALL SHARP EDGES		
	DECIMAL	ANGULAR	
	XX = ±	±	
FINISH	XXX = ±		
	DO NOT SCALE DRAWING		DRWG NO 127-0072-001 REV D
			D SCALE SHT 3 OF 5

U21 SHT.(3)

P1 A7 A6 A5 A4 A3 A2 A1 A0

74LS193 U37

DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

+5

U36 93412/422

U35 93412/422

D7 D6 D5 D4 D3 D2 D1 D0

P1 A3 A2 A1 A0

74LS193 U29

74LS11 U30

U23

ENVIDEO+ SHT.(3)

R58 SHT. 3

DOT CLK/2

1/2 74574 U5

DOT CLK/2 SOURCE SHT.3

R217 270

J1 DOT CLK

HRTC

P1 IO/M

A15 A14 A13 A12 A11 A10 A9 A8

U38 6301-1 35-004

C213 .001uf

C214 .001uf

R59 270

U18 LS32

MEMWR

WR

IOEN

1/2 74S139 U24

D4 D5 D6 D7

CTL REG SEL- SHT.(2,5)

SET OFF SET- SHT.(2)

SET TRIG - SHT.(2)

DØ

ENVIDEO + SHT.(3)

ENVIDEO - SHT.(3)

R54 20K

C31 .01

R53 100K

R55 100Ω

U12

-1.00 SOURCE (VR-)

C32 .01

+6.0

R48 43Ω, 5%

TP2- SET TO 5.00 ± .01 V

R49 50Ω

R50 330Ω 5%

C30 33uf 6V

VREF SHT.(2)

R52 10K

R51 100K

+6

-6

-.50 SOURCE

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR	PARATRONICS INC.	
	CK		
	APPR		
MAT'L	BREAK ALL SHARP EDGES		
	DECIMAL ANGULAR		
FINISH	XX = ± 1		
	XXX = ±		
	DO NOT SCALE DRAWING	DWG NO 127-0072-001	REV D
		D SCALE	SHT 4 OF 5

VIN SHT(2)

CTL REG SEL- SHT. (4,2)

CTINT SOURCE

CT P2 6

1/274574 U26

U28 TDC1014J

U27

U25 10125

U31 10116

DL1 20NS DELAY

U34 10124 EN

U33 10124 EN

U40 10124 EN

U32 EN

U41

U42 10186

RP3 470 5IP

R56 470

R57 470

R47 270

R46 180

R60 470 -5

RP3 470

-6.0 +5 -5 +5 -5.2

P2

49 WD5
19 WD4
50 WD3
20 WD2
51 WD1
21 WD0
18 WD6

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR		PARATRONICS INC.
	CK		
	APPR.		
MAT'L	BREAK ALL SHARP EDGES		
	DECIMAL	ANGULAR	
FINISH	.XX = ±	±	DPWG NO 127-0072-001 REV D
	.XXX = ±		
	DO NOT SCALE DRAWING		D SCALE SHT 5 OF 5

PARATRONICS INC.

SINGLE LEVEL EXPLOSION

09/05/80

PAR143-0072-0090-00 DESCRIPTION : WAVEFORM PC ASSY. ECO#: 163 REV.CD.: D

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
110-0005-0031-00	D	47 OHM 1/4 W 5% CF RES	1	1	0	08/30/80	OPEN	0	R23
110-0005-0049-00	D	270 OHM 1/4W 5% RES	2	1	0	08/30/80	OPEN	0	R217
R59									
111-0207-0103-00	D	22 UF 16V CAP. ELECTRO.,RAD.	12	1	0	08/21/80	OPEN	0	C107
C104 C201 C23	C29	C30 C81 C82 C83	C84	C85	C86				
112-0215-0001-00	D	DIODE, 1N916	1	1	0	05/06/80	OPEN	0	CR1
110-0003-0058-00	D	649 OHM 1/4W,1% RES. CF	4	1	0	OPEN	OPEN	0	R31
R33 R36 R37									
110-0005-0030-00	D	43 OHM 1/4W,5% RES. CF	1	1	0	OPEN	OPEN	0	R48
110-0005-0035-00	D	68 OHM 1/4 W 5% CF RES	1	1	0	OPEN	OPEN	0	R218
110-0005-0051-00	D	330 OHM 1/4W 5% CF RES	1	1	0	OPEN	OPEN	0	R16
R50									
110-0005-0079-00	D	4.7 K OHM 1/4 W CF RES	1	1	0	OPEN	OPEN	0	R58
110-0005-0087-00	D	10K OHM 1/4 W CF RES	1	1	0	OPEN	OPEN	0	R219
110-0005-0127-00	D	470K OHM 1/4 W CF RES	1	1	0	OPEN	OPEN	0	R8
111-0004-0072-00	D	.1 UF 25V CAP. CD	1	1	0	OPEN	OPEN	0	C20
111-0006-0050-00	D	.001UF 50V CAP. CD	3	1	0	08/30/80	OPEN	0	C12
C213 C214									
111-0012-0030-00	D	100 PF 1KV CAP. CD	1	1	0	OPEN	OPEN	0	C215
121-0027-0002-00	D	3 UH INDUCTOR, DALE IM-2	1	1	0	OPEN	OPEN	0	L1
112-0120-0001-00	D	REG.+6V,TO92,UA78L62AWC,FSC	1	1	0	OPEN	OPEN	0	U43
112-0119-0001-00	D	REG.-6V,TO220,7906UC, FSC	1	1	0	OPEN	OPEN	0	U39
110-0005-0039-00	D	100 OHM 1/4W 5% CF RES	2	1	0	01/29/80	OPEN	0	R45
R55									
110-0008-0001-00	D	470OHM X-7 RESISTOR NETWORK	2	1	0	01/29/80	OPEN	0	RP1
RP3									
110-0014-0001-00	D	4.7K X 9, RES N'WORK 4310R-101	1	1	0	01/29/80	OPEN	0	RP2
112-0214-0001-00	D	1N702 DIODE	1	1	0	01/29/80	OPEN	0	VR1
110-0005-0025-00	D	27 OHM 1/4 W 5% CF RES	5	1	0	01/17/80	OPEN	0	R11
R210 R211 R32	R38								
110-0005-0032-00	D	51 OHM 1/4W 5% RES CF	1	1	0	01/17/80	OPEN	0	R10
110-0005-0033-00	D	56 OHM 1/4W 5% RES CF	1	1	0	01/17/80	OPEN	0	R24
110-0005-0037-00	D	82 OHM 1/4 W 5% CF RES	2	1	0	01/17/80	OPEN	0	R215
R216									
110-0005-0055-00	D	470 OHM 1/4W 5% CF RES	6	1	0	01/17/80	OPEN	0	R13
R18 R56 R57	R60	R70							
110-0005-0059-00	D	680 OHM 1/4W 5% CF RES	1	1	0	01/17/80	OPEN	0	R26
110-0005-0063-00	D	1K OHM 1/4W 5% CF RES	6	1	0	01/17/80	OPEN	0	R1
R27 R39 R42									
110-0005-0067-00	D	1.5KOHM 1/4W 5% CF RES	2	1	0	01/17/80	OPEN	0	R40
R43									
110-0005-0070-00	D	2 K OHM 1/4W 5% CF RES	2	1	0	01/17/80	OPEN	0	R41
R44									
110-0003-0055-00	D	475 OHM 1/4W 1% RES MF	5	1	0	01/17/80	OPEN	0	R20
R21 R212 R213	R214								
110-0003-0063-00	D	1K 1/4W 1% RES MF	1	1	0	01/17/80	OPEN	0	R7

BM301A

P A R A T R O N I C S I N C .

S I N G L E L E V E L E X P L O S I O N

09/05/80

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
110-0003-0066-00	D	1.3K 1/4W 1% RES MF	2	1	0	01/17/80	OPEN	0	R22
R25									
110-0003-0087-00	D	10K 1/4W 1% RES MF	6	1	0	01/17/80	OPEN	0	R29
R30 R34 R35	R5	R52							
110-0003-0094-00	D	20K 1/4W 1% RES MF	1	1	0	01/17/80	OPEN	0	R54
110-0003-0111-00	D	100K 1/4W 1% RES MF	2	1	0	01/17/80	OPEN	0	R51
R53									
110-0003-0114-00	D	113K 1/4W 1% RES MF	1	1	0	01/17/80	OPEN	0	R3
110-0003-0134-00	D	909K 1/4W 1% RES MF	1	1	0	01/17/80	OPEN	0	R2
110-0003-0135-00	D	1 MEG OHM 1/4W 1% RES.	2	1	0	01/17/80	OPEN	0	R6
R9									
110-0003-0141-00	D	1.96 MEG OHM 1/4W 1% RES.	1	1	0	01/17/80	OPEN	0	R4
110-0003-0142-00	D	2 MEG OHM 1/4W 1% RES.	1	1	0	01/17/80	OPEN	0	R61
110-0007-0039-00	D	100 OHM 1/2W 5% RES.	1	1	0	01/17/80	OPEN	0	R28
110-0205-0001-00	D	3329H-50, 50 OHM POT, BOURNS	2	1	0	01/17/80	OPEN	0	R12
R49									
110-0205-0004-00	D	3329H-1-501,500 OHM POT,BOURNS	2	1	0	01/17/80	OPEN	0	R17
R19									
111-0004-0066-00	D	.01 UF 25V CAP. CD	57	1	0	01/17/80	OPEN	0	C14
C15 C202 C25	C26	C27 C28 C31 C32	C33	C34	C35	C36	C37	C38	C39 C40
C41 C42 C43	C44	C45 C46 C47 C48	C49	C50	C51	C52	C53	C54	C55 C56
C57 C58 C59	C60	C61 C62 C63 C64	C65	C66	C67	C68	C69	C70	C71 C72
C73 C74 C75	C76	C77 C78 C79 C80							
111-0008-0064-00	D	.0068 MF 100V CAP,CW20A682K	1	1	0	01/17/80	OPEN	0	C11
111-0012-0013-00	D	15 PF 1KV CAP. CD	1	1	0	01/17/80	OPEN	0	C24
111-0012-0020-00	D	33PF 1KV CAP CD	1	1	0	01/17/80	OPEN	0	C17
C19 C21 C5									
111-0012-0022-00	D	47 PF 1KV CAP. CD	2	1	0	01/17/80	OPEN	0	C16
111-0012-0045-00	D	560 PF 1KV CAP CD .	1	1	0	01/17/80	OPEN	0	C8
111-0417-0068-00	D	.22 MF 200V CAP MYLAR	1	1	0	01/17/80	OPEN	0	C1
111-0800-0001-00	D	9611 TRIMMER CAP.	3	1	0	01/17/80	OPEN	0	C18
C3 C6 C9									
111-0800-0002-00	D	9613 TRIMMER CAP.	3	1	0	01/17/80	OPEN	0	C10
C4 C7									
112-0100-0001-00	D	TRANSISTOR, 2N3904	1	1	0	01/17/80	OPEN	0	Q2
112-0114-0001-00	D	XISTOR E420 SILICONIX	1	1	0	01/17/80	OPEN	0	Q1
112-0204-0001-00	D	DIODE ,1N3600	11	1	0	01/17/80	OPEN	0	CR10
CR11 CR12 CR2	CR3	CR4 CR5 CR6 CR7	CR8	CR9					
112-0307-0001-00	D	REED RELAY,191TE2A1-5G SIGMA	4	1	0	01/17/80	OPEN	0	K2
K5									
112-0308-0001-00	D	REED RELAY,191TE1A1-5S SIGMA	4	1	0	01/17/80	OPEN	0	K1
K6 K7 K8									
115-0003-0001-00	D	SOCKET,14PIN	11	1	0	01/17/80	OPEN	0	U12
U13 U18 U19	U22	U23 U26 U3 U30	U4	U5					
115-0005-0001-00	D	SOCKET,16PIN	22	1	0	01/17/80	OPEN	0	J1
U1 U14 U15	U16	U17 U2 U20 U24	U25	U29	U31	U32	U33	U34	U37 U38

P A R A T R O N I C S I N C .

S I N G L E L E V E L E X P L O S I O N

09/05/80

	PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
U40	U41 U42									
	115-0009-0001-00	D	SOCKET,20PIN	4	1	0	01/17/80	OPEN	0	U10
U11	U21 U6									
	115-0010-0001-00	D	SOCKET,22PIN	2	1	0	01/17/80	OPEN	0	U35
U36										
	115-0011-0001-00	D	SOCKET,24PIN	2	1	0	01/17/80	OPEN	0	U27
U28										
	117-0030-0001-00	D	TERMINAL, 120-1032-04, CAMBION	3	1	0	01/17/80	OPEN	0	TP1
TP2	TP3									
	121-0027-0001-00	D	1 MH INDUCTOR, DALE IMS-5	1	1	0	01/17/80	OPEN	0	L2
	126-0072-0001-00	D	540 WAVEFORM PC FAB	1	1	0	01/17/80	OPEN	0	

LEGEND UM : 01=EACH 02=INCH 03=FEET 04=BULK 05=AS REQUIRED 06=OTHER
LEGEND KEY: A=W/PARTS LIST D=W/O PARTS LIST R=REFERENCE DOCUMENT S=SPECIFICATION

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PARATRONICS INC.

SINGLE LEVEL EXPLOSION

09/05/80

PAR143-0072-0001-00 DESCRIPTION : WAVEFORM PC ASSY. ECO#: 163 REV.CU.: D

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
113-0002-0139-00	D	74S139 I.C.	1	1	0	01/17/80	OPEN	0	U24
112-0117-0001-00	D	NE592N OP AMP , SIG.	1	1	0	01/17/80	OPEN	0	U13
112-0118-0001-00	D	LH0024CH, OP AMP, NSC	1	1	0	01/17/80	OPEN	0	U9
113-0001-0006-00	D	I.C., 7406	1	1	0	01/17/80	OPEN	0	U19
113-0002-0011-00	D	74S11, IC	1	1	0	01/17/80	OPEN	0	U30
113-0002-0064-00	D	I.C., 74S64	1	1	0	01/17/80	OPEN	0	U3
113-0002-0074-00	D	I.C., 74S74	4	1	0	01/17/80	OPEN	0	U23
U26 U4 U5									
113-0003-0030-00	D	74LS30, IC	1	1	0	01/17/80	OPEN	0	U22
113-0003-0032-00	D	I.C., 74LS32	1	1	0	01/17/80	OPEN	0	U18
113-0003-0085-00	D	74LS85, IC	4	1	0	01/17/80	OPEN	0	U14
U15 U16 U17									
113-0003-0161-00	D	I.C., 74LS161	2	1	0	01/17/80	OPEN	0	U1
U2									
113-0003-0193-00	D	I.C., 74LS193	2	1	0	01/17/80	OPEN	0	U29
U37									
113-0003-0374-00	D	I.C., 74LS374	2	1	0	01/17/80	OPEN	0	U21
U6									
113-0017-0002-00	D	I.C., 93L422, 93422, 93412	2	1	0	01/17/80	OPEN	0	U35
U36									
113-0029-0001-00	D	I.C., TL084CN, TI	1	1	0	01/17/80	OPEN	0	U12
113-0035-0004-00	D	6301-1 PROM	1	1	0	01/17/80	OPEN	0	U38
113-0043-0001-00	D	I.C., AM6080	2	1	0	01/17/80	OPEN	0	U10
U11									
113-0048-0001-00	D	AM687 I.C.	1	1	0	01/17/80	OPEN	0	U8
113-0057-0001-00	D	A-D CONVERTER,TDC1014J, TRW	2	1	0	01/17/80	OPEN	0	U27
U28									
113-0200-0102-00	D	I.C.,MC10102	1	1	0	01/17/80	OPEN	0	U7
113-0200-0116-00	D	IC,MC10116	1	1	0	01/17/80	OPEN	0	U31
113-0200-0124-00	D	I.C., MC10124	4	1	0	01/17/80	OPEN	0	U32
U33 U34 U40									
113-0200-0125-00	D	I.C., MC10125	1	1	0	01/17/80	OPEN	0	U25
113-0200-0131-00	D	I.C.,MC10131	1	1	0	01/17/80	OPEN	0	U20
113-0200-0176-00	D	MC10176 IC	1	1	0	01/17/80	OPEN	0	U42
143-0072-0090-00	D	WAVEFORM PC ASSY.	1	1	0	01/17/80	OPEN	163	

LEGEND UM : 01=EACH 02=INCH 03=FEET 04=BULK 05=AS REQUIRED 06=OTHER
LEGEND KEY: A=W/PARTS LIST D=W/O PARTS LIST R=REFERENCE DOCUMENT S=SPECIFICATION

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13.0 INPUT PROBES

13.1 MODEL 51A PROBE

13.1.1 INTRODUCTION

The Model 51A Probe interfaces the State Analyzer to the system under test. The Model 51A Probe incorporates comparators for high input impedance and variable threshold selection. Each Probe interfaces 16 data bits, 2 qualifiers bits, and a clock input. A switch on the probe is provided to present a fixed TTL threshold of 1.6 V for convenience. A monitoring point permits measuring the threshold voltage which can be adjusted over the range of ±6 V. The voltage at this monitoring point with respect to probe ground is 1/2, or 50%, of the actual threshold voltage. The Model 51A also incorporates a data complement (invert) switch for active-low bus conventions. The impedance for all inputs is 44K ohms shunted with 15 pF.

13.1.2 FUNCTIONAL DESCRIPTION

For the following discussion, please refer to the schematic diagram, board layout, and parts list at the end of this section.

Resistors RN1—RN4 form voltage dividers which apply 1/2 of the input voltage to U1—U5, Motorola MC3430 or National DS3651 high-speed quad comparators. The input capacitance of the comparators is compensated by capacitors C1—C19. Resistors R4, R5, and R7 provide approximately 200 mV of hysteresis to the clock input. Comparators U1—U5 accept a threshold reference from the voltage divider formed by R10—R12 or R8, R9. These high-speed comparators convert the variable input voltages to TTL levels. Switch S1 controls whether buffers U6—U10 operate in a true or complement mode. U10 also selects clock polarity and provides buffering for clock and qualifier signals. The probe receives ±5 V power from the analyzer through the ribbon cable.

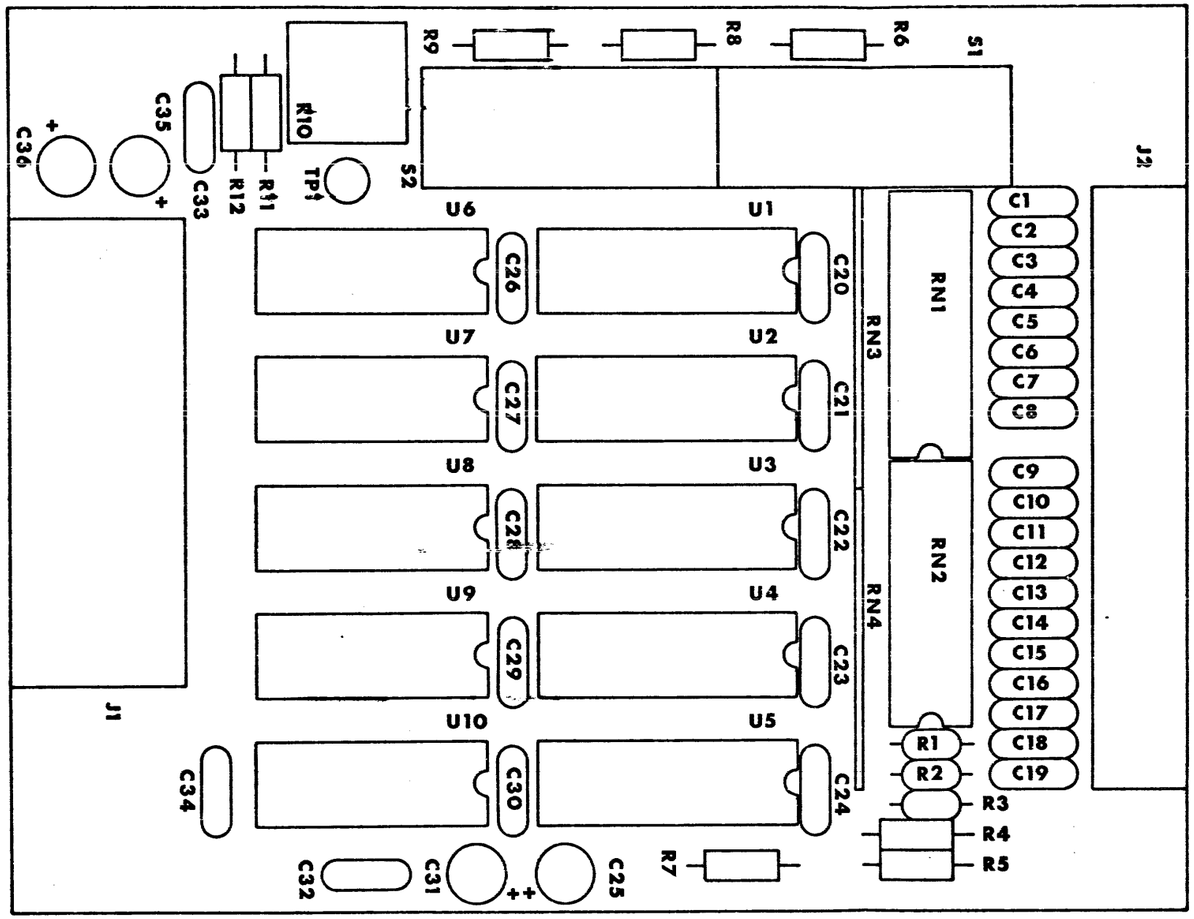
The Model 51A Probe receives a functional check when plugged into the PI 540 self-test port using the Model 53 Adapter, or when used in the analyzer self-test with the Logic Analyzer Demo Card (For details, please refer to subsections 1.4.3 and 1.4.4 in the Introduction.)

Although the input resistor divider provides some input protection, volatges higher than ±25 V may damage the dividers or comparators and should be avoided.

13.1.3 SCHEMATIC, BOARD LAYOUT, & PARTS LIST

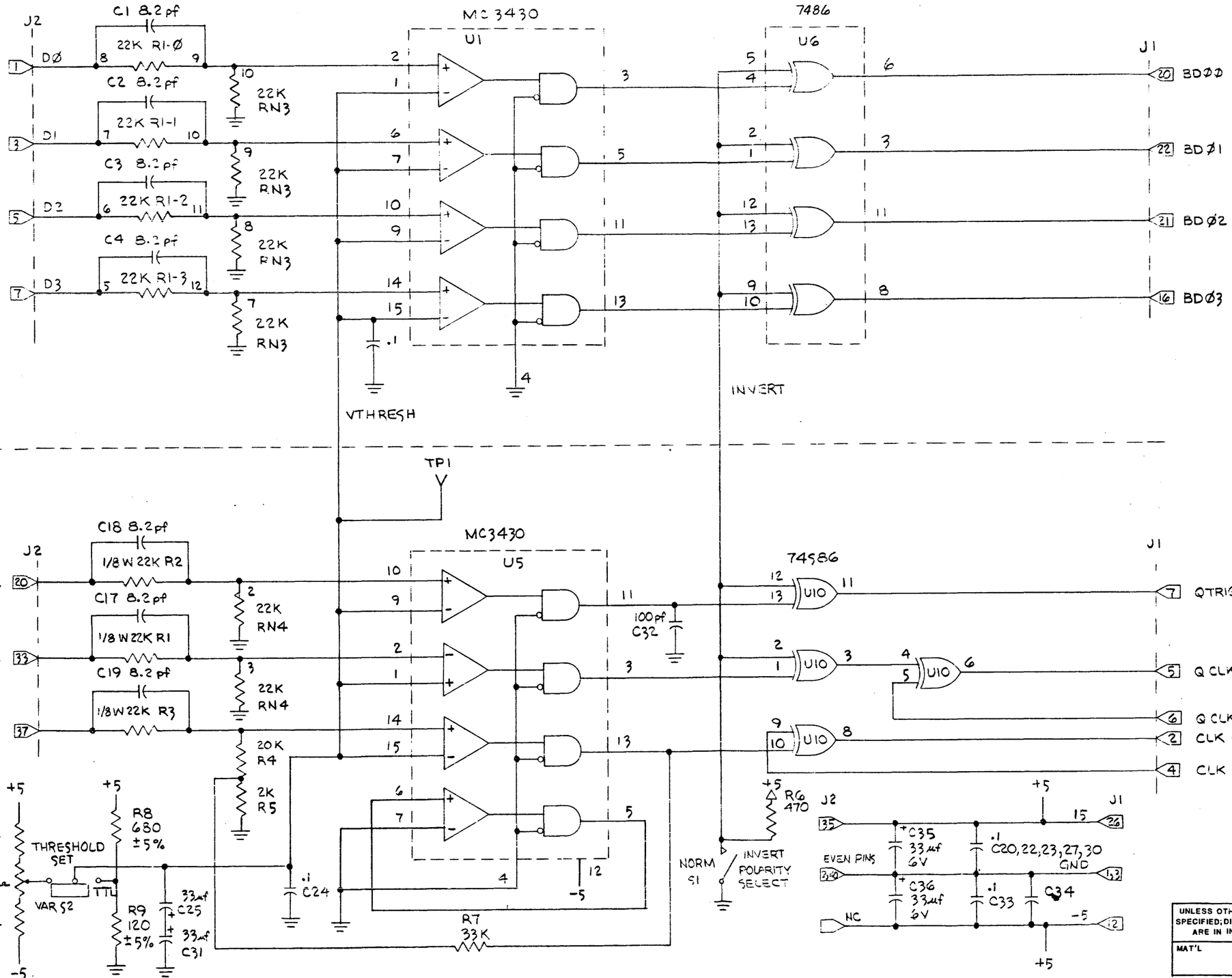
The schematic diagram, board layout, and parts list for the Model 51A Probe are contained on the following pages.

REV	DESCRIPTION	DATE	APPROVED



UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR G.S.	11-26-79	PARATRONICS INC.
	CK RFH	11-27-79	
	APPR LFH	11-27-79	LEGEND MASTER
MAT'L	BREAK ALL SHARP EDGES		MODEL 51 A PROBE
FINISH	DECIMAL: XX = ± ; XXX = ±	ANGULAR: ±	
	DO NOT SCALE DRAWING		DRWG NO 126-0015-201 REV A
			D SCALE — SHT 1 OF 1

REV	DESCRIPTION	DATE	APPROVED
B	REV PER ECO 104	[illegible]	3-2-80
C	REV. PER ECO 138	MCP ES.	3-21-80



POWER DISTRIBUTION				
U NO.	TYPE	+5	GND	-5
U1-U5	MC3430	16	8	12
U6-U9	7486	14	8	—
U10	74S86	14	8	—
RN3,RN4	9X22K	—	1	—

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR G.C. 1-14-80	PARATRONICS INC.	
	CK M.C.P. 1-16-80	SCHEMATIC DIAGRAM MODEL 51 A PROBE	
	APPR.		
MAT'L	BREAK ALL SHARP EDGES		
FINISH	DECIMAL XX ± ± XXX ± ± ANGULAR °		
	DO NOT SCALE DRAWING	DRWG NO 127-0015-002 REV. C	
	D	SCALE — SHT 1 OF 2	

REV	DESCRIPTION	DATE	APPROVED
C	SEE SHT. 1		

J2 D4 (9) — C5 8.2pf — 22K RN1 (4, 13) — RN3 22K (6)
J2 D5 (11) — C6 8.2pf — 22K RN1 (3, 4) — RN3 22K (5)
J2 D6 (13) — C7 8.2pf — 22K RN1 (2, 15) — RN3 22K (4)
J2 D7 (15) — C8 8.2pf — 22K RN1 (1, 16) — RN3 22K (3)

MC3430 U2: (2, 1, 6, 7, 10, 9, 14, 5) → (3, 5, 11, 13); (.1 C21, 4, 12, -5)

7486 U7: (5, 4, 2, 1, 12, 13, 9, 10) → (6, 3, 11, 8)

INVERT SHT.1 U10

VTHRESH SHT.1 U5

J1: (33) BDØ4, (19) BDØ5, (24) BDØ6, (25) BDØ7

J2 D8 (17) — C9 8.2pf — 22K RN2 (8, 9) — RN3 22K (2)
J2 D9 (19) — C10 8.2pf — 22K RN2 (7, 10) — RN4 22K (10)
J2 D10 (21) — C11 8.2pf — 22K RN2 (6, 11) — RN4 22K (9)
J2 D11 (23) — C12 8.2pf — 22K RN2 (5, 12) — RN4 22K (8)

MC3430 U3: (2, 1, 6, 7, 10, 9, 14, 15) → (3, 5, 11, 13); (.1 C28, 4, 12, -5)

7486 U8: (5, 4, 2, 1, 12, 13, 9, 10) → (6, 3, 11, 8)

INVERT SHT.1 U10

VTHRESH SHT.1 U5

J1: (18) BDØ8, (17) BDØ9, (15) BD10, (14) BD11

J2 D12 (25) — C13 8.2pf — 22K RN2 (4, 13) — RN4 22K (7)
J2 D13 (27) — C14 8.2pf — 22K RN2 (3, 14) — RN4 22K (6)
J2 D14 (29) — C15 8.2pf — 22K RN2 (2, 15) — RN4 22K (5)
J2 D15 (31) — C16 8.2pf — 22K RN2 (1, 16) — RN4 22K (4)

MC3430 U4: (2, 1, 6, 7, 10, 9, 14, 15) → (3, 5, 11, 13); (.1 C29, 4, 12, -5)

7486 U9: (5, 4, 2, 1, 12, 13, 9, 10) → (6, 3, 11, 8)

INVERT SHT.1 U10

VTHRESH SHT.1 U5

J1: (13) BD12, (8) BD13, (10) BD14, (11) BD15

UNLESS OTHERWISE SPECIFIED; DIMENSIONS ARE IN INCHES	DR	PARATRONICS INC.
MAT'L	CK	
FINISH	APPR	
	BREAK ALL SHARP EDGES DECIMAL ANGULAR .XX ± .1 1° .XXX ± .01 DO NOT SCALE DRAWING	DRWG NO 127-0015-002 REV C D SCALE SHT 2 OF 2

PARATRONICS INC.

SINGLE LEVEL EXPLOSION

09/05/80

PAR143-0015-0090-00 DESCRIPTION : M 51 PROBE PC ASY OUTSIDE ECO#: 0 REV.CU.:

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
117-0034-0001-00	D	TERMINAL, 180-7337-02-05,CAMBI	1	1	0	OPEN	OPEN	0	
126-0015-0001-00	D	MODEL 51 PROBE PCB FAB	1	1	0	OPEN	OPEN	0	
116-0006-0001-00	D	SWITCH, DPDT, GF-126-0161,CW	2	1	0	OPEN	OPEN	0	S1
S2									
115-0009-0001-00	D	SOCKET,20PIN	4	1	0	OPEN	OPEN	0	U2
U3 U4 U5									
115-0005-0001-00	D	SOCKET,16PIN	5	1	0	OPEN	OPEN	0	U10
U6 U7 U8 U9									
115-0003-0001-00	D	SOCKET,14PIN	1	1	0	OPEN	OPEN	0	U1
111-0012-0039-00	D	330 PF 1KV CAP. CD	2	1	0	OPEN	OPEN	0	C7
C8									
111-0012-0030-00	D	100 PF 1KV CAP. CD	1	1	0	OPEN	OPEN	0	C11
111-0012-0003-00	D	2.2 PF 1KV CAP. CD	1	1	0	OPEN	OPEN	0	C12
111-0004-0072-00	D	.1 UF 25V CAP. CD	11	1	0	OPEN	OPEN	0	C1
C10 C13 C14 C15		C2 C3 C4 C5 C6 C9							
110-0300-0001-00	D	RES. NETWORK,STKPOLE S10-9-1	2	1	0	OPEN	OPEN	0	R20
R21 R22 R23 R24		R25 R26 R27 R28 R29 R30 R31 R32 R33 R34 R35 R36							
R37									
110-0201-0001-00	D	POT, BOURNS 3386P-1-102	1	1	0	OPEN	OPEN	0	R47
110-0005-0079-00	D	4.7 K OHM 1/4 W CF RES	2	1	0	OPEN	OPEN	0	R44
R45									
110-0005-0037-00	D	82 OHM 1/4 W 5% CF RES	1	1	0	OPEN	OPEN	0	R52
110-0005-0063-00	D	1K OHM 1/4W 5% CF RES	6	1	0	OPEN	OPEN	0	R39
R40 R41 R42 R43		R51							
110-0005-0047-00	D	220 OHM 1/4W 5% CF RES	4	1	0	OPEN	OPEN	0	R46
R48 R49 R50									
110-0002-0101-00	D	39K 1/8 W 5% CF RES	19	1	0	OPEN	OPEN	0	R1
R10 R11 R12 R13		R14 R15 R16 R17 R18 R19 R2 R3 R4 R5 R6 R7							
R8 R9									
110-0002-0087-00	D	10K 1/8 W 5% CF RES	1	1	0	OPEN	OPEN	0	R38

LEGEND UM : 01=EACH 02=INCH 03=FEET 04=BULK 05=AS REQUIRED 06=OTHER
LEGEND KEY: A=W/PARTS LIST D=W/O PARTS LIST R=REFERENCE DOCUMENT S=SPECIFICATION

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S I N G L E L E V E L E X P L O S I O N

09/05/80

PAR143-0015-0001-00 DESCRIPTION : M51 PROBE PCB ASSY IN HOUSE ECO#: 0 REV.CU.:

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
143-0015-0090-00	D	M 51 PROBE PC ASY OUTSIDE	1	1	0	OPEN	OPEN	0	
124-0001-0001-00	D	MODEL 50/51 PROBE CABLE ASSY	1	1	0	OPEN	OPEN	0	J1
120-0004-0001-00	D	MODEL 51 PROBE TOP COVER	1	1	0	OPEN	OPEN	0	
120-0001-0001-00	D	MODEL 50/51 BOTTOM COVER	1	1	0	OPEN	OPEN	0	
119-0012-0001-00	D	THIS SIDE UP LABEL	1	1	0	OPEN	OPEN	0	
119-0002-0001-00	D	MODEL 51 PROBE LABEL	1	1	0	OPEN	OPEN	0	
117-1250-0005-00	D	4-40X 3/8PHMS,NYLON, SLOTTED	4	1	0	OPEN	OPEN	0	
114-0003-0001-00	D	CONN.20PIN,DUAL,6-AA-02-20-1PX	1	1	0	OPEN	OPEN	0	J2
113-0021-0001-00	D	I.C., MC3430P, MOT	5	1	0	OPEN	OPEN	0	U10
U6 U7 U8 U9									
113-0003-0244-00	D	I.C., 74LS244	2	1	0	OPEN	OPEN	0	U3
U5									
113-0003-0240-00	D	I.C., 74LS240	2	1	0	OPEN	OPEN	0	U2
U4									
113-0002-0086-00	D	I.C., 74S86	1	1	0	OPEN	OPEN	0	U1

13.0 INPUT PROBES

There are three types of input probes used with the PI 540 Analyzer; the Model 51A Probe (for the State section), the Model 80 Probe (for the Timing section), and the Model 90 Probe (for the Waveform section). The basic purpose of these probes is to provide high impedance signal inputs that can be placed physically close to the source of target signals and to convert the acquired signals to a form suitable for transmission to the PI 540 for analysis.

The Model 51A Probe, used for input to the State Analyzer section, provides inputs for 16 data signals, one clock signal, and two qualifier signals. (Two Model 51A Probes are used if the analyzer is to be operated in the 32-bit mode.) The qualifier signals may be applied (by keyboard instructions) to the clock signal and, at the same time, to any or all of the 16 levels of trigger words. The nominal impedance of all inputs is 44K ohms shunted by 15 pF. The probe contains a manual adjustment for setting the logic threshold of the incoming signals, and it contains a switch for presetting this threshold to TTL level. The probe also contains a switch for inverting all incoming signals if desired.

The Model 80 Probe, used for input to the Timing Analyzer section, provides inputs for 8 data signals, a clock signal, and a clock-qualifier signal. The nominal impedance of all inputs is 100K ohms shunted by 10 pF. The logic threshold voltage for these inputs is variable and is set by keyboard entry. Also, the inputs have a hysteresis function that can be turned on or off from the keyboard.

The Model 90 Probe, used for input to the Waveform Analyzer section, provides a single input that can be manually switched between two input impedance levels; 10M ohms shunted by 12 pF and having a 10:1 attenuation ratio, and 1M ohm shunted by 70 pF and having a 1:1 attenuation ratio.

These probes are described in greater detail in the following subsections.

13.2 MODEL 80 PROBE

13.2.1 INTRODUCTION

The Model 80 Probe is used for input to the Timing Analyzer section. It provides inputs for 8 data signals, a clock signal, and a clock-qualifier signal. The nominal impedance of all inputs is 100K ohms shunted by 10 pf. The logic threshold voltage for these inputs is variable and is set by keyboard entry. Also, the inputs have a hysteresis function that can be turned on or off from the keyboard.

13.2.2 FUNCTIONAL DESCRIPTION

When appropriate during the following discussion, please refer to the schematic diagram, board layout, and parts list which are included at the end of this section. Also, tables of connector pins versus signal names for all motherboard connectors are provided in section 15 along with an alphabetical list of all interboard signals. And, should the need arise, a Glossary in section 16 offers explanations of acronyms or terms that may be unfamiliar.

For each of its 10 input channels, the Model 80 Probe contains an Input Buffer and a Comparator. Because the circuits of all channels are identical, the schematic diagram shows the first two channels in detail and the remaining channels in an abbreviated form.

13.2.2.1 Input Buffers

There are 10 Input Buffers; one for each of the 8 data inputs, one for the clock input, and one for the clock-qualifier input. Because all the Buffers are identical, only one will be described and that description can be applied to all the others.

The Channel-0 Input Buffer consists of: Q1, a Siliconix E420 dual J-FET transistor; CR1 and CR2, both 1N3600 diodes; and various capacitors and resistors. The major functions of the Buffer are to provide signal isolation and high input impedance.

Because of the high input impedance of Q1A, the impedance presented to the incoming signal is essentially determined by the 3:1 passive divider made up of R1, R2, C1, C2, and stray capacity. This input impedance is nominally 100K ohms shunted by 10 pf. CR1 and CR2 are clamping diodes that provide overvoltage protection for Q1A against input voltage peaks as high as ±100 V. The usable input voltage swing (before clipping by these diodes begins) is ±9 V. Q1A is connected in cascade with Q1B in a zero-offset source follower circuit. The output of this circuit is fed to the Channel-0 Comparator.

Variable resistor R5 is used to compensate for any mismatch that may exist between Q1A and Q1B. R5 is adjusted so that, with the signal input grounded, the voltage at pin 9 of U1B is 0.0 V ± .005 V.

13.2.2.2 Comparators

As with the Input Buffers, there are 10 identical Comparators and only one will be described.

The Channel-0 Comparator consists solely of U1B, 1/2 of an AMD AM687 high-speed dual comparator with complementary ECL outputs. The major function of the Comparator is to convert a variety of logic-signal inputs with a range of amplitudes and transition times into logic-signal outputs with preestablished ECL logic levels and fast transition times.

The Comparator's plus input, U1B-9, is fed with the low impedance signal from the Channel-0 Buffer. The minus input, U1B-10, is fed with threshold voltage THRESHA (Threshold A) against which the incoming signal is compared. (As the input signal crosses this threshold from below, the output of the comparator switches from logic low to logic high; and as the input signal crosses this threshold from above, the output of the comparator switches from logic high to logic low.) THRESHA comes, via connector pin J6-5, from a D/A convertor on the Timing Memory Board (ref. Timing Memory schematic sheet 1) and is keyboard-specified over a range of -6.4 V to +6.35 V in .05 V steps. The default value is +1.60 V, suitable for TTL logic. Threshold voltage accuracy is ±0.05 V.

The comparator's LE (Latch Enable) input, U1B-13, is grounded. Under this condition, if LE- is held negative (below -100 mV), the comparator operates in a normal manner. But if LE- is driven high (above +100 mV), the comparator outputs are latched in their existing logic states. The latched mode is not used in this application. However, the internal circuitry of the AM687 is such that in the transition region between latched and unlatched modes there is a small voltage range for LE- that produces hysteresis at the comparator inputs, and this feature is used in our circuit.

When the input hysteresis function has been keyboard-specified as ON, a nominal voltage of +1.7 V is sent to the probe as signal HYST at connector pin J6-34. This voltage is divided down by R6 and R8 to a nominal +45 mV at the LE- input, U1B-12, where it produces a hysteresis of 67 mV at the comparator input. This translates into a nominal 200 mV hysteresis at the probe input (because of the 3:1 input divider, R1-R2). When the input hysteresis function has been keyboard-specified as OFF, signal HYST becomes -5.1 V, which divides down to -134 mV at LE- and puts the comparator in the nonhysteresis, nonlatch mode. The signal HYST comes from the Control Port on the Timing Memory Board via connector pin S2-15 (ref. Timing Memory schematic sheet 1).

The nature of comparators is such that oscillations will occur if input signals with slow rise or fall times take longer than the propagation time of the comparator (8 ns in this case) to traverse the transition region around the threshold voltage. However, in our circuit such oscillations are prevented if the hysteresis function is in effect. For this reason, it is recommended that hysteresis be used habitually unless some special application requires an investigation of the transition region. Accordingly, the default hysteresis condition is ON.

The Comparator provides a differential output at ECL levels. The output signals, DO+ and DO-, are fed through connector pins J6-33 and J6-32 to the

Timing Memory Board at pins S2-52 and S2-53 (ref. Timing Memory schematic sheets 3 and 4). The outputs of U1B are open emitters, and the necessary pull-down resistors are provided on the Timing Memory Board. These pull-down resistors, in parallel with resistors to ground that are also on the Timing Memory Board, provide a 60-ohm termination for each of the signal lines. Both polarities of the data signals are needed by the glitch detecting circuitry on the Timing Memory Board. But the positive signal alone is used when the sample mode, rather than the glitch-capture mode, has been keyboard selected.

The clock channel output signals, CLK+ and CLK-, are fed through pins J6-3 and J6-2 to Clock Control on the Timing Control Board at pins S2-56 and S2-55 for possible keyboard selection as the operating clock (ref. Timing Control schematic sheet 8). The clock-qualifier channel output signals, QCLK+ and QCLK-, are fed through pins J6-9 and J6-8 to Clock Control on the Timing Control Board at pins S2-58 and S2-57 for possible use as a clock qualifier if the probe clock has been selected as the operating clock. Both polarities of the clock and clock-qualifier signals are needed by the logic in the Clock Control circuits.

13.2.2.3 Application

The following brief comments are intended to help clarify the internal workings of the Probe-Analyzer system rather than to treat the very extensive uses of the instrument in analyzing a target system. (Please refer to the Operator's Manual for more information on the many uses of the PI 540.)

Because the Model 80 Probe is designed for use with the PI 540's Timing Analyzer section which can be used for both timing and state analysis, the Model 80 Probe will be applied in both types of analysis. Essentially, the only difference between the two applications from the standpoint of the probe itself is in the use of the clock and clock-qualifier inputs.

In the timing analysis mode, the clock will probably be selected as internal, and the probe's clock and clock-qualifier inputs will not be connected to the system under test. (Any signal at the clock-qualifier input has no effect when an internal clock is being used.)

The state analysis mode may be either an 8-bit mode, in which the Timing Analyzer section is used by itself as a state analyzer, or it may be a 40-bit mode, in which the 8-bit Timing Analyzer section is used in cascade with the 32-bit State Analyzer section as a 40-bit state analyzer.

In the 8-bit state analysis mode, the clock will probably be selected as external, and the probe's clock input will be connected to the system under test in order to provide the external clock. The clock-qualifier input may also be connected if qualification of the clock signal is desired. But the qualifier signal cannot be applied to the arm or trigger words (as the Model 51A Probe's qualifier signals can with the State Analyzer section).

In the 40-bit state analysis mode, the 40-bit analyzer is restricted to the more limited state analysis capabilities of the Timing Analyzer section. The clock will probably be selected as external, and the Model 80 Probe's clock input will be connected to the system under test and will provide the

external clock for both sections of the combined analyzer. (The State section automatically receives the same clock selected for the Timing section.) The clock inputs of the two Model 51A Probes cannot be used in the 40-bit mode and will not be connected. Also, the two qualifier inputs on each of the Model 51A Probes cannot be used as clock qualifiers, and data-word clock qualification is not available. The single clock-qualifier input of the Model 80 Probe is the only clock qualifier that can be used. The keyboard control of the Model 80 Probe's input threshold levels and hysteresis selection is still in effect.

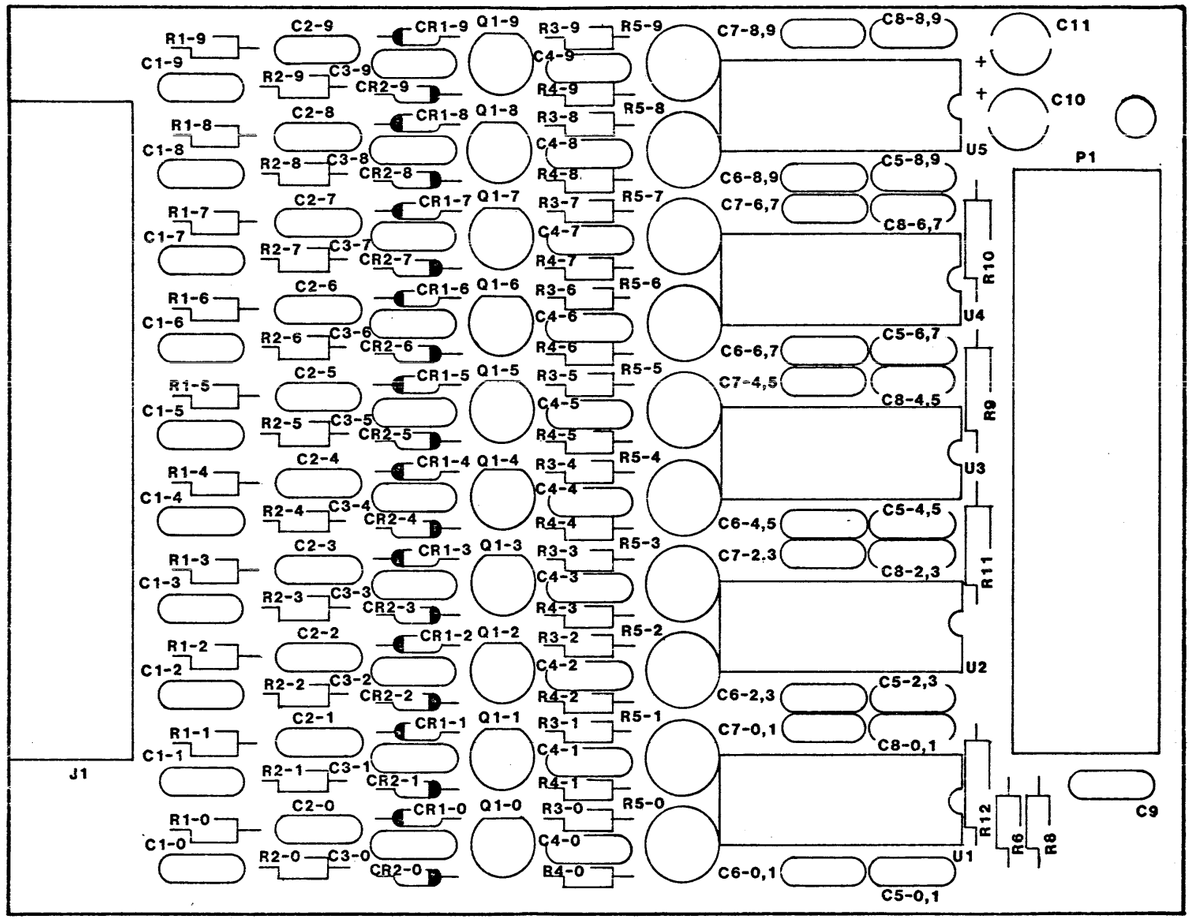
In this 40-bit mode, only two levels of nested trigger words are available (called the arm word and trigger word in timing analysis) instead of the 16 levels that are ordinarily used in the State Analyzer section. However, these two words are the full 40 bits long and can be qualified by the four Model 51A Probe qualifier bits and by the External and Waveform links. Also, the Timing Analyzer section's delay functions can be applied. The memory depth is limited to the 250 words of the 32-bit State Analyzer.

Although these restrictions should be kept in mind for proper application, a 40-bit x 250-word state analyzer with a clock-qualifier bit and two levels of nested 40-bit trigger words with four qualifiers, two linkages, and a flexible delay function is nevertheless a very powerful instrument. It only seems limited in comparison with the unusually extensive features of the State Analyzer section when used in the 32- or 16-bit modes.

13.2.3 SCHEMATIC, BOARD LAYOUT, & PARTS LIST

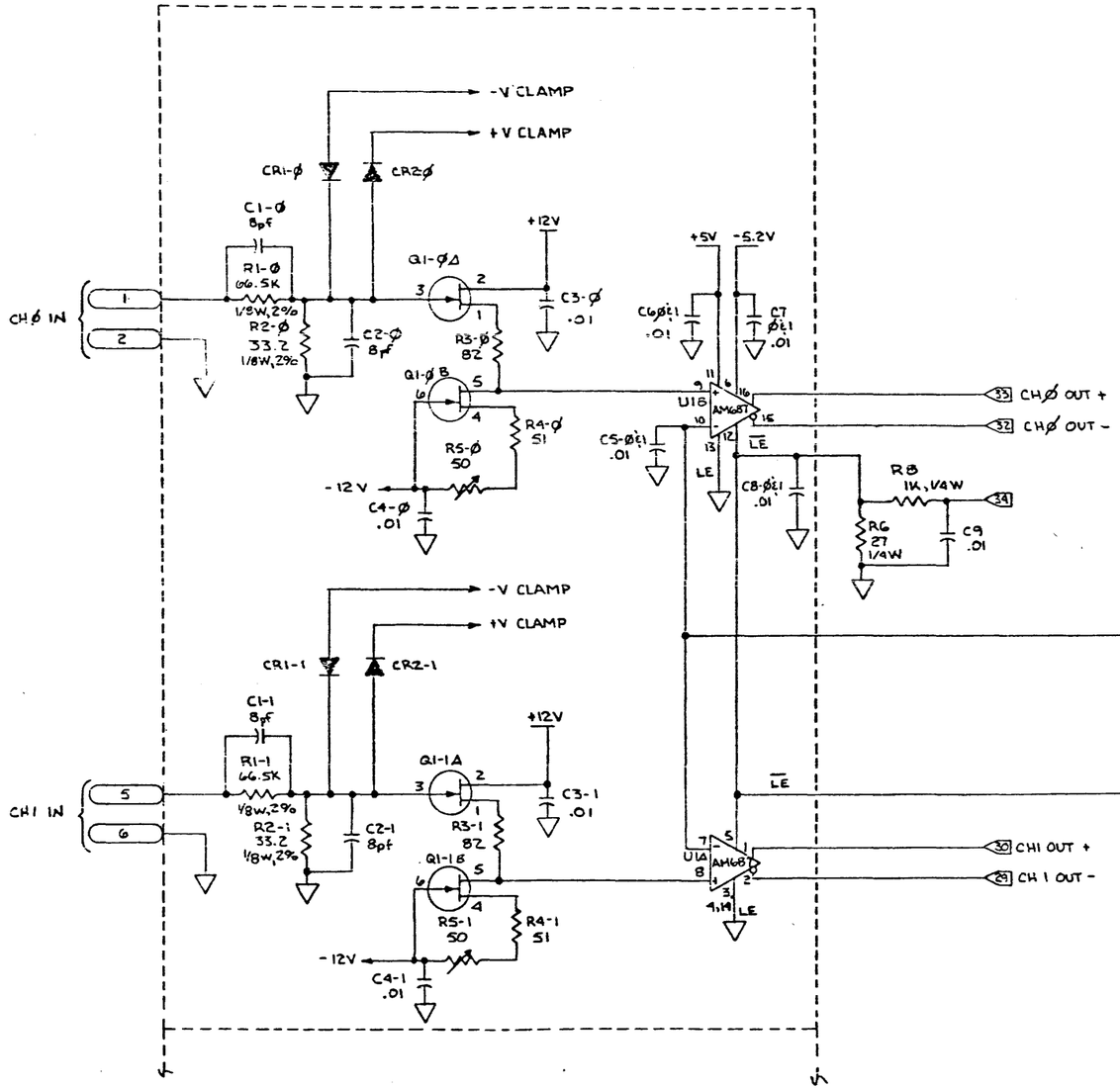
The schematic diagram, board layout, and parts list for the Model 80 Probe are contained on the following pages.

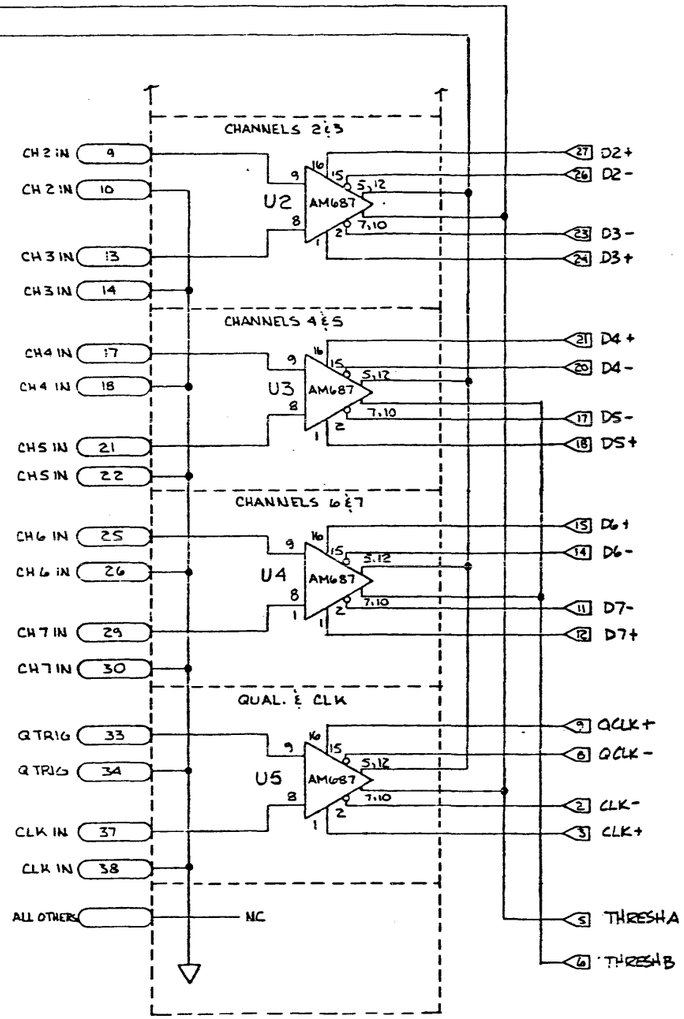
REV	DESCRIPTION	DATE	APPRO'VED

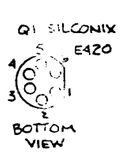


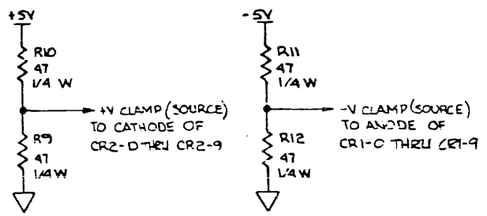
DRAWN BY: RCC	DATE: 12-27-79	PARATRONICS INC.	
CHECKED BY:	DATE:		
ENG: DMS	DATE: 12/15/79	DESCRIPTION: LEGENDMASTER 80 PROBE	
APPR. REL:	DATE:		
DECIMAL .XXX ± .005 .XX ± .02 FRACTIONAL ± 1/64 ANGULAR ± 0°30'		D	DRAWING NO: 126-0052-201 A
BREAK ALL SHARP EDGES		SCALE: 4/1	SHT: 1 OF 1 REV.
DO NOT SCALE DRAWING			

REV	DESCRIPTION	DATE	APPD
B	REVISED 179	12-1	

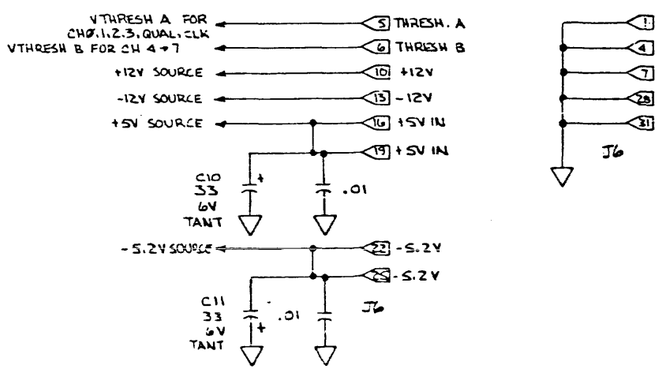








NOTES: UNLESS OTHERWISE SPECIFIED
2. ALL CAPS ARE IN. — FARRADS
1. ALL RES ARE 1/8 W, 5%.
3. ALL DIODES ARE IN3600



PARATRONICS INC.

SCHEMATIC DIAGRAM

Model 80 Probe

DRAWING NO. 127-0052-001 E

P A R A T R O N I C S I N C .

S I N G L E L E V E L E X P L O S I O N

09/05/80

PAR143-0052-0090-00 DESCRIPTION : MODEL 80 PROBE, OUTSIDE ECO#: 0 REV.CU.: A

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
111-0207-0103-00	D	22 UF 16V CAP. ELECTRO.,RAD.	2	1	0	08/21/80	OPEN	0	C10 C11
110-0205-0001-00	D	3329H-50, 50 OHM POT, BOURNS	10	1	0	OPEN	OPEN	0	R5-1 R5-10 R5-2 R5-3 R5-4 R5-5 R5-6 R5-7 R5-8 R5-9
117-0030-0001-00	D	TERMINAL, 120-1032-04, CAMBION	1	1	0	OPEN	OPEN	0	TP1
110-0002-0025-00	D	27 OHM 1/8 W,CF RESISTOR	1	1	0	OPEN	OPEN	0	R6
110-0005-0031-00	D	47 OHM 1/4 W 5% CF RES	4	1	0	OPEN	OPEN	0	R10 R11 R12 R9
110-0002-0063-00	D	1K 1/8W 5%	1	1	0	OPEN	OPEN	0	R8
110-0002-0032-00	D	510HM 1/8W 5%	10	1	0	OPEN	OPEN	0	R4-1 R4-10 R4-2 R4-3 R4-4 R4-5 R4-6 R4-7 R4-8 R4-9
110-0002-0037-00	D	820HM 1/8W 5%	10	1	0	OPEN	OPEN	0	R3-1 R3-10 R3-2 R3-3 R3-4 R3-5 R3-6 R3-7 R3-8 R3-9
110-0001-0099-00	D	33.2K 1/8W 2% RES	10	1	0	OPEN	OPEN	0	R2-1 R2-10 R2-2 R2-3 R2-4 R2-5 R2-6 R2-7 R2-8 R2-9
110-0001-0107-00	D	66.5K 1/8W 2% RES	10	1	0	OPEN	OPEN	0	R1-1 R1-10 R1-2 R1-3 R1-4 R1-5 R1-6 R1-7 R1-8 R1-9
111-0004-0066-00	D	.01 UF 25V CAP. CD	41	1	0	OPEN	OPEN	0	C3-1 C3-10 C3-2 C3-3 C3-4 C3-5 C3-6 C3-7 C3-8 C3-9 C4-1 C4-10 C4-2 C4-3 C4-4 C4-5 C4-6 C4-7 C4-8 C4-9 C5-1 C5-2 C5-3 C5-4 C5-5 C6-1 C6-2 C6-3 C6-4 C6-5 C7-1 C7-2 C7-3 C7-4 C7-5 C8-1 C8-2 C8-3 C8-4 C8-5 C9
111-0012-0010-00	D	8.2PF CERAMIC CAP	20	1	0	OPEN	OPEN	0	C1-1 C1-10 C1-2 C1-3 C1-4 C1-5 C1-6 C1-7 C1-8 C1-9 C2-1 C2-10 C2-2 C2-3 C2-4 C2-5 C2-6 C2-7 C2-8 C2-9
112-0204-0001-00	D	DIODE ,1N3600	20	1	0	OPEN	OPEN	0	D1-1 D1-10 D1-2 D1-3 D1-4 D1-5 D1-6 D1-7 D1-8 D1-9 D2-1 D2-10 D2-2 D2-3 D2-4 D2-5 D2-6 D2-7 D2-8 D2-9
112-0114-0001-00	D	XISTOR E420 SILICONIX	10	1	0	OPEN	OPEN	0	Q1-1 Q1-10 Q1-2 Q1-3 Q1-4 Q1-5 Q1-6 Q1-7 Q1-8 Q1-9
115-0005-0001-00	D	SOCKET,16PIN	5	1	0	OPEN	OPEN	0	U1 U2 U3 U4 U5
126-0052-0001-00	D	MODEL 80 PCB FAB	1	1	0	OPEN	OPEN	0	

LEGEND UM : 01=EACH 02=INCH 03=FEET 04=BULK 05=AS REQUIRED 06=OTHER
LEGEND KEY: A=W/PARTS LIST D=W/O PARTS LIST R=REFERENCE DOCUMENT S=SPECIFICATION

****

P A R A T R O N I C S I N C .

S I N G L E L E V E L E X P L O S I O N

09/05/80

PAR143-0052-0001-00 DESCRIPTION : MODEL 80 PCB ASSY ECO#: 0 REV.CU.: A

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
114-0003-0001-00	D	CONN.20PIN,DUAL,6-AA-02-20-1PX	1	1	0	OPEN	OPEN	0	
143-0052-0090-00	D	MODEL 80 PROBE, OUTSIDE	1	1	0	OPEN	OPEN	0	
113-0048-0001-00	D	AM687 I.C.	5	1	0	OPEN	OPEN	0	U1
U2 U3 U4 U5									
124-0029-0001-00	D	MODEL 80 CABLE ASSY	1	1	0	OPEN	OPEN	0	
117-1250-0005-00	D	4-40X 3/8PHMS,NYLON, SLOTTED	4	1	0	OPEN	OPEN	0	
119-0022-0001-00	D	MODEL 80 PROBE LABEL	1	1	0	OPEN	OPEN	0	
120-0001-0002-00	D	MODEL 80 BOTTOM COVER	1	1	0	OPEN	OPEN	0	
120-0002-0002-00	D	MODEL 80 TOP COVER	1	1	0	OPEN	OPEN	0	

LEGEND UM : 01=EACH 02=INCH 03=FEET 04=BULK 05=AS REQUIRED 06=OTHER
LEGEND KEY: A=W/PARTS LIST D=W/O PARTS LIST R=REFERENCE DOCUMENT S=SPECIFICATION

****

13.3 MODEL 90 PROBE

13.3.1 INTRODUCTION

The Model 90 Probe interfaces the Waveform Analyzer to the system under test. It is a high-quality oscilloscope probe selected for its suitability to this application.

13.3.2 FUNCTIONAL DESCRIPTION

The Model 90 Probe is a passive probe with a three position slide switch in the probe body. The three switch positions are: x 10 (10:1 attenuation); REF (ground reference); and x1 (1:1 attenuation). The probe specifications at the three switch positions are as follows:

x10 Position

Bandwidth:	dc to 100 MHz
Rise Time:	3.5 ns
Input Resistance:	10M ohm
Input Capacity:	12 pF
Working Voltage:	600 V dc, peak

REF Position

Input Resistance:	Probe tip, 9M ohm; analyzer input, grounded

x1 Position

Bandwidth:	dc to 10 MHz
Input Resistance:	1M ohm
Input Capacity:	70 pF
Working Voltage:	600 V dc, peak

13.3.3 ACCESSORIES

The following accessories are supplied as standard equipment:

- Insulating Tip
- Sprung Hook
- IC Adapter
- BNC Adapter
- Trimmer Tool

14.0 OPTIONS

14.1 SERIAL INTERFACE BOARD (RS-232-C, 20 mA)

14.1.1 INTRODUCTION

The Serial Interface Board (SIB) interfaces the PI 540 to remote RS-232-C or 20 mA current-loop peripheral devices. This option permits remote listing of data collected by the PI 540. The SIB interfaces to the bus and contains 2K bytes of PROM for the resident SIB software. The board can be configured for standard RS-232-C or 20 mA current-loop signal levels.

14.1.2 FUNCTIONAL DESCRIPTION

When appropriate during the following discussion, please refer to the schematic diagram, board layout, and parts list that are included at the end of this section.

Crystal Y1, IC U8, and baud rate select switches S1—S4, generate a clock 16 times the desired baud rate. This clock is applied to the RXC and TXC inputs of USART U5. U6 and U7 decode I/O and memory addresses and enable the interfacing of the 2K-byte SIB PROM U3 or the USART U5 to the PI 540 bus.

Transceiver U4 provides the necessary TTL buffering. USART U5 is initialized by the PI 540's 8085 microprocessor using the SIB software to provide full duplex serial data communication between the analyzer and the peripheral device.

Line receiver U1 converts signals DATA IN, DSR, and CTS from RS-232-C levels to TTL levels. U2 and Q1—Q3 convert the TTL output from U5 to RS-232-C levels of ±5 volts. Optional resistor R12 and jumpers J7 and J8 permit use of 20 mA current-loop signals instead of RS-232-C levels.

14.1.3 ALTERNATE CONFIGURATIONS

There are several alternate configurations and modifications possible for the Serial Interface Board:

a. Expanded software—For normal 2K SIB software, U6 pin 5 is connected via jumper J5 to A11. For expanded 4K software, U6 pin 5 is grounded via jumper J6.

b. Interrupt jumpers—The SIB has provisions for interrupt driven operations using jumpers J1—J4. Normal SIB software does not use the interrupt functions so these jumpers are left out.

c. RS-232-C signal level configuration (normally supplied from factory)—Resistor R12 is not present. Input and outputs are RS-232-C compatible.

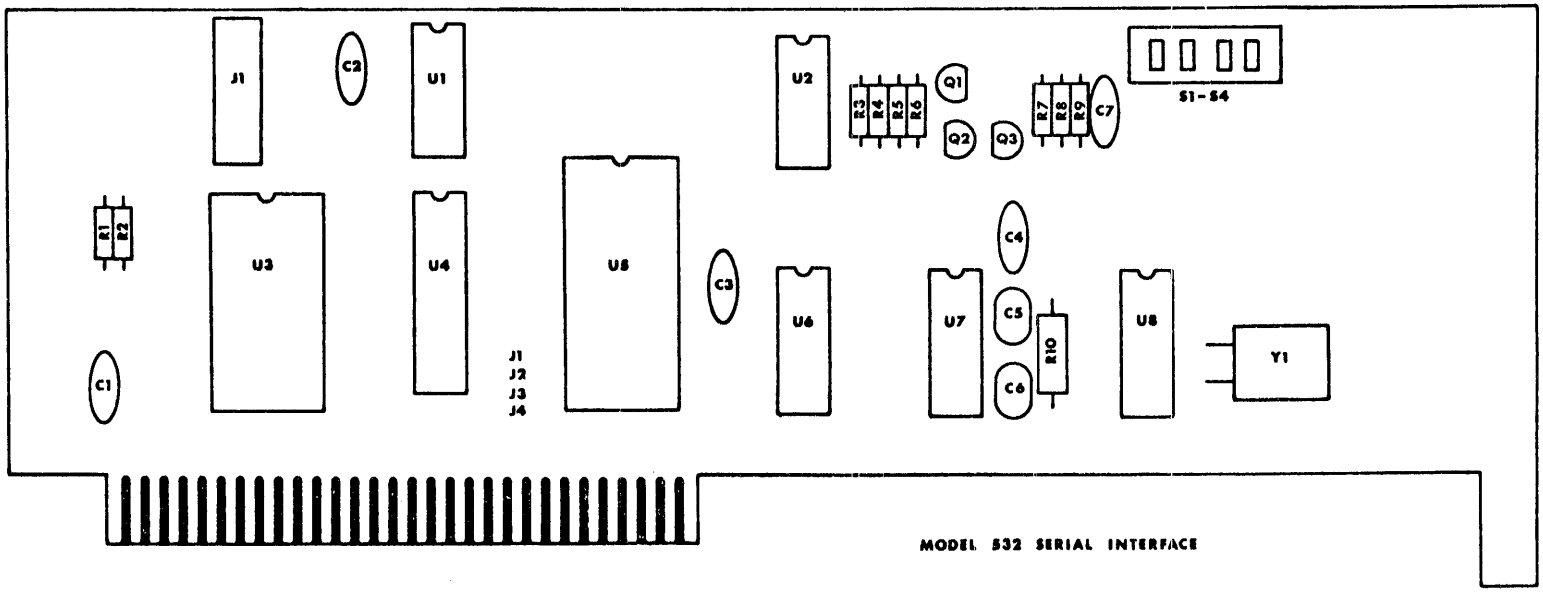
d. 20 mA current-loop configuration—Resistor R12 and jumpers J8 and J7 are installed. The 20 mA current loop is connected between pins 3

and 4 of the rear panel connector socket. The terminal keyboard (normally closed) is connected between pins 2 and 14 on the same socket.

e. Non-standard USART initialization—The SIB initialization software can be customized to provide different serial protocol.

14.1.4 SCHEMATIC, BOARD LAYOUT, & PARTS LIST

The schematic diagram, board layout, and parts list for the Serial Interface Board are contained on the following pages.



MODEL 532 SERIAL INTERFACE

PARATRONICS INC.	DRAWING NO. 126-0012-201			
TITLE: LEGENDMASTER, SERIAL INTERFACE	SCALE 2/1		REV.	
	DRAWN BY Ken	DATE	ENG	DATE
	CHECKED BY	DATE	APPR. REL.	DATE

RS-232/TTY SERIAL INTERFACE

UNUM	+5	GND
1	14	7
2	14	7
3	24	12
4	20	10
5	26	9
6	16	8
7	16	8
8	16	8

P/O P1

TRAP 24
RST 5.5 22
RST 6.5 53
RST 7.5 23

INTERRUPT JUMPERS J1 J2 J3 J4

BAUD RATE SELECT S1 S2 S3 S4

U8 34702: C6 47PF, C5 47PF, R10 10M 1/2W, Y1 2.4576MHZ, 16X CLK

RST 55

U5 8251: CLK RST RXC TXC; D0 D1 D2 D3 D4 D5 D6 D7; TXD RXRDY TXRDY SD/BD TxEMPTY; DSR CTS RXD; WR RD C/D CS

U4 8304: B0 B1 B2 B3 B4 B5 B6 B7 T/R CD; A0 A1 A2 A3 A4 A5 A6 A7

DB0 17
DB1 16
DB2 46
DB3 48
DB4 47
DB5 45
DB6 14
DB7 44

S1 18
WR 4
RD 3

R/W 56

U2

A00 10
A01 41
A02 7
A03 37
A04 42
A05 40
A06 9
A07 8
A08 13
A09 12
A10 11

U3 2716: A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 PGM; D0 D1 D2 D3 D4 D5 D6 D7; CS

+5V

U7 74LS138: G1 G2A C G2B A B; Y4

U2

A14 51
A15 20
A11 38

J5 J6

U6 74LS138: G1 G2A G2B A B C; Y0 Y7

A12 39
A13 21
IO/M 50

I/O ADDRESSES USED
(BOTH READ AND WRITE)

74 AND 75 (HEX)

MEMORY SPACE USED
4000 — 47FF (HEX)

74LS00 U2

Q2 2N3905, Q1 2N3905, Q3 2N3904

R4 4.7K, R5 11K, R3 4.7K, R6 11K, R7 470, R8 470, R9 4.7K, C7 0.1UF

TX

J7*

J1

14 DATA OUT RS232 (3)

U1 9617

R12* 470, R11* 470

11 DATA SET READY RS232 (6)

12 CLEAR TO SEND RS232 (5)

RX

15 DATA IN RS232 (2)

R1 470, R2 470

C1 0.1UF, C2 0.1UF, C3 0.1UF, C4 0.1UF, C7 0.1UF

13 RQST TO SEND RS232 (4)

7 DATA TERM RDY RS232 (20)

16 PROTECTIVE GROUND RS232 (1)

10 SIGNAL GROUND RS232 (7)

J8*

1 -5V RS232 (14)

NOTES: UNLESS OTHERWISE SPECIFIED

1. * INSTALL FOR 20 MA CURRENT LOOP
2. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 WATT

PARATRONICS INC.

127-0012-001 SERIAL INTERFACE

SIZE		INIT.	DATE	REV NO.	DATE
D	DRAWN	GFM	4/30/75	B	12/1/78
	CHECK	GFM	4/30/75		
	DESIGNER	M Mills	5/1/78		

PARATRONICS INC.

SINGLE LEVEL EXPLOSION

09/05/80

PAR143-0012-0090-00 DESCRIPTION : RS 232 PCB ASSY OUTSIDE ECO#: 0 REV.CU.: C

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
111-0004-0072-00	D	.1 UF 25V CAP. CD	5	1	0	OPEN	OPEN	0	C1
C2 C3 C4 C7									
126-0012-0001-00	D	RS 232 PCB FAB	1	1	0	OPEN	OPEN	0	
116-0001-0001-00	D	SWITCH, SPST, 76TC04,GRAYHILL	1	1	0	OPEN	OPEN	0	S1
S2 S3 S4									
115-0012-0001-00	D	SOCKET,28PIN	1	1	0	OPEN	OPEN	0	U5
115-0011-0001-00	D	SOCKET,24PIN	1	1	0	OPEN	OPEN	0	U3
115-0009-0001-00	D	SOCKET,20PIN	1	1	0	OPEN	OPEN	0	U4
115-0005-0001-00	D	SOCKET,16PIN	4	1	0	OPEN	OPEN	0	J1
U6 U7 U8									
115-0003-0001-00	D	SOCKET,14PIN	2	1	0	OPEN	OPEN	0	U1
U2									
112-0300-0001-00	D	CRYSTAL, 2.4576 MHZ, MP2PR	1	1	0	OPEN	OPEN	0	Y1
112-0101-0001-00	D	TRANSISTOR, 2N3905	2	1	0	OPEN	OPEN	0	Q1
Q2									
112-0100-0001-00	D	TRANS STOR, 2N3904	1	1	0	OPEN	OPEN	0	Q3
111-0012-0022-00	D	47 P 1KV CAP. CD	2	1	0	OPEN	OPEN	0	C5
C6									
110-0007-0161-00	D	10M OHM 1/2 W CF RES	1	1	0	OPEN	OPEN	0	R10
110-0005-0088-00	D	11K 1/4 W 5% CF RES	2	1	0	OPEN	OPEN	0	R5
R6									
110-0005-0079-00	D	4.7 K OHM 1/4 W CF RES	3	1	0	OPEN	OPEN	0	R31
R4 R9									
110-0005-0075-00	D	3.3 K OHM 1/4 W CF RES	1	1	0	OPEN	OPEN	0	R11
110-0005-0055-00	D	470 OHM 1/4W 5% CF RES	4	1	0	OPEN	OPEN	0	R1
R2 R7 R8									

LEGEND UM : 01=EACH 02=INCH 03=FEET 04=BULK 05=AS REQUIRED 06=OTHER
LEGEND KEY: A=W/PARTS LIST D=W/O PARTS LIST R=REFERENCE DOCUMENT S=SPECIFICATION

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P A R A T R O N I C S I N C .

S I N G L E L E V E L E X P L O S I O N

09/05/80

PAR143-0012-0001-00 DESCRIPTION / RS232 PCB ASY.IN HOUSE ECO#: 0 REV.CU.:

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
113-0037-0001-00	D	IC, 1489L	1	1	0	04/21/80	OPEN	0	U1
143-0012-0090-00	D	RS 232 PCB ASSY OUTSIDE	1	1	0	OPEN	OPEN	0	
113-0014-0001-00	D	I.C., DP8304N, NSC, AMD,	1	1	0	OPEN	OPEN	0	U4
113-0012-0001-00	D	I.C., P8251, INT., NEC.	1	1	0	OPEN	OPEN	0	U5
113-0009-0001-00	D	I.C., F4702BPC	1	1	0	OPEN	OPEN	0	U8
113-0020-0001-00	D	I.C., CN13025,(2616) SIG	1	1	0	OPEN	OPEN	0	U3
113-0003-0138-00	D	I.C., 74LS138	2	1	0	OPEN	OPEN	0	U6
U7									
113-0003-0000-00	D	I.C., 74LS00	1	1	0	OPEN	OPEN	0	U2

LEGEND UM : 01=EACH 02=INCH 03=FEET 04=BULK 05=AS REQUIRED 06=OTHER
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14.2 GPIB INTERFACE BOARD (IEEE-488-1978)

14.2.1 INTRODUCTION

The GPIB (General Purpose Interface Bus) Interface is contained on a standard PI 540 Microcomputing Section PC board. It can reside in any card slot on the Microcomputing Motherboard and connects via a flat ribbon cable to a GPIB connector on the chassis rear panel. The GPIB Interface Board contains the hardware interface between the PI 540 bus and the GPIB as well as up to 4K bytes of software which determines bus protocol.

14.2.2 FUNCTIONAL DESCRIPTION

When appropriate during the following discussion, please refer to the State Diagram, figure 14.2-1, and to the schematic diagram, board layout, and parts list that are included at the end of this section.

U10 and U13 decode the PROM address and the MC68488 I/O ports and generate the appropriate chip selects and bus buffer enable signals. U4 provides the necessary handshaking for communications on the GPIB, as well as buffering the actual transferred data. The interface to the bus is accomplished through U2, U3, U5, and U6 which are bus drivers designed specifically for the GPIB. These buffers normally operate in the open-collector mode, which is required if a parallel-poll operation is to be performed. If 3-state operation is desired, a jumper may be opened.

Upon a Read-Address-Switch-Register command to the MC68488, one-half of U1 feeds the Interface Address Select Switches to the data bus. The other half of U1 is used for inverters. The circuits consisting of U11, U12, U13, and U15 form a pair of state machines used to synchronize the operation of the MC68488 GPIA (General Purpose Interface Adapter) to the PI 540's 8085 processor. U14 divides the 8085 clock to a frequency compatible with the MC68488 and provides clock phase (Ø0 and Ø3) information for the state machines.

The chip select sync state machine holds off the MC68488 address select (488SEL-) from the 8085 until the MC68488 clock goes high (Ø0 time). The chip select is then held low until 488SEL- goes high.

The MC68488 is too slow to run directly as an 8085 peripheral so it operates semi-asynchronously to the 8085. A RW sync state machine is required for 8085 accesses to the MC68488 to be performed properly. This machine pulls the READY line low one state time after the MC68488 is accessed, to hold the processor in its read/write operation. It then waits until just before the MC68488 clock goes low (read), or just after (write), before letting the READY line go high again. This provides the proper synchronization between the MC68488 and the 8085.

14.2.3 ALTERNATE CONFIGURATIONS

A jumper is provided to allow either open collector or active (3-state) interface to the GPIB. For those systems employing parallel polling, open

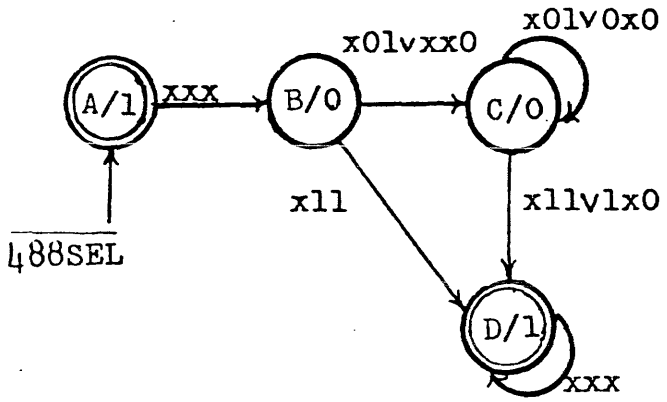
collector operation is required. The board is normally shipped from the factory in the open collector configuration (with jumper installed).

14.2.4 SCHEMATIC, BOARD LAYOUT, & PARTS LIST

The schematic diagram, board layout, and parts list for the GPIB Interface Board are contained on the following pages.

RW SYNC: INPUTS: $\phi 0, \phi 3, \overline{WR}, (\overline{488\ SEL})$ CLOCK: 8085 CLOCK

OUTPUTS: RDY U12, U13, U15

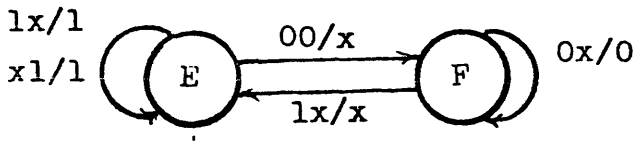


STATE	Q2	Q1	RDY	
A	0	0	1	SOURCE STATE
B	0	1	0	SET RDY LOW
C	1	1	0	HOLD RDY LOW UNTIL ACCESS SYNC'D.
D	1	0	1	SINK STATE

CHIP SELECT SYNC: INPUTS: $\overline{488SEL}, \overline{\phi 0}$

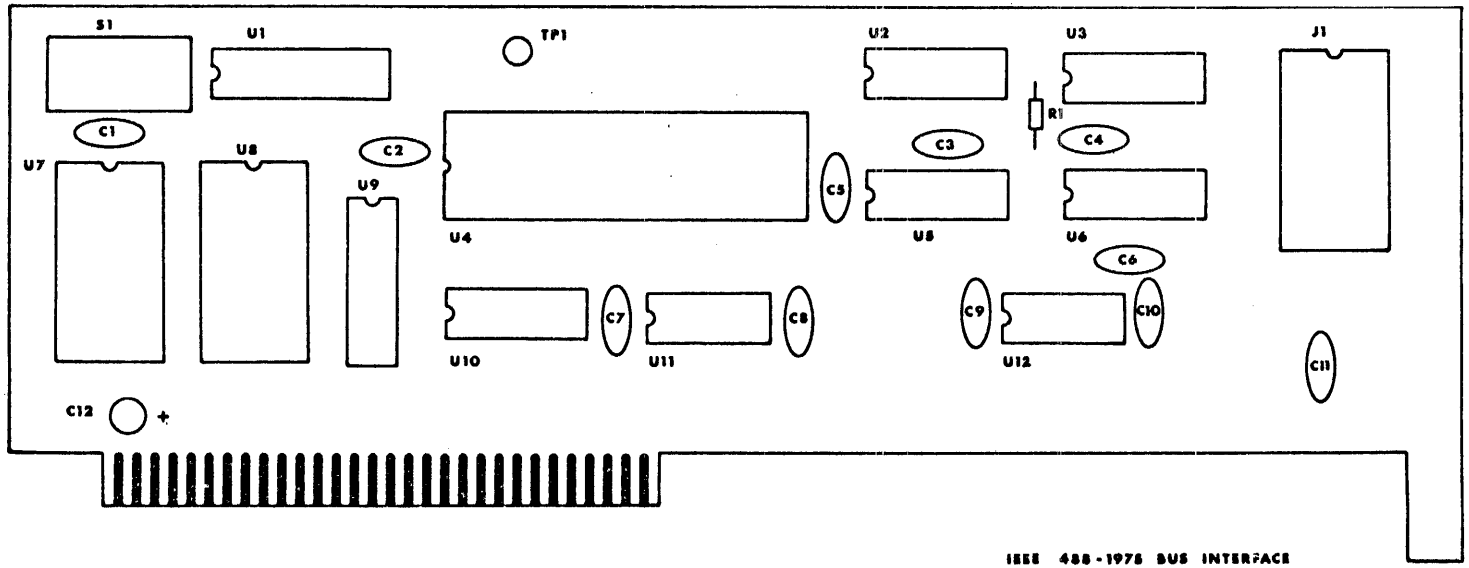
OUTPUTS: $\overline{CS\ 488}$

U11, U12



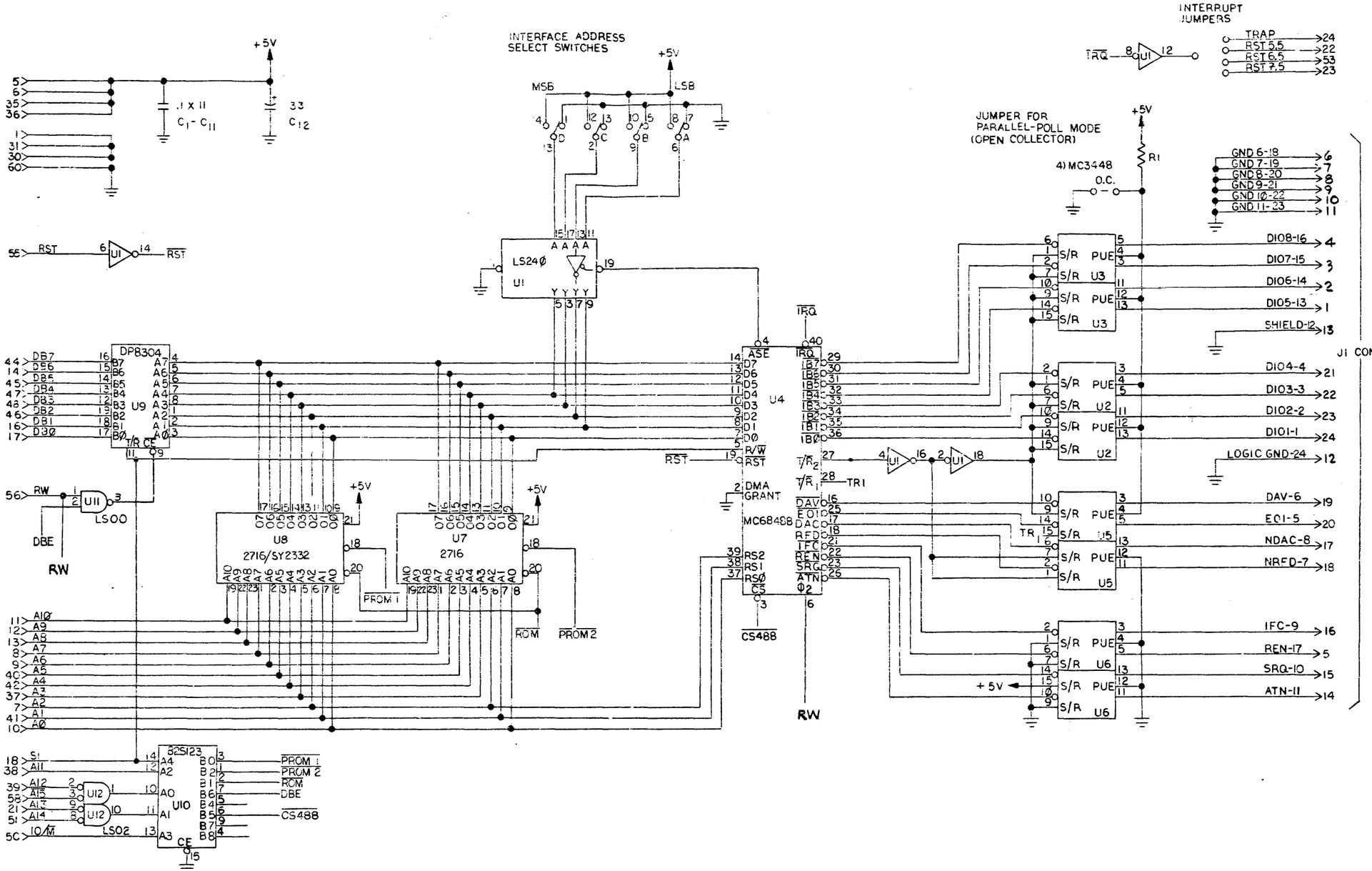
STATE DIAGRAM.

REV	DESCRIPTION	DATE	APPROVED
C	REVISED PER ECO 135	8-20-80	



IEEE 488-1978 BUS INTERFACE

DRAWN BY: [illegible]	DATE: 5-20-80	PARATRONICS INC.	
CHECKED BY	DATE		
ENG	DATE	DESCRIPTION: LEGENDMASTER IEEE 488-1975 BUS INTERFACE	
APPR REL	DATE		
DECIMAL XXX = ±.005 XX = ±.02 FRACTIONAL ± 1/64 ANGULAR ± 0°30'		C	DRAWING NO 126-0013-201 C
BREAK ALL SHARP EDGES			SCALE 2:1 SHT 1 OF 1 REV
DO NOT SCALE DRAWING			



REVISIONS			
REV	DATE	DESCRIPTION	APP'D
A	2-22-80	REV PER ECO 119	WDS
B	3-13-80	REV PER ECO 135	WDS

	IC	+5	GND
U4	68488	20	1
U7, U8	2716	24	12
U9	DP8304	20	10
U2,3,5,6	MC3448	16	8
U1	74LS240	20	10
U11	74LS00	14	7
U12	74LS02	14	7
U10	82S123	16	8

NOTES: UNLESS OTHERWISE SPECIFIED

1) ALL RESISTORS 4.7K 1/4 W
2) ALL CAPACITORS ARE IN MICROFARADS

TOLERANCES (EXCEPT AS NOTED): DECIMAL ± FRACTIONAL ± ANGULAR ±

REVISIONS			
NO	DATE	BY	
1	[illegible]	WDS	
2			
3			
4			
5			

PARATRONICS INC.

IEEE 488-1975 BUS INTERFACE

SCHEMATIC ASSEMBLY 143-0013-001

DRAWN BY [illegible] SCALE — MATERIAL

CHK'D W. Swan DATE DRAWING NO. 127-0013-001

APP'D [illegible]

P A R A T R O N I C S I N C .

S I N G L E L E V E L E X P L O S I O N

09/05/80

PAR143-0013-0090-00 DESCRIPTION : IEEE 488 PCB ASY OUTSIDE ECO#: 0 REV.CU.:

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
111-0207-0103-00	D	22 UF 16V CAP. ELECTRO.,RAD.	1	1	0	08/21/80	OPEN	0	C12
126-0013-0001-00	D	IEEE 488PCB FAB	1	1	0	OPEN	OPEN	0	
117-0030-0001-00	D	TERMINAL, 120-1032-04, CAMBION	1	1	0	OPEN	OPEN	0	
116-0001-0001-00	D	SWITCH, SPST, 76TC04,GRAYHILL	1	1	0	OPEN	OPEN	0	S1
115-0013-0001-00	D	SOCKET,40PIN	1	1	0	OPEN	OPEN	0	U4
115-0011-0001-00	D	SOCKET,24PIN	2	1	0	OPEN	OPEN	0	J1
U7									
115-0009-0001-00	D	SOCKET,20PIN	2	1	0	OPEN	OPEN	0	U1
U9									
115-0005-0001-00	D	SOCKET,16PIN	5	1	0	OPEN	OPEN	0	U10
U2 U3 U5 U6									
115-0003-0001-00	D	SOCKET,14PIN	5	1	0	OPEN	OPEN	0	U11
U12 U13 U14 U15									
111-0004-0072-00	D	.1 UF 25V CAP. CD	11	1	0	OPEN	OPEN	0	C1
C10 C11 C2 C3 C4 C5 C6 C7 C8 C9									
110-0005-0079-00	D	4.7 K OHM 1/4 W CF RES	4	1	0	OPEN	OPEN	0	R1
R2 R3 R4									

LEGEND UM : 01=EACH 02=INCH 03=FEET 04=BULK 05=AS REQUIRED 06=OTHER
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P A R A T R O N I C S I N C .

S I N G L E L E V E L E X P L O S I O N

09/05/80

PAR143-0013-0001-00 DESCRIPTION : IEEE PCB ASY.IN HOUSE ECO#: 0 REV.CU.:

PART NUMBER	KEY	PART DESCRIPTION	QTY. PER	UM	CON. CD	EFFECTIVITY START	EFFECTIVITY STOP	ECO#	
115-0052-0002-00	D	STAND OFF, AMPHENOL	2	1	0	OPEN	OPEN	0	
124-0010-0001-00	D	IEEE-488 CABLE ASSY, M532	1	1	0	OPEN	OPEN	0	
143-0013-0090-00	D	IEEE 488 PCB ASY OUTSIDE	1	1	0	OPEN	OPEN	0	
113-0007-0001-00	D	I.C., 2716	1	1	0	OPEN	OPEN	0	U7
113-0034-0002-00	D	I.C., 6331-1(34-002).N82S123F	1	1	0	OPEN	OPEN	0	U10
113-0032-0001-00	D	I.C., MC3448AP, MOT	4	1	0	OPEN	OPEN	0	U2
U3 U5 U6									
113-0031-0001-00	D	I.C., MC68488P, MOT	1	1	0	OPEN	OPEN	0	U4
113-0014-0001-00	D	I.C., DP8304N, NSC, AMD,	1	1	0	OPEN	OPEN	0	U9
113-0003-0240-00	D	I.C., 74LS240	1	1	0	OPEN	OPEN	0	U1
113-0003-0073-00	D	I.C., 74LS73	1	1	0	OPEN	OPEN	0	U15
113-0003-0051-00	D	I.C., 74LS51	1	1	0	OPEN	OPEN	0	U12
113-0003-0002-00	D	I.C., 74LS02	1	1	0	OPEN	OPEN	0	U13
113-0002-0074-00	D	I.C., 74S74	1	1	0	OPEN	OPEN	0	U14
113-0001-0001-00	D	I.C., 7401	1	1	0	OPEN	OPEN	0	U11

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LEGEND KEY: A=W/PARTS LIST D=W/O PARTS LIST R=REFERENCE DOCUMENT S=SPECIFICATION

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15.0 SIGNAL & INTERCONNECTION TABLES

15.0 SIGNAL AND INTERCONNECTION TABLES

15.1 INTRODUCTION

The following tables are available for reference as needed:

Table 1, Interboard Signals —a list of all signals that go between circuit boards. The list is arranged alphabetically by signal acronym. Each entry comprises the signal acronym, the expanded signal name, and the source and destination connector pins.

Table 2, Microcomputer S1 Connector —the pin-out for all the S1 connectors on the Microcomputer Motherboard. The table is arranged by pin number and gives signal acronyms only. For signal name expansion or source and destination information on a particular signal, please refer to table 1.

Table 3, Function S1 Connector —the pin-out for all the S1 connectors on the Function Motherboard. The table is arranged the by pin number and gives signal acronyms only.

Table 4; J3 Connector, Function Motherboard; J2 Connector, Microcomputer Motherboard —the pin-out of the two connectors for the interconnecting cable between the two motherboards. For cross-reference purposes, the table also lists, for each signal acronym, the corresponding MS1 and FS1 connector pins (regarding MS1 and FS1, please refer to the symbol explanation given later in this Introduction).

Table 5; S2 Connectors, Function Motherboard —the pin-out for each S2 connector on the Function Motherboard. The table consists of signal acronyms arranged in a matrix of pin-number x circuit-board-name (and slot letter).

Table 6; J4 Connector, State Probe, B Channel —the pin-out for connector J4, State inputs from the Model 51A Probe for the B channel.

Table 7; J5 Connector, State Probe, A Channel —the pin-out for connector J5, State inputs from the Model 51A Probe for the A channel.

Table 8; J6 Connector, Timing Probe —the pin-out for connector J6, the Timing input from the Model 80 Probe.

Table 9; J7 Connector, Self-Test Data/Status —the pin-out for connector J7, the Self Test output for Data and Status information.

Table 10; J8 Connector, Self-Test Address —the pin-out for connector J8, the Self Test output for Address information.

Table 11; J14 Connector, Video Display; J11 Connector, Display Module; J12 Connector, Display Module —a composite pin-out of connectors J11, J12, and J14 showing the interconnections between these three connectors. J11 connects to the Display Module and is wired to J12 and P14; J12 mates to P12 in a two-conductor cable coming from the Power Supply; and J14 is on the Video Display Board. (Please refer to the Connector/Cables Diagram in section 2.1, Chassis, for further details.)

Table 12; J21 Connector, Waveform; J15 Connector, Video Display —the pin-out for connectors J15 and J21 that terminate an interconnecting cable carrying video-related signals between the Video Display Board and the Waveform board.

Table 13; J10 Connector, Keyboard; J1 Connector, Microcomputer Motherboard —the pin-out for connectors J1 and J10 that terminate an interconnecting cable carrying keyboard signals between the Microcomputer Motherboard and the Keyboard Interface Board. (J10 is actually a hole pattern on the Keyboard Interface Board into which a header on the cable is soldered.)

Table 14; J9 Connector, Function Motherboard Power —the pin-out of the Function Motherboard connector J9, which terminates a cable bringing power from the Power Supply.

Table 15; P13 Connector, Power Supply —the pin-out for connector P13, which terminates a cable hard-wired to the Power Supply. P13 connects to J13, a connector that terminates a cable bringing input voltages to the Power Supply from the Chassis.

Following is an explanation of the symbols used in these tables to designate the connector pins:

MS1-35 —the M indicates the Microcomputer Motherboard; the S1 is the connector designator; and the 35 is the pin number. (Recall that the S1 connections for all circuit boards in the Microcomputer Section are the same.)

FS1-35 —the F indicates the Function Motherboard. The function of the remaining characters is the same as above. (The S1 connections for all circuit boards in the Applications Section are the same; but the FS1 connections are different from the MS1 connections.)

S2B-35 —the B indicates the B slot in the Function Motherboard. (The S2 connections are different for each board in the Applications Section. There is no S2 in the Microcomputer Section.)

J8-35 —the J8 is the connector designator. The leter J is used for board-mounted connectors that accept mating connectors that terminate a cable; the letter S is used for board-mounted connectors that accept the edge-connector of another PC board. (J is also used for cable-terminating connectors. but S is not.)

The slot assignments for the circuit boards in the Applications Section are repeated here for convenient reference when using table 1:

Slot	Circuit Board
G (Front)	Spare, for expansion
F	State Memory Board, B Group
E	State Control Board
D	State Memory Board, A Group
C	Timing Control Board
B	Timing Memory Board
A	Waveform Board

15.2 TABLES

The tables described in the preceding paragraphs are presented on the following pages.

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TABLE 1

INTERBOARD SIGNALS

Destination	Source	Signal	Name Expansion
J8-1, FS1-55	MS1-10	A0	Processor Address Bus, bit 0
J8-2, FS1-24	MS1-41	A1	Processor Address Bus, bit 1
J8-3, FS1-58	MS1-7	A2	Processor Address Bus, bit 2
J8-4, FS1-28	MS1-37	A3	Processor Address Bus, bit 3
	MS1-59	A3-	Processor Address, bit 3-
J8-5, FS1-23	MS1-42	A4	Processor Address Bus, bit 4
J8-6, FS1-25	MS1-40	A5	Processor Address Bus, bit 5
J8-7, FS1-56	MS1-9	A6	Processor Address Bus, bit 6
J8-8, FS1-57	MS1-8	A7	Processor Address Bus, bit 7
J8-9, FS1-52	MS1-13	A8	Processor Address Bus, bit 8
J8-10, FS1-53	MS1-12	A9	Processor Address Bus, bit 9
J8-11, FS1-54	MS1-11	A10	Processor Address Bus, bit 10
J8-12, FS1-27	MS1-38	A11	Processor Address Bus, bit 11
J8-13, FS1-26	MS1-39	A12	Processor Address Bus, bit 12
J8-14, FS1-44	MS1-21	A13	Processor Address Bus, bit 13
J8-15, FS1-14	MS1-51	A14	Processor Address Bus, bit 14
J8-16, FS1-45	MS1-20	A15	Processor Address Bus, bit 15
	MS1-58	A15-	Processor Address, bit 15-
S2D-7	S2E-7	ACLKINH+	Clock Inhibit, A channel
S2D-37	S2E-8	ACLKQUALIN-	Clock Qualifier In, A channel
J5-4	S2E-24	ACLKSEL	Clock Select, A channel
J5-9	S2E-27	ACONTROL	(for future use)
S2E-21	S2D-19	ACQ1	Clock Qual-word-1 match, A ch
S2E-22	S2D-18	ACQ2	Clock Qual-word-2 match, A ch
#S2E-6	S2D-6	ADLYWE-	Delayed Write Enable, A chan
S2D-4	S2E-4	ALATCHCLK	Latch Clock, A channel
FS1-50	MS1-15	ALE	Address Latch Enable (8085)
S2A-29	*BNC	ANALOGIN	Waveform analog signal in
S2D-56	J5-20	APD0	A Probe Data, bit 0, State
S2D-54	J5-22	APD1	A Probe Data, bit 1, State
S2D-55	J5-21	APD2	A Probe Data, bit 2, State
S2D-29	J5-16	APD3	A Probe Data, bit 3, State
S2D-53	J5-23	APD4	A Probe Data, bit 4, State
S2D-57	J5-19	APD5	A Probe Data, bit 5, State
S2D-52	J5-24	APD6	A Probe Data, bit 6, State
S2D-51	J5-25	APD7	A Probe Data, bit 7, State
S2D-58	J5-18	APD8	A Probe Data, bit 8, State
S2D-59	J5-17	APD9	A Probe Data, bit 9, State
S2D-28	J5-15	APD10	A Probe Data, bit 10, State
S2D-27	J5-14	APD11	A Probe Data, bit 11, State
S2D-26	J5-13	APD12	A Probe Data, bit 12, State
S2D-23	J5-8	APD13	A Probe Data, bit 13, State
S2D-24	J5-10	APD14	A Probe Data, bit 14, State
S2D-25	J5-11	APD15	A Probe Data, bit 15, State
S2E-23	J5-2	APROBCLK	Probe Clock, A channel
S2D-14	S2E-43	APROBDREN-	Probe Data Remote Enable, A

Destination	Source	Signal	Name Expansion
S2D-21, S2E-25	J5-5	AQ1	Probe Qualifier bit 1, A chan
S2D-22	J5-7	AQ2	Probe Qualifier bit 2, A chan
J5-6	S2E-26	AQCLKSEL	Clock Qualifier Select, A cha
	@S2D-20	ARMA	State Arm-word match (TTL), A
	@S2F-20	ARMB	State Arm-word match (TTL), B
S2E-47	S2D-17	ARST	RESTART-word match, A channel
S2E-45	S2D-16	ATRIG+	Trigger-word match, A channel
#S2E-5	S2D-5	AWE+	Write Enable, A channel
J10-9	J1-9	BA0+	Buffered Address Bus, bit 0+
J10-6	J1-6	BA0-	Buffered Address Bus, bit 0-
J10-5	J1-5	BA1-	Buffered Address Bus, bit 1-
J10-7	J1-7	BA2-	Buffered Address Bus, bit 2-
J10-8	J1-8	BA3-	Buffered Address Bus, bit 3-
S2F-7	S2E-38	BCLKINH+	Clock Inhibit, B channel
S2F-37	S2E-39	BCLKQUALIN-	Clock Qualifier In, B channel
J4-4	S2E-56	BCLKSEL	Clock Select, B channel
S2E-53	J4-9	BCONTROL	(for future use)
S2E-51	S2F-19	BCQ1	Clock Qual-word-1 match, B ch
S2E-52	S2F-18	BCQ2	Clock Qual-word-2 match, B ch
J1-12	J10-12	BDB0	Buffered Data Bus, bit 0
J1-13	J10-13	BDB1	Buffered Data Bus, bit 1
J1-14	J10-14	BDB2	Buffered Data Bus, bit 2
J1-15	J10-15	BDB3	Buffered Data Bus, bit 3
J1-16	J10-16	BDB4	Buffered Data Bus, bit 4
J1-17	J10-17	BDB5	Buffered Data Bus, bit 5
J1-18	J10-18	BDB6	Buffered Data Bus, bit 6
J1-19	J10-19	BDB7	Buffered Data Bus, bit 7
S2E-37	S2F-6	BDLYWE-	Delayed Write Enable, B chan
S2F-4	S2E-34	BLATCHCLK	Latch Clock, B channel
S2F-56	J4-20	BPD0	B Probe Data, bit 0, State
S2F-54	J4-22	BPD1	B Probe Data, bit 1, State
S2F-55	J4-21	BPD2	B Probe Data, bit 2, State
S2F-29	J4-16	BPD3	B Probe Data, bit 3, State
S2F-53	J4-23	BPD4	B Probe Data, bit 4, State
S2F-57	J4-19	BPD5	B Probe Data, bit 5, State
S2F-52	J4-24	BPD6	B Probe Data, bit 6, State
S2F-51	J4-25	BPD7	B Probe Data, bit 7, State
S2F-58	J4-18	BPD8	B Probe Data, bit 8, State
S2F-59	J4-17	BPD9	B Probe Data, bit 9, State
S2F-28	J4-15	BPD10	B Probe Data, bit 10, State
S2F-27	J4-14	BPD11	B Probe Data, bit 11, State
S2F-26	J4-13	BPD12	B Probe Data, bit 12, State
S2F-23	J4-8	BPD13	B Probe Data, bit 13, State
S2F-24	J4-10	BPD14	B Probe Data, bit 14, State
S2F-25	J4-11	BPD15	B Probe Data, bit 15, State
S2E-57	J4-2	BPROBCLK	Probe Clock, B channel
S2F-14	S2E-44	BPROBDREN-	Probe Data Remote Enable, B
S2F-21, S2E-55	J4-5	BQ1	Probe Qualifier bit 1, B chan
S2F-22	J4-7	BQ2	Probe Qualifier bit 2, B chan
J4-6	S2E-54	BQCLKSEL	Clock Qualifier Select, B cha
S2E-48	S2F-17	BRST	RESTART-word match, B channel

Destination	Source	Signal	Name Expansion
@S2D-15, S2F-15		BSELECT-	Selects Bd B by GND at S2F-15
S2E-46	S2F-16	BTRIG+	Trigger-word match, B channel
S2E-35	S2F-5	BWE+	Write Enable, B channel
	J15-5	CCLK-	Character Clock- (Video)
FS1-11	MS1-54	CLK	Clock (8085)
S2C-56	J6-3	CLK+	Clock+, Timing
S2C-55	J6-2	CLK-	Clock-, Timing
S2B-43	S2C-43	CLKTTL	Delayed CT Clock, TTL level
S2A-6, S2B-6, S2E-36	S2C-6	CT	Selected Clock, Timing
S2B-52	J6-33	D0+	Timing Probe Data, bit 0+
S2B-53	J6-32	D0-	Timing Probe Data, bit 0-
S2B-54	J6-30	D1+	Timing Probe Data, bit 1+
S2B-55	J6-29	D1-	Timing Probe Data, bit 1-
S2B-56	J6-27	D2+	Timing Probe Data, bit 2+
S2B-57	J6-26	D2-	Timing Probe Data, bit 2-
S2B-58	J6-24	D3+	Timing Probe Data, bit 3+
S2B-59	J6-23	D3-	Timing Probe Data, bit 3-
S2B-29	J6-21	D4+	Timing Probe Data, bit 4+
S2B-28	J6-20	D4-	Timing Probe Data, bit 4-
S2B-27	J6-18	D5+	Timing Probe Data, bit 5+
S2B-26	J6-17	D5-	Timing Probe Data, bit 5-
S2B-25	J6-15	D6+	Timing Probe Data, bit 6+
S2B-24	J6-14	D6-	Timing Probe Data, bit 6-
S2B-23	J6-12	D7+	Timing Probe Data, bit 7+
S2B-22	J6-11	D7-	Timing Probe Data, bit 7-
J7-1, FS1-48	MS1-17	DB0	Processor Data Bus, bit 0
J7-2, FS1-49	MS1-16	DB1	Processor Data Bus, bit 1
J7-3, FS1-19	MS1-46	DB2	Processor Data Bus, bit 2
J7-4, FS1-17	MS1-48	DB3	Processor Data Bus, bit 3
J7-5, FS1-18	MS1-47	DB4	Processor Data Bus, bit 4
J7-6, FS1-20	MS1-45	DB5	Processor Data Bus, bit 5
J7-7, FS1-51	MS1-14	DB6	Processor Data Bus, bit 6
J7-8, FS1-21	MS1-44	DB7	Processor Data Bus, bit 7
J21-2	J15-2	DCLK2	Dot Clock 2 (Video)
S2C-12, S2D-12, S2F-12	*BNC	EXT	External trigger signal
J15-4	J21-4	EXTVID-	External Video- (Waveform)
J10-4,	J1-4	FPENB-	Front Panel Enable-
*BNC , S2C-42	S2E-42	FS	State trigger conditions met
*BNC, S2D-11, S2F-11	S2C-11	FT	Timing trigger conditions met
(Many)		GND	Signal and Power Ground
FS1-7	MS1-28	HLDA	Hold Acknowledge (8085)
MS1-26	FS1-39	HOLD	Hold (8085)
J21-1	J15-1	HRTC-	Horizontal Retrace- (Video)
J6-34	S2B-15	HYST	Hysteresis control, Timing
J7-12, FS1-37	MS1-29	INTA-	Interrupt Asknowledge (8085)
MS1-52	FS1-13	INTR	Interrupt Request (8085)
J1-3, J10-3, FS1-8	MS1-57	IOEN-	I/O Enable
J7-17, J8-18, FS1-15	MS1-50	IO+/M-	Input/Output+ or Memory-
J7-11			
S2C-58	J6-9	QCLK+	Clock Qualifier +, Timing
S2C-57	J6-8	QCLK-	Clock Qualifier -, Timing

Destination	Source	Signal	Name Expansion
S2D-46, S2F-46	S2E-16	RA0	RAM Address, bit 0, State
S2D-45, S2F-45	S2E-15	RA1	RAM Address, bit 1, State
S2D-44, S2F-44	S2E-14	RA2	RAM Address, bit 2, State
S2D-43, S2F-43	S2E-13	RA3	RAM Address, bit 3, State
S2D-42, S2F-42	S2E-12	RA4	RAM Address, bit 4, State
S2D-41, S2F-41	S2E-11	RA5	RAM Address, bit 5, State
S2D-40, S2F-40	S2E-10	RA6	RAM Address, bit 6, State
S2D-39, S2F-39	S2E-9	RA7	RAM Address, bit 7, State
J7-18, J8-17, FS1-59	MS1-3	RD-	Read (8085)
MS1-27	FS1-38	RDY	Ready (8085)
FS1-10	MS1-55	RST	RESET OUT (8085)
MS1-22	FS1-43	RST 5.5	Interrupt, RESTART at 002CH
MS1-53	FS1-12	RST 6.5	Interrupt, RESTART at 0034H
MS1-23	FS1-42	RST 7.5	Interrupt, RESTART at 003CH
J7-19, J8-19, FS1-9	MS1-56	RW	Read or Write
J8-9, FS1-46	MS1-19	S0	Data Bus Status, bit 0 (8085)
J8-10, J1-11, FS1-47	MS1-18	S1	Data Bus Status, bit 1 (8085)
J10-11			
S2C-38	S2D-9	SAA-	State Arm-word match, A chan
S2C-9	S2F-9	SAB-	State Arm-word match, B chan
J7-13, MS1-25	FS1-40	SID	Serial Input Data (8085)
J7-14, FS1-16	MS1-49	SOD	Serial Output Data (8085)
*U2-11, S2C-39	S2D-10	STA-	State Trigger-word match, A
S2C-10	S2F-10	STB-	State Trigger-word match, B
S2C-7	S2B-7	TA-	Timing Arm-word match
J6-5	S2B-14	THRESHA	Threshold V, Timing 0—3,Q,CLK
J6-6	S2B-45	THRESHB	Threshold V, Timing chan 4—7
MS1-24	FS1-41	TRAP	Interrupt, RESTART at 0024H
S2D-50, S2F-50	S2E-20	TSA0	Trigger Stack Address, bit 0
S2D-49, S2F-49	S2E-19	TSA1	Trigger Stack Address, bit 1
S2D-48, S2F-48	S2E-18	TSA2	Trigger Stack Address, bit 2
S2D-47, S2F-47	S2E-17	TSA3	Trigger Stack Address, bit 3
*U2-15, S2C-8	S2B-8	TT-	Timing Trigger-word match
*BNC, J11-8	J14-2	VIDEO	Composite Video
J21-3	J15-3	VRTC-	Vertical Retrace- (Video)
S2B-21	S2A-21	WD0	Digitized Waveform Data bit 0
S2B-51	S2A-51	WD1	Digitized Waveform Data bit 1
S2B-20	S2A-20	WD2	Digitized Waveform Data bit 2
S2B-50	S2A-50	WD3	Digitized Waveform Data bit 3
S2B-19	S2A-19	WD4	Digitized Waveform Data bit 4
S2B-49	S2A-49	WD5	Digitized Waveform Data bit 5
S2B-18	S2A-18	WD6	Digitized Waveform Data bit 6
S2B-48	#S2A-48	WD7	Digitized Waveform Data bit 7
FS1-29	MS1-4	WR-	Write (8085)
S2C-40	S2A-40	WTRIG+	Waveform Trigger cond. met
MS1-35, MS1-36, J9-1,2	---	+5 V	+5-volt supply from Pwr Sup
MS1-6, MS1-5, FS1-36			
FS1-35, FS1-6, FS1-5			
J10-10, J6-19, J6-16			
J5-26, J4-26, J1-10			

Destination	Source	Signal	Name Expansion
J11-7	J12-1	+12 V	+12 V, Display Module from PS
J6-10		+12 V	+12 V, Probe from Timing Mem
S2B-2, S2B-32, J9-12 S2A,32, S2A-2		+15 V	+15-volt supply from Pwr Sup
FS1-34, MS1-34, J9-11 FS1-4		+30 V	+30-volt supply (optional)
FS1-33, MS1-33, J9-5,6 FS1-32, FS1-3, FS1-2 J6-22, J6-25, J5-12 J4-12		-5.2 V	-5.2-volt supply from Pwr Sup
J6-13		-12 V	-12 V, Probe from Timing Mem
S2B-33, J10-20, J9-9 S2B-3, S2A-33, S2A-3 S1-20		-15 V	-15-volt supply from Pwr Sup

* U2 is an IC (10125 quad ECL-to-TTL translator) on the Function Motherboard. BNCs are connectors on the chassis back plate (labeled on the back plate).

No connection to this pin on the circuit board in this slot.

@ No connection to this pin on the motherboard.

TABLE 2

MICROCOMPUTER S1 CONNECTOR

PIN	SIGNAL	PIN	SIGNAL
1	GND	31	GND
2	SPARE	32	SPARE
3	RD-	33	-5.2 V
4	WR-	34	+30 V
5	+5 V	35	+5 V
6	+5 V	36	+5 V
7	A2	37	A3
8	A7	38	A11
9	A6	39	A12
10	A0	40	A5
11	A10	41	A1
12	A9	42	A4
13	A8	43	SPARE
14	DB6	44	DB7
15	ALE	45	DB5
16	DB1	46	DB2
17	DB0	47	DB4
18	S1	48	DB3
19	S0	49	SOD
20	A15	50	IO+/M-
21	A13	51	A14
22	RST 5.5	52	INTR
23	RST 7.5	53	RST 6.5
24	TRAP	54	CLK
25	SID	55	RST
26	HOLD	56	RW
27	RDY	57	IOEN-
28	HLDA	58	A15-
29	INTA-	59	A3-
30	GND	60	GND

TABLE 3

FUNCTION S1 CONNECTOR

PIN	SIGNAL	PIN	SIGNAL
1	GND	31	GND
2	-5.2 V	32	-5.2 V
3	-5.2 V	33	-5.2 V
4	+30 V	34	+30 V
5	+5 V	35	+5 V
6	+5 V	36	+5 V
7	HLDA	37	INTA-
8	IOEN-	38	RDY
9	RW	39	HOLD
10	RST	40	SID
11	CLK	41	TRAP
12	RST 6.5	42	RST 7.5
13	INTR	43	RST 5.5
14	A14	44	A13
15	IO+/M-	45	A15
16	SOD	46	SO
17	DB3	47	S1
18	DB4	48	DB0
19	DB2	49	DB1
20	DB5	50	ALE
21	DB7	51	DB6
22	SPARE	52	A8
23	A4	53	A9
24	A1	54	A10
25	A5	55	A0
26	A12	56	A6
27	A11	57	A7
28	A3	58	A2
29	WR-	59	RD-
30	GND	60	GND

TABLE 4

J3 CONNECTOR, FUNCTION MOTHERBOARD
J2 CONNECTOR, MICROCOMPUTER MOTHERBOARD

*J2,3 PIN	SIGNAL	#MS1 PIN	#FS1 PIN	J2,3 PIN	SIGNAL	MS1 PIN	FS1 PIN
1	GND	1	1	26	DB4	47	18
2	GND	30	30	27	S1	18	47
3	RD-	3	59	28	INTR	52	13
4	WR-	4	29	29	SO	19	46
5	A2	7	58	30	A14	51	14
6	A3	37	28	31	A15	20	45
7	A7	8	57	32	IO+/M-	50	15
8	A11	38	27	33	A13	21	44
9	A6	9	56	34	SOD	49	16
10	A12	39	26	35	RST 5.5	22	43
11	A0	10	55	36	DB3	48	17
12	A5	40	25	37	RST 7.5	23	42
13	A10	11	54	38	RST 6.5	53	12
14	A1	41	24	39	TRAP	24	41
15	A9	12	53	40	CLK	54	11
16	A4	42	23	41	SID	25	40
17	A8	13	52	42	RST	55	10
18	SPARE	2	22	43	HOLD	26	39
19	DB6	14	51	44	RW	56	9
20	DB7	44	21	45	RDY	27	38
21	ALE	15	50	46	IOEN-	57	8
22	DB5	45	20	47	INTA-	29	37
23	DB1	16	49	48	HLDA	28	7
24	DB2	46	19	49	GND	31	31
25	DB0	17	48	50	GND	60	60

* J2 and J3 are interconnected on a pin-1-to-pin-1 bassis by a flat ribbon cable. (CAUTION: Because of the geometry of the motherboard placements, a fold in the cable is necessary. This fold invalidates the pin-1 markers on the P2 and P3 cable-plug bodies. When inserting the plugs, honor the pin-1 markers on the pull tabs rather than those on the plug bodies. Match the pull-tab markers to those on the J2 and J3 connector bodies.)

# MS1 = S1 sockets on the Microcomputer Motherboard.
FS1 = S1 societs on the Function Motherboard.

TABLE 5

S2 CONNECTORS, FUNCTION MB

WAVEFORM SLOT A	TIMING MEMORY SLOT B	TIMING CONTROL SLOT C	PIN	STATE MEMORY A SLOT D	STATE CONTROL SLOT E	STATE MEMORY B SLOT F
GND	GND	GND	1	GND	GND	GND
+15 V	+15 V	---	2	(KEY)	---	(KEY)
-15 V	-15 V	---	3	---	(KEY)	---
---	---	---	4	ALATCHCLK	ALATCHCLK	BLATCHCLK
---	---	---	5	AWE+	AWE+	BWE+
CT	CT	CT	6	ADLYWE-	ADLYWE-	BDLYWE-
---	TA-	TA-	7	ACLKINH+	ACLKINH+	BCLKINH+
---	TT-	TT-	8	---	ACLKQUALIN-	---
---	---	SAB-	9	SAA-	RA7	SAB-
---	(KEY)	STB-	10	STA-	RA6	STB-
---	---	FT	11	FT	RA5	FT
---	---	EXT	12	EXT	RA4	EXT
---	---	---	13	---	RA3	---
---	THRESHA	---	14	APROBDREN-	RA2	BPROBDREN-
---	HYST	(KEY)	15	---	RA1	BSELECT-
---	---	---	16	ATRIG+	RA0	BTRIG+
---	---	---	17	ARST	TSA3	BRST
WD6	WD6	---	18	ACQ2	TSA2	BCQ2
WD4	WD4	---	19	ACQ1	TSA1	BCQ1
WD2	WD2	---	20	ARMA	TSA0	ARMB
WD0	WD0	---	21	AQ1	ACQ1	BQ1
---	D7-	---	22	AQ2	ACQ2	BQ2
---	D7+	---	23	APD13	APROBCLK	BPD13
---	D6-	---	24	APD14	ACLKSEL	BPD14
---	D6+	---	25	APD15	AQ1	BPD15
---	D5-	---	26	APD12	AQCLKSEL	BPD12
(KEY)	D5+	---	27	APD11	ACONTROL	BPD11
GND	D4-	---	28	APD10	---	BPD10
ANALOGIN	D4+	---	29	APD3	---	BPD3
GND	GND	GND	30	GND	GND	GND

WAVEFORM SLOT A	TIMING MEMORY SLOT B	TIMING CONTROL SLOT C	PIN	STATE MEMORY A SLOT D	STATE CONTROL SLOT E	STATE MEMORY B SLOT F	C/T/SA SLOT G
GND	GND	GND	31	GND	GND	GND	GND
+15 V	+15 V	+15 V	32	(KEY)	---	(KEY)	+15 V
-15 V	-15 V	-15 V	33	DQ2	DQ2	DQ2	-15 V
---	---	---	34	GND	BLATCHCLK	GND	---
GND	GND	GND	35	GND	BWE+	GND	BWE+
GND	GND	GND	36	GND	CT	GND	---
---	---	---	37	ACLKQUALIN-	BDLYWE-	BCLKQUALIN-	---
---	---	SAA-	38	GND	BCLKINH+	GND	---
---	---	STA-	39	RA7	BCLKQUALIN-	RA7	---
WTRIG+	(KEY)	WTRIG+	40	RA6	---	RA6	---
---	---	---	41	RA5	---	RA5	GND
---	---	FS	42	RA4	FS	RA4	PROBE
---	CLKTTL	CLKTTL	43	RA3	APROBDREN-	RA3	---
---	+12 V	---	44	RA2	BPROBDREN-	RA2	---
---	THRESHB	(KEY)	45	RA1	ATRIG+	RA1	---
---	---	---	46	RA0	BTRIG+	RA0	---
---	---	---	47	TSA3	ARST	TSA3	---
WD7	WD7	---	48	TSA2	BRST	TSA2	---
WD5	WD5	---	49	TSA1	---	TSA1	---
WD3	WD3	---	50	TSA0	---	TSA0	---
WD1	WD1	---	51	APD7	BCQ1	BPD7	---
---	D0+	---	52	APD6	BCQ2	BPD6	---
---	D0-	---	53	APD4	BCONTROL	BPD4	---
---	D1+	---	54	APD1	BQCLKSEL	BPD1	---
---	D1-	CLK-	55	APD2	BQ1	BPD2	---
---	D2+	CLK+	56	APD0	BCLKSEL	BPD0	---
(KEY)	D2-	QCLK-	57	APD5	BPROBCLK	BPD5	---
GND	D3+	QCLK+	58	APD8	---	BPD8	---
GND	D3-	---	59	APD9	---	BPD9	---
GND	GND	GND	60	GND	GND	GND	GND

TABLE 6

J4 CONNECTOR, STATE PROBE, B CHANNEL

PIN	SIGNAL	PIN	SIGNAL
1	GND	14	BPD11
2	BPROBCLK	15	BPD10
3	GND	16	BPD3
4	BCLKSEL	17	BPD9
5	BQ1	18	BPD8
6	BQCLKSEL	19	BPD5
7	BQ2	20	BPD0
8	BPD13	21	BPD2
9	BCONTROL	22	BPD1
10	BPD14	23	BPD4
11	BPD15	24	BPD6
12	-5.2 V	25	BPD7
13	BPD12	26	+5 V

TABLE 7

J5 CONNECTOR, STATE PROBE, A CHANNEL

PIN	SIGNAL	PIN	SIGNAL
1	GND	14	APD11
2	APROBCLK	15	APD10
3	GND	16	APD3
4	ACLKSEL	17	APD9
5	AQ1	18	APD8
6	AQCLKSEL	19	APD5
7	AQ2	20	APD0
8	APD13	21	APD2
9	ACONTROL	22	APD1
10	APD14	23	APD4
11	APD15	24	APD6
12	-5.2 V	25	APD7
13	APD12	26	+5 V

TABLE 8

J6 CONNECTOR, TIMING PROB

PIN	SIGNAL	PIN	SIGNAL
1	GND	18	D5+
2	CLK-	19	+5 V
3	CLK+	20	D4-
4	GND	21	D4+
5	THRESHA	22	-5.2 V
6	THRESHB	23	D3-
7	GND	24	D3+
8	QCLK-	25	-5.2 V
9	QCLK+	26	D2-
10	+12 V	27	D2+
11	D7-	28	GND
12	D7+	29	D1-
13	-12 V	30	D1+
14	D6-	31	GND
15	D6+	32	D0-
16	+5 V	33	D0+
17	D5-	34	HYST

TABLE 9

J7 CONNECTOR, SELF-TEST DATA/STATUS

PIN	SIGNAL	PIN	SIGNAL
1	DB0	11	IO+/M-
2	DB1	12	INTA-
3	DB2	13	SID
4	DB3	14	SOD
5	DB4	15	GND
6	DB5	16	GND
7	DB6	17	IO+/M-
8	DB7	18	RD-
9	S0	19	RW
10	S1	20	GND

TABLE 10

J8 CONNECTOR, SELF-TEST ADDRESS

PIN	SIGNAL	PIN	SIGNAL
1	A0	11	A10
2	A1	12	A11
3	A2	13	A12
4	A3	14	A13
5	A4	15	A14
6	A5	16	A15
7	A6	17	RD-
8	A7	18	IO+/M-
9	A8	19	RW
10	A9	20	GND

TABLE 11

*J14 CONNECTOR, VIDEO DISPLAY
J11 CONNECTOR, DISPLAY MODULE
J12 CONNECTOR, DISPLAY MODULE (IN CABLE FROM POWER SUPPLY)

J11 PIN	SIGNAL	J12 PIN	J14 PIN
1	GND		1
2	---		
3	---		
4	---		
5	---		
6	---		
7	+12 V	1	
8	VIDEO		2
9	---		
10	GND	2	3

* See the Connector/Cables Diagram in section 2.1, Chassis, for the relationship of J11, J12, and J14.

TABLE 12

J21 CONNECTOR, WAVEFORM
J15 CONNECTOR, VIDEO DISPLAY

PIN	SIGNAL	PIN	SIGNAL
1	HRTC-	8	---
2	DCLK2	9	GND
3	VRTC-	10	GND
4	EXTVID-	11	GND
5	CCLK-	12	GND
6	---	13	GND
7	---	14	GND

TABLE 13

J10 CONNECTOR, KEYBOARD
J1 CONNECTOR, MICROCOMPUTER MOTHERBOARD

PIN	SIGNAL	PIN	SIGNAL
1	GND	11	S1-
2	GND	12	BDB0
3	IOEN-	13	BDB1
4	FPENB-	14	BDB2
5	BA1-	15	BDB3
6	BA0-	16	BDB4
7	BA2-	17	BDB5
8	BA3-	18	BDB6
9	BA0+	19	BDB7
10	+5 V	20	-15 V

TABLE 14

J9 CONNECTOR, FUNCTION MOTHERBOARD POWER

PIN	SIGNAL	PIN	SIGNAL
1	+5 V	7	SPARE
2	+5 V	8	SPARE
3	SPARE	9	-15 V
4	GND	10	GND
5	-5.2 V	11	+30 V
6	-5.2 V	12	+15 V

TABLE 15

P13 CONNECTOR, POWER SUPPLY

PIN	SIGNAL	PIN	SIGNAL
1	AUX 110 Vac	4	AUX 110 Vac
2	MAINS Vac (LINE)	5	EARTH GND
3	100—115 Vac (NEUT)	6	220 Vac (NEUT)

16.0 GLOSSARY

16.0 GLOSSARY

Words in the body of an explanation that are underlined are explained elsewhere in the Glossary. Please refer to them there if necessary.

A/D	Analog-to-Digital (converter)
ASCII	American Standard Code for Information Interchange
BNC	A coaxial connector type-designation; offered by most manufacturers
Boolean	A type of binary algebra used in logic design
CMOS	Complementary-Metal-Oxide-Silicon; a family of ICs named after the manufacturing technology
CRT	Cathode-Ray Tube
CRTC	CRT Controller; a special-purpose LSI circuit
D/A	Digital-to-Analog (converter)
DMA	Direct Memory Access; memory access that is not under supervision of the controlling microprocessor
ECL	Emitter-Coupled Logic; a family of high-speed, digital logic ICs
EPROM	Erasable Programmable Read-Only Memory; can be erased with ultra-violet light and reprogrammed
FET	Field-Effect Transistor
Glitch	(Please see definition at the beginning of the Data Comparators subsection 11.2.4 in the Timing Memory section)
GPIB	General Purpose Interface Bus; another name for the IEEE-488 bus
H	Hexadecimal; indicates, when placed after a number (which may include alpha characters A — F) that the number is in base-16 notation
Hex	see H, above
IC	Integrated Circuit
IEEE-488	An Institute of Electrical and Electronics Engineers standard digital interface for programmable instrumentation (the full name of the standard is ANSI/IEEE Std 488-1978)
K	A unit multiplier meaning x 1000
LED	Light Emitting Diode
LSI	Large-Scale Integrated circuit
Mains	The public utility ac power lines
MMI	Monolithic Memories, Inc.; a manufacturer of IC devices
OC	Open Collector, a type of IC circuit design
Op Amp	Operational Amplifier; usually a linear IC.
PC	Printed Circuit
PI	Paratronics, Inc.; manufacturer of the PI 540 Logic Analysis System
Pin-out	A list of device pins (connector, IC, relay, etc.) versus input or output signals or voltages.
PROM	Programmable Read-Only Memory; manufactured in the unprogrammed state and can be programmed once, before installation
RAM	Random Access Memory; implies both read and write capabilities
ROM	Read-Only Memory; memory that can be read from but not written into; programmed during manufacture
RS-232-C	An Electronic Industries Association standard for a data communication interface
SIB	Serial Interface Board; an optional circuit board for the PI 540
SIP	Single In-line Package; the term is related to DIP (Dual In-line Package)

TTI	Transistor-Transistor Logic; a family of general purpose, digital logic ICs
USART	Universal Synchronous/Asynchronous Receiver-Transmitter; an LSI communications device

NICOLET PARATRONICS CORPORATION

A NICOLET INSTRUMENT SUBSIDIARY

201 Fourier Avenue
Fremont, California 94539

TWX: 910-381-7030