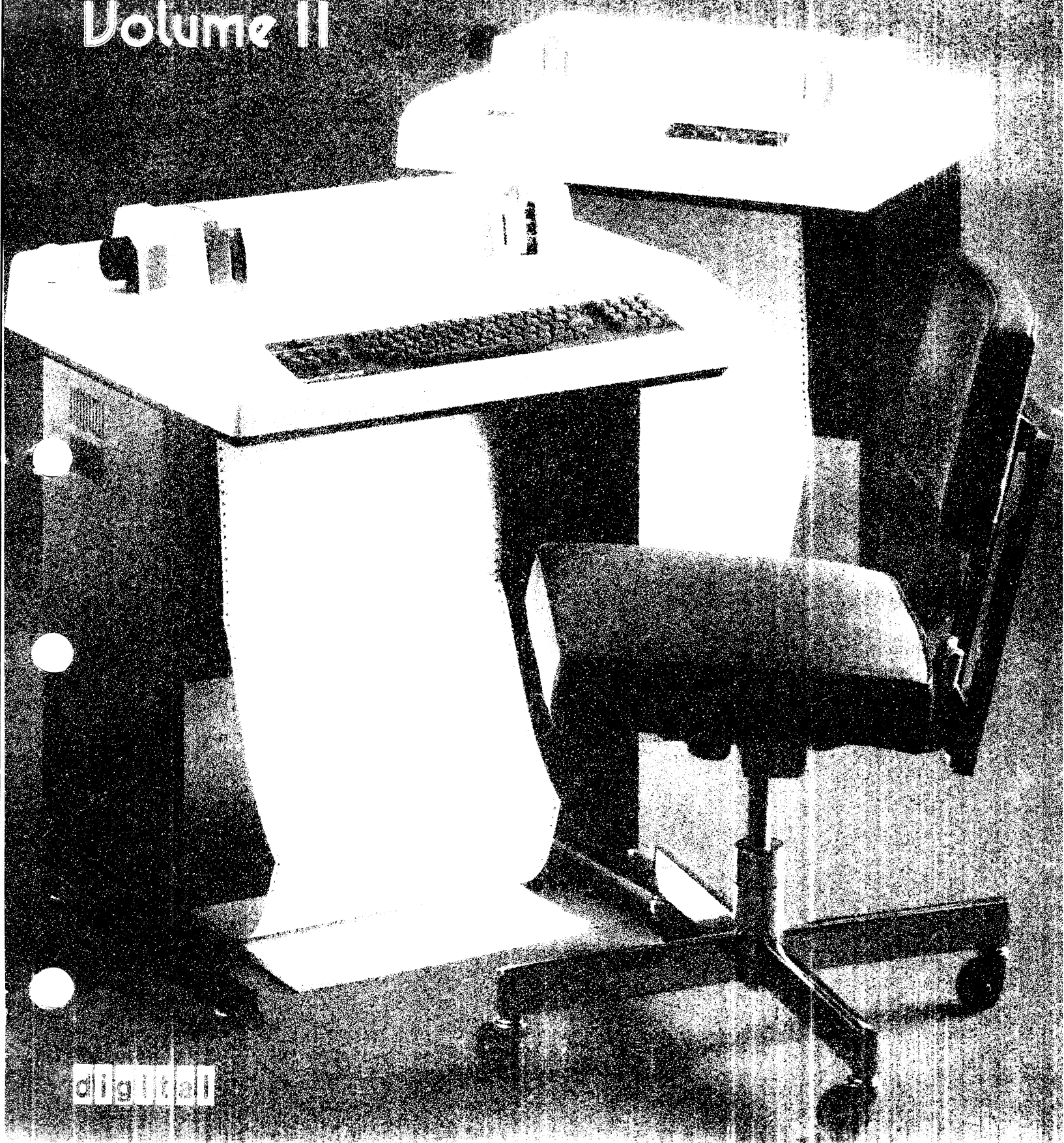


EH507/EH55 DECIMATE II
Maintenance Manual
Volume II



**LA36 DECwriter II
MAINTENANCE MANUAL
Volume II**

1st Edition, November 1976

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CHAPTER 9 UPGRADED LA36

9.1 GENERAL

The purpose of this chapter is to upgrade the maintenance manual for the LA36 DECwriter II so that it reflects the equipment changes incurred since the original publication. Changes of significant importance include:

1. M7723 Logic Board
2. M7728 Logic Board
3. Power Board Changes
4. Constant Voltage Transformer
5. New Bezel
6. Caps Lock Keyboard
7. Addition of Options

9.2 LA35/LA36 MODEL VARIATIONS

The variations and associated model numbers for the LA35/LA36 are listed below.

Model No.	Designation	Variation
LA35		
LA35-CE	LA35	90-132 V, 60 Hz
LA35-CF	LA35	180-264 V, 60 Hz
LA35-CH	LA35	90-132 V, 50 Hz
LA35-CJ	LA35	180-264 V, 50 Hz
LA35-DE	LA35	90-132 V, 60 Hz
LA35-DJ	LA35	180-264 V, 50 Hz
LA36		
LA36-CE	LA36 with Numeric Pad and Paper Out	90-132 V, 60 Hz
LA36-CF	LA36 with Numeric Pad and Paper Out	180-264 V, 60 Hz
LA36-CH	LA36 with Numeric Pad and Paper Out	90-132 V, 50 Hz
LA36-CJ	LA36 with Numeric Pad and Paper Out	180-264 V, 50 Hz
LA36-DE	LA36	90-132 V, 60 Hz
LA36-DF	LA36	180-264 V, 60 Hz
LA36-DH	LA36	90-132 V, 50 Hz
LA36-DJ	LA36	180-264 V, 50 Hz

9.3 EASY IDENTIFICATION OF LOGIC BOARDS

There are three possible Logic Board models that can be installed in a DECwriter: M7722, M7723 and M7728. The M7722 board is typically factory installed in earlier LA36s while the M7723 and M7728 boards are found in newer terminals. The M7728 performs all functions of the M7722 and M7723 and is backward compatible for a direct replacement for either board. Replacing either board with an M7728 does not enhance the capabilities of the terminal in which the M7728 board is installed.

Figure 9-1 shows the obvious physical differences between the three Logic Boards that permit easy identification. The M7722 and M7723 boards each have four connectors while the M7728 has five connectors. The M7723 and M7728 boards have solder dot test points around the perimeter and the M7722 does not have these test points.

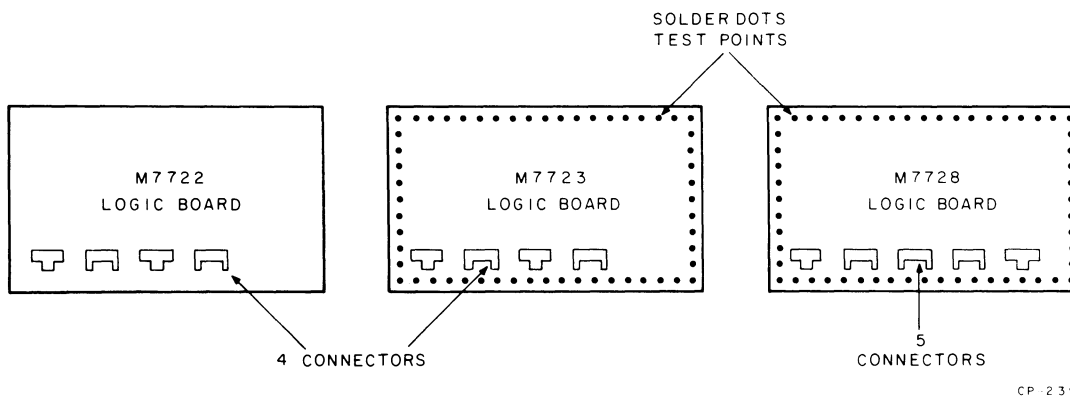


Figure 9-1 Physical Characteristics of M7722, M7723, and M7728 Logic Boards

9.3.1 Major Functional Differences Between M7722 and M7723 Logic Boards

There are three major functional differences between the M7722 and the M7723 Logic Boards:

1. Local Copy Feature

M7722 – No local capability when terminal is operating on-line (sometimes called half-duplex mode)

M7723 – Has local copy feature. Three-position front panel rocker switch permits printing when in local or on-line in half- or full-duplex mode.

2. Parity Selection

M7722 – No received parity capabilities. Only even or no parity selection on transmission. No eighth bit spacing capability.

M7723 – Choice of even or odd parity for both receiving or transmitting.

3. Paper Out Option

M7722 – No provision for accepting the Paper Out Switch.

M7723 Compatible with Paper Out Switch.

9.3.2 M7723 Jumper Configurations

Figure 9-2 shows the location and function of all jumpers on the M7723 Logic Board.

Jumper Configurations for M7723 Logic Board

Function	W2	W3	W4	W5	W6	W7	W8	W9	W13	W14
Full-Duplex Active	0	0	0	0	1	1	1	1	1	1
Full-Duplex Passive	1	1	1	1	0	0	0	0	0	0
Passive Receive/ Active Transmit	1	1	0	0	1	0	1	0	0	1
Active Receive/ Passive Transmit	0	0	1	1	0	1	0	1	1	0
Half-Duplex Active*	1	1	1	1	1	0	0	1	0	0
Half-Duplex Passive*	1	1	1	1	0	0	0	0	0	0

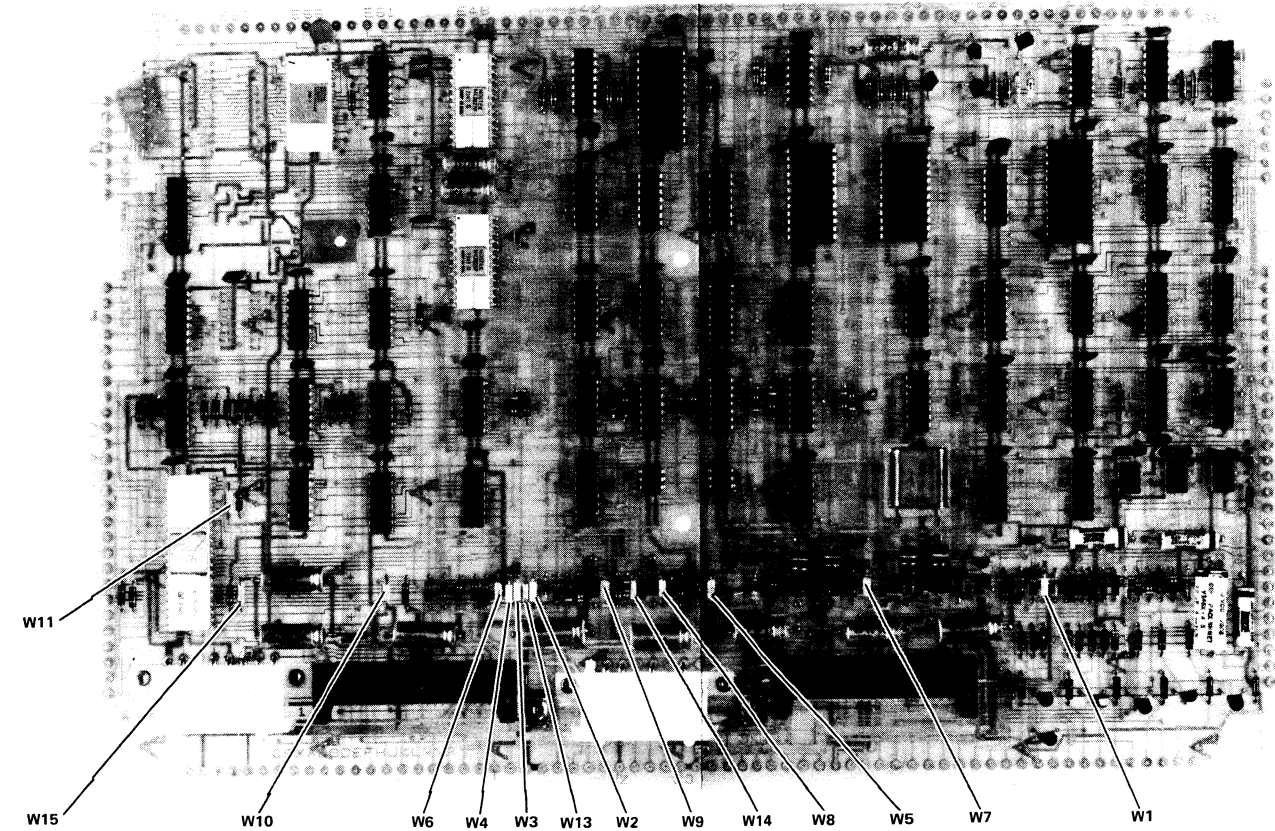
*Connect user-manufactured cable between J3-3 and 5 and operating system.

Function	W10	W11	W15
8th BIT MARKING	0	X	0
8th BIT SPACING	0	X	1
EVEN PARITY	1	0	X
ODD PARITY	1	1	X

Legend:

- 1 = Jumper Installed
- 0 = Jumper Not Installed
- X = Do Not Care

- W1 Installed - Standard Bell Volume
- W1 Not Installed - Lower Bell Volume
- W12 Not Used - No Function



8142-1

Figure 9-2 Location of Jumpers on M7723 Logic Board

9.3.3 Functional Differences Between M7723 and M7728 Logic Boards

In addition to having all the features of the M7723 board, the M7728 can also provide the data and signal interface required when options are installed in an upgradable LA35/LA36. The M7728 has the same possible transmit and receive parity configuration as the M7723. In addition, the received parity error print indication (three vertical bars) can be suppressed in certain instances when the eight level bit is used as a control code for the options.

9.3.4 M7728 Jumper Configurations

Figure 9-3 shows the location and function of all jumpers on the M7728 Logic Board.

9.3.5 M7728 Cabling Configurations

The possible cabling configurations for the M7728 Logic Board are shown in Figure 9-4.

CAUTION

The ribbon cables between the Logic Board and the Expander Board must be installed so that one cable end (either end) has the ribbed side of the cable facing up and the other end has the smooth side up. Ensure that A connects to A at each cable end. Failure to observe this polarity may cause a Logic Board failure.

9.4 MAJOR POWER SUPPLY CHANGES

There are four major changes to the power supply:

1. The rating of the ac line fuse was increased from 2 A SB to 3 A SB for 115 V and from 1 A SB to 1.5 A SB for 230 V.
2. The two 1 A SB fuses in the line feed motor drive circuit were replaced with four 3/4 A SB fuses.
3. The 18000 μ F capacitor in the capacitor bank was replaced with a 37000 μ F capacitor.
4. A Constant Voltage Transformer (CVT) replaced the original power transformer.

9.4.1 New Power Transformers

Upgradable LA35/LA36s have constant voltage power transformers installed to accommodate the increased power requirements of the options. There is a unique transformer model for 50 Hz operation and another model for 60 Hz operation. Both models function on either 115 or 220 Vac primary voltage and provide ± 24 and +11 Vdc at the secondary.

9.5 NEW KEYBOARD BEZELS

The keyboard bezel associated with the upgradable LA36 is shown in Figure 9-5. There is no change in the bezel for upgradable LA35s. The LA36 also has another bezel configuration that accepts the 14-Key Numeric Keypad Option which mounts to the right of the standard keyboard.

9.6 CAPS LOCK KEYBOARD

The Caps Lock Keyboard has a CAPS LOCK key substituted for the SHIFT LOCK key normally found on office equipment. When the CAPS LOCK is depressed, the 26-letter keys transmit only upper case codes; all other keys print in lower case.

9.7 LA35/LA36 OPTIONS

All options listed in Table 9-1 can be installed in a LA35/LA36 DECwriter except for the 14-Key Numeric Keypad and the Paper Out Options.

Jumper Configurations for M7728 Logic Board

Function	W2	W3	W4	W5	W6	W7	W8	W9	W13	W14
Full-Duplex Active	0	0	0	0	1	1	1	1	1	1
Full-Duplex Passive	1	1	1	1	0	0	0	0	0	0
Passive Receive/ Active Transmit	1	1	0	0	1	0	1	0	0	1
Active Receive/ Passive Transmit	0	0	1	1	0	1	0	1	1	0
Half-Duplex Active*	1	1	1	1	1	0	0	1	0	0
Half-Duplex Passive*	1	1	1	1	0	0	0	0	0	0

*Connect user-manufactured cable between J3-3 and 5 and operating system.

Function	W10	W11	W15
8th BIT MARKING	0	X	0
8th BIT SPACING	0	X	1
EVEN PARITY	1	0	X
ODD PARITY	1	1	X

Legend:

1 = Jumper Installed
 0 = Jumper Not Installed
 X = Do Not Care

Function	W18	W19	W20
Print Parity Error Indication	1	0	1
Eight Bit Control Over Options (No parity detection)	0	1	0

- W1 Inserted - Standard Bell Volume
- W1 Not Inserted - Lower Bell Volume
- W12 Inserted - Print all characters typed whether LOCAL or ON LINE in Full or Half Duplex
- W12 Not Installed - Position of FDX/HDX switch establishes whether transmitted characters are printed
- W16 Not Used - No Function
- W17 Not Used - No Function

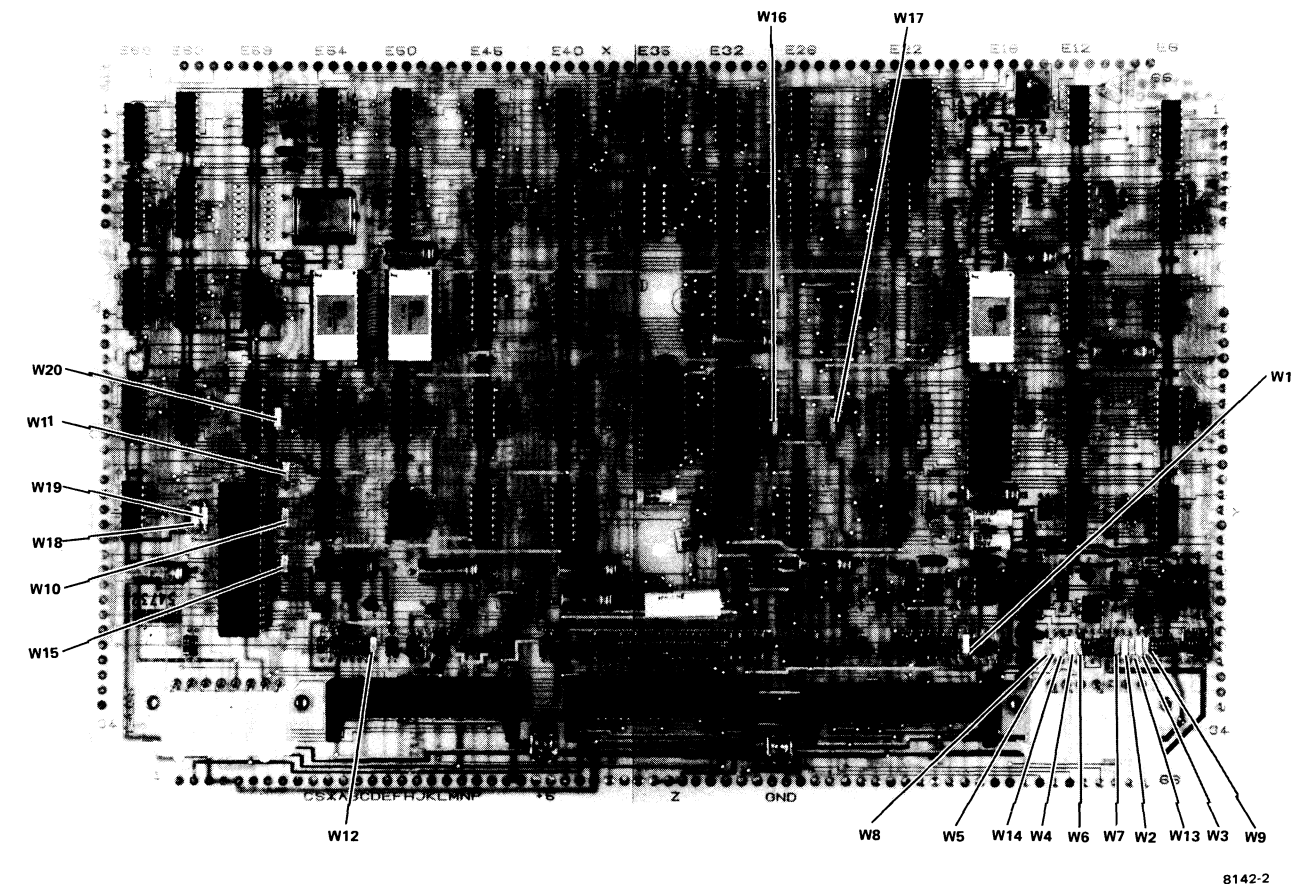


Figure 9-3 Location of Jumpers on M7728 Logic Board

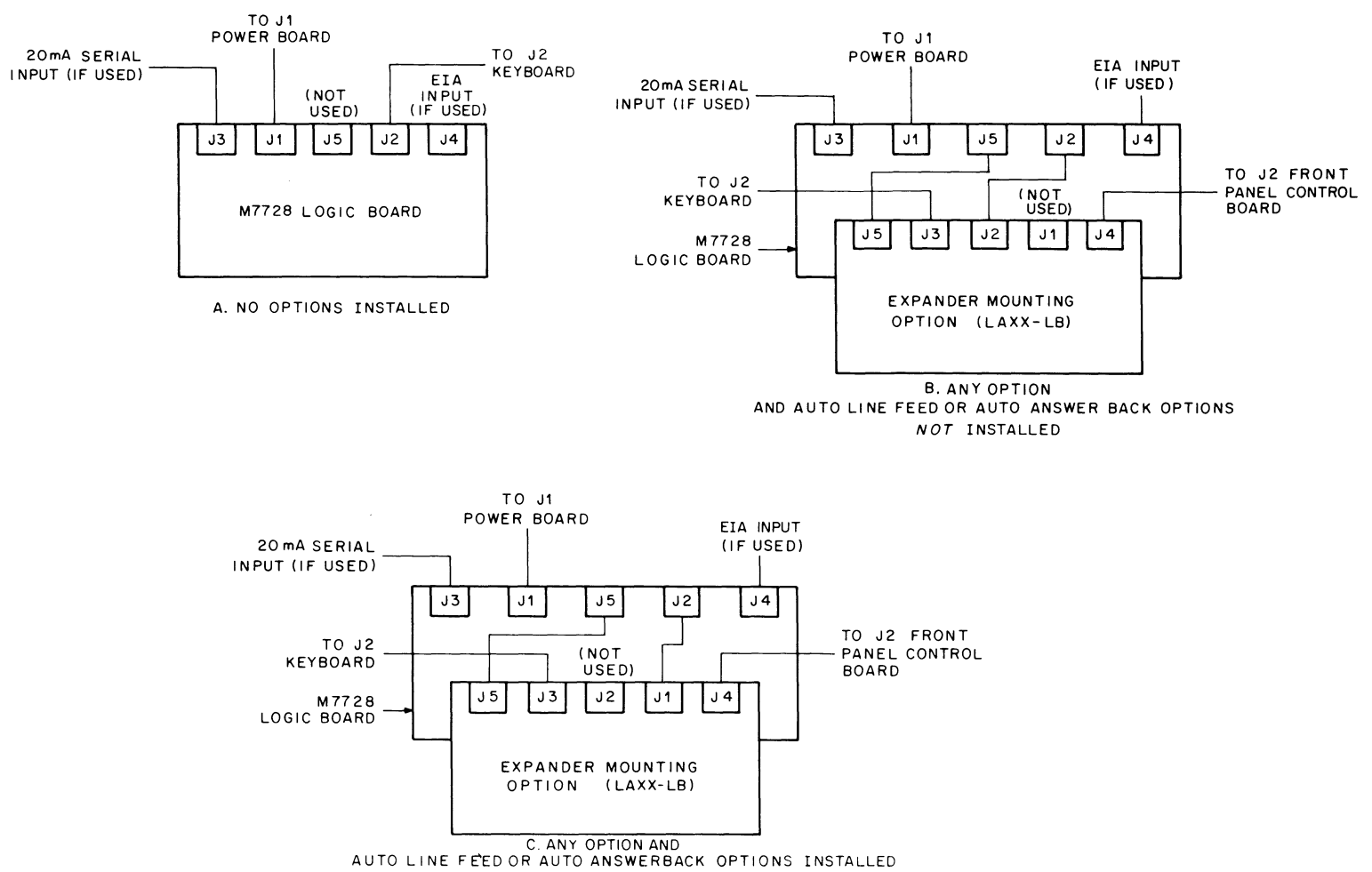
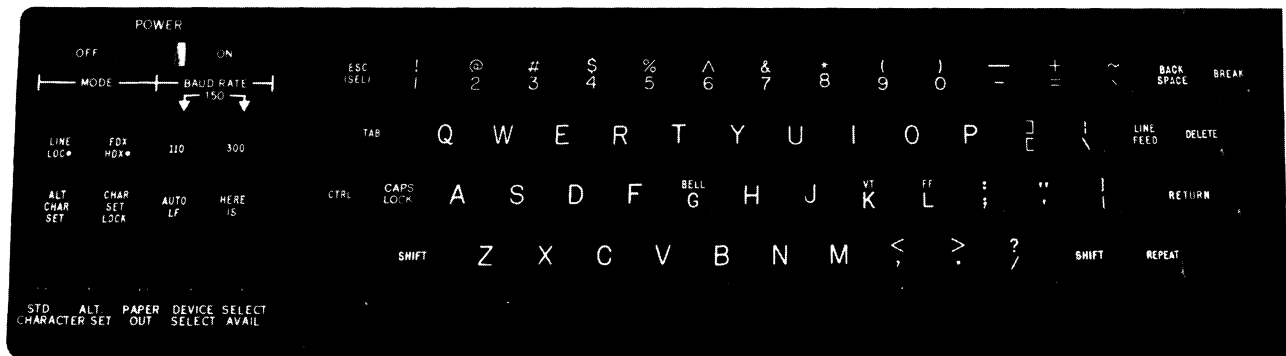


Figure 9-4 Cabling Configurations for the M7728 Logic Board



7622-28

Figure 9-5 LA36 Keyboard Bezel

9.8 UPGRADED LA36 FUNCTIONAL DESCRIPTION

The following LA35/LA36 printers are designated as option-upgradable DECwriters.

- LA36 Manufactured in U.S.A. – Serial numbers 02-21933 and higher
- LA36 Manufactured in Ireland – Serial numbers 04-10450 and higher
- LA35 Manufactured in U.S.A. – Serial numbers 5001 and higher

These printers have the increased power supply capability and the M7728 Logic Board required to accommodate the various available options.

The basic block diagram for the M7728 Logic Board is shown in Figure 9-6. The major difference between this diagram and the diagrams for the M7722 and M7723 boards is in the Data Conversion Block. All other functional areas operate in the same manner as in the other boards. The three items added to the data conversion are are:

1. Expander Board
2. Options
3. Tri-State Buffer

The Data Conversion Block still performs its basic function of taking Serial In (SI) ASCII data and converting it to a 7 × 7 dot pattern that drives the print head. Transmitted keyboard data is converted to Serial Out (SO) ASCII data by the Data Conversion Block. These functions do not change in an upgradable printer; only now, certain options exercise control over both the receive and transmit data lines by blocking, inserting, or allowing data to pass.

**Table 9-1
LA35/36 Options**

Options	Name	Control Switch/Indicator	Description
LAXX-LB	Expander Option	None	The Expander Option Mounting Kit includes the logic, cables, and mounting hardware required to expand the LA36 to include options LAXX-LA, LAXX-KV, LAXX-KW, LAXX-KX, LAXX-KY, and LAXX-PK.
LAXX-PK	APL/ASCII Dual Character Set	ALT CHAR SET, CHAR SET LOCK, and STD/ALT CHARACTER SET Indicators	This option provides an APL alternate character set for use with the standard character set in the LA35/LA36.
LAXX-LA	Auto LF After CR	AUTO LF	When the AUTO LF switch is activated, the printer will automatically insert a line feed after each carriage return code typed during transmission. The LAXX-LA option can also be configured to execute a line feed after each received carriage return code. Any combination of these options can be used.
LAXX-KV	Top of Forms Control	FORMS LENGTH Switch and SET TOP OF FORM Pushbutton	Controls mounted under the top cover provide the operator with a method of selecting the length of the paper to be used. After the desired setting is selected and the paper is lined up for proper vertical alignment, the operator presses the SET TOP OF FORM switch so that the internal logic will be preset to the paper length defined by the operator.
LAXX-KW	Selective Addressing	DEVICE SELECT and SELECT AVAIL Lamps	The Selective Addressing Option allows the LA36 to communicate with other terminals on a single data communications channel.
LAXX-KX	Auto Answerback and Auto LF Options	HERE IS, AUTO LF	The Automatic Answerback Option allows the terminal to transmit a pre-programmed message of 20 characters (maximum). The message is initiated by pressing the HERE IS pushbutton, or upon receipt of the ENQ control code from another device. The LAXX-KX also incorporates the features of the Auto LF option (LAXX-LA).

Table 9-1 (Cont)
LA35/36 Options

Options	Name	Control Switch/Indicator	Description
LAXX-KY	Forms Control and Vertical and Horizontal Tabs	Keyboard Keys	The Forms and Tabbing Option enables the terminal to set horizontal and vertical tab positions either locally or via the system software. This option also incorporates features of the Top of Forms Option (LAXX-KV) and operates in the same manner.
LAXX-LG	EIA/CCITT Interface	None	The LAXX-LG interface provides the user with an RS/232-C interface with modem control and includes a 9-ft (3.54-m) cable terminated with a standard EIA connector.
LAXX-KH	DF11 Mounting Kit	None	The DF11 Mounting Kit enables the user to mount one of the DIGITAL series DF11 Communication Options in the LA36.
LAXX-KJ	Compressed Font Option	None	The Compressed Font Option is a mechanical option that provides the LA36 with the ability to print 132 columns on a form 8-1/2 in. (21.59-cm) wide.
LAXX-KX*	14-Key Numeric Keypad	Keyboard Keys	The 14-Key Numeric Keypad is located to the right of the keyboard and provides the operator with a convenient method of entering mathematical number sequences.
LAXX-LZ**	Paper Out	PAPER OUT Lamp	Provides a visual indication for a paper-out condition. Prevents keyboard and received data from printing.
LAXX-LC	TTL to CCITT (V28) Converter and Modem Protector	None	The TTL to CCITT (V28) Converter and Modem Protector is a BPO DATEL services interface that meets the requirements of CCITT (V28) with BPO-required modem protection circuitry.
LAXX-LH	Current Loop Cable	None	20 mA current loop with Mate-N-Lok.
LAXX-LK	Current Loop Cable	None	20 mA current loop with 4-pin plug for DEC10.

*Not available on the LA35

**Standard on the LA35

**Table 9-1 (Cont)
LA35/36 Options**

Options	Name	Control Switch/Indicator	Description
LAXX-KG	EIA Interface	None	The LAXX-LG interface includes a 9-ft (3.54-m) cable terminated with a standard EIA connector (no modem control features).
LAXX-LN	Scale, Pointer, and Window Kit	Column scale, Line Indicator, and Column Pointer	Operator convenience items that assist in positioning the print head on preprinted forms and in locating horizontal tabs.
LAXX-LM	Acoustic Coupler	Carrier Detect Lamp	Provides a data interface between DEC-writer and standard telephone handset.

The control logic for the M7728 board is shown in Figure 9-7. As stated previously, there is no difference in the operation, configuration, or programming of the Microprogrammed Controller. New identification numbers are assigned to the components and their physical location on the circuit board are changed, but the basic function of each remains the same. The new numbers and schematic sheet locations are noted on Figure 9-7.

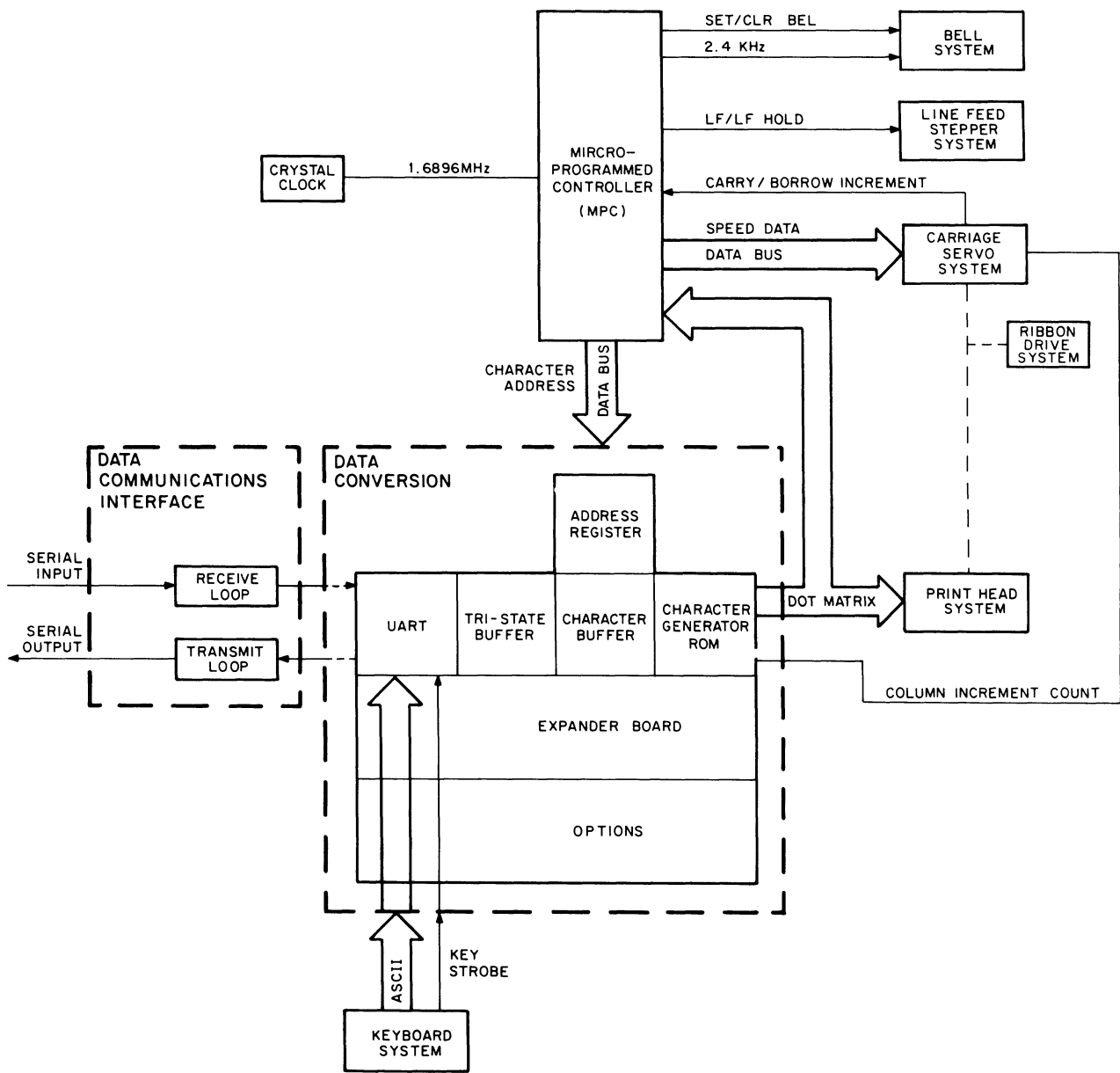
The major area of change effects the receive and transmit data paths.

9.8.1 New Transmit Path

Keyboard data now passes through the Expander Board before it is applied to the transmit section of the UART. As this data is routed across the Expander, two switching methods are employed to ensure that installed options can break this data path and insert characters into the transmit data. This keyboard steering is shown in Figure 9-8. Hardware steering is accomplished by physically moving the cable to the UART between connectors J1 and J2 on the Expander Board. When inserted in J2, keyboard data and the keystroke is routed right across the Expander without any interruptions. When the Automatic Answerback Option or the Automatic Line Feed Option is installed, the cable is moved to J1 and the data path is now through these options. There is a logic switch in these options that allows the options to break the keyboard data path and insert either an answerback message or a line feed command. After inserting the option-generated characters and keystrokes, the logic switch allows keyboard data to pass out to the UART again.

9.8.2 New Receive Path

On the M7728 board, received data and parity error are routed through the UART to the Tri-State Buffer rather than right to the Character Buffer as on the M7722 and M7723 boards. This Tri-State Buffer permits the options to sample the UART output data before the Character Buffer receives it. The options monitor the incoming data on the bi-directional line and can insert data on this line to be applied to the Character Buffer. The output of the Character Buffer can be sampled by an Optional Character Set Option which can substitute a new dot matrix pattern for the pattern normally generated for this character by the Character Generator ROM.



CP-2333

Figure 9-6 Basic Block Diagram of M7728 Logic Board

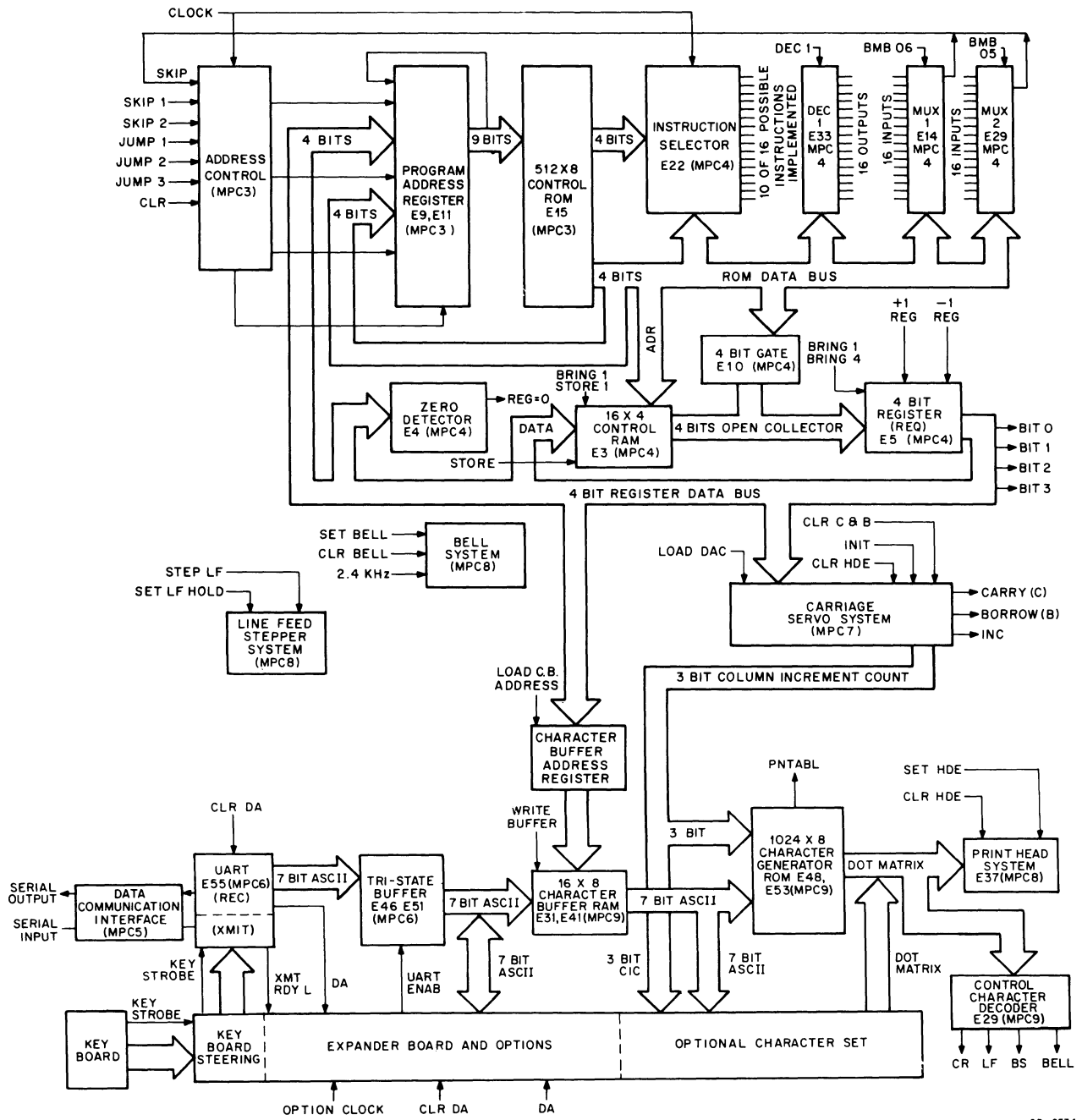
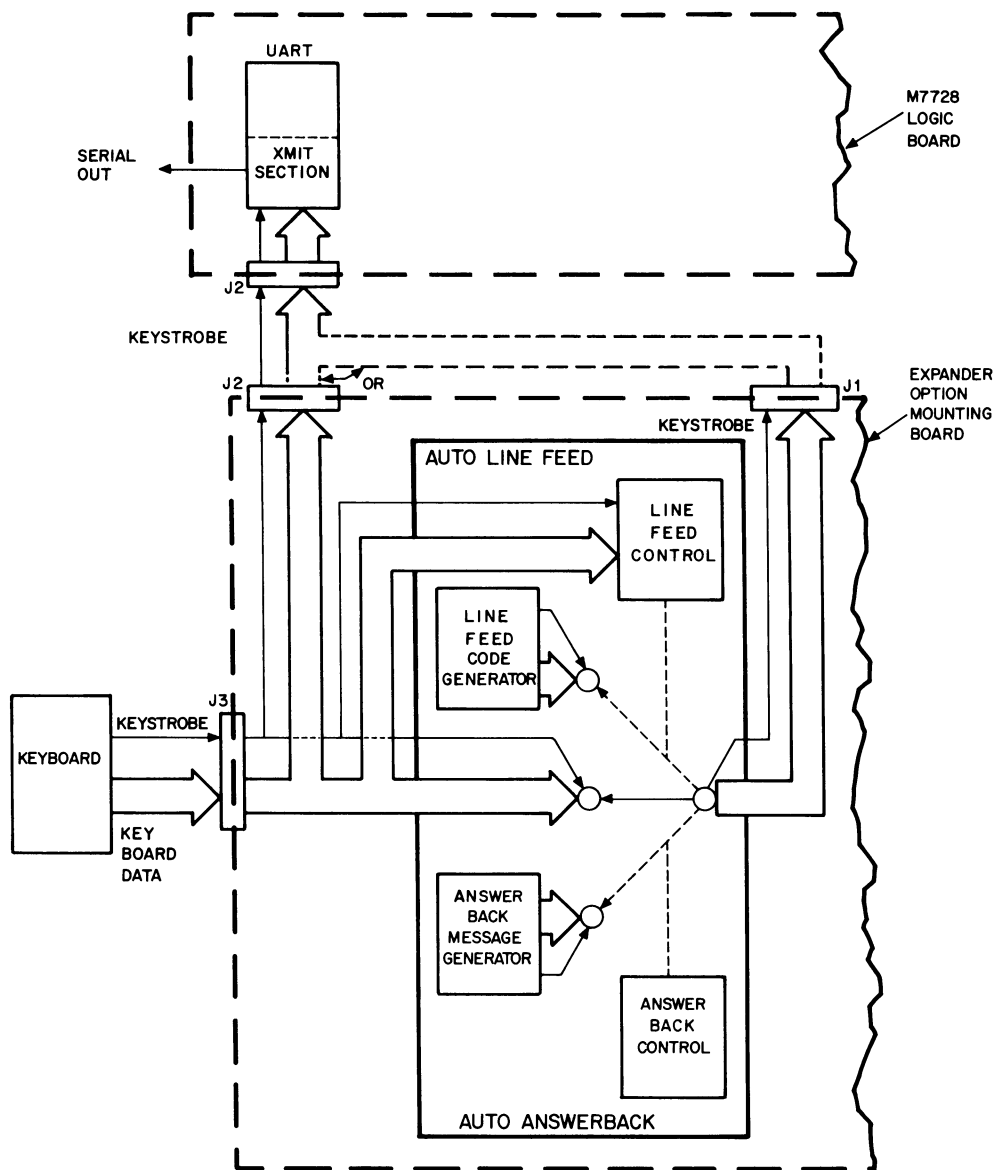


Figure 9-7 M7728 Control Logic Diagram



CP-2335

Figure 9-8 Steering of Keyboard Data

9.8.3 Transmit Operation with Options Installed

Options that insert data into the keyboard data path between the keyboard and the transmit section of the UART require a timing control signal to ensure that the UART is ready to accept more data. This control signal is the XMIT RDY L signal which is a high level when the UART is not ready to accept another character and is low when another character can be processed. This signal is used to stroke both the option-generated character and keystroke out of the option. The XMIT RDY L signal associated with the last character generated by the option causes the logic switch to revert back to the normal position and allow keyboard data to pass again.

9.8.4 Receive Operation with Options Installed

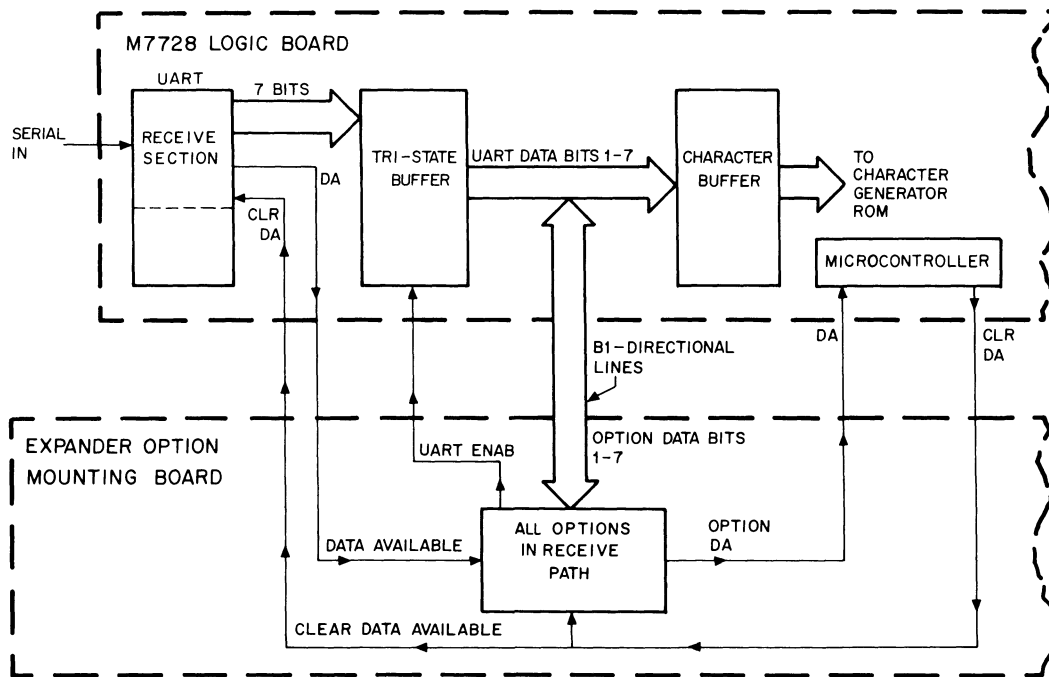
Figure 9-9 shows the signals and components that effect the receive operation. After the UART converts incoming serial data into seven parallel bits, it places these bits on the data lines to the Tri-State Buffer. Normally, as the UART is ready to output data the DATA AVAILABLE (DA) line goes to a low level. The microprocessor uses this low level to load the seven bits into the Character Buffer. In the M7728 board this DA signal is applied serially through all receive options before it is sent to the microprocessor.

At each option the DA signal initiates an option-decoding function on the character present on the bidirectional lines from the Tri-State Buffer. If the character is a command or code that is not recognized by the first option, the DA signal is passed along to the next option to be used to decode the character at that option.

After being routed through all options to the microprocessor, the character is loaded into the Character Buffer through the Tri-State Buffer. The remaining processes to the print head are the same as in the M7722 and M7723 boards.

If the character present at the output of the UART is decoded by an option, this option blocks the data through the Tri-State Buffer (using the UART ENAB signal). The option then places a character on the bidirectional lines to the Character Buffer and issues the DA signal to the microprocessor. As before, the microprocessor commands the Character Buffer to load, but now the character loaded is taken from the option, not from the UART through the Tri-State Buffer.

After processing a character, the microprocessor issues the CLEAR DATA AVAILABLE (CLR DA) signal which causes the UART to place the next incoming character on the lines to the Tri-State Buffer. If an option is going to insert more than one character (as when performing a top-of-form operation), the option holds the Tri-State Buffer disabled, places another character on the bidirectional line and issues another option-generated DA signal. This action continues until the option has finished inserting characters. The CLR DA signal associated with the last character inserted enables the Tri-State Buffer and received data now passes through in a normal manner.



CP-2336

Figure 9-9 Receive Operations of M7728 Logic Board

CHAPTER 10

COMPRESSED FONT OPTION KIT (LAXX-KJ)

10.1 INTRODUCTION TO COMPRESSED FONT

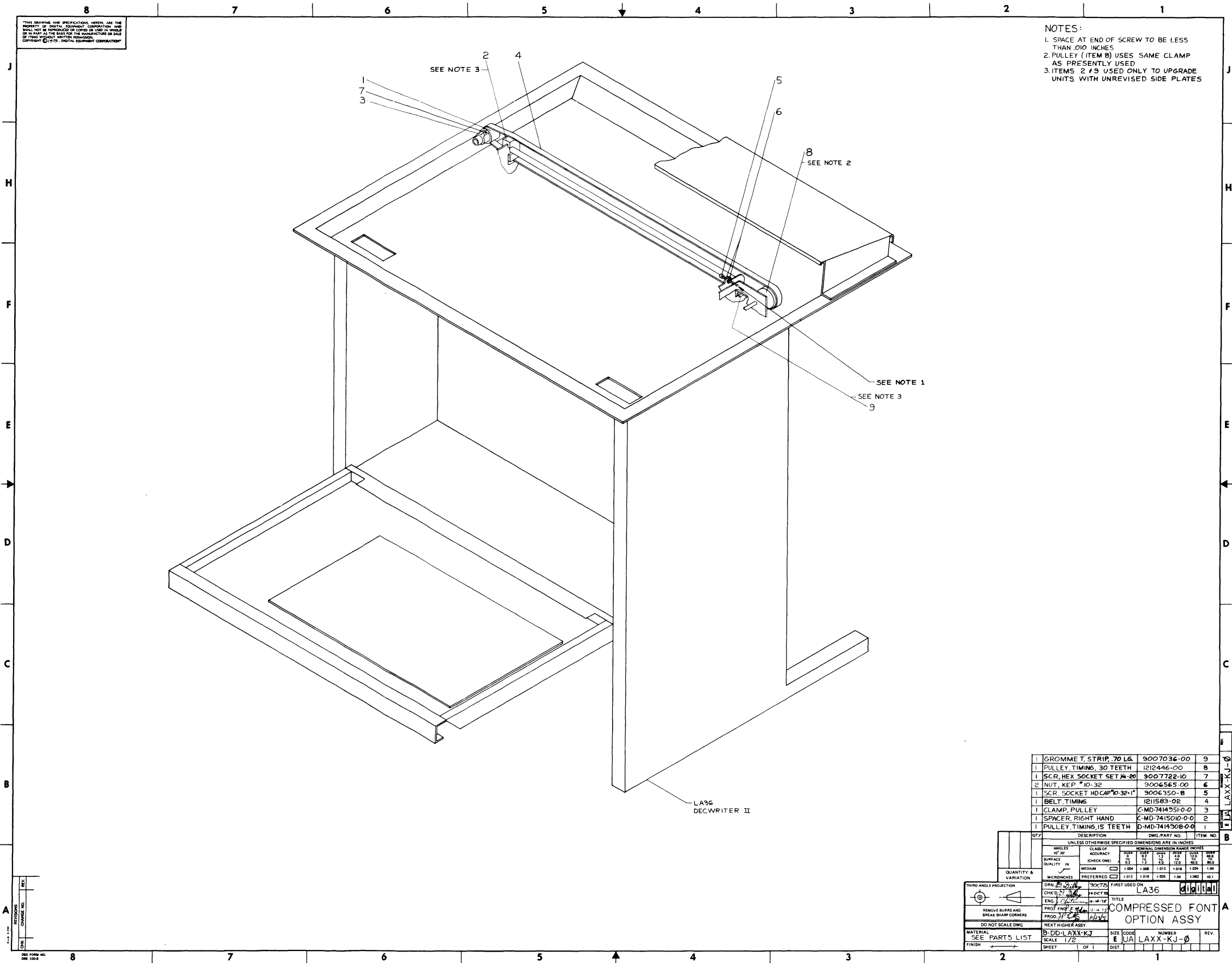
The Compressed Font Option permits a DECwriter to print 132 characters on a 8-1/2 in. line. (Normally, the DECwriter prints 132 characters in 13.2 in.)

The option does not make any electrical or functional changes to the basic operation of the DECwriter. Only slight mechanical changes are required to modify the character spacing along a line. These changes include replacing the two timing pulleys with new pulleys having a greater number of teeth and installing a timing belt that matches these new pulleys.

All timing sequences and printing speeds remain the same. The printed characters retain the same vertical height; only their horizontal width is decreased.

10.2 LAXX-KJ PRINT SET

The figure at the end of this chapter is the LAXX-KJ print set.



QTY	DESCRIPTION	DWG. PART NO.	ITEM NO.
1	GROMMET, STRIP, .70 LG.	9007036-00	9
1	PULLEY, TIMING, 30 TEETH	I212446-00	8
1	SCR, HEX. SOCKET SET #4-20	9007722-10	7
2	NUT, KEP #10-32	9006565-00	6
1	SCR, SOCKET HD CAP #10-32*1"	9006350-B	5
1	BELT, TIMING	I211583-02	4
1	CLAMP, PULLEY	C-MD-7414251-0-0	3
1	SPACER, RIGHT HAND	C-MD-7415010-0-0	2
1	PULLEY, TIMING, 15 TEETH	D-MD-7414908-0-0	1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	
ANGLES	CLASS OF ACCURACY
H° 30'	0 15 30 45 60 75 90
SURFACE QUALITY	CHECK ONE
IN	33 75 15 126 200 300
QUANTITY & VARIATION	MEDIUM
QUANTITY	1.004 1.008 1.012 1.016 1.020 1.024
VARIATION	PREFERRED
MICROINCHES	1.012 1.016 1.020 1.024 1.028
THIRD ANGLE PROJECTION	FIRST USE ON
DATE	PROJECT
CHKD BY	LA36
ENG BY	TITLE
PROJ ENGR	COMPRESSED FONT
PROD BY	OPTION ASSY
DO NOT SCALE DWG	NEXT HIGHER ASSY
MATERIAL SEE PARTS LIST	SIZE CODE NUMBER
FINISH	SCALE 1/2" = 1" DIST

CHAPTER 11

FORMS CONTROL OPTION KIT (LAXX-KV)

11.1 FORMS CONTROL INTRODUCTION

The Forms Control Option adds a top-of-form capability to a DECwriter. The primary function of the option is to locate the top of form by monitoring the number of line feed actions performed by the printer mechanism. Then, when commanded by a form feed code, this option issues the correct number of option-generated line feed (LF) codes required to advance the paper to the next top of form.

The option samples data out of the UART and performs all internal incrementing, resetting, and line feed generating functions before the character is passed on to the Character Buffer for normal terminal action.

11.2 FORMS CONTROL FUNCTIONAL DIAGRAM

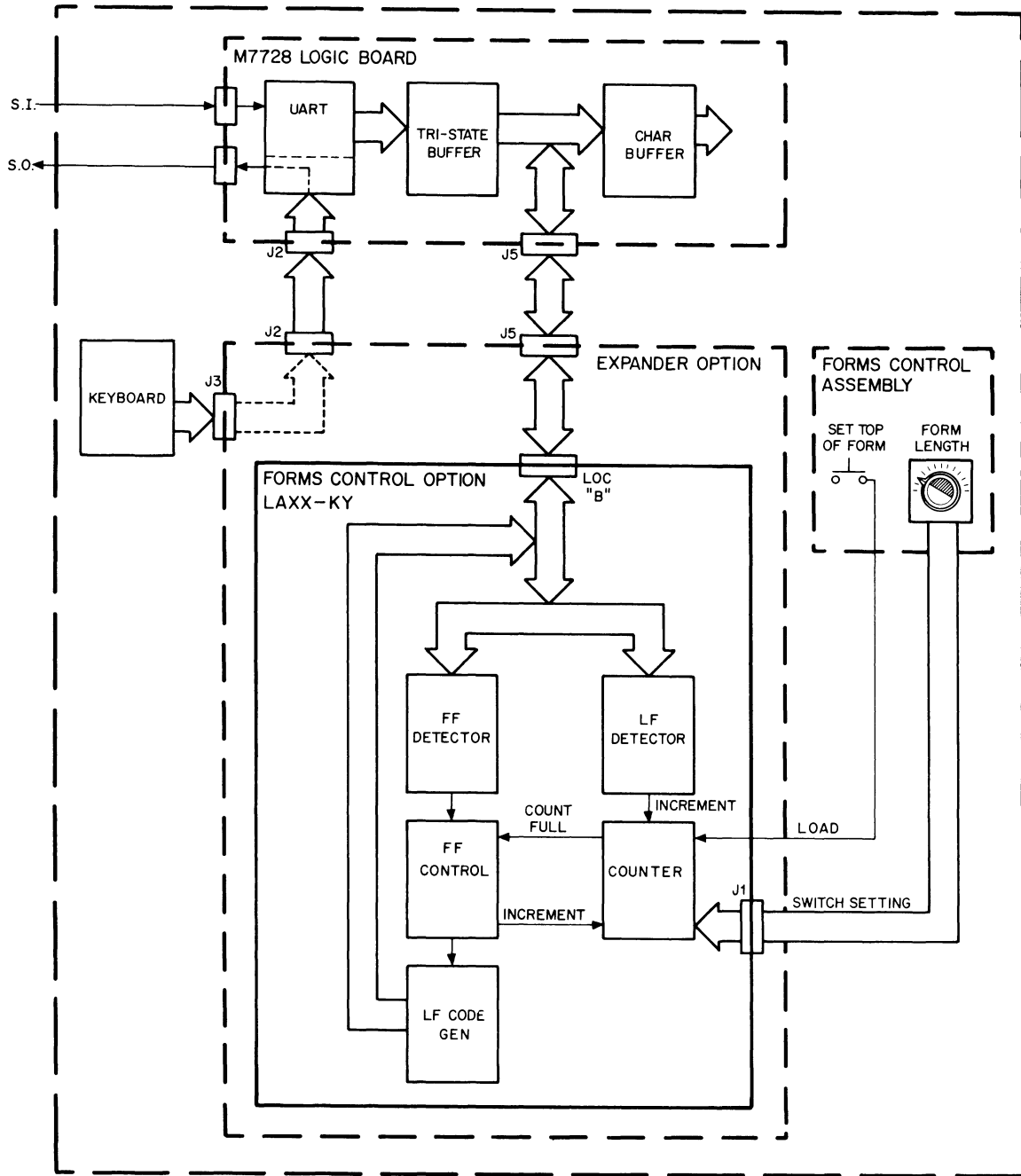
Figure 11-1 shows the Forms Control Option in a typical installation. The Forms Control Assembly is physically attached to the right side of the printer mechanism and the circuit board is connected by an edge connector at location B of the Expander Option Mounting Kit. A cable harness connects the two assemblies. At each end of this harness is a Mate-N-Lok connector and a pair of Faston terminals. One connector is connected to J1 on the option circuit board, the other end to the FORMS LENGTH switch on the Forms Control Assembly. The Faston terminals connect to lugs on the SET TOP OF FORM switch and lugs on the option circuit board. The FORMS LENGTH switch is a 12-position rotary switch and the SET TOP OF FORM switch is a momentary-contact pushbutton. Each position of the FORMS LENGTH switch represents the length (in inches) of a pre-established format (such as a preprinted form) that can be used with the option. In normal operation, the FORMS LENGTH switch is set to the length of the form being used; then the SET TOP OF FORM switch is depressed to load this value into the Counter on the option circuit board.

Data processed by the UART, whether incoming SI or locally generated at the keyboard, is available at location B on the Expander Option Mounting Board. The option monitors this data for either a line feed code or a form feed code. All other codes or characters do not effect the option.

When a line feed code is detected (indicating that the paper will advance one line), the Counter holding the form length value is incremented by one line. Each successive line feed code increments the Counter until its value equals the preset value established by the FORMS LENGTH switch. At this point the print head is at the top of the next form and the Counter is automatically preset with the value of the FORMS LENGTH switch again.

When a form feed (FF) code is detected by the option, four major events occur:

1. UART is disabled.
2. Line Feed Code Generator is enabled.
3. Counter is incremented.
4. Option-generated Data Available (DA) signal is sent to the Character Buffer.



CP-2343

Figure 11-1 Forms Control Functional Block Diagram

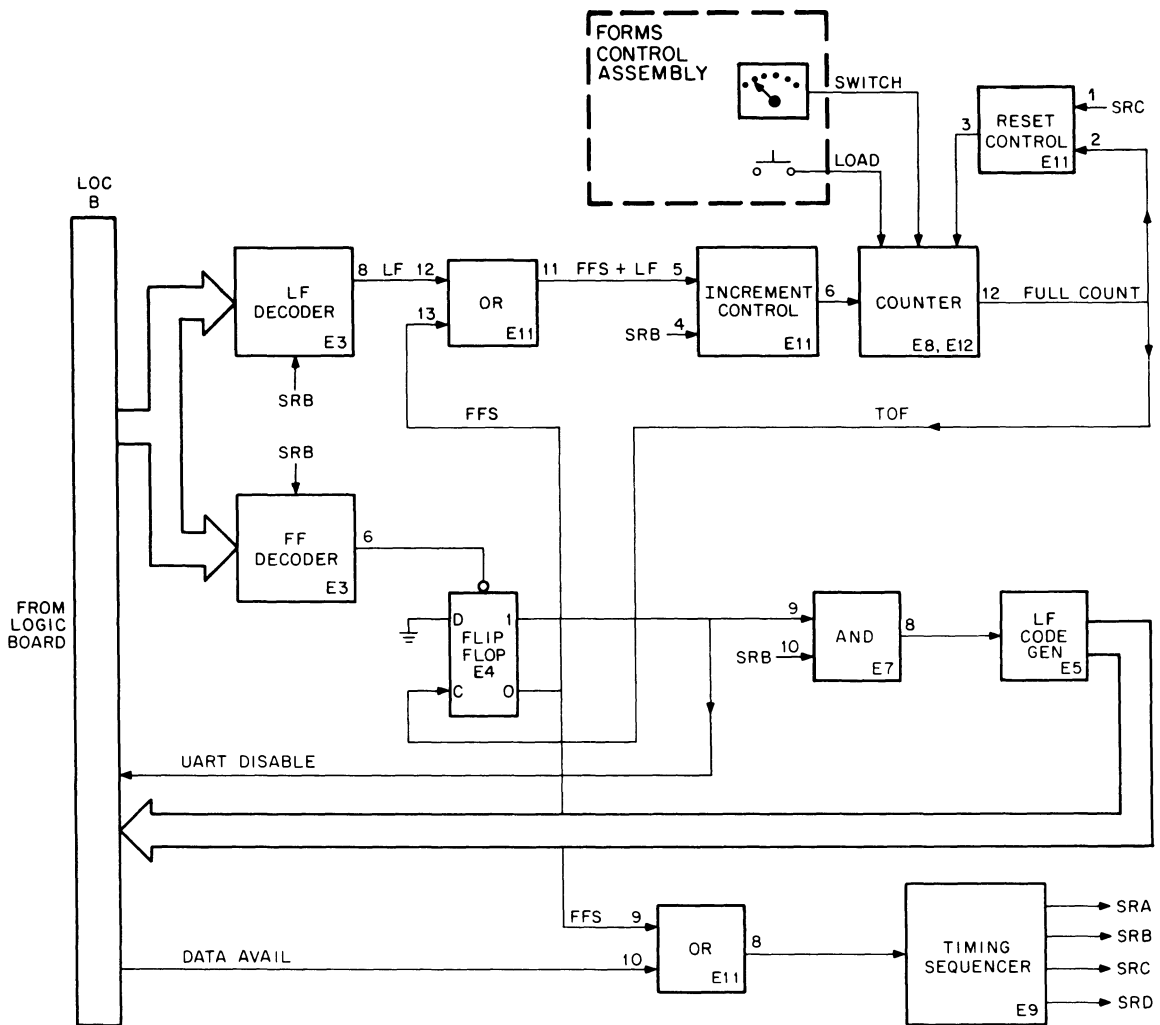
The option holds the UART disabled, continues to generate line feed codes, and increments the Counter until the count overflows. At this time the printer mechanism is at the top of the next form and the following three events occur:

1. Counter is preset to the value of FORMS LENGTH switch setting.
2. Line Feed Code Generator is disabled.
3. UART is enabled.

With the UART enabled again, data passes from the UART to the Character Buffer and the option monitors for line feed and form feed codes.

11.3 FORMS CONTROL BASIC BLOCK DIAGRAM

The basic block diagram for the Forms Control Option is shown in Figure 11-2. This diagram is a simplified representation of the forms control circuit schematic (D-CS-M7735-0-1). Circuit designations and pin numbers indicated on Figure 11-2 correlate with corresponding components on the schematic. Buffers, inverters, and other components that do not have major operational functions are omitted from the block diagram.



CP-2344

Figure 11-2 Forms Control Basic Block Diagram

The Forms Control Option can be divided into the following three functional areas:

1. Counter Circuit
2. Option Timing
3. Operational Sequences

11.3.1 Counter Circuit

The Counter circuit consists of the following four units:

1. Counter (E8 and E12)
2. Increment Control (E11)
3. Reset Control (E11)
4. SET TOP OF FORM and FORMS LENGTH Switches on Forms Control Assembly

The Counter chips (E8 and E12) form a 256-bit (line) up counter that is incremented by a low signal transition on E8-8. The Counter accepts one of 12 preset values as determined by the position of the FORMS LENGTH switch. Each switch position loads a number that is 128 minus the maximum number of lines on a specific form. For instance: if an 11-in. form is to be used, the FORMS LENGTH switch is set to position No. 11 and the SET TOP OF FORM switch is depressed. On an 11-in. form, the maximum number of printable lines is 66 (11 in. times 6 lines per inch). The 256-line Counter is preset with 62 lines from switch position No. 11, leaving 66 lines to be filled. Each line feed code received by the option increments the count upwards by one line. So, if after printing 45 lines (45 line feed codes received) a Top of Form command (form feed code) is received, the paper must be advanced 21 lines to reach the top of the next form. As the option generates these 21 line feed codes, the Increment Control E11 increments the Counter. When the Counter overflows (after 128 increments: preset value plus the number of option-generated line feed codes), the Reset Control E11 reloads the value of the FORMS LENGTH switch back into the Counter again.

11.3.2 Option Timing

The Timing Sequencer E9 establishes all control timing for the Forms Control Option. The timer is a 4-bit shift register that produces the following four sequential timing signals at the designated outputs:

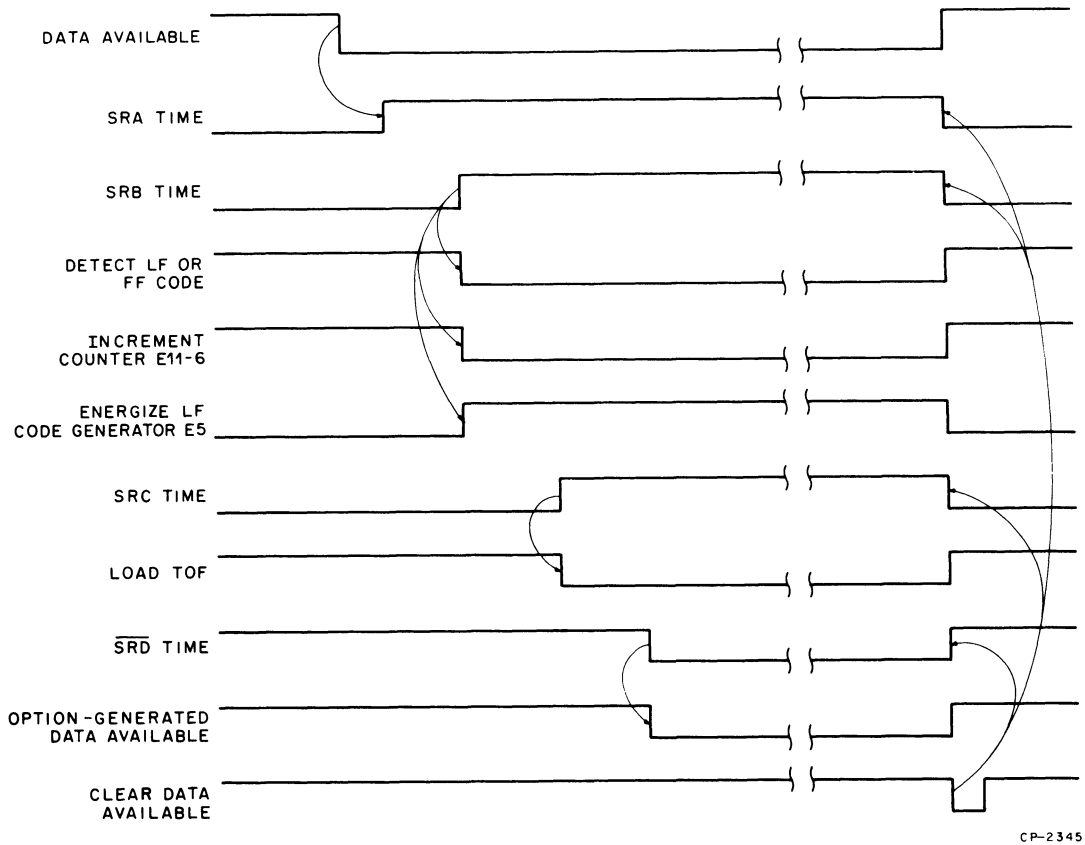
- pin 5 ; SRA
- pin 7 ; SRB
- pin 9 ; SRC
- pin 12 ; SRD

A high level signal on the LD and SHF pins (1 and 13) of E9 cause the high level at pin 4 to be shifted right at the rate of the Option Clock input at pin 6 (approximately 1.2 μ s per shift). Either the Data Available signal from the UART or the Form Feed Stored signal from FF flip-flop E4 activates the Timing Sequencer.

The following events occur at each of the four sequencer outputs:

Time	Event
SRA	<ul style="list-style-type: none">• Not used – but provides a 1.2 μs delay for data stabilization
SRB	<ul style="list-style-type: none">• Decode line feed code• Decode form feed code• Increment Counter• Enable Line Feed Code Generator
SRC	<ul style="list-style-type: none">• Reload Counter
SRD	<ul style="list-style-type: none">• Issue Data Available signal to Character Buffer

Figure 11-3 shows the timing sequence for the Forms Control Option.



CP-2345

Figure 11-3 Timing Sequence for Forms Control Option

11.4 OPERATIONAL SEQUENCES

The Forms Control Option has three basic operational sequences that are dependent on what character is being sent by the UART. These are:

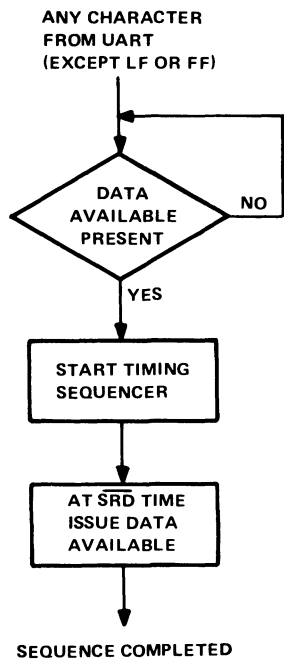
1. Receive any character but line feed code or form feed code
2. Decode a line feed code
3. Decode a form feed code

11.4.1 Any Character Received

Figure 11-4 shows the operational sequence performed when any character is received. When the option receives a Data Available signal from the UART, a character code is present on the data lines at location B. If this code is for any character, but neither a line feed nor form feed code, the only action on the option is the initiation of the Timing Sequencer by the Data Available signal. At SRD time (approximately $4.8 \mu\text{s}$ after receiving the Data Available signal) the option issues the option-generated Data Available signal which is sent to the microprocessor. The character can now pass out from the UART in a normal manner.

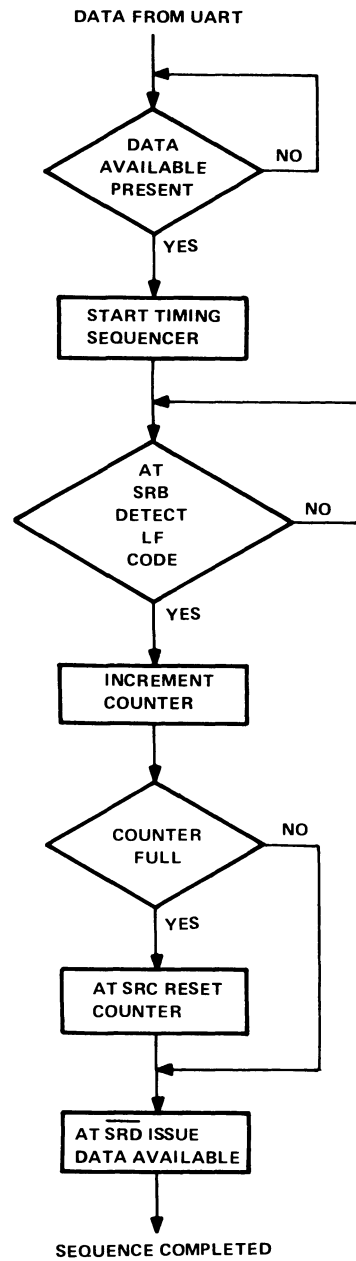
11.4.2 Line Feed Code Decoded

Figure 11-5 shows the operational sequence performed when a line feed code is received. A line feed code and Data Available signal from the UART are decoded during SRB time by LF Decoder E3. The output from pin 8 of the LF Decoder is applied through the Increment Control E11 to the Counter E8 and E12. Each line feed code increments the Counter by one line. If the Counter increments to a full count, which indicates having reached the top of the next form, the Counter outputs a TOF signal on pin 12. This TOF signal is used at SRC time to reset the Counter with the value set by the FORMS CONTROL switch.



CP-2346

Figure 11-4 Forms Control Operational Sequence When Any Character Received



CP-2347

Figure 11-5 Forms Control Operational Sequence When Line Feed Code Received

If the Counter does not overflow (no TOF signal) when incremented, no further action is taken until SRD time when the option-generated Data Available signal is sent to the microprocessor. The Character Buffer now accepts the line feed code from the UART and processes it in a normal manner.

11.4.3 Form Feed Code Decoded

Figure 11-6 shows the operational sequence performed when a form feed code is received. A form feed code and the Data Available signal from the UART are decoded during SRB time by FF Decoder E3. This action initiates the major function of the option: issuing the proper number of line feed codes to advance the paper to the next top of form position. The output of FF Decoder E3 sets FF flip-flop EA which causes the following three actions to occur during SRB time.

1. Disables the UART (held disabled until FF sequence completed)
2. Enables the Line Feed Code Generator E5
3. Increments the Counter E8 and E12

Disabling the UART prevents incoming data from being applied to the Character Buffer and allows option-generated line feed codes to be sent to the Character Buffer. As the Line Feed Code Generator E5 is energized, the Increment Control E11 increments the Counter by one line. If the Counter increments to a full count, it outputs a TOF signal on pin 12. This TOF signal is used to clock E4 pin 5 to a high level and to reset the Counter with the FORMS LENGTH switch value at SRC time. At SRD time the option-generated Data Available signal is issued and a line feed code is sent to the microprocessor. When the CLR DA signal is sent back to the option indicating that the line feed code was processed, the CLR DA signal resets E4 at pin 1. The TOFSL signal generated when E4 resets causes the FF flip-flop E4 to reset also.

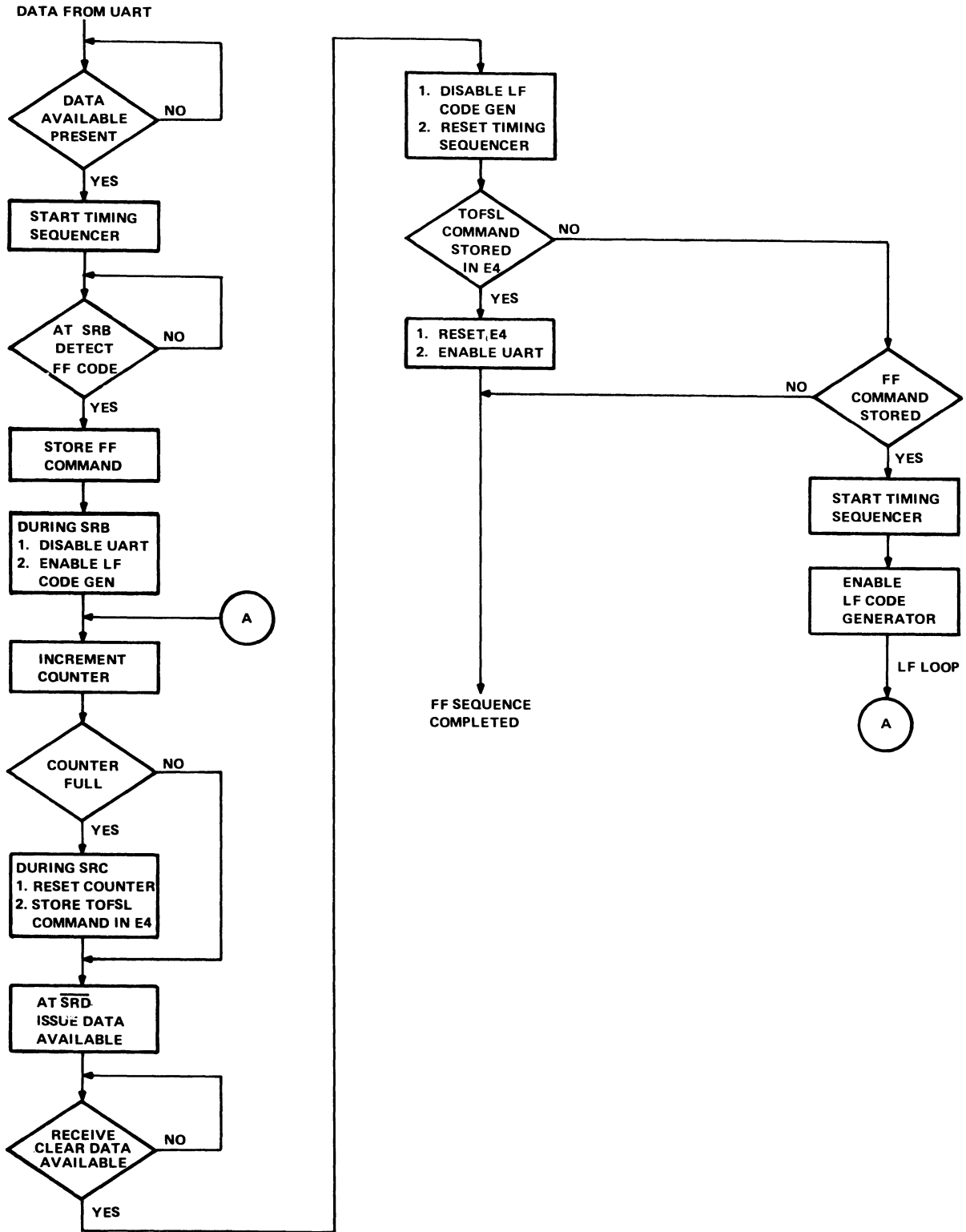
If the Counter does not overflow after being incremented (no TOF signal), the FF flip-flop E4 remains set, holding the UART disabled and the Line Feed Code Generator E5 enabled. The CLR DA signal returning after the first line feed code was processed resets the Timing Sequencer. But because the FF flip-flop is still set, the Form Feed Stored (FFS) signal immediately restarts the Timing Sequencer again. At SRB time, the Counter is incremented again and the Line Feed Code Generator issues another line feed code. If this increment still does not overflow the Counter, the line feed code generation sequence is repeated again and again until the TOF signal is present at pin 12 of the Counter. When the CLR DA from the last LF returns, the Counter resets and the option removes the disable from the UART and disables the Line Feed Code Generator E5. The option has completed the top of form sequence and is now waiting for line feed or form feed codes before starting any action

11.5 TROUBLESHOOTING

The troubleshooting chart in Table 11-1 lists the common trouble symptoms that could be observed during installation checkout or normal operation.

11.6 LAXX-KV PRINT SET

Figure 11-7 is the supporting diode matrix for the LAXX-KV print set. The print set is shown at the end of this chapter.

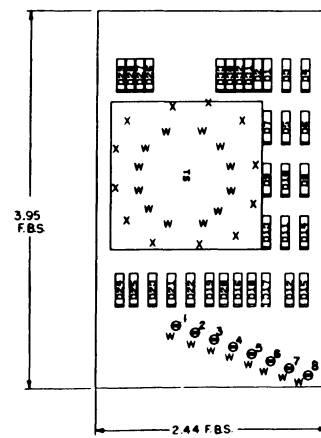
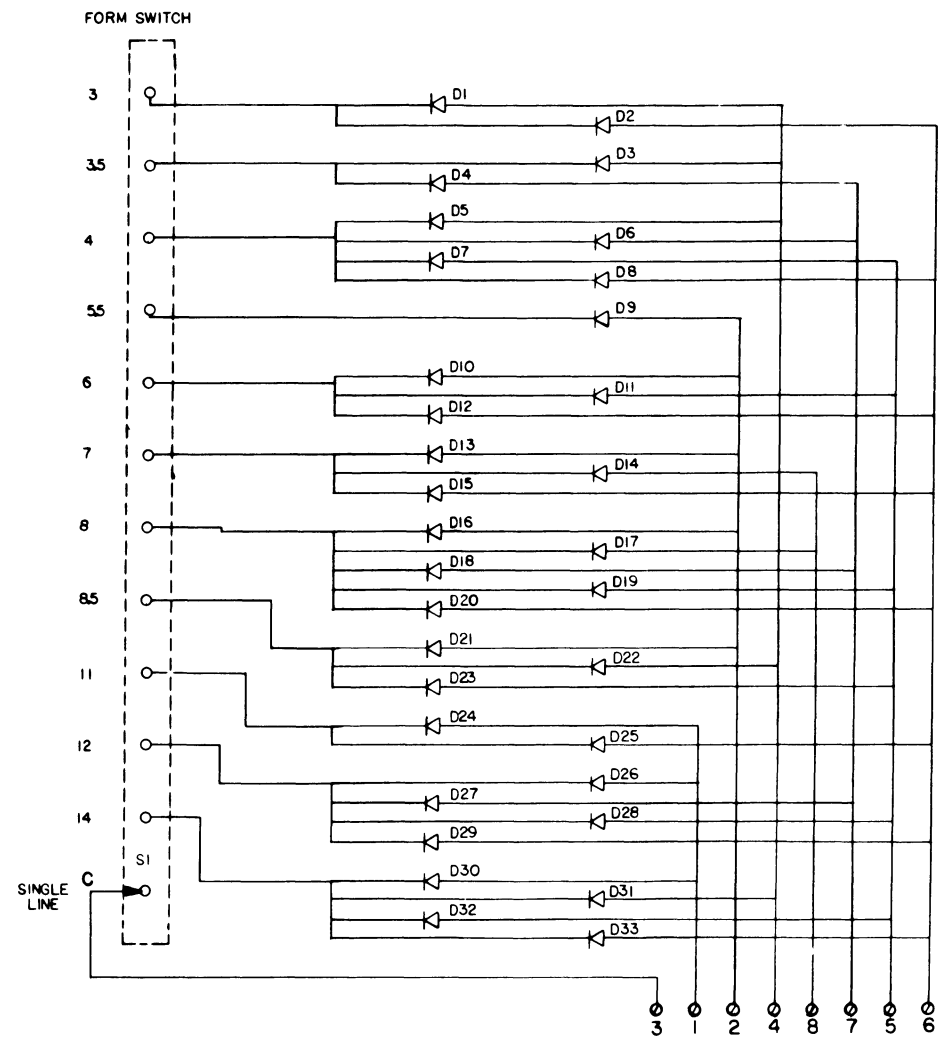


CP-2348

Figure 11-6 Forms Control Operational Sequence When Form Feed Code Received

**Table 11-1
Troubleshooting for Forms Control Option Kit (LAXX-KV)**

Symptom	Problem Area	Probable Cause	Action	Reference
1. After installation improper operation or no operation of terminal	Cabling	Wrong cabling connections	Check all cabling between M7728 Logic Board, Expander Board, and TOF Assembly beneath top cover	Figure 9-4
	Option location	Option inserted in wrong location on Expander Board	Install TOF option in locations A and B	
	Data Available signal distribution	Signal path interrupted	Check for Data Available signal at E11 pin 10 and at E9 pin 12 for the output	D-CS-M7735-0-1, Sheet 3
2. Terminal does not advance to TOF when CTRL L or FF is received	Form Feed Decoder	FF not being decoded	Check E3 pin 6 for indication of FF code	D-CS-M7735-0-1, Sheet 2
	LF Code Generator	LF code not being generated	Check E5 and E2 for the LF code	D-CS-M7735-0-1, Sheet 2



Forms Control Board Pin Numbers

3	1	2	4	8	7	5	6
---	---	---	---	---	---	---	---

Single Line	0	1	1	1	1	1	1
3.0	0	1	1	0	1	1	0
3.5	0	1	1	0	1	0	1
4.0	0	1	1	0	1	0	0
5.5	0	1	0	1	1	1	1
6.0	0	1	0	1	1	1	0
7.0	0	1	0	1	0	1	0
8.0	0	1	0	1	0	0	0
8.5	0	1	0	0	1	1	0
11.0	0	0	1	1	1	1	0
12.0	0	0	1	1	1	0	0
14.0	0	0	1	0	1	1	0

MSB							LSB	
	8	7	6	5	4	3	2	1

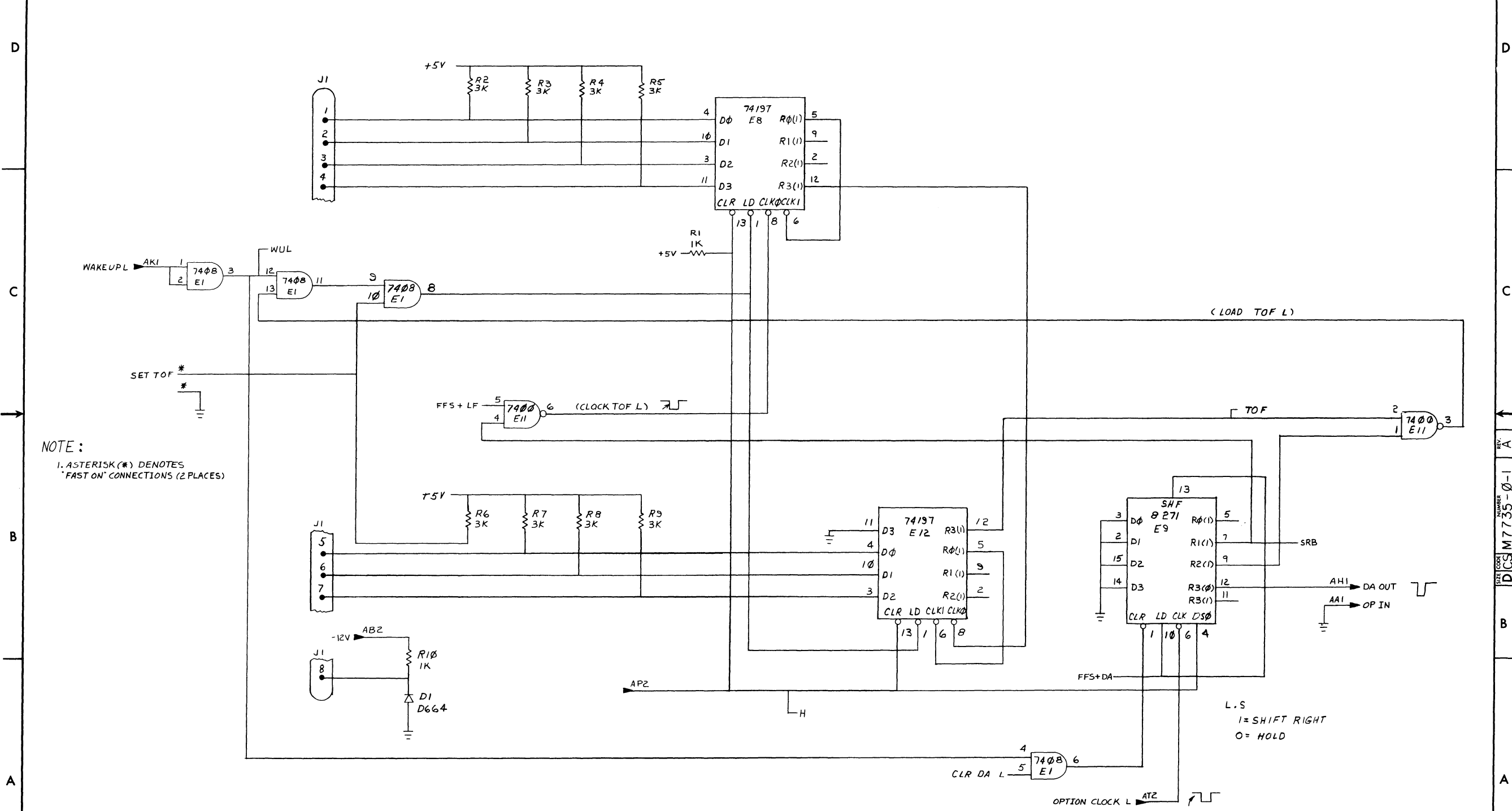
J1 M7735
Sheet 3 of 3

J1 M7736
Sheet 2 of 5

BINARY PATTERN/FORMS LENGTH SELECTED

Figure 11-7 LAXX-KV Form Feed Diode Matrix

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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	TOF OPTION	SIZE CODE	D CS	NUMBER	M 7735 - 0 - 1	REV.	A
SCALE	1:1	SHEET	3	OF	3	DIST.	

CHAPTER 12

SELECTIVE ADDRESSING OPTION (LAXX-KW)

12.1 SELECTIVE ADDRESSING INTRODUCTION

The Selective Addressing Option allows a DECwriter to communicate with other terminals in a multipoint communications network. Generally, it operates in conjunction with the EIA Interface Option (LAXX-LG) and the Automatic Answerback Option (LAXX-KX) to provide the user with a versatile network that is easily configured to receive or transmit data to and from each terminal.

The Selective Addressing Option has two primary functions in the terminal in which it is installed:

1. To allow or inhibit the terminal from transmitting data out from the keyboard.
2. To allow or inhibit the terminal from responding to received data.

12.1.1 Transmit Conditions

A terminal is able to transmit (transmit enabled) when it is the master in the communications network or when it is a uniquely selected slave that has been addressed by the master using its unique address code. As the master, the terminal can select which slave terminals are going to receive and print messages sent from the master's keyboard. When operated as an uniquely selected slave, the terminal's keyboard is activated and two-way conversation can take place between the master and this slave. Only one uniquely selected slave is transmit enabled in the network at any one time and it is always the last slave terminal selected by the master. All other slaves in the network are transmit disabled.

12.1.2 Receive Conditions

The ability of a slave terminal to receive data transmitted by the master is determined by the address class of the terminal. There are three possible address classes for each terminal that permit received data to print.

1. **Broadcast Slaves** – All terminals in the network receive data transmitted by the master.
2. **Group Select Slaves** – Group Address is established by setting switch S2 on the option circuit board. All slaves with the same Group Address receive data transmitted by the master.
3. **Unique Select Slaves** – Each terminal can have a Unique Address which is different than its Group Address and is established by the setting of switch S1. When addressed by the master using this Unique Address, it is possible to have communications between these two terminals and no other terminals in the network. In addition, the master can sequentially address multiple Unique Addresses to form a specific group that receives data from the master.

A terminal prints transmitted characters if it is selected as a slave and is not in the address mode. If not selected, all received characters are automatically converted to the non-printing, non-spacing ACK code. The only exception is if the terminal is in the address mode and an ENQ code is received. This code is not converted to an ACK but is allowed to pass through the Selective Addressing Option to the Answerback Option where it is used.

12.1.3 Operational Modes

Slave terminals operate in either the address mode or the data mode. In the address mode, terminals respond to codes for their Broadcast, Unique Address, or Group Address. In the data mode, slave terminals do not acknowledge their addresses, even though the address is present on the communications line. The master terminal establishes whether the slave terminals are in one mode or the other.

NOTE

After power-up sequence, terminal is in the data mode.

Six commands (generated by five codes) are sent from the master terminal to control the operation of the slaves. Three commands switch the slave terminal from the data mode to the address mode:

1. EOT (CTRL D - 004₈)
2. ETX (CTRL C - 003₈)

The STX (CTRL B - 002₈) command switches the terminal from the address mode back to the data mode. The BELL (CTRL G - 007₈) configures all the slaves in the broadcast mode. The ENQ (CTRL E - 005₈) code is used with Unique Select Slaves to request the stored answerback message. It is also used to transmit disable a Unique Select Slave.

NOTE

Refer to the *LA35/LA36 DECwriter II User's Manual* for a complete description of these codes.

12.2 SELECTIVE ADDRESSING FUNCTIONAL BLOCK DIAGRAM

Figure 12-1 shows the functional block diagram of the Selective Addressing Option. Received data is monitored at the output of the UART for address codes and mode switching commands. When in the address mode, the terminal only responds to codes that select it to receive data. These codes are the Unique or Group Address codes that match addresses stored in the two 7-bit dip switches or the BELL code. When the terminal is not conditioned to receive data transmitted by the master (not selected), it disables the UART and substitutes an ACK code (006₈) for each received ASCII character or command. This ACK code is a non-spacing, non-printing code that has no effect on the terminal. As discussed in the description of the Expander Mounting Board, all incoming data passes through the Selective Addressing Option before the other options in the terminal monitor the data. Therefore, when the terminal is not selected to receive data and all incoming characters are converted to ACK codes, the other options never have a chance to decode their respective commands and the terminal appears to be off-line to the transmitted data.

When the terminal is the master or a transmit-enabled slave, the data from the keyboard is monitored by the EOT Decoder for an EOT code. This code indicates that the transmitted message has ended and the terminal is relinquishing the master or transmit-enable status.

The trilevel line that interconnects the EIA, Auto Answerback, and Selective Addressing Options is used to disable the keyboard (by inhibiting the keystroke) when the terminal is a transmit-disabled slave. When the Selective Addressing Option places an "O" level on this line (transmit disabling the terminal), it cannot be overridden by any of the other options and the "O" level remains until the terminal becomes the master, switches to local, or becomes a transmit-enabled slave.

The DEVICE SELECT and SELECT AVAIL front panel indicators provide a visual indication of the terminal's status. When the DEVICE SELECT light is illuminated, it indicates that the terminal is transmit enabled. When the SELECT AVAIL light is illuminated, the communications network is available and the terminal can become master. When both lights are illuminated, the terminal is the master.

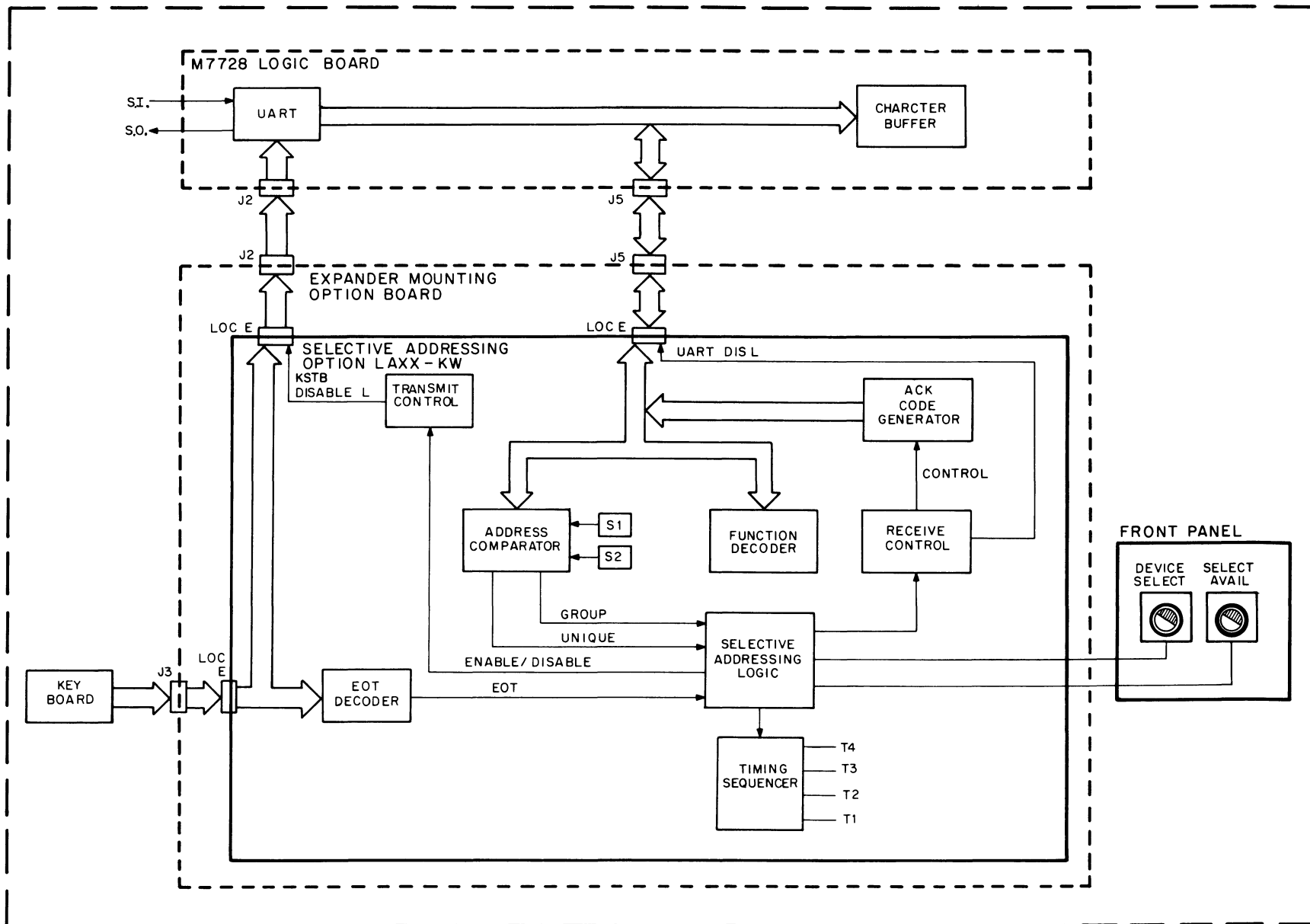


Figure 12-1 Selective Addressing Functional Block Diagram

12.3 SELECTIVE ADDRESSING BASIC BLOCK DIAGRAM

The basic block diagram for the Selective Addressing Option is shown in Figure 12-2. This diagram is a simplified representation of the selective addressing circuit schematic (D-CS-M7737-0-1). Circuit designations and pin numbers indicated on Figure 12-2 correlate with corresponding components on the schematic. Buffers, inverters, and other components that do not have major operational functions are omitted from the block diagram.

12.3.1 Power-Up Sequence

The selective addressing power-up sequence is initiated by the WAKE UP L signal which performs the following four events:

1. Clocks Address flip-flop E11 at pin 3 and places the terminal in the data mode
2. Resets Master flip-flop E11 and places a high level on pin 8 which is applied through Faston connector A to the EIA Interface to indicate that the terminal is not the master
3. Resets SELECT AVAIL flip-flop E10 and places a high level on pin 8 which qualifies half of AND gate E4 at pin 4. The low level from pin 9 of E10 illuminates the SELECT AVAIL light
4. Resets Device Select flip-flop E16 and places a low level on pin 5. This low level sets Xmit No. 1 flip-flop E10 and Xmit No. 2 flip-flop E16

After the wake-up sequence is completed, the terminal can be configured as the master by typing CTRL D and CTRL SPACE or as a slave (non-selected) by receiving a character from another master.

NOTE

If the terminal powered up while another terminal in the network was transmitting, the SELECT AVAIL light would not illuminate or flicker and the terminal would not receive the transmitted data. The extinguishing of the SELECT AVAIL light indicates that there already is a master terminal established in the network. Therefore, the terminal just powering up cannot become the master. The terminal does not print because it was never properly addressed; at wake up it went directly into the data mode. All incoming characters are converted into ACK codes which are disregarded by the terminal.

Typing a CTRL D on the keyboard produces the EOT code which is detected by the EOT Decoder E1, E9, E14, E15, and applied to E4 at pin 5. If no characters have been received by the terminal since wake up, there is a high level at pin 4 of E4. These two high levels qualify AND gate E4 and clock Master flip-flop E11. Pin 8 of E11 goes to a low level which is applied through Faston connector A to the EIA, establishing this terminal as the master. The low from pin 8 of E11 also sets Device Select flip-flop E16 and produces an H level on the trilevel line (KSTBDISABLE L) through NOR E17 and Inverter E8. As Device Select flip-flop sets, the low level on pin 6 and the H level on the KSTB DISABLE L line combine through Q1 and Q2 to illuminate the DEVICE SELECT light. The terminal has now established itself as the master in the communications network.

If after powering up and before typing CTRL D, the terminal receives a character sent by an already-established master, the Data Available signal (DA IN L) associated with this received character starts the Timing Sequencer E13. This sequencer is a 4-bit shift register that shifts the high level on pin 4 to the right at the Option Clock rate (approximately 1.2 μ s per shift). Between T1 and T3 the terminal can decode incoming commands. At T2 time, the high level on pin 8 of Master flip-flop E11 (E11 reset at wake up) is clocked through SELECT AVAIL flip-flop E10 to extinguish the SELECT AVAIL light. As SELECT AVAIL flip-flop E10 clocks, a low level from pin

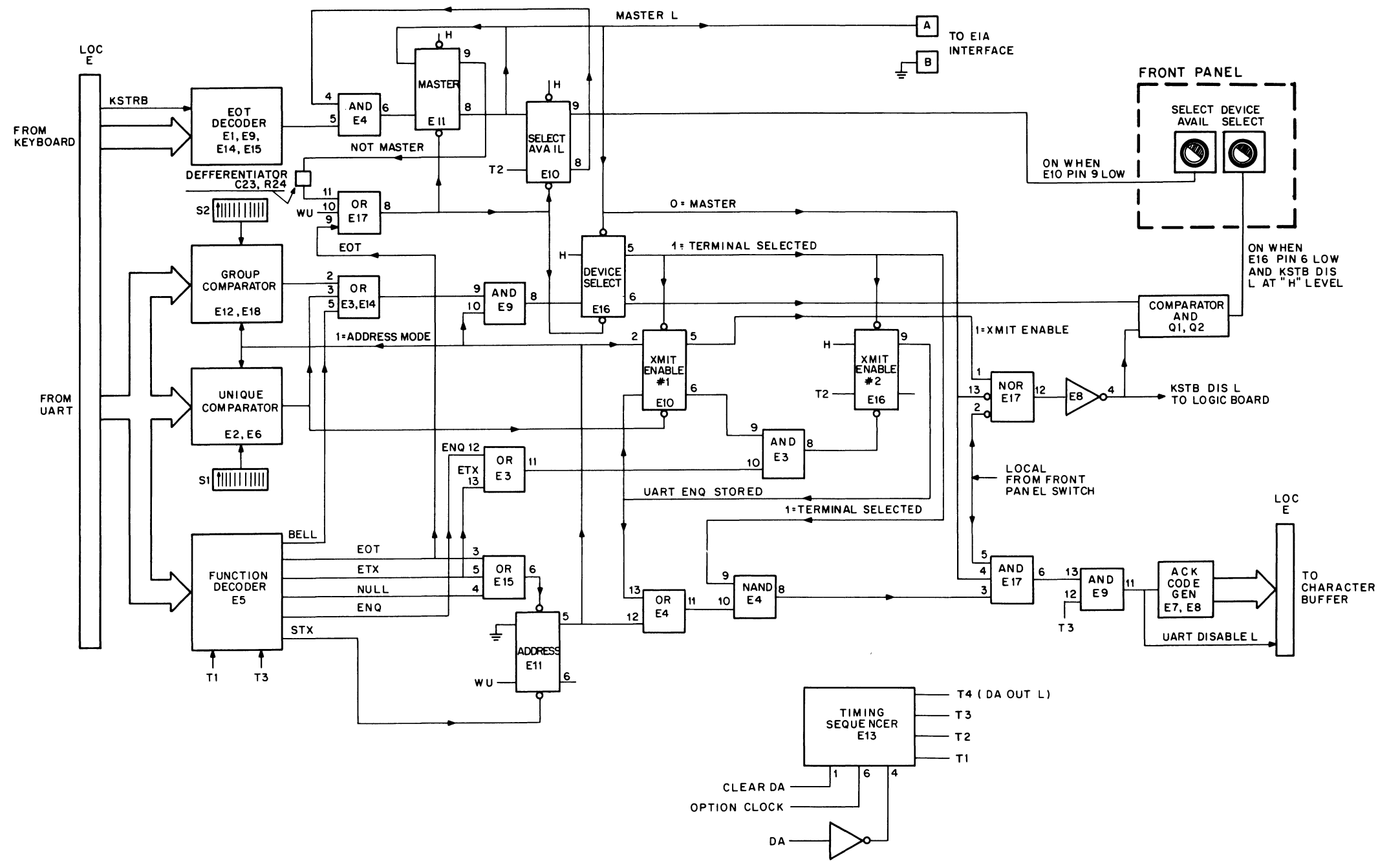


Figure 12-2 Selective Addressing Basic Block Diagram

8 is applied to pin 4 of AND gate E4 to inhibit any attempt by the terminal to become master by typing CTRL D on the keyboard. At this time the terminal is not master and has not been selected as a slave (because at wake up it went directly into the data mode not the address mode). Therefore, at T4 time AND gate E9 is qualified and enables the ACK Code Generator E7, E8; disables the UART through E8 pin 12; and issues the option-generated Data Available signal out of E13 pin 12. Thus, the incoming character code is converted to an ACK code and the terminal does not respond to any data on the line. This action continues until the master ends its transmission with an EOT code (CTRL D). This EOT code is received by all terminals in the network and causes the previously selected slave terminals to become deselected. The EOT indication from the Function Decoder E5 is applied through E17 pin 9 to reset Master flip-flop E11, SELECT AVAIL flip-flop E10, and Device Select flip-flop E16. As E10 resets, the SELECT AVAIL light illuminates and as E16 resets, the terminal becomes deselected. The EOT indication also sets the Address flip-flop E11 and applies a high to E4 pin 4. This high is inverted once through E4 pin 11, then again through E4 pin 8, and coupled through E17 pin 6 to combine at AND gate E9 at T3 time to disable the UART, enable the ACK Code Generator, and issue the Data Available signal at T4. This action substitutes an ACK code for the incoming EOT code.

12.3.2 Address Mode

In the address mode, the Function Decoder E5 and the Group E12, E18 and Unique E2, E6 Comparators are monitoring the incoming data for their respective address codes. Prior to transmitting an address code the master issues a NULL code (CTRL SPACE) which places all slaves in the address mode. The NULL code is detected by Function Decoder E5 during T1 and T3 then applied through E15 to set Address flip-flop E11. As E11 sets, the high level from pin 5 initiates the following four actions:

1. Disables the UART and enables the ACK Code Generator. This action takes place through E4 pin 12, E4 pin 10, E17 pin 3, and E9 pin 11. This converts the NULL code to an ACK code.
2. The high level enables both the Group and Unique Address Comparators, which are exclusive ORs that compare the programmed setting in the 7-bit dip switches to the code present on the UART lines.
3. The high is also applied to pin 10 of AND gate E9. If either a Group or Unique Address or BELL code is detected when the terminal is in the address mode, E9 is qualified and it clocks Device Select flip-flop E16. This action causes the terminal to be selected as a slave.
4. The other location where the high level from pin 5 of the Address flip-flop is applied is to the D input (pin 2) of Xmit No. 1 flip-flop E10.

After being selected as a slave, there are four possible types of slaves; Broadcast, Group, Unique one-way, and Unique two-way.

12.3.2.1 Broadcast Slaves – These slaves are addressed by the master using the BELL code which is detected by the Function Decoder E5, coupled through E3 and E9 to clock E16. The low level from E16 pin 6 is applied to Q1, Q2, which act as both an AND gate and a Comparator. The Comparator Section monitors the status of the trilevel line. To illuminate the DEVICE SELECT light, the trilevel line must be at the H state and the output of E16 pin 6 must be low.

Receiving an STX code resets Address flip-flop E11 and places the terminal in the data mode. All received characters now print.

12.3.2.2 Group Slaves – Receiving an address code that corresponds to the code setting of switch S2 produces a group indication that is transferred through E14, E3, and E9 to clock Device Select flip-flop E16. Again the received Group Address code is converted to an ACK code and sent on to the Character Buffer. Also all group slaves are transmit disabled in the same manner as the Broadcast Slaves. (Trilevel line is “O”.)

Decoding an STX code places the terminal in the data mode and all received characters are printed.

12.3.2.3 Unique One-Way Slaves – Receiving the Unique code that matches the S1 switch setting produces the same action as the Broadcast and Group Address codes; the UART is disabled, the Unique code is converted to an ACK code, and it is transferred to the Character Buffer at T4 time. In addition, the Unique code indication resets Xmit Enable No. 1 flip-flop E10, placing a low level on pin 5. This low level from pin 5 is applied through E17 and E8 to transmit enable the terminal (the trilevel KSTB DISABLE L signal goes to the “H” level providing the EIA is clear to send). The next code received is the ENQ code (CTRL E) which resets Xmit Enable No. 2 flip-flop E16 placing a low level on pin 9. To transmit disable this terminal the next character received must be any character but a valid address. The Data Available signal for this character starts the timing sequence and at T2 E16 clocks a high level out on pin 9. This high causes Xmit Enable No. 1 flip-flop E10 to clock the high level on pin 2 (established when the terminal is in the Address Mode) out on pin 5. The high level from pin 5 of E11 is applied through E17 pin 1 to E8 and forces the trilevel line to the “O” state which transmit disables the terminal. The master then sends the STX code (CTRL B) which places the terminal in the data mode. The terminal can now receive but not transmit back to the master.

12.3.2.4 Unique Two-Way Slaves – The master establishes two-way communications with a designated slave by typing the Unique Address code, then the ENQ code, then the STX code. The only difference between this configuration and the one-way configuration is that there is no character sent between the ENQ and the STX codes. The action at the slave terminal is the same except that when the terminal goes to the transmit enable condition as the Unique code is detected (Xmit Enable No. 1 flip-flop E10 resets and places a low level on pin 5) it stays transmit enabled. The ENQ code resets Xmit Enable No. 2 flip-flop E16 in the same manner placing a low level on pin 9 which does not cause E10 to clock. The next character received is the STX code which resets Address flip-flop E11 and causes the terminal to switch to the data mode. As E11 resets, a low level is placed on pin 2 of E10. At T2 time E16 clocks, causing E10 to clock this low level out pin 5 to E17 to keep the terminal transmit enabled (trilevel line stays at “H” level providing the EIA is clear to send). The terminal can transmit to and receive from the master.

Figure 12-3 contains the timing diagram for the code sequence that establish unique one-way or two-way slaves.

12.3.2.5 Select Add-On Slaves – To add other terminals already selected – without having to readdress all previously selected terminals – the ETX code (CTRL C) is used. This code resets all terminals in the address mode and allows the new terminals to respond to their addresses. The ETX code affects the terminals just as the ENQ code does. The last terminal addressed is also transmit enabled if the last unique address is not followed by a non-valid dummy address.

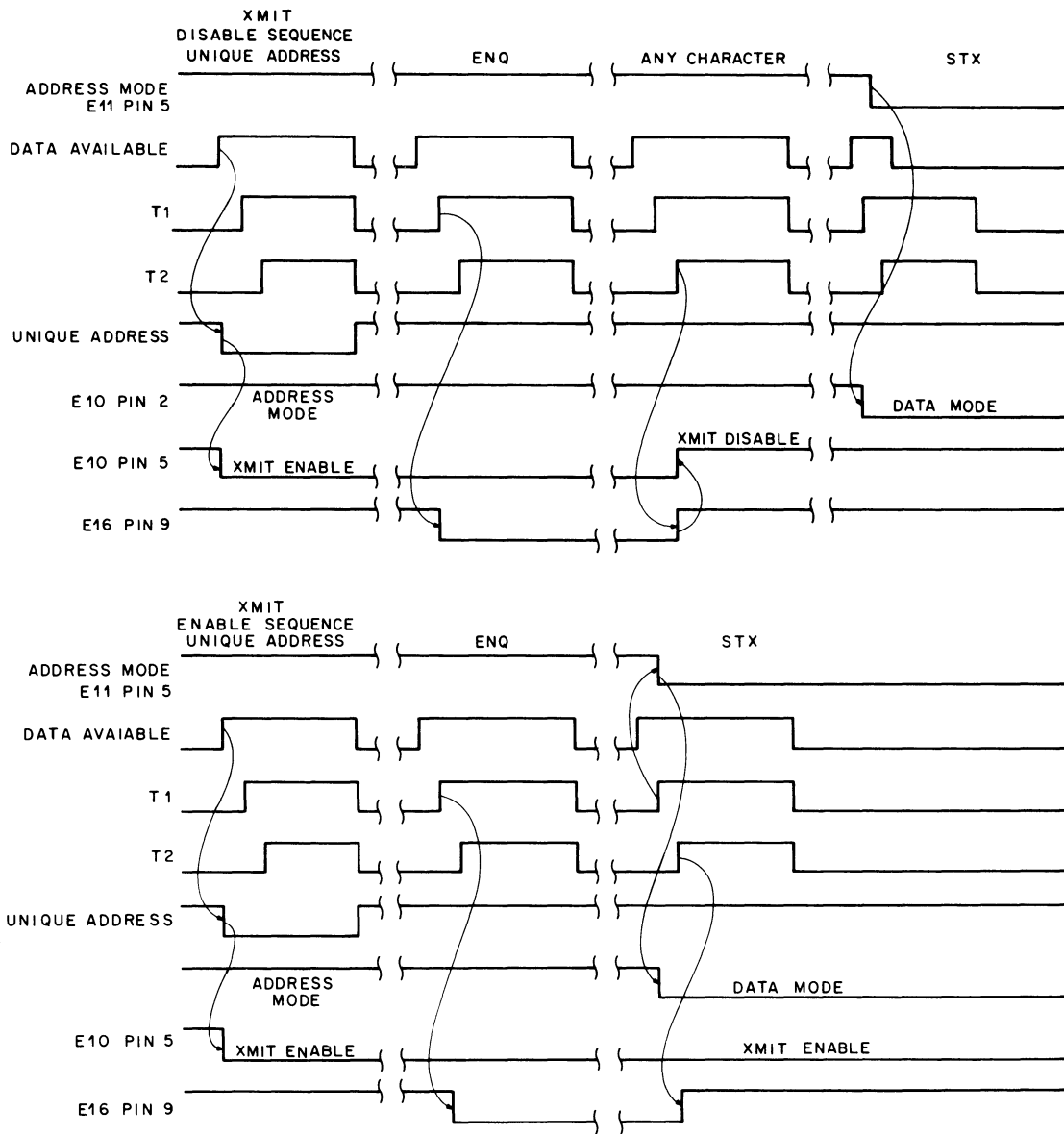
Refer to the *LA35/LA36 DECwriter II User's Manual* for complete programming instructions for terminals containing the Selective Addressing Option.

12.4 TROUBLESHOOTING

The troubleshooting chart in Table 12-1 lists the common trouble symptoms that could be observed during installation checkout or normal operation.

12.5 LAXX-KW PRINT SET

The figures at the end of this chapter are the LAXX-KW print set.



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Figure 12-3 Timing Diagram for Transmit Enable and Disable Sequence

Table 12-1
Troubleshooting for Selective Addressing Option (LAXX-KW)

Symptom	Problem Area	Probable Cause	Action	Reference
1. After installation, incorrect operation or on operation—SELECT AVAIL light not illuminated at power-up	Cabling	Wrong cabling connection	Check all cabling between M7728 Logic Board and Expander Board	Figure 9-4
	Option location	Option inserted in wrong location on Expander Board	Install Selective Addressing Option in location F	
	Data Available signal distribution	Signal path interrupted	Check E8 pin 5 for incoming Data Available signal and E13 pin 12 for output to next option	D-CS-M7737-0-1, Sheet 1
2. Does not respond to any address	Address mode	Not switching to address mode	Check E11 pin 5 for a high level at EOT, NULL, or ETX	D-CS-M7737-0-1, Sheet 1
3. Responds to Group Address when Unique Address sent – or vice versa	Address switches	Addresses are in wrong locations	Interchange addresses between switches S1 should have Unique Address and S2 should have Group Address	D-CS-M7737-0-1, Sheet 2
4. Will not switch out of address mode to data mode	Address flip-flop	Not being reset	Check E11 pin 5 for a low level at STX	D-CS-M7737-0-1, Sheet 1
5. Data is printed when not selected	Tri-State Buffer on Logic Board not disabled	UART ENA H signal from option not sent to Logic Board	Check E8 pin 12 for the UART ENA H signal when selected	D-CS-M7737-0-1, Sheet 1
	ACK Generator	ACK Code Generator not energized	Check E7 for ACK code	D-CS-M7737-0-1, Sheet 1

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NOTES:

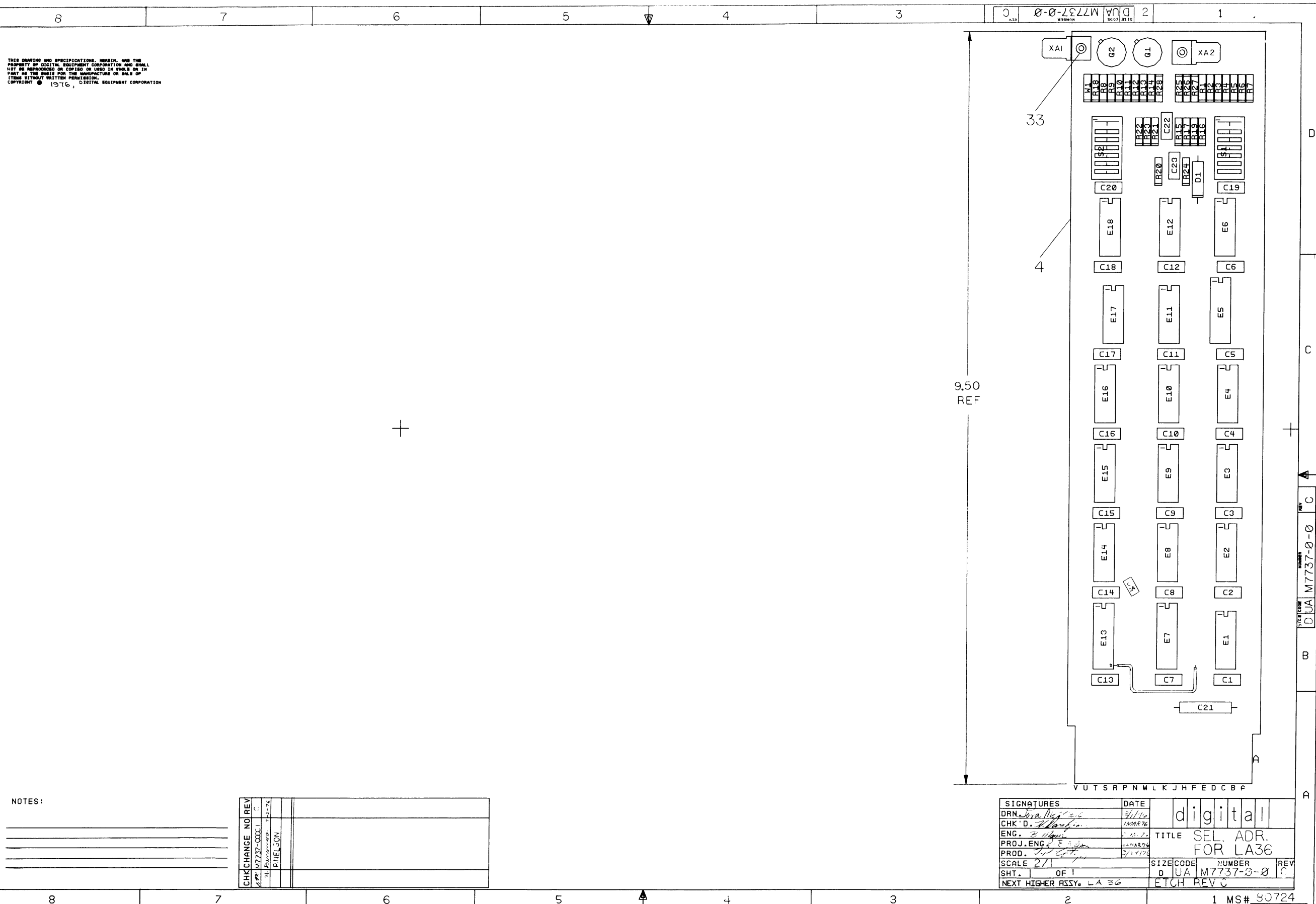
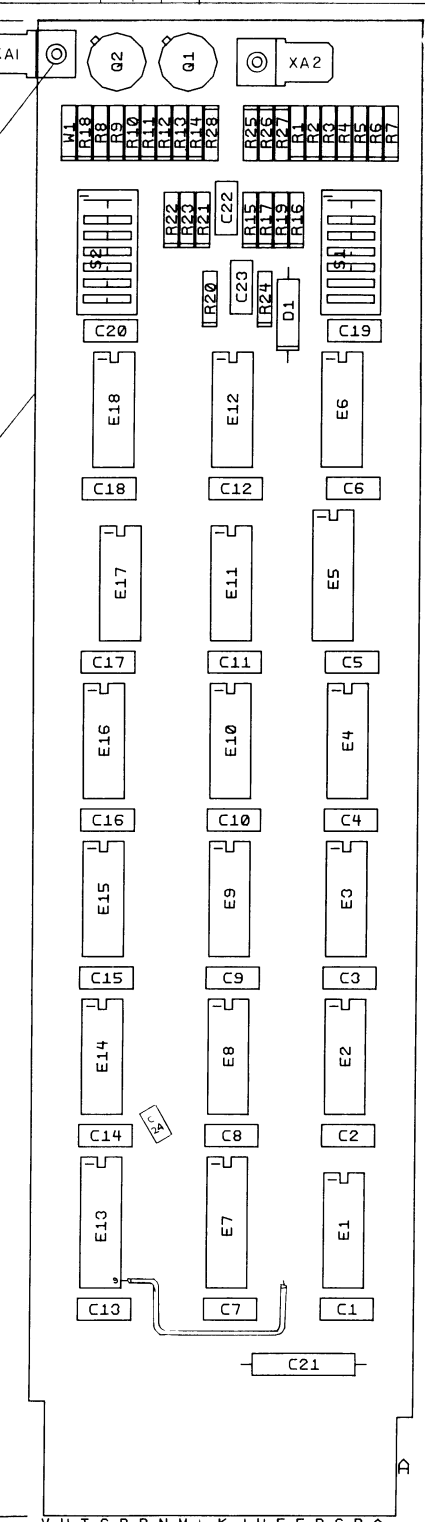
CHKCHANGE NO	REV	DATE	BY
1			
2			
3			
4			
5			
6			
7			
8			

SIZE CODE D UA M7737-0-0

SIGNATURES	DATE	TITLE	SEL. ADR.
DRN. <i>[Signature]</i>	3/1/76	digital	
CHK'D. <i>[Signature]</i>	10 MAR 76		
ENG. <i>[Signature]</i>	2 11 76		
PROJ. ENG. <i>[Signature]</i>	24 MAR 76		
PROD. <i>[Signature]</i>	3/2/76		
SCALE 2/1		SIZE CODE	NUMBER
SHT. 1 OF 1		D UA	M7737-0-0
NEXT HIGHER ASSY. LA 36		ETCH REV C	

1 MS# 93724

9.50 REF



CHAPTER 13

AUTOMATIC ANSWERBACK OPTION (LAXX-KX)

13.1 AUTOMATIC ANSWERBACK INTRODUCTION

The Automatic Answerback Option performs two distinct functions: the storage of a 20-character pre-programmed message and the insertion of line feed codes as in the Automatic Line Feed Option LAXX-LA.

The answerback message has up to 20 character positions (spaces are counted as characters) that can be programmed by utilizing slide switches located on the option circuit board. The message is activated by depressing the front panel HERE IS key or by receiving the ENQ code (005₈). When the terminal is on-line, the answerback message is transmitted down the line. When in local, the message is printed out at the terminal.

NOTE

When operating on-line in the echo mode, the answerback message is also printed out at the terminal in addition to being transmitted.

The Line Feed Section of the option can be configured to automatically insert a line feed code after each transmitted carriage return and insert a line feed code after each received carriage return code. The Option Board contains jumpers that can be removed to inhibit both or either of the insertion functions. The normal action of the AUTO LF switch can also be overridden by these jumpers.

The Answerback Section of the option interacts with two other DECwriter options (EIA Interface, LAXX-LG or Selective Addressing, LAXX-KW) if they are installed. The trilevel line (KSTRB DIS L signal) interconnects these options and establishes whether the Answerback Section can respond to a command requesting the answerback message. The EIA interface can inhibit the Answerback Option when the modem is not ready to accept transmitted data. The Selective Addressing Option can, if the terminal is not selected as the master or a transmit-enabled slave, also inhibit the Answerback Section from responding to received codes. Refer to the EIA description for a complete discussion of this interaction.

NOTE

When operating in the local mode, these options have no effect on the operation of the Answerback Option.

13.2 ANSWERBACK OPTION FUNCTIONAL BLOCK DIAGRAM

Figure 13-1 shows the Answerback Option in a typical DECwriter installation. The option's circuit board installs in locations C and D on the Expander Option Mounting Board and has an edge connector at each location to couple signals between the two boards. A variation in the basic coupling configuration between the M7728 Logic Board and the Expander Board is required when the Answerback or Auto Line Feed Options are installed. Normally, without either of these options, ASCII data from the keyboard is routed right across the Expander Board (in from the keyboard on J3 and out to the Logic Board on J29). When the Answerback Option is installed, the keyboard data path is now through this option and out to the Logic Board on J1.

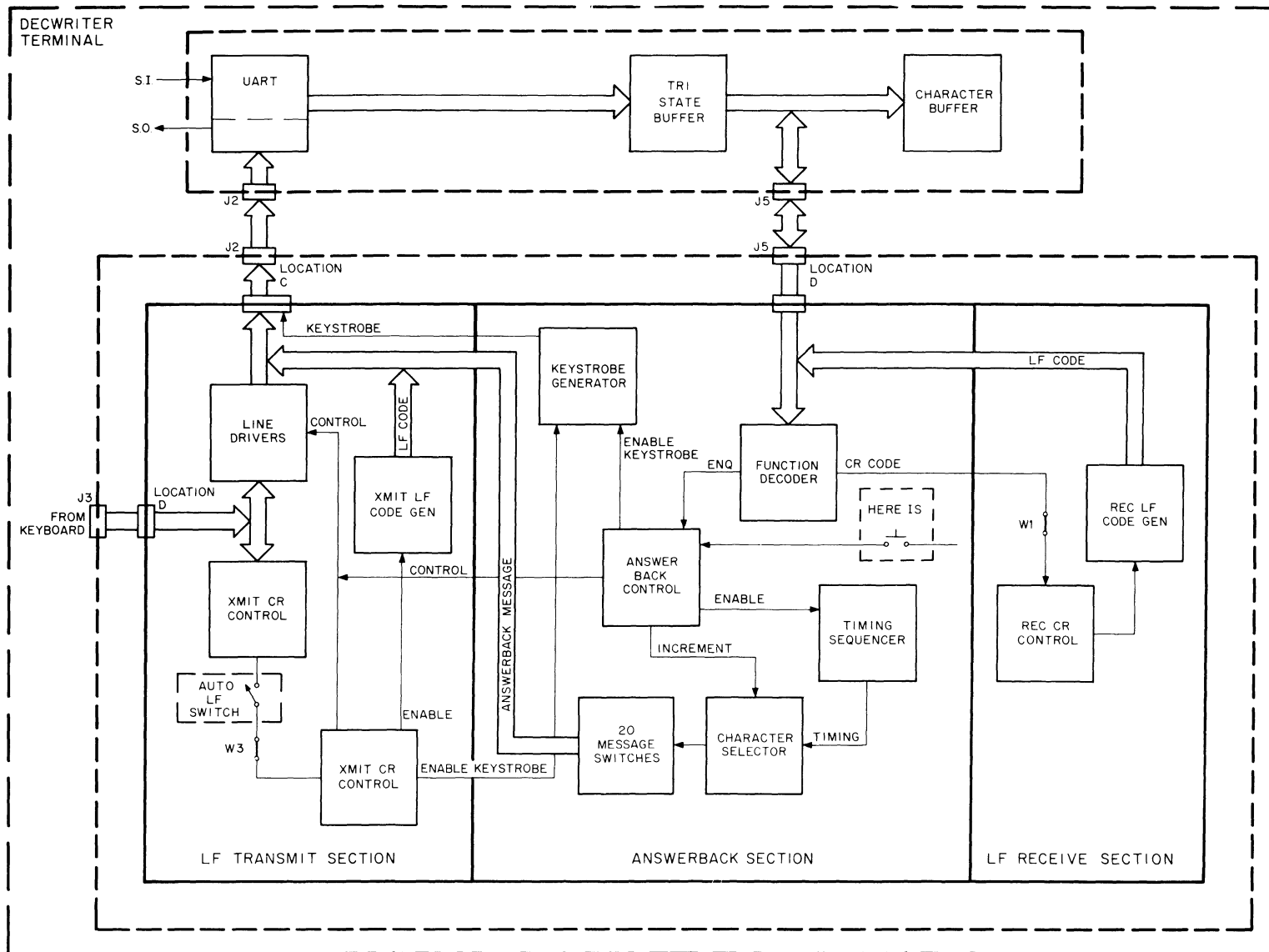


Figure 13-1 Automatic Answerback Option Functional Block Diagram

As shown in Figure 13-1, the Answerback Option is divided into the three following functional sections:

1. LF Transmit Section
2. LF Receive Section
3. Answerback Section

13.2.1 Operation of LF Transmit Section

ASCII data from the keyboard is applied to both the Line Drivers and the Xmit CR Decoder through location D. Normally this data is routed right through the option to the UART. Two conditions cause the Line Drivers to block this data path.

1. When the LF Transmit Section is issuing a line feed code.
2. When the Answerback Section is issuing the answerback message.

If a carriage return code from the keyboard is detected and the front panel AUTO LF switch is depressed and Jumper W3 is installed, the Xmit CR Control initiates the following three actions:

1. Disables the Line Drivers blocking the data path from the keyboard to the UART.
2. Enables the Xmit LF Code Generator placing an LF code on the lines to the UART.
3. When clear to send from EIA is high, generates the keystrobe that transfers the LF code to the UART.

After the LF code is accepted by the microprocessor, the Xmit LF Code Generator is disabled and the Line Drivers are enabled, allowing normal data flow from the keyboard.

As shown in Figure 13-1, Jumper W3 is in series with the AUTO LF switch. If this jumper is removed, all control is removed from the switch and the LF Transmit Section of the option is disabled.

Figure 13-2 contains the operational sequence for the LF Transmit Section.

13.2.2 Operation of LF Receive Section

The LF Receive Section of the option monitors the data out of the UART and, if Jumper W1 is installed, automatically inserts a line feed code after each received carriage return code. When the Function Decoder detects a carriage return code out of the UART, the Rcvr CR Control initiates the following three functions:

1. After the carriage return code is processed, disables the UART.
2. Enables the Rcvr LF Code Generator, placing an LF code on the bidirectional lines to the Character Buffer.
3. Issues an option-generated Data Available signal out on OP IN line. (Refer to Expander Board description for discussion of Data Available signal steering.)

After the LF code is processed by the microprocessor, the UART is enabled and the LF Code Generator is disabled.

Removing Jumper W1 disables the LF Receive Section of the option.

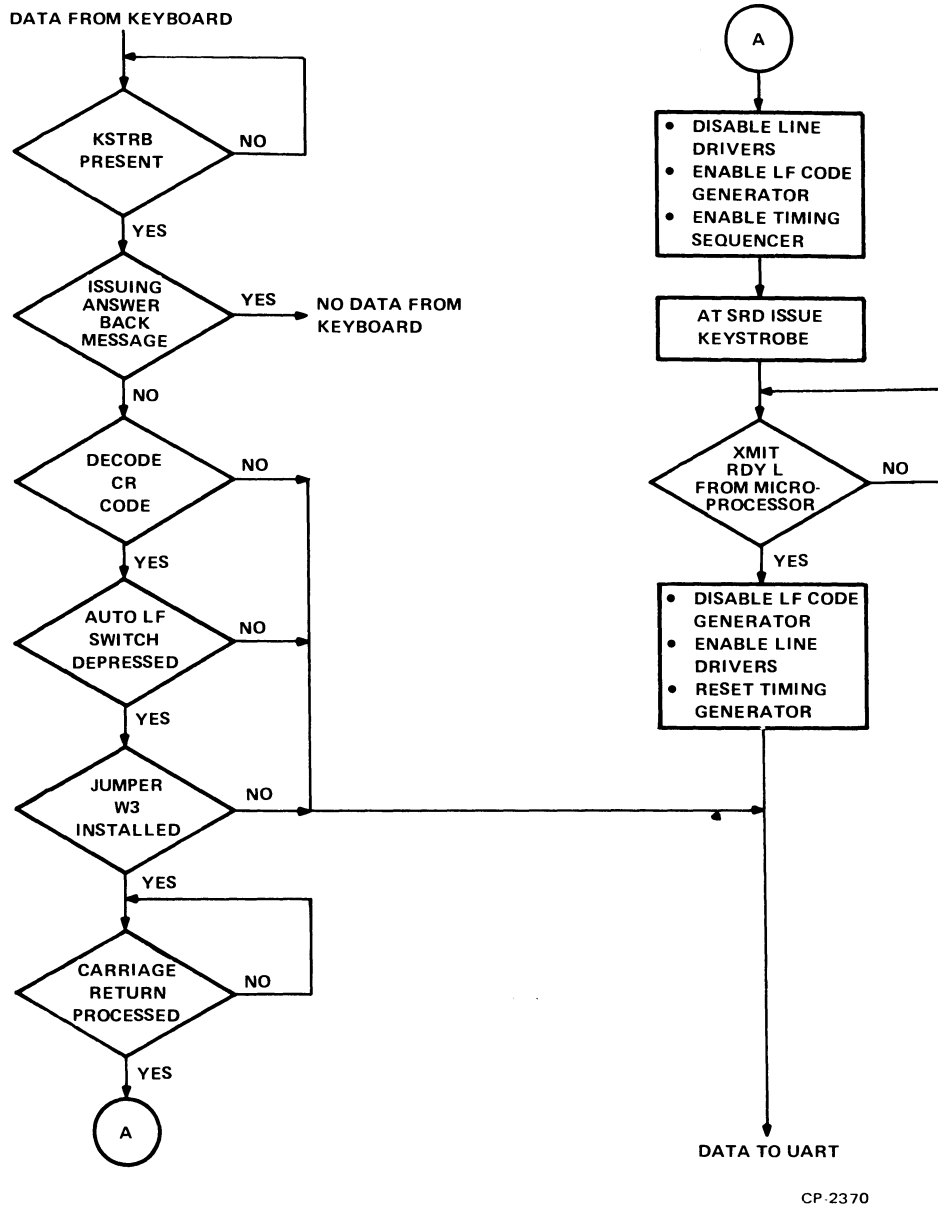


Figure 13-2 Operational Sequence for LF Transmit Section

If the terminal is operated in the local mode, with the front panel AUTO LF switch depressed and Jumpers W1 and W3 inserted on the option circuit board, a carriage return code from the keyboard causes a carriage return and two line feed increments at the printer mechanism. This action occurs because the LF Transmit Section of the option adds a line feed code after the carriage return from the keyboard, then the LF Receive Section of the option inserts another line feed code as the carriage return code leaves the UART for the Character Buffer. Thus, two line feed codes are acted on by the printer mechanism.

NOTE

When the terminal is on-line, transmitting in an echo mode, and the AUTO LF switch is in the down position, the option generates a line feed code after each carriage return. In this operational configuration, the printer mechanism advances two lines for each carriage return even though only one line feed code is being transmitted out from the terminal. The second line feed occurring at the terminal is generated by the returning (echoing) carriage return as it is processed by the LF Receive Section of the option. This same action occurs when the terminal is operated in the local mode.

Figure 13-3 contains the operational sequence for the LF Receive Section.

13.2.3 Operation of Answerback Section

The Answerback Section utilizes the Function Decoder to detect received requests (ENQ code) for the stored answerback message. In the local mode, depressing the HERE IS key activates this section and causes the message to be printed out at the terminal. The AB Control initiates the following sequence when commanded to output the answerback message:

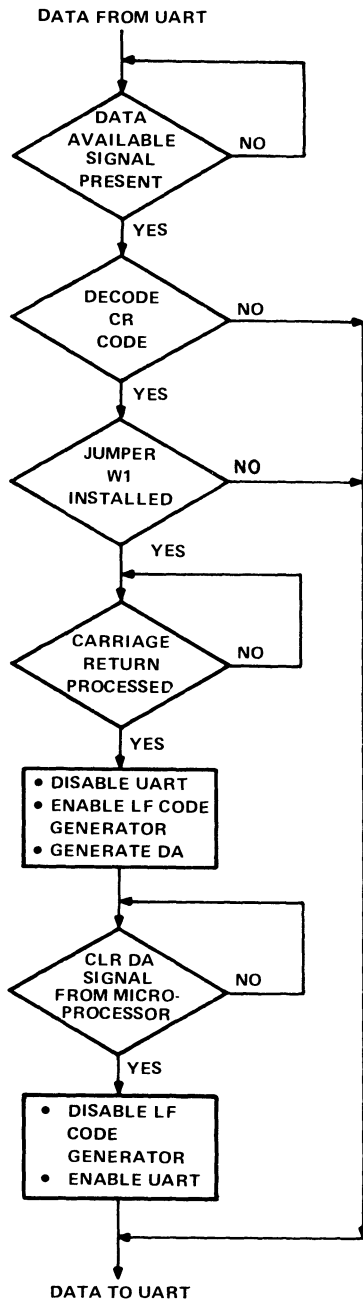
1. Disable the Line Drivers blocking all keyboard data.
2. Increment the Character Selector by one (from zero to first character in message).
3. Enable the Timing Sequencer.
4. Monitor for last character in message.
5. Produce option-generated keystroke to transfer answerback character to UART.

NOTE

As can be seen in Figure 13-1, the answerback message is applied to the UART just as if it were typed on the keyboard. The message is NOT applied on the bidirectional lines to the Character Buffer as in the case of other options.

After the microprocessor has accepted the first character, the next character and its keystroke are ready to be processed in the same manner. This action continues until the last character of the answerback message is transferred out. At this time the Line Drivers are enabled again and normal terminal action is resumed.

Figure 13-4 contains the operational sequence for the Answerback Section.



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Figure 13-3 Operational Sequence for LF Receive Section

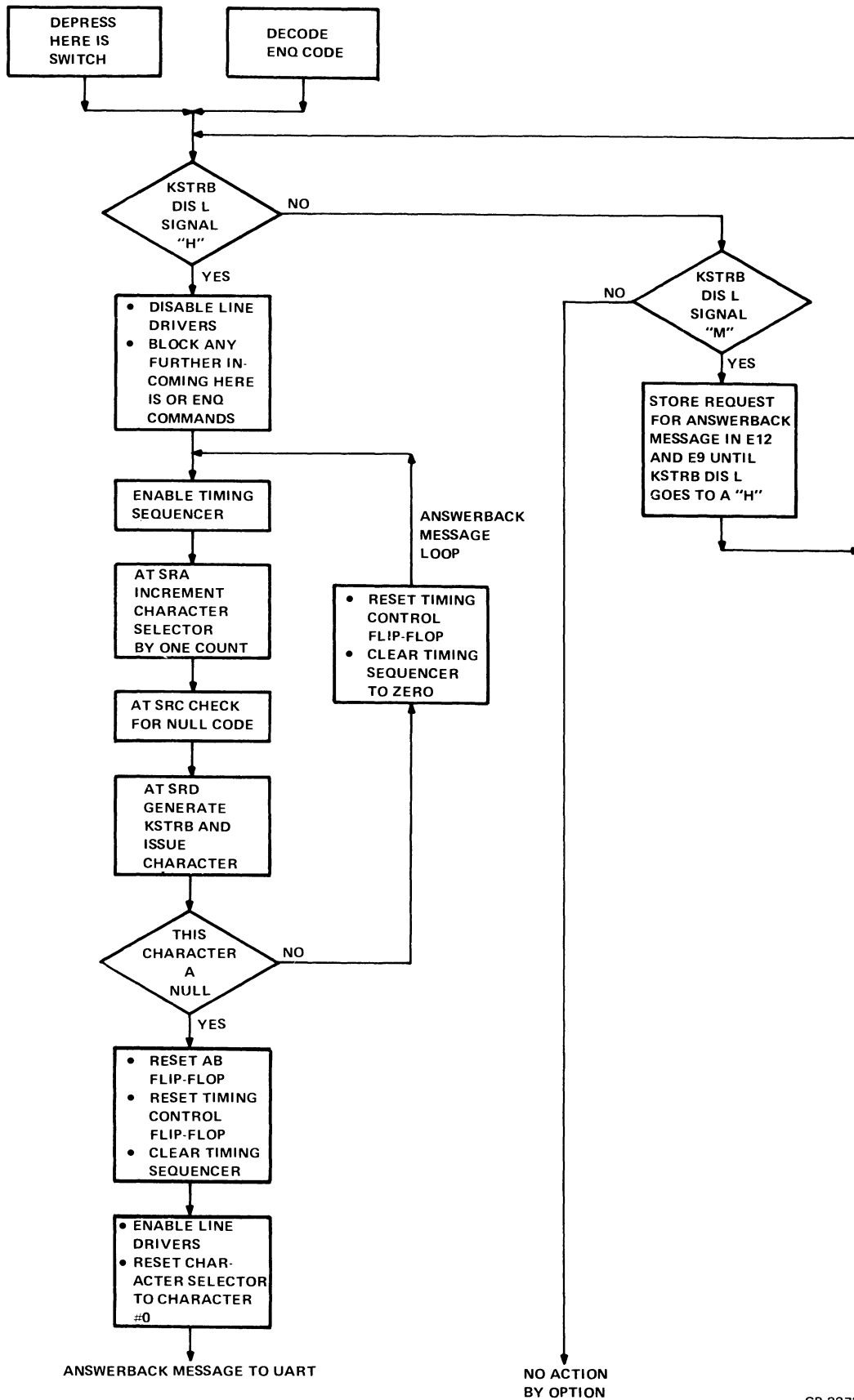


Figure 13-4 Operational Sequence for Answerback Section

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13.3 AUTOMATIC ANSWERBACK BASIC BLOCK DIAGRAM

The basic block diagrams for the Automatic Answerback Option are shown in Figures 13-5 and 13-8. These diagrams are simplified representations of the automatic answerback circuit schematic (D-CS-M7733-0-1). Circuit designations and pin numbers indicated on these figures correlate with corresponding components on the schematic. Buffers, inverters, and other components that do not have major operational functions are omitted from the block diagrams.

The Answerback Option is divided into three areas:

1. LF Transmit Section
2. LF Receive Section
3. Answerback Section

13.3.1 LF Transmit Section Basic Block Diagram

The basic block diagram for the LF Transmit Section is shown in the top half of Figure 13-5. Normally, ASCII data from the keyboard passes through the Line Drivers E17, E23 to the UART. If the Answerback Section is *not* generating the answerback message, the keystroke for each character from the keyboard passes through E15 to the microprocessor. When a carriage return is typed, the keystroke associated with the carriage return is utilized by the Xmit CR Decoder E22 to detect the CR code. If the AUTO LF switch is depressed and Jumper W3 is installed, the carriage return indication passes through functional AND gate E3 and sets Xmit No. 1 flip-flop E24. After the carriage return is processed and the UART is ready to accept the next character, the XMIT RDY L signal is applied to pin 5 of Inverter E21. This inverted signal clocks the Xmit No. 2 flip-flop E24, producing the LF ON H and LF ON L signals.

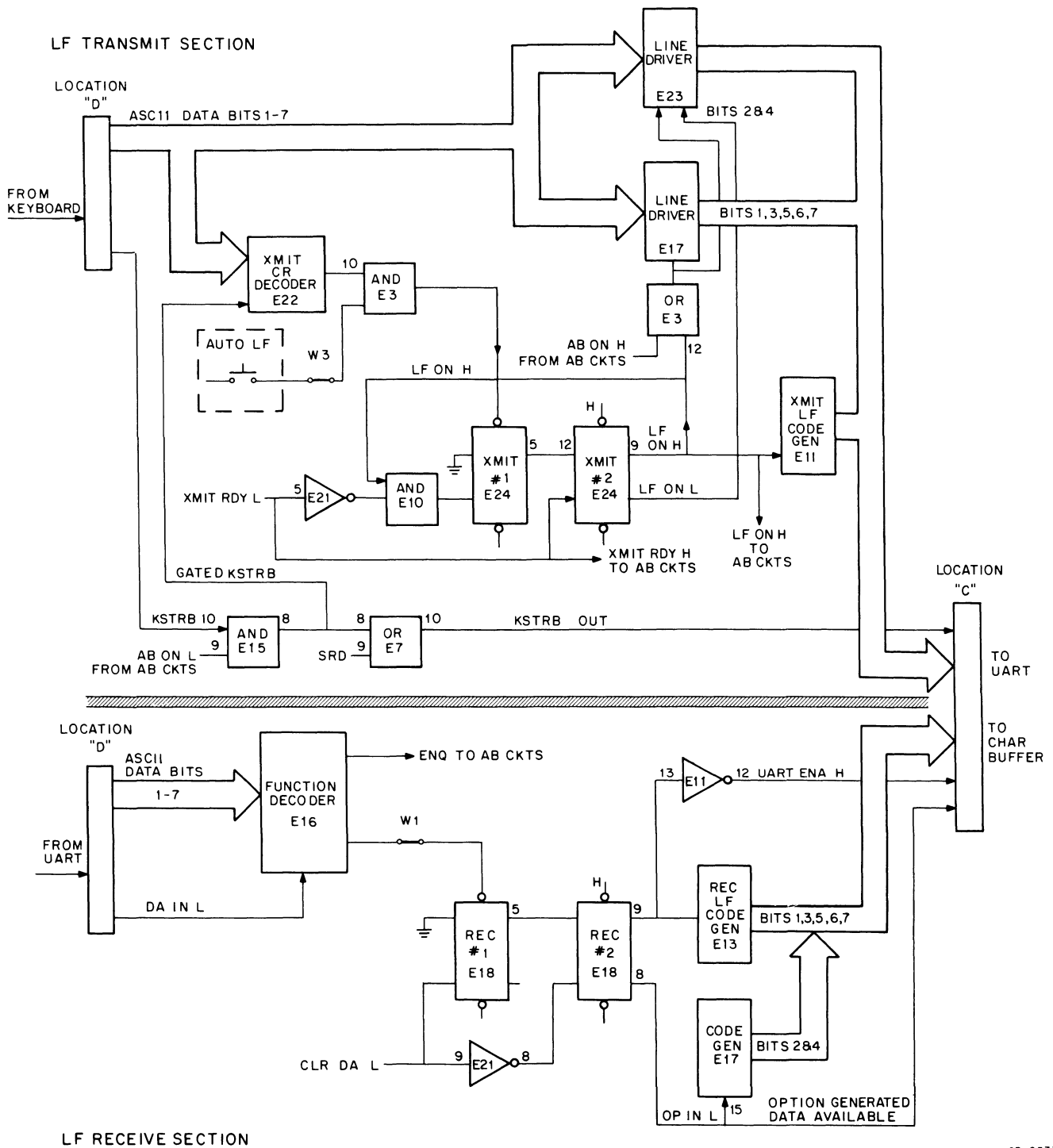
The LF ON H signal performs the following four actions:

1. Disables the Line Drivers through E3 blocking any further data from the keyboard.
2. Enables the Xmit LF Code Generator E11, producing the zero bits of the line feed code (bits 1, 3, 5, 6, 7).
3. Clocks Timing Controller E9 in the Answerback Section starting the Timing Sequencer E2.
4. Conditions NAND gate E10 at pin 9 so that after the LF code is accepted by the microprocessor, the returning XMIT RDY L signal can clock and clear both sections of E24.

The LF ON L signal from E24 pin 8 is applied to pin 15 of Line Driver E23 and produces the two 1-level bits of the LF code (bits 2 and 4).

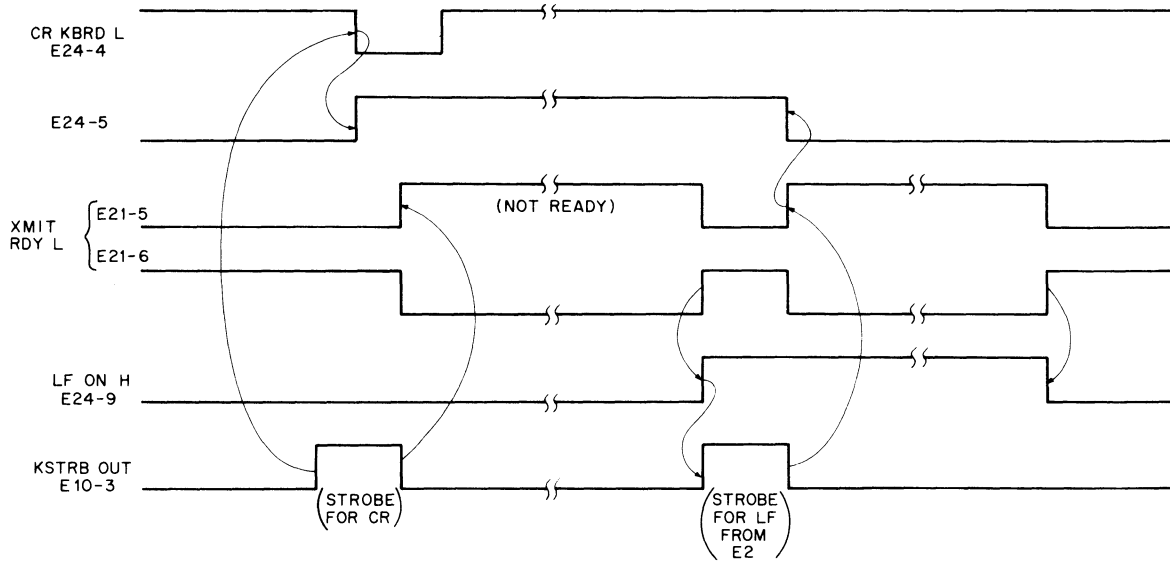
At SRD time, the KSTRB OUT signal is generated at E7 pin 10. After the UART accepts the LF code, the leading edge of the returning XMIT RDY L signal clocks a low through E24 to pin 5 and the trailing edge clocks this low through Xmit No. 2 flip-flop to enable the Line Drivers, disable the LF Code Generator, and allow keyboard data to pass through the option again. The XMIT RDY H signal clears Timing Sequencer E2 and resets Timing Controller E9.

The timing sequence for the LF Section is shown in Figure 13-6.



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Figure 13-5 LF Sections of Answerback Option



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Figure 13-6 LF Transmit Section Timing Sequence

13.3.2 LF Receive Section Basic Block Diagram

The basic block diagram for the LF Receive Section is shown in the bottom half of Figure 13-5. This section monitors the received data at a point that is between the output of the UART and the input to the Character Buffer. This data is present at the option on the bidirectional line through the edge connector at location D. Receiving both a carriage return code and the DA IN L signal (data available signal from the UART) at the Function Decoder E16 produces the CR UART L signal that is coupled through Jumper W1 to set Rec No. 1 flip-flop E18.

After the carriage return code is processed by the terminal, the microprocessor sends the CLR DA L signal back to the option at Inverter E21-9. The leading edge of this signal clocks the high level on E18-12 through to E18-9 and forces E18-8 to a low level. The trailing edge of CLR DA resets E18 at pin 3. The high through pin 13 of E11 produces the signal UART ENA H which disables the UART. This high level also generates the zero bits of the LF code (bits 1, 3, 5, 6, 7) through E13. The 1 level bits of the LF code are generated by the OP IN L signal which is applied to E17 pin 15. The option-generated data available signal is represented by the low level of the OPT IN L signal. (The steering gates on the Expander Option Mounting Board convert this OPT IN L signal to a signal that has the same effect as the Option Data Available signal.) After the microprocessor accepts the option-generated line feed code and data available, it sends a second CLR DA L signal back to the option. This resets flip-flop E18 at pin 11 which then allows the UART to pass received data to the Character Buffer in a normal manner.

The Timing Sequencer for the LF Receive Section is shown in Figure 13-7.

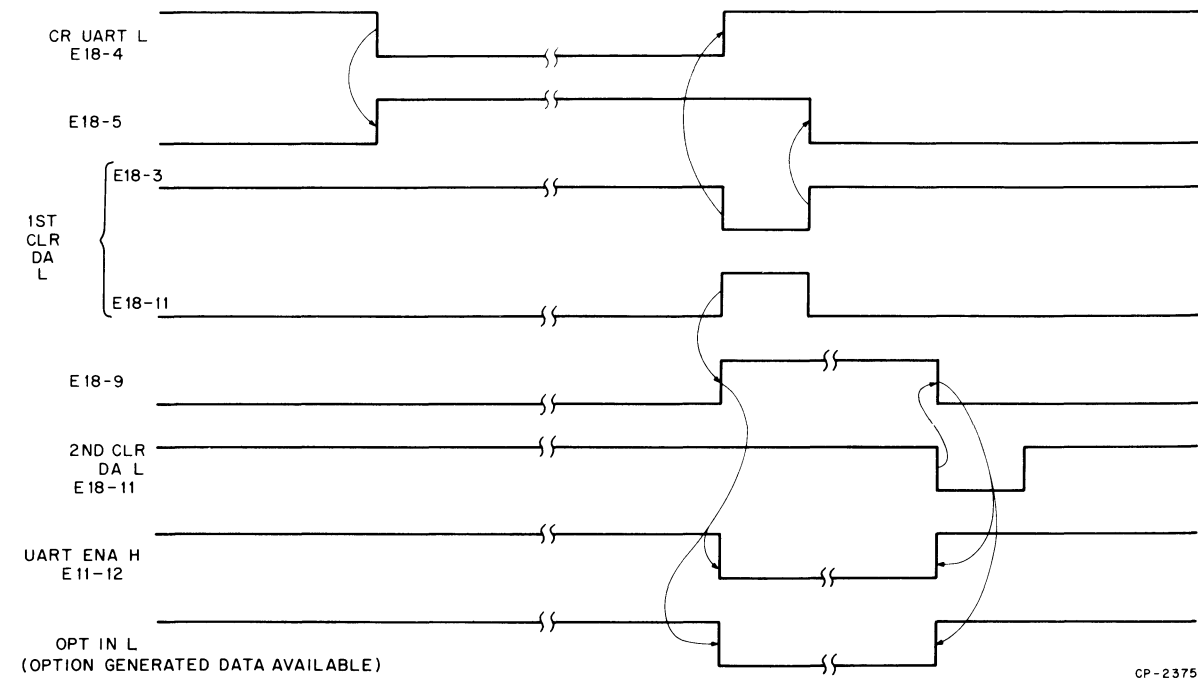


Figure 13-7 LF Receive Section Timing Sequence

13.3.3 Answerback Section Basic Block Diagram

Figure 13-8 contains the basic block diagram for the Answerback Section. When the HERE IS key is depressed or the ENQ command is received, either of these two indications is coupled out of E14 pin 8 to AND gate E10. If the KSTRB DISABLE L signal level is either an H or M level and AB ON H is not set, E10 is qualified and both sections of flip-flop E12 set. The high level produced on pin 5 of E12 (AB ON H signal) initiates the following three events:

1. Disables Line Drivers E17, E23 through E3.
2. Blocks any other incoming requests for the answerback message by placing a low on E10 pin 5 through E7.
3. Conditions E14 pin 4 with a high level so that when the last character in the answerback message is detected E13 can reset.

The low level on pin 6 of E12 (AB ON L) initiates the following events:

1. Disables the keyboard by blocking the KSTRB IN H signal path through E15.
2. Enables the Character Drives E1, E8 which send the answerback message to the UART through location C.

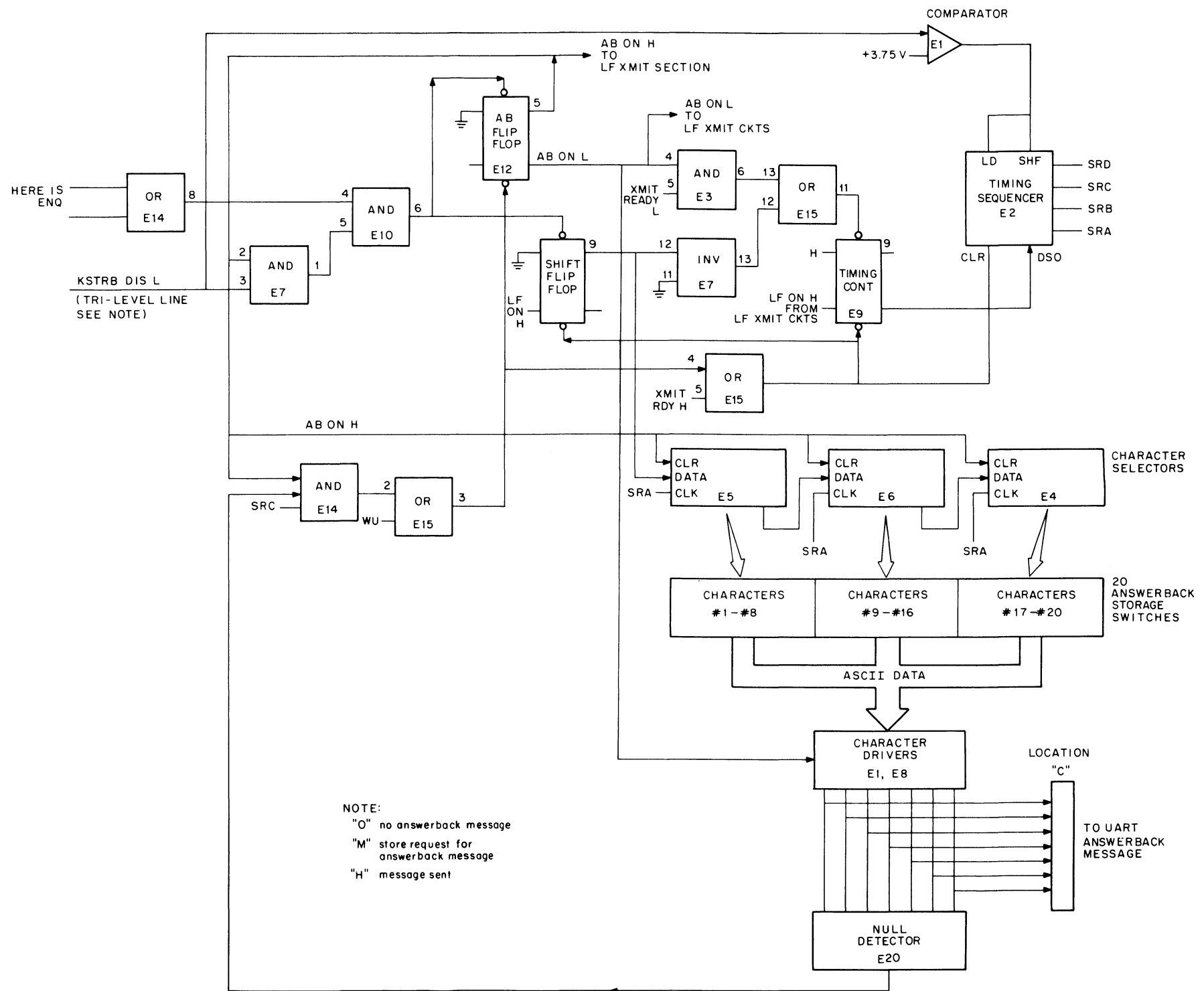


Figure 13-8 Answerback Section
 Basic Block Diagram

As Shift flip-flop E12 sets, a high level on pin 9 (AB SHIFT 0) is applied to Character Selector E5. E4, E5, and E6 are configured as a shift register that ripples a high level up through each output line every time the register is clocked. The AB SHIFT 0 signal from pin 9 of E12 is inverted by E7 and passed through the functional OR E15 on pin 11 to set E9. When E9 sets, a high level is applied on the DS0 input of E2. The Timing Sequencer E2 is a 4-bit shift register that shifts the high DS0 level to the right at the rate of the Option Clock (approximately 1.2 μ s per shift) when the CLEAR TO SEND signal is applied to the shift and load inputs (pins 13 and 10 respectively). The CLEAR TO SEND signal is only present when the KSTRB DIS L signal is in the H level. When at the M level the KSTRB DIS L signal does not overcome the 3.75 V bias level on Comparator E1 and the CLEAR TO SEND signal is not produced.

NOTE

The M level allows E12 to set and hold a request for the answerback message but the message is not transmitted until the tri-state line becomes an H level.

At SRA time, the Character Selector E5 increments from character no. 0 to character no. 1 and a high level is applied to one side of each of the seven slide switches that comprise character no. 1. A closed switch produces a "1" in the bit position and an open switch a "0." Figure 13-9 shows the switch settings for the letter A in character no. 1. To produce the code 1000001 for the A, the switches in bits 1 and 7 are closed while all the rest are open. The Character Drivers send this code out of location C to the UART. The Null Detector E20 monitors these lines for the null code (0000000) and, when decoded, produces the AB DONE signal which resets E12 and the Timing Sequencer at SRC time. At SRD time, the KSTRB OUT signal is generated at E7 and character no. 1 is sent to the UART. As the UART accepts this character, the XMIT RDY H signal is sent back to the option at E15 pin 5 and initiates three actions:

1. Shift flip-flop E12 resets and removes the high from E5 (E12 remains reset until message is sent).
2. Timing Controller E9 resets and removes the high level from the DS0 input of the Timing Sequencer.
3. Timing Sequencer clears to zero.

After the UART has processed the character, the XMIT RDY L signal is sent to the option where it combines with the AB ON L signal at functional AND gate E3. When E3 is qualified, a low pulse from pin 11 of functional OR E15 sets the Timing Controller E9. As E9 sets, a high level is applied at the DS0 input of the Timing Sequencer. If the CLEAR TO SEND signal is present, the Timing Sequencer starts and at SRA the Character Selector increments a high level to the switch containing the next character and at SRD this character is strobed to the UART.

This character generation continues until the Character Selector increments to the twenty-first character location, which does not exist. Therefore, a null is detected at E20 and at SRC time AND gate E14 couples this last character indication through E15 to reset the AB flip-flop E12, Timing Controller E9, and Timing Sequencer E2. At this time the Answerback Sequence is completed.

NOTE

If an answerback message of less than 20 characters is stored in the switches and the last character is coded as a null, the Answerback Section will reset after detecting this null rather than sequencing through the remaining uncoded switch positions.

Figure 13-10 contains the timing sequence for the Answerback Section.

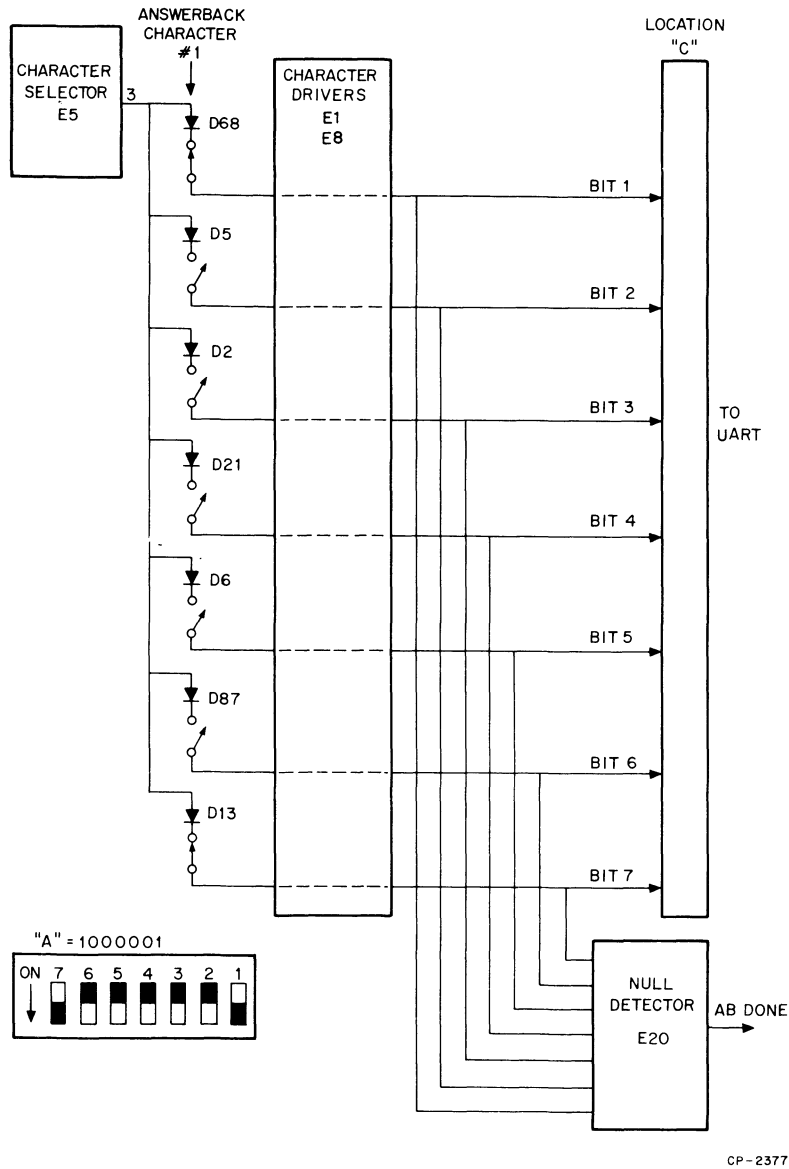


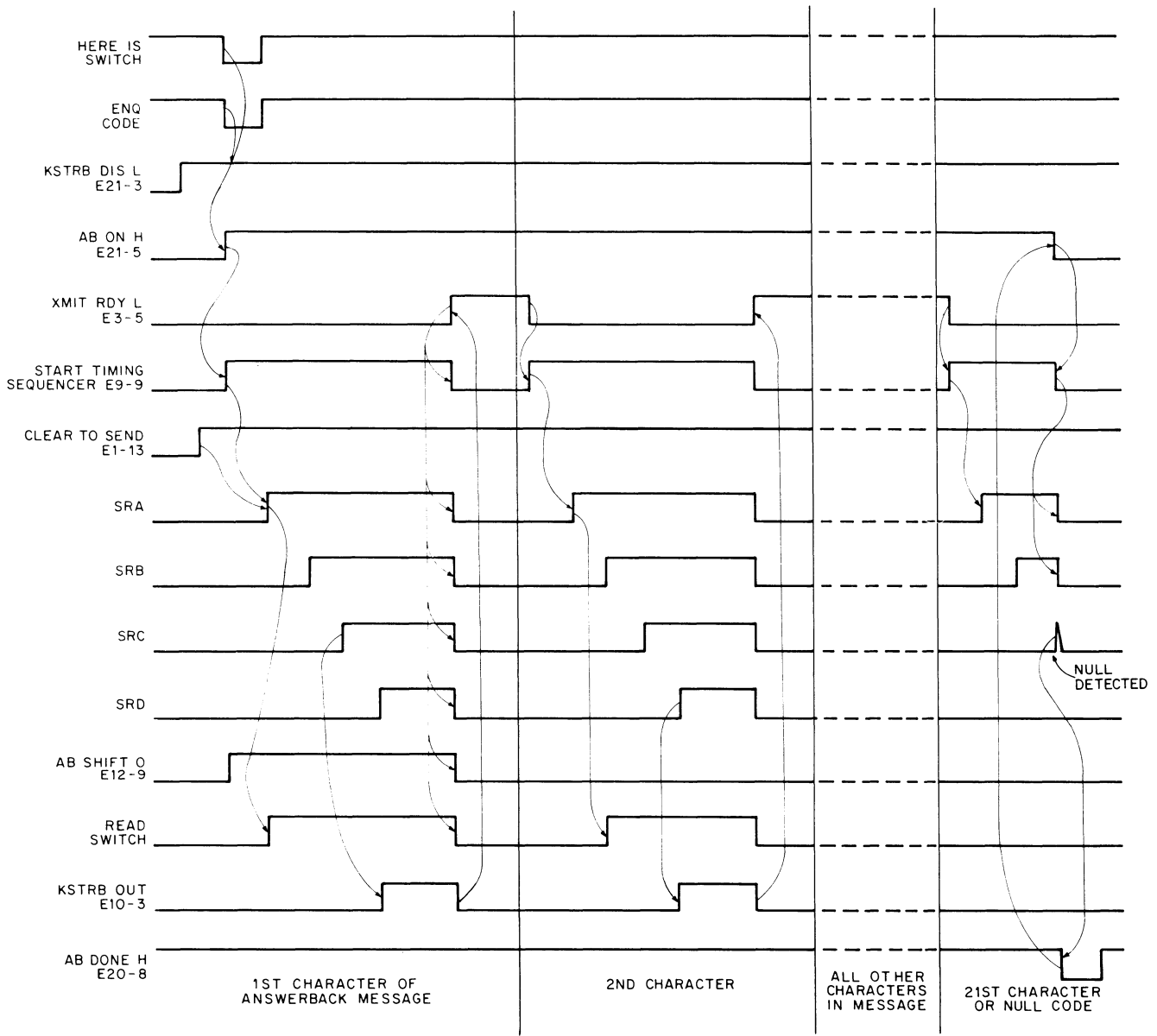
Figure 13-9 Typical Answerback Character Programming

13.4 TROUBLESHOOTING

The troubleshooting chart in Table 13-1 lists the common trouble symptoms that could be observed during installation checkout or normal operation.

13.5 LAXX-KX PRINT SET

The figures at the end of this chapter are the LAXX-KX print set.



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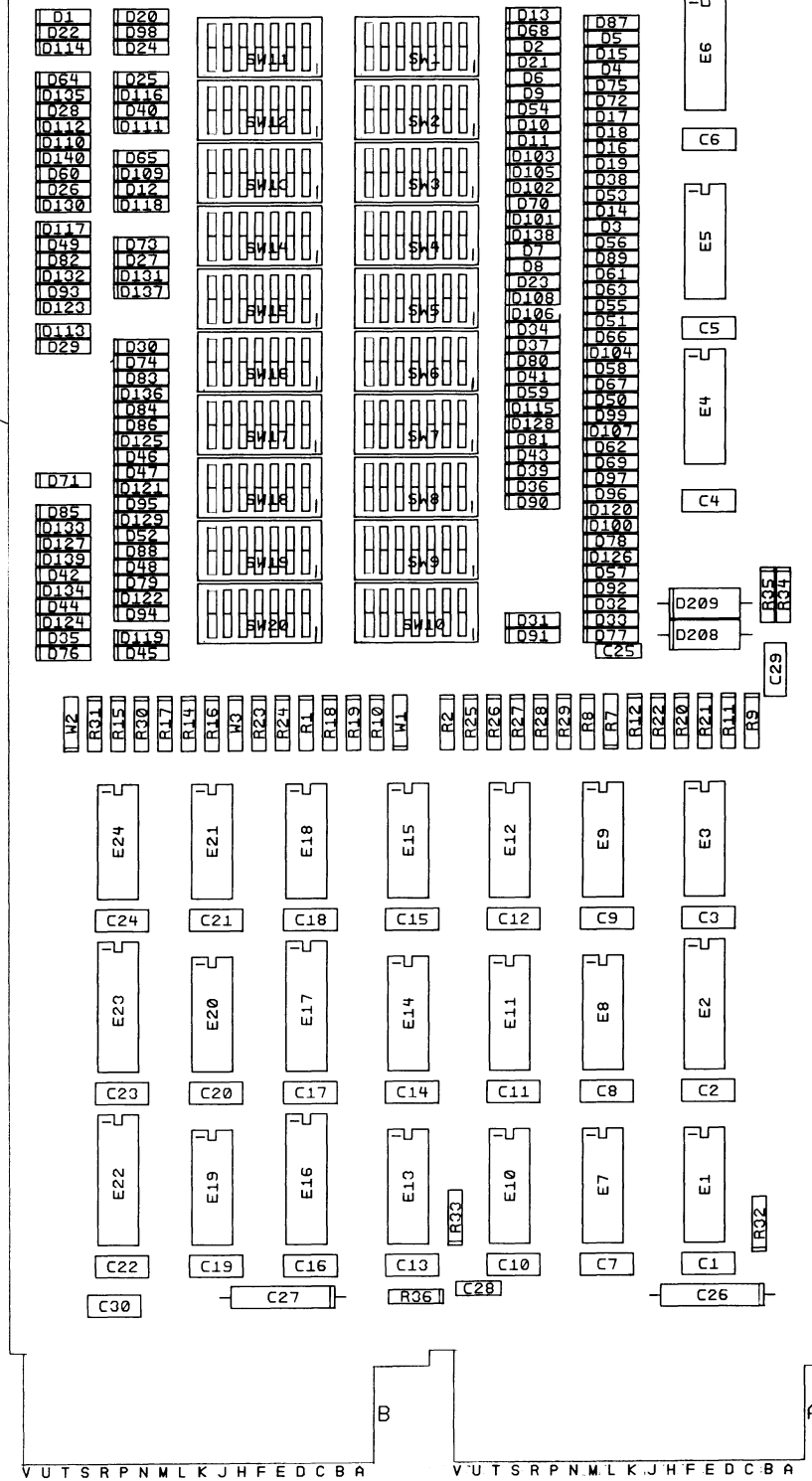
Figure 13-10 Answerback Section Timing Sequence

Table 13-1
Troubleshooting for Automatic Answerback Option (LAXX-KX)

Symptom	Problem Area	Probable Cause	Action	Reference
1. After installation, characters typed on keyboard not transmitted	Cabling	Wrong cabling connections	Check all cabling between M7728 Logic Board and Expander Board	Figure 9-4
	Option location	Option inserted in wrong location on Expander Board	Install Answerback Option in locations C and D	
	Keystrobe signal distribution	Signal path interrupted	Check for Keystrobe signal into Option Board at E15 pin 10 and out of board at E10 pin 3	D-CS-M7733-0-1, Sheet 3
	Line Drivers	Line Drivers on option not enabled	Check E3 pin 11 for low level	D-CS-M7733-0-1, Sheet 1
2. After installation, received characters not printing	Data Available signal distribution	Signal path interrupted	Check for Data Available signal at E16 pin 15	D-CS-M7733-0-1, Sheet 1
	Tri-State Buffer on M7728 Logic Board	Tri-State Buffer held disabled by option	Check E11 pin 12 for high level when option not performing answerback or line feed operation	D-CS-M7733-0-1, Sheet 2
3. Line feed code not inserted after carriage return typed	AUTO LF switch	AUTO LF switch not depressed	Depress switch – if depressed and W3 installed and still no LF code, replace switch	
	Keystrobe signal	Signal not being generated by option	Check E10 pin 3 for keystrobe signal associated with line feed code	D-CS-M7733-0-1, Sheet 3
	Line Feed Code Generator	Line feed code not being generated	Check for line feed code at E11 and E23	D-CS-M7733-0-1, Sheet 1

Table 13-1 (Cont)
Troubleshooting for Automatic Answerback Option (LAXX-KX)

Symptom	Problem Area	Probable Cause	Action	Reference
4. Line Feed Code not inserted after received Carriage Return	Jumper W1	W1 not installed	Connect W1	D-CS-M7733-0-1, Sheet 1
	Data Available signal	Option not generating Data Available signal	Check for pulse at E18 pin 8	D-CS-M7733-0-1, Sheet 2
	Line Feed Code Generator	Line feed code not being generated	Check for line feed code at E13 and E17	D-CS-M7733-0-1, Sheets 1 and 2
5. No message is printed when HERE IS switch is depressed in local or CTRL E is received when on-line and Carriage Return/Line Feed Section does not operate	Option activation	Timing Control flip-flop not setting	Check that E9 sets on either line feed or answerback operation	D-CS-M7733-0-1, Sheet 3
		Timing Sequences not operating	Check E2 for outputs at pins 5, 7, 9, and 12	D-CS-M7733-0-1, Sheet 3
6. Same as no. 5 above except Carriage Return/Line Feed Section operates	Answerback Section	AB flip-flop or Shift flip-flop not operating	Check both sections of E12 to ensure that they set when answerback message activated	D-CS-M7733-0-1, Sheet 3
7. Message prints on received CTRL E but not when HERE IS switch is depressed in local	HERE IS switch	Faulty switch or cabling	Check switch operation and signal path to E14 pin 10	D-CS-M7733-0-1, Sheet 3
8. Depress HERE IS switch – no answerback message – just last character typed prints	Message storage	Shorted diode in one of the 20 character switch positions or any malfunction that shorts any two lines of shift register E4, E5, E6 together	Check for shorts in message array	D-CS-M7733-0-1, Sheets 5, 6, or 7
9. Message starts to print, then stops without finishing	Shift register	Shift register not able to sequence through complete message	Check all 20 outputs of E4, E5, E6	D-CS-M7733-0-1, Sheets 5, 6, or 7



NOTES:

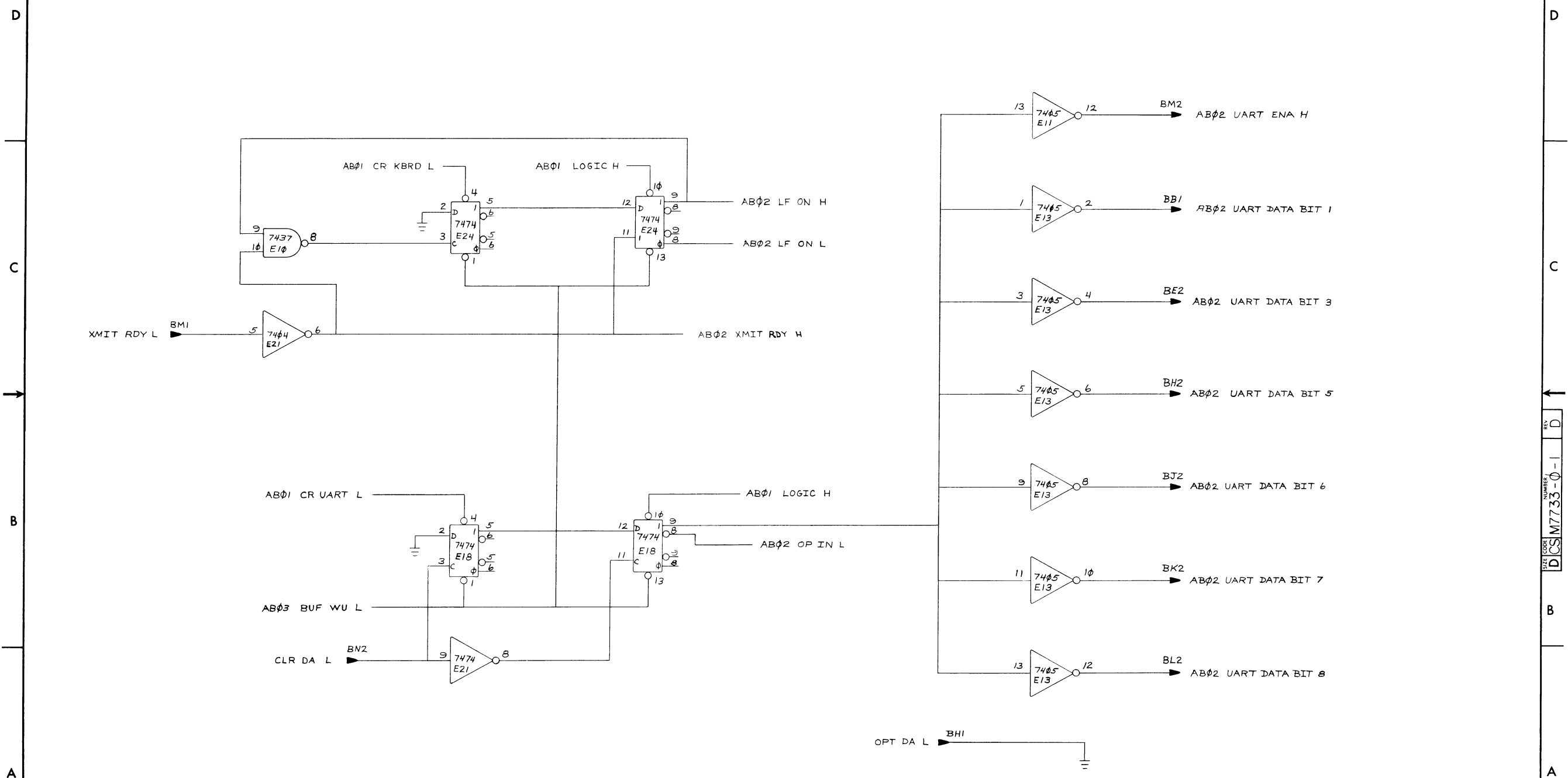
1. DO NOT INSTALL W2
2. NO HANDLES

CHK	CHANGE NO	REV

SIGNATURES	DATE	
DRN. <i>[Signature]</i>	10/31/76	
CHK'D. <i>[Signature]</i>	2/3/77	TITLE ANSWERBACK OPT
ENG. <i>[Signature]</i>	2/9/76	
PROJ. ENG. <i>[Signature]</i>	2/10/76	
PROD. <i>[Signature]</i>	4/10/76	
SCALE 2/1		SIZE CODE NUMBER REV D U A M 7733-0-0 D
SHT. 1 OF 1		
ETCH REV E FIRST USED ON		LA3C

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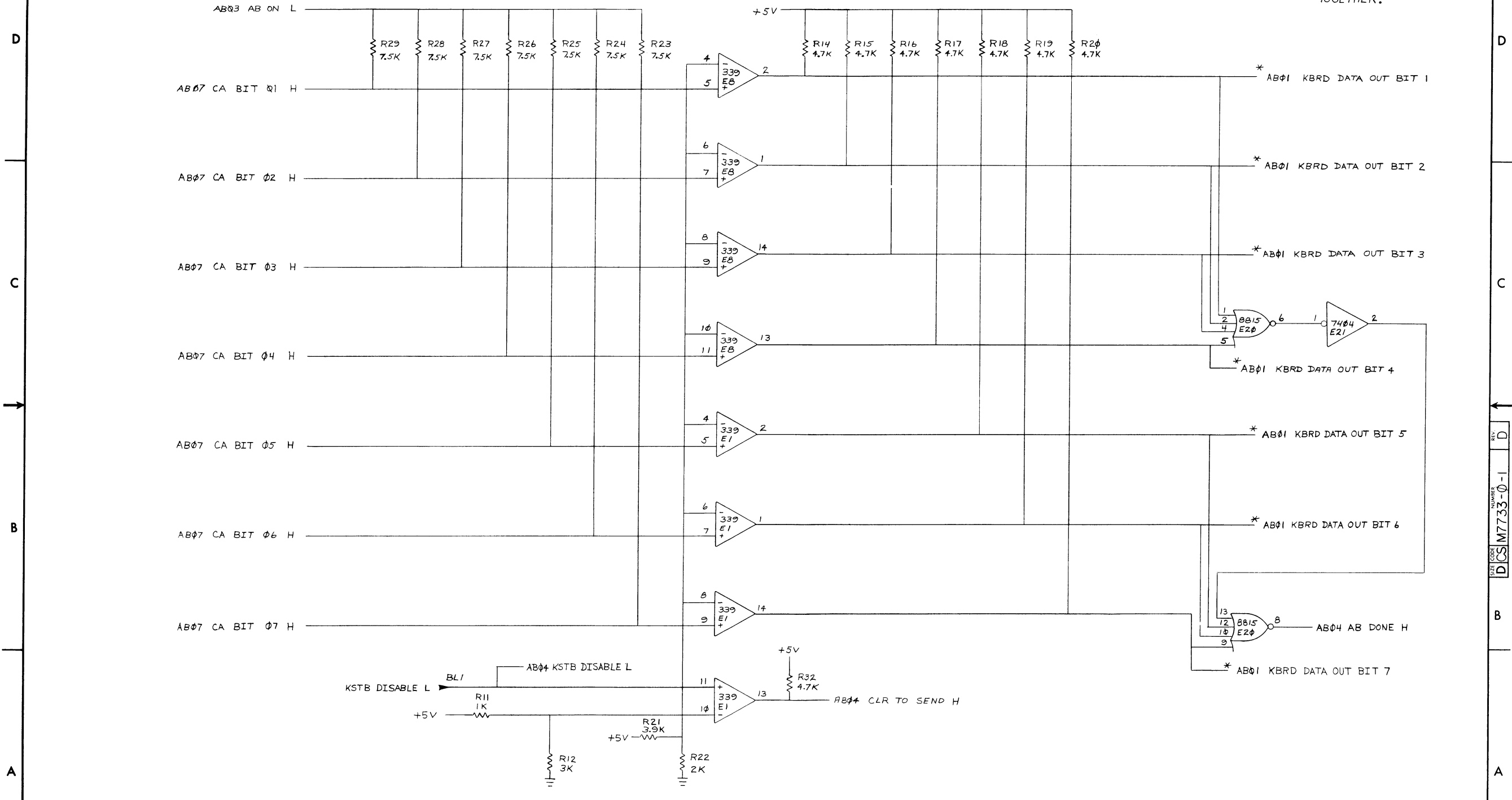
D CS M7733-0-1



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NOTE: SIGNALS MARKED "*" ARE WIRED-ORED TOGETHER.

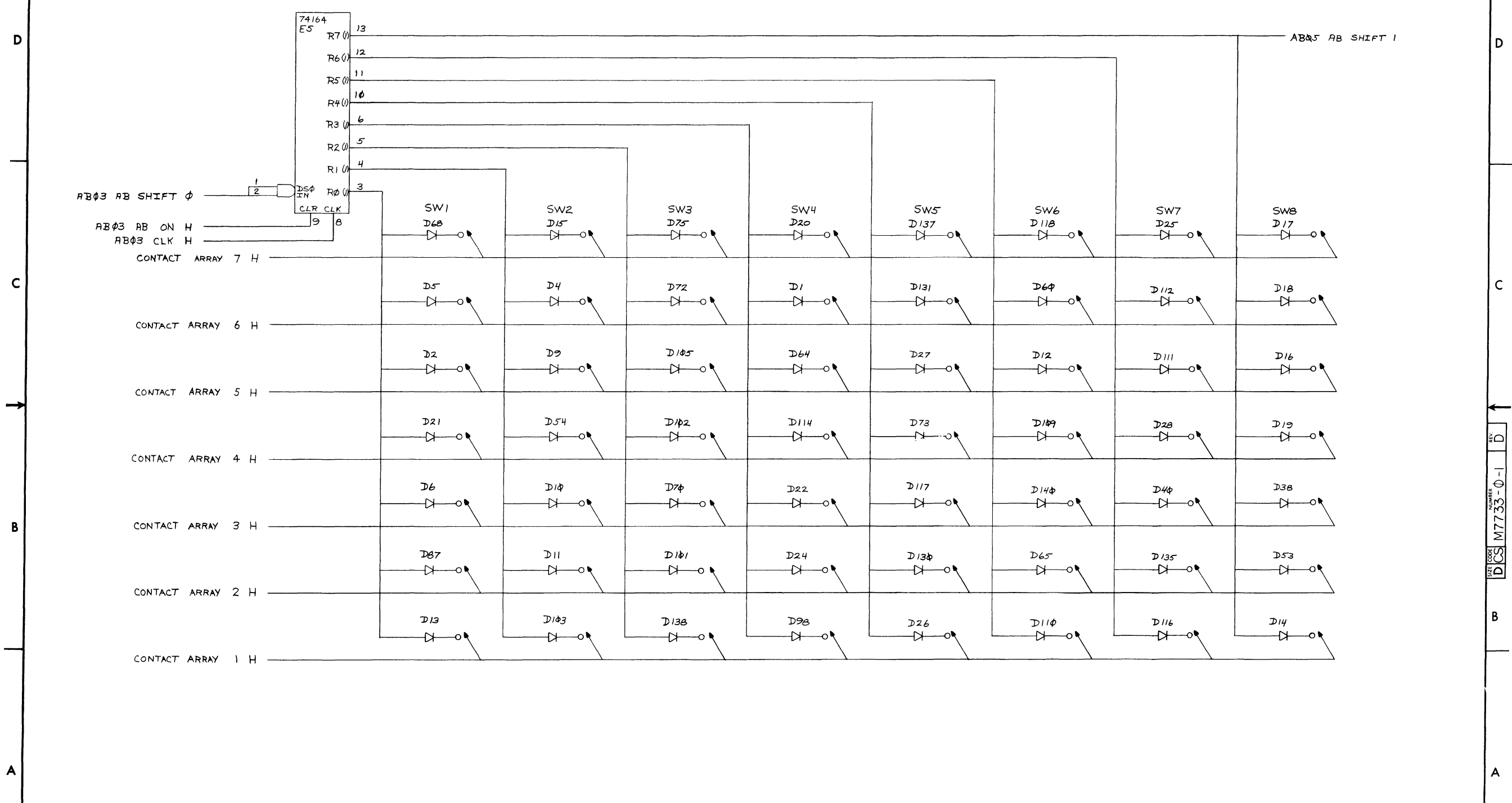


REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	(AB04)	SIZE CODE	NUMBER	REV.
ANSWERBACK OPT		D CS	M7733-0-1	D
SCALE	1/1	SHEET	4 OF 7	DIST.

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REVISIONS		
CHK	CHANGE NO.	REV.

8

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3

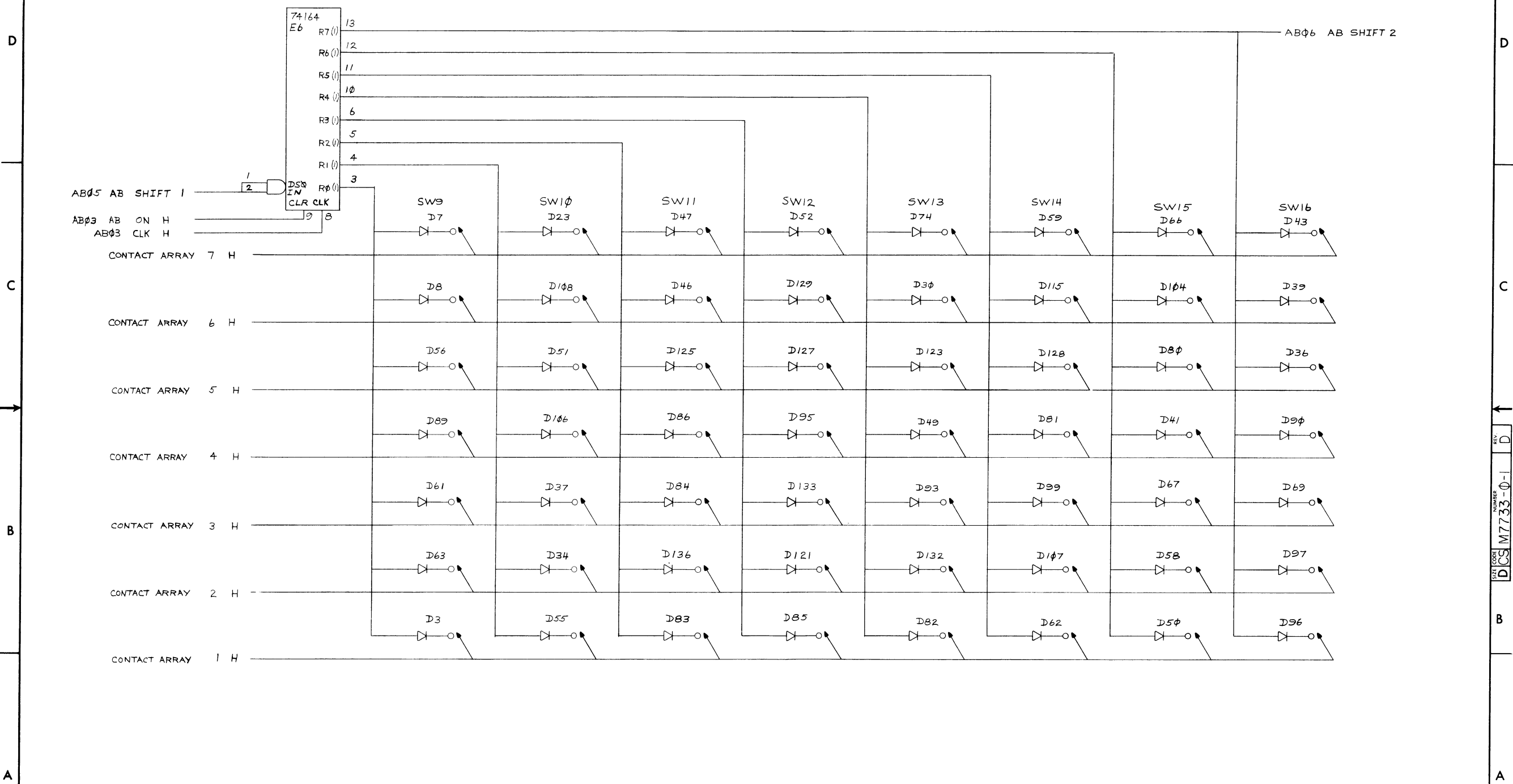
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DCS M7733-0-1



REVISIONS		
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TITLE	(ABφ6)	SIZE CODE	NUMBER	REV.
ANSWERBACK OPT		DCS	M7733-0-1	D
SCALE	1/1	SHEET	6 OF 7	DIST.

DEC FORM NO. DRD 138

8

7

6

5

4

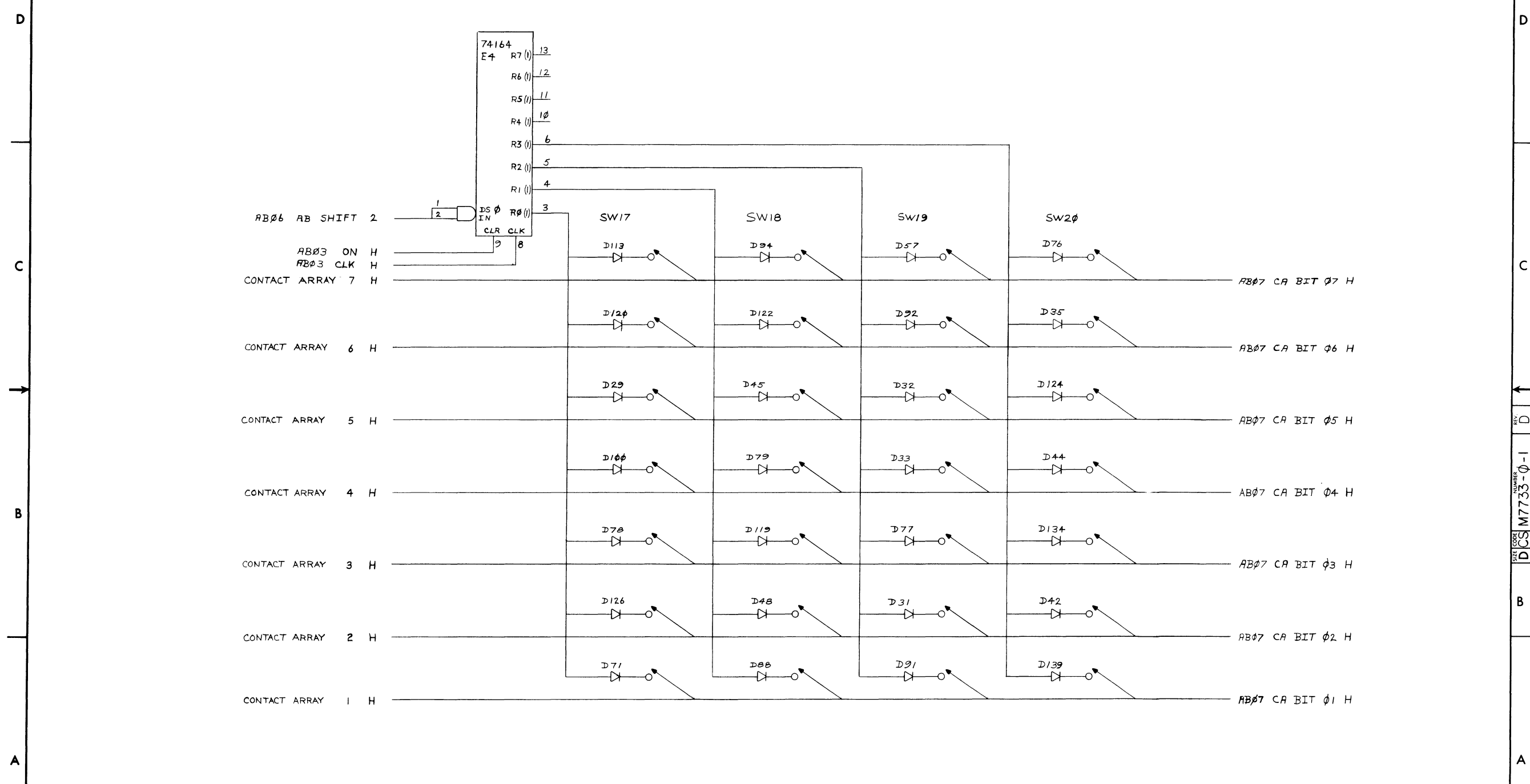
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REVISIONS		
CHK	CHANGE NO.	REV.

REV. D
NUMBER M7733-0-1
DATE CODE DCS

CHAPTER 14

FORMS CONTROL, VERTICAL TABULATION, AND HORIZONTAL TABULATION OPTION (LAXX-KY)

14.1 TABS OPTION INTRODUCTION

This option (hereinafter called Tabs Option) provides a DECwriter with three major functions:

1. Forms Control – Top of form capability
2. Vertical Tabs – Storage of vertical tab locations
3. Horizontal Tabs – Storage of horizontal tab locations

The Forms Control Section of the option stores the preset form length and compares it with the number of line feed actions performed by the printer mechanism. Then, when commanded by a form feed code, it issues the correct number of option-generated line feed codes required to advance the paper to the next top of form.

The Horizontal Tab Section stores tab locations and monitors the position of the print head in the 132 printable columns. When a Horizontal Tab command is received it issues the proper number of space codes to move the print head to the right to the next horizontal tab location.

The Vertical Tab Section stores tab locations and monitors the number of lines the paper advances. This section operates in conjunction with the Forms Control TOF setting which establishes the maximum number of printable lines for the form being used. A vertical tab can be established on any line on a form. On receipt of a Vertical Tab command this section issues the proper number of line feed codes to advance the paper to the next vertical tab location.

Each section of the option performs all internal housekeeping functions (incrementing, line feed, or space code generating, etc.) before option-generated data is passed on to the Character Buffer for normal terminal action.

14.2 TABS OPTION FUNCTIONAL DIAGRAM

Figure 14-1 shows the Tabs Option in a typical installation. The Forms Control Assembly is physically attached to the right-hand side of the printer mechanism and the circuit board is connected by an edge connector at location A of the Expander Option Mounting Kit. A cable harness connects the two assemblies. At each end of this harness is a Mate-N-Lok connector and a pair of Faston terminals. One connector is connected to J1 on the option circuit board, the other end to the FORMS LENGTH switch on the Forms Control Assembly. The Faston terminals connect to lugs on the SET TOP OF FORM switch and lugs on the option circuit board. The FORMS LENGTH switch is a 12-position rotary switch and the SET TOP OF FORM switch is a momentary-contact pushbutton. Each position of the FORMS LENGTH switch represents the length (in inches) of a pre-established format (such as a preprinted form) that can be used with the option. In normal operation, the FORMS LENGTH switch is set to the length of the form being used, then the SET TOP OF FORM switch is depressed to load this value into the Vertical Position Counter on the option circuit board.

Data processed by the UART, whether incoming serial information or locally generated at the keyboard, is available at location A on the Expander Option Mounting Board. All option-generated output signals (line feed or space codes and control signals) are also available at location A. No edge connector is installed at location B; the exposed fingers of the circuit board provide convenient locations for monitoring circuit signals.

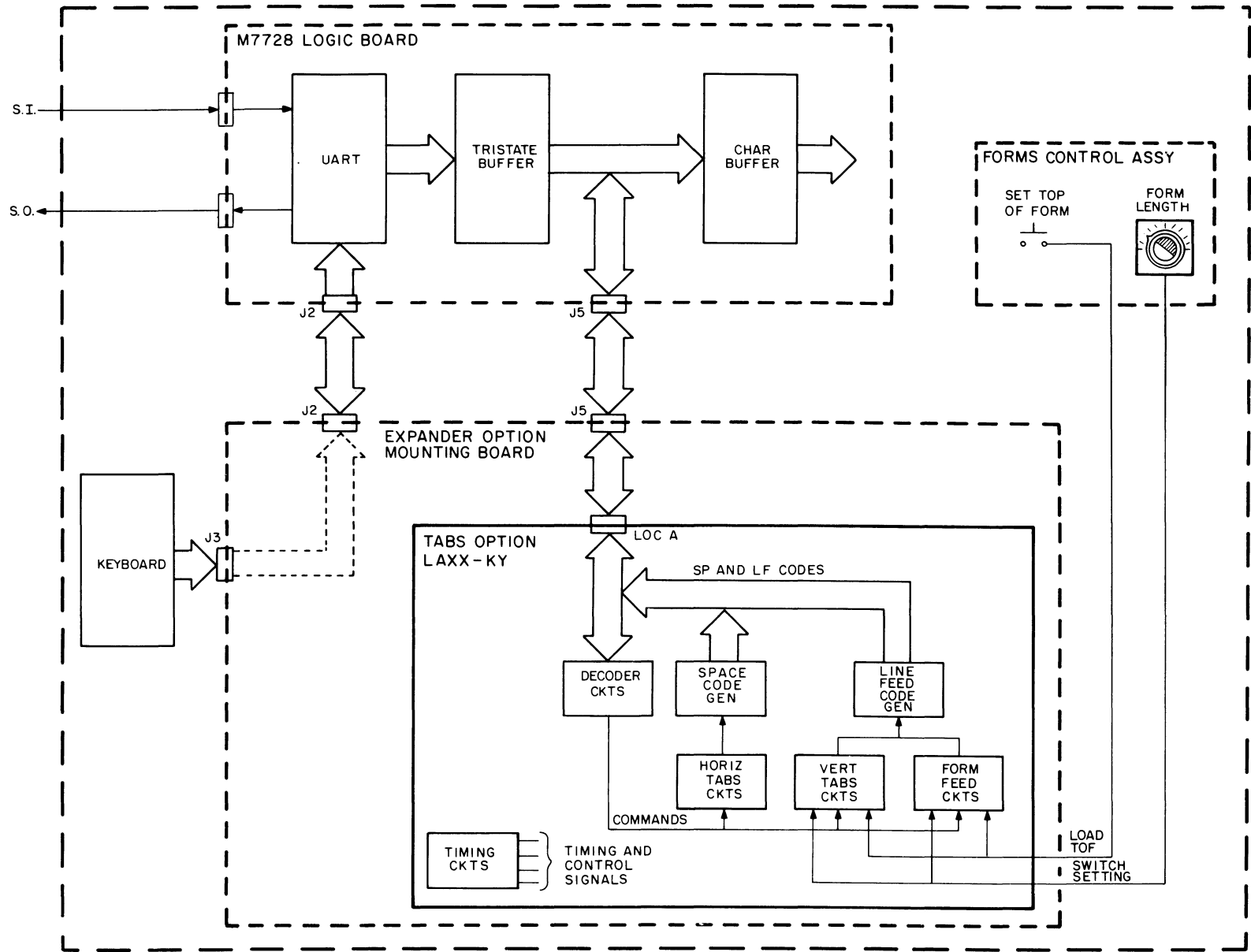


Figure 14-1 Tabs Option Functional Block Diagram

The Decoder Circuits monitor the incoming data for commands and other pertinent codes that are required in the three operational sections. Table 14-1 lists the various codes detected by the Decoder Circuits and the sections where these codes are used.

**Table 14-1
Codes Decoded By Tabs Option**

Codes Detected	Section Used in		
	Horizontal Tabs	Vertical Tabs	Forms Control
CR	Yes		
FF		Yes	Yes
VT		Yes	Yes
HT	Yes		
BS	Yes		
LF		Yes	Yes
ESC1	Yes		
ESC2	Yes		
ESC3		Yes	
ESC4		Yes	

The Line Feed Code Generator and Space Code Generator send codes back up the bidirectional line to the Character Buffer on the Logic Board. The Space Code Generator is controlled by the horizontal tab circuits and the Line Feed Code Generator by either the vertical tab or forms control circuits.

The timing circuits establish the controlling signals for all functional sections of the option. Sequential timing is required for the critical storage, loading, resetting, and clearing functions performed in typical tabbing operations. The timing circuits utilize the Data Available signal from the UART plus commands from the functional section of the option and the Option Clock timing pulses to initiate these timing sequences. Whenever the option is performing one of its three major functions, the UART is disabled by a signal from these timing circuits.

14.3 SIMPLIFIED OPERATION OF TABS OPTION

Each of the three option functions (VT, HT, and TOF) can be set to a value (store a location), commanded to perform a function (go to next top of form), and cleared of all positions or settings. Table 14-2 shows the commands, both local and remote, that set, command, and clear each of the functions.

**Table 14-2
Control Commands for Major Tab Operations**

Function Section	Set Up By		Controlled By		Cleared By	
	Local	Remote	Local	Remote	Local	Remote
Horizontal Tabs	ESC1	033 ₈ and 061 ₈	TAB key (HT)	011 ₈	ESC2	033 ₈ and 062 ₈
Vertical Tabs	ESC3	033 ₈ and 063 ₈	CTRL K (VT)	013 ₈	ESC4	033 ₈ and 064 ₈
Top of Form	Set length Depress TOF or at wake-up	None	CTRL L (FF)	014 ₈	Change length Depress TOF	None

14.3.1 Horizontal Tabs Operation

The Horizontal Tabs Section of the option can be considered as a counter with 132 locations; each location represents one of 132 printable positions the print head passes through on each horizontal printing line. When the print head is at the left-hand margin (just after a carriage return or a power-up sequence), this Horizontal Position Counter is at zero. As the print head moves across to the right, the counter increments; back spacing (movement to the left) decrements the counter. The Horizontal Position Counter always contains the count of the column in which the print head is positioned.

To set a horizontal tab, the print head must be physically positioned at the location of the desired tab; then the storage command is either typed locally (ESC1) or received (033₈ and 061₈). This action causes the HT RAM that is monitoring the output of the Horizontal Position Counter to store this print head position. Any number of horizontal tabs (up to 132) can be stored on a line.

Typing the TAB key in local or receiving an HT code (011₈) causes the option to block any incoming data from the UART and issue space codes until the print head moves to the right to the first location where a tab had been set. This location is determined by the output of the HT RAM. If a Horizontal Tab command is given and there are no tabs set between the present print head location and the right-hand margin, the option generates space codes until the print head reaches column no. 132. The print head remains there until either a carriage return or line feed code is received. The printing function is disabled while the head is at column 132.

All horizontal tab locations are cleared when either an ESC2 is typed locally or 033₈ and 062₈ is received. The horizontal tab clearing action initiates the following sequence:

1. Value of Horizontal Counter is stored in latch.
2. Horizontal Counter is reset to zero.
3. Horizontal Counter is incremented up to 132 and all horizontal tabs stored in HT RAM are erased.
4. Value in latches is loaded back into Horizontal Counter.

This action ensures that the Horizontal Counter always contains the actual position of the print head and is ready to accept new tab locations right after the old tabs are erased. For, if the clearing command is given when the print head is in the middle of a line and the Counter is just reset to zero and not reloaded with the actual position, any tabs set on this line are not accurate because of the discrepancy between head position and Counter value.

14.3.2 Top of Form (TOF) Operation

The primary component of the TOF Section is a 128-bit Counter. Each bit of this counter represents a printable line on a form. This Vertical Counter accepts one of 12 preset values as determined by the position of the FORMS LENGTH switch. Each switch position loads a number that is 128 minus the maximum number of lines on a specific form. For instance; if an 14-inch form is to be used, the FORMS LENGTH switch is set to position no.14 and the SET TOP OF FORM switch is depressed. On a 14-inch form the maximum number of printable lines is 84 (14 inches times 6 lines per inch). The 128-line counter is preset with 44 lines from switch position no. 14, leaving 84 lines to be filled. Each line feed code received by the option or each line feed code generated by the Vertical Tabs Section of the option increments the count upwards by one line. So, if after advancing 61 lines (61 line feed codes received or generated), a Top of Form command (form feed code) is received the paper must be advanced 23 lines to reach the top of the next form. As the option generates these 23 line feed codes, the Vertical Counter is incremented once for each line feed code. When the Vertical Counter overflows (after 128 increments – preset value plus the number of option-generated line feed codes) the value of the FORMS LENGTH switch is reloaded back into the Vertical Counter again.

NOTE

There is no way to completely clear the DECwriter of a TOF value. Everytime the Vertical Counter overflows, the FORMS LENGTH switch setting is automatically reloaded to establish a new top of form.

14.3.3 Vertical Tabs Operation

The Vertical Tabs Section can be considered as a unique variation of the TOF function. Both respond to operator commands and advance paper through the DECwriter by issuing line feed codes until a specific number of lines have been advanced. The TOF circuits stop the paper from advancing when the Vertical Counter is full, indicating that the next top of form has been reached. The vertical tabs circuits stop the paper from advancing when the location of a previously set vertical position is reached. Thus, the FORMS LENGTH switch setting used in the TOF circuits actually establishes the boundaries where vertical tabs can be set.

A vertical tab is set by either typing ESC3 or receiving 033₈ and 063₈. At the time when this storage command is received, the vertical location of the print head is stored in the VT RAM that is monitoring the output of the Vertical Counter.

Typing CTRL L in local or receiving 014₈ activates the vertical tab function. This action causes the Vertical Tabs Section to block any incoming data from the UART and issue line feed codes until the paper advances to the next vertical tab location as determined by the VT RAM. If a VT command is given and there are no vertical tabs set between the present head location and the next top of form, the paper advances to the next top of form.

All vertical tab locations are cleared when ESC4 is typed locally or 033₈ and 064₈ is received. The vertical tab clearing action initiates the following sequence:

1. Value of Vertical Counter is stored in a latch.
2. Vertical Counter is reset to zero.
3. Vertical Counter is incremented to overflow and all vertical tabs stored in VT RAM are erased.
4. At TOF (overflow) the value in latches loaded back into Vertical Counter.

This action ensures that the Vertical Counter always contains the actual position of the print head and is ready to accept TOF commands or new tab locations right after the old tab locations are cleared. This prevents discrepancies between head position and Vertical Counter values. If the clearing command was given in the middle of a form and the Vertical Counter was just reset to zero and not reloaded with the actual position, any TOF or VT command given before the next top of form was reached would not perform correctly.

14.4 TABS OPTION BASIC BLOCK DIAGRAM

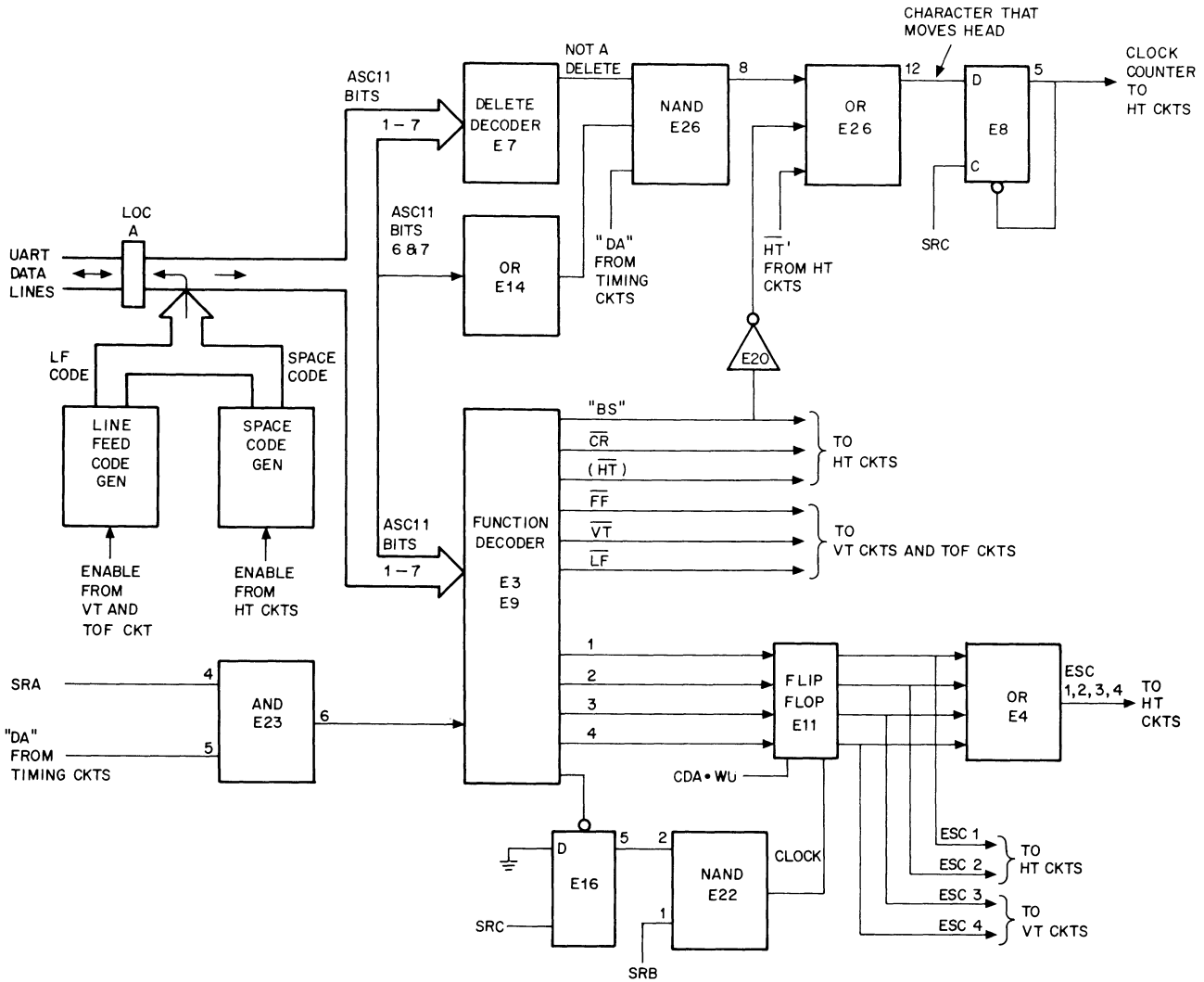
The basic block diagrams for the Tabs Option are shown in Figures 14-2, 14-4, 14-5, 14-7, 14-9, and 14-10. These diagrams are simplified representations of the HT, VT, TOF circuit schematic (D-CS-M7736-0-1). Circuit designations and pin numbers indicated on these figures correlate with corresponding components on the schematic. Buffers, inverters, and other components that do not have major operational functions are omitted from these block diagrams.

The Tabs Option can be divided into the following five functional areas:

1. Decoding and Generating Circuits
2. Timing Circuits
3. Horizontal Tabs Circuits
4. Top of Form Circuits
5. Vertical Tabs Circuits

14.4.1 Decoding and Generating Circuits Basic Block Diagram

The basic block diagram for the decoding and generating circuits is shown in Figure 4-2. Incoming ASCII-coded data present on the bidirectional UART data lines connects to the decoding circuits. Outgoing data, either a line feed or space code generated by the option is sent back to the Character Buffer via these lines too.



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Figure 14-2 Decoding and Generating Circuits Basic Block Diagram

14.4.1.1 Decoding – The decoding circuits perform two main functions: (1) detecting commands that the option requires for operation and (2) monitoring the UART data lines for characters or codes that cause the print head to move either forward or backward. The Function Decoders E3 and E9 sample the seven ASCII bits when the DA signal and the SRA timing pulse are present.

NOTE

Both bit 7 and Parity Error are required at AND gate E23 before DA and SRA allow the decoding action.

Decoding of standard codes (HT, CR, LF, etc.) is performed in a normal manner but the special commands ESC1, 2, 3, and 4 require a somewhat different decoding scheme. Each of these commands consist of two codes (the ESC code and either 1, 2, 3, or 4) which must be decoded in the correct sequence to be recognized by the options as legitimate commands. When the ESC code is detected at SRA time, E16 sets placing a high level on pin 2 of E22. This high level out of E16 pin 5 remains high through the duration of the ESC decoding. It appears that at SRC time E16 will clock but it does not because SRC has no effect while the ESC code is keeping E16 set.

If the next character after the ESC code is either 1, 2, 3, or 4, the Function Decoder detects these codes and applies one of them to E11. At SRB time of this second character NAND gate E22 is qualified and clocks the second character through E11 to the appropriate circuit. If the character following an ESC command is not 1, 2, 3, or 4, there is no decoded signal at the input of E11 to be clocked through at SRB time. In either case, at SRC time of the second character E16 clocks low. Now, even if the third character received is 1, 2, 3, or 4, and after being decoded is applied to E11, there is no clock signal from E16 to transfer it through E11. Therefore, only these specific combinations of the ESC code and 1, 2, 3, or 4 are decoded as option-operational commands. The timing diagram for ESC command decoding is shown in Figure 14-3.

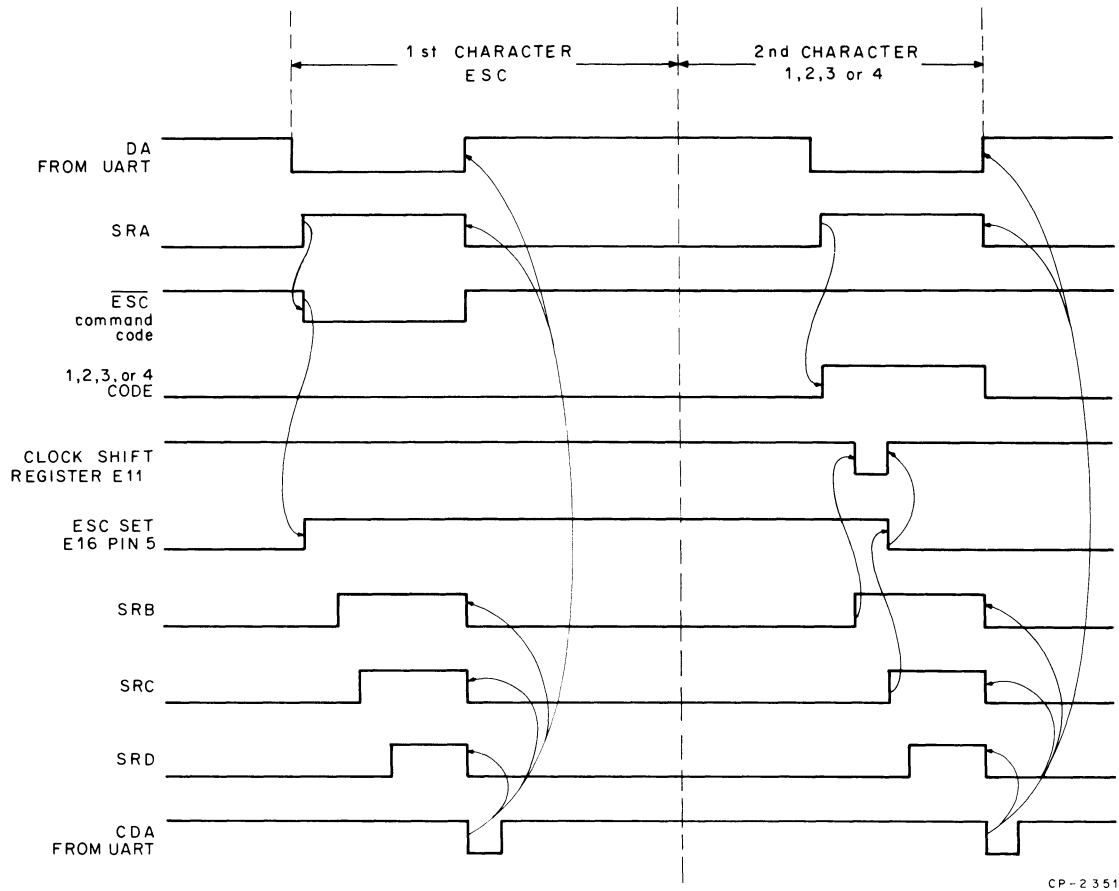


Figure 14-3 Timing for ESC Command Decoding

The other decoding function is performed by E7 and E14 which are also monitoring the incoming ASCII data. The function of these Decoders is to detect all characters or codes that cause the print head to move either to the left or right. Only two gates are required to decode all these possible character combinations. This is because of the unique bit assignments in the ASCII structure where all of these characters (except three) have a 1 in bit 6 or 7. The characters that move the head and do not have this 1 in bit 6 or 7 are: delete, back space, and horizontal tab. Back space and HT are decoded by the Function Decoder E3, E9. The delete code (all bits are 1) is detected by E7. Therefore, if a character is detected having a 1 in either bit 6 or 7 and it is *not* the delete code, the DA signal from the timing circuits qualifies AND gate E26. A back space, horizontal tab, and head moving indication is passed through OR gate E26 to the data input (pin 2) of E8. At SRC time, E8 clocks this information out to the horizontal tabs circuits. After clocking, E8 resets and awaits another indication that the next character will cause the print head to move.

14.4.1.2 Generating – The option-generated line feed codes and space codes are issued by the combination of E1 and E10. Enabling the Space Code Generator places the binary code 0100000 on the UART lines. The line feed code (0001010) is also generated by these same gates but uses E10 in a different manner.

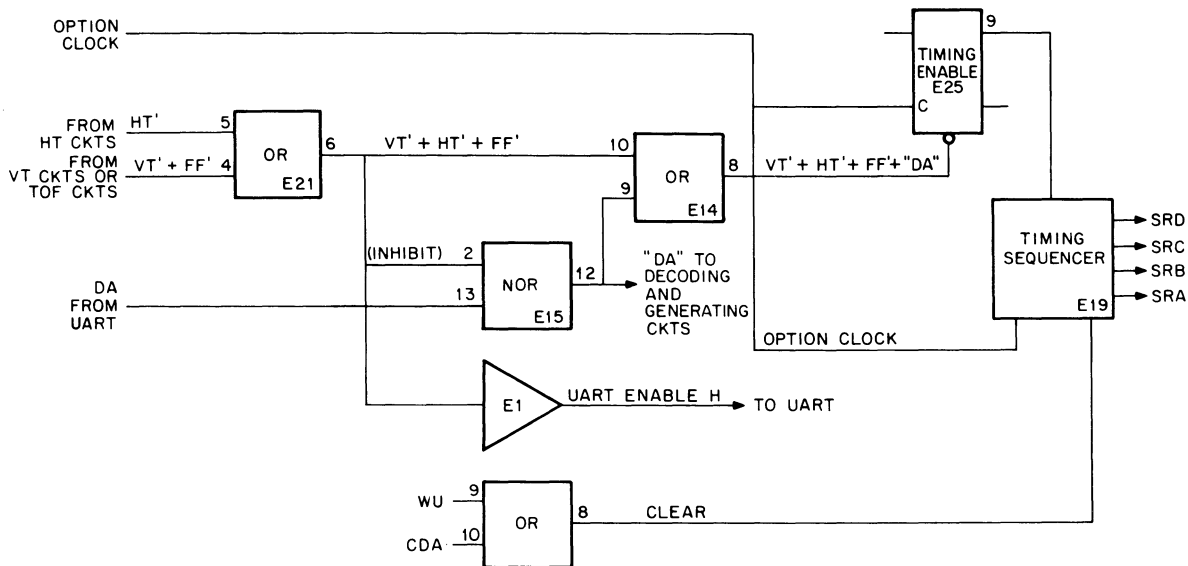
NOTE

Both codes have the same bit pattern in four locations (bits 1, 3, 5, and 7) and always use E1 to generate these four bits.

14.4.2 Timing Circuits Basic Block Diagram

The basic block diagram for the timing circuits is shown in Figure 14-4. The primary component of this circuit is the Timing Sequencer E19, a 4-bit shift register that produces four sequential timing signals (SRA, SRB, SRC, SRD). Any of four signals applied to the reset pin of flip-flop E25 enables the Timing Sequencer and causes the high level at pin 4 to shift right at the rate of the Option Clock input at pin 6 (approximately 1.2 μs per shift). The four possible enabling signals are:

1. HT' Horizontal Tab command
2. VT' Vertical Tab command
3. FF' Form Feed command
4. DA (Data Available) signal



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Figure 14-4 Timing Circuits Basic Block Diagram

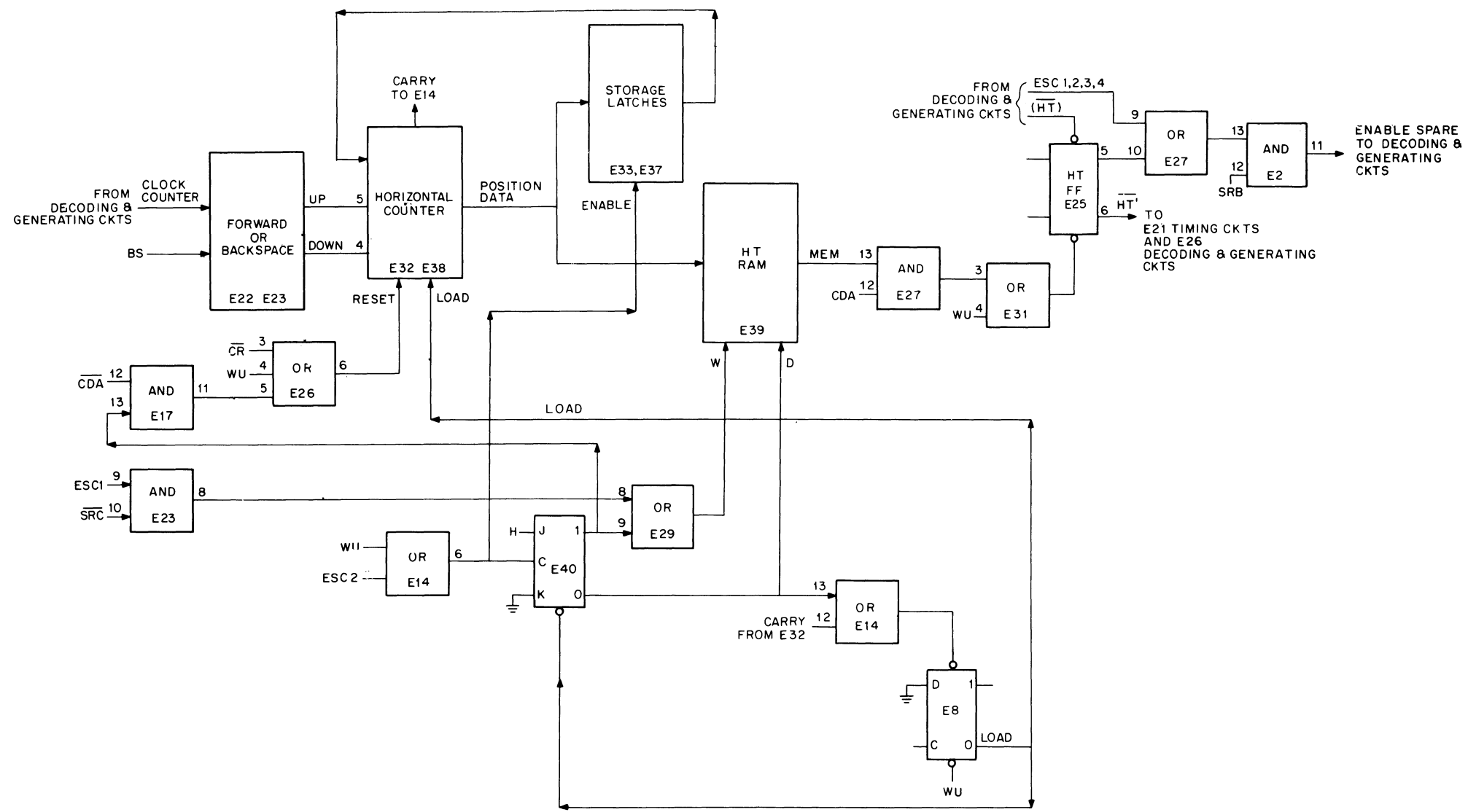
The DA signal from pin 12 of E15 (which is the Data Available signal from the UART) is only present when the other three signals are *not* present. This blocking action ensures that once a tab or TOF routine has started, no other incoming command or character is processed until the option function is completed. Table 14-3 contains the major events of each option function that occurs during each timing period.

14.4.3 Horizontal Tabs Circuits Basic Block Diagram

The basic block diagram for the horizontal tabs circuits is shown in Figure 14-5 and the operational sequence flow diagram is shown in Figure 14-6.

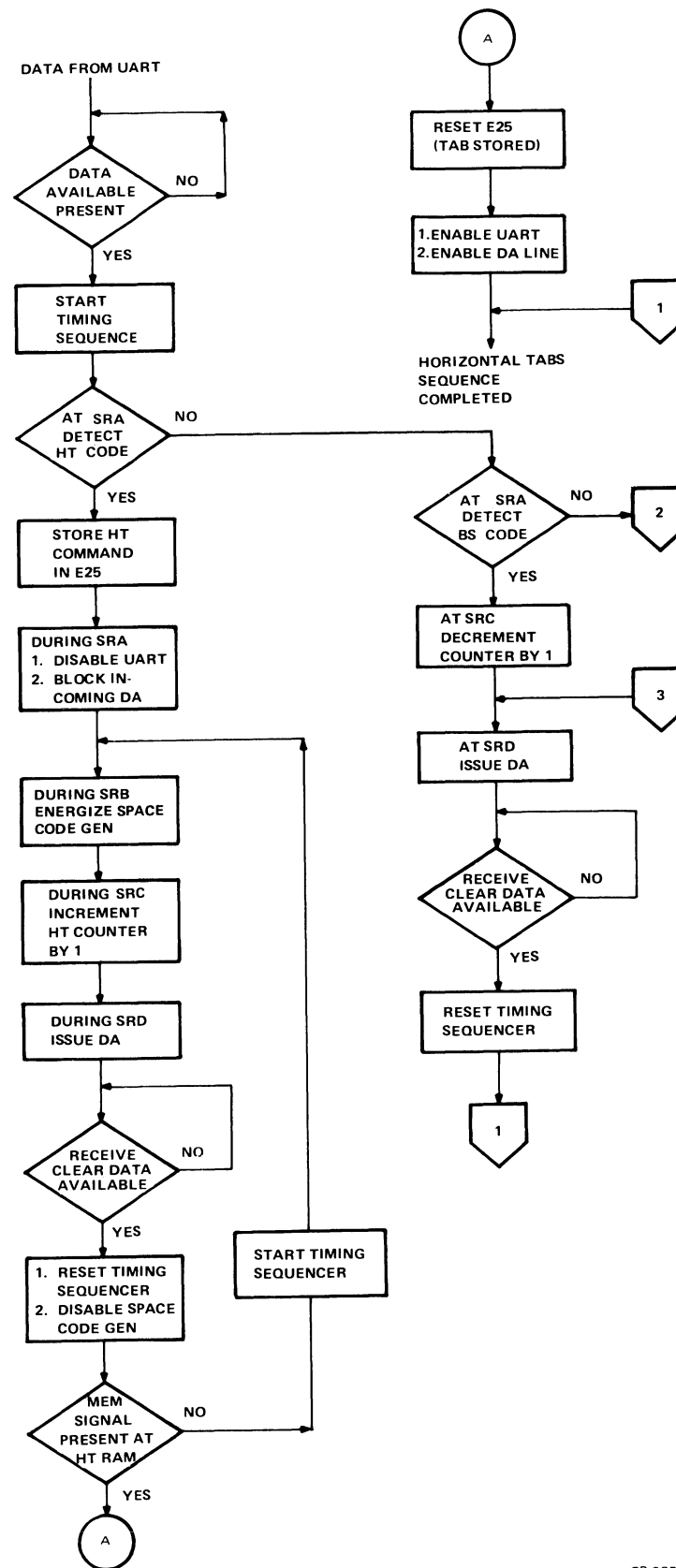
Table 14-3
Timing Sequencer Major Events

Functional Sections of Option				
Timing Sequencer Periods	Decoding and Generating Circuits	Horizontal Tabs Circuits	Vertical Tabs Circuits	Top of Form Circuits
SRA	<ul style="list-style-type: none"> • Enable Function Decoder 	<ul style="list-style-type: none"> • HT command detected • CR code resets HT Counter • BS code detected • Disable UART 	<ul style="list-style-type: none"> • VT command detected • FF command detected • LF code detected • Disable UART 	<ul style="list-style-type: none"> • FF command detected • VT command detected • LF code detected • Disable UART
SRB	<ul style="list-style-type: none"> • Clock ESC command 	<ul style="list-style-type: none"> • ESC 1 decoded • ESC 2 decoded • Enable Space Code Generator • Set HT tab in HT RAM (ESC 1) 	<ul style="list-style-type: none"> • ESC 3 decoded • ESC 4 decoded • Enable Line Feed Code Generator • Clock VT Counter 	<ul style="list-style-type: none"> • Enable Line Feed Code Generator • Clock VT Counter
SRC	<ul style="list-style-type: none"> • Reset ESC FF 	<ul style="list-style-type: none"> • Clock HT Counter 	<ul style="list-style-type: none"> • Load VT Counter with switch setting after TOF 	<ul style="list-style-type: none"> • Load VT Counter with switch setting after TOF
SRD	<ul style="list-style-type: none"> • Generate DA 	N/A	<ul style="list-style-type: none"> • Set VT tab in VT RAM (ESC 3) 	N/A

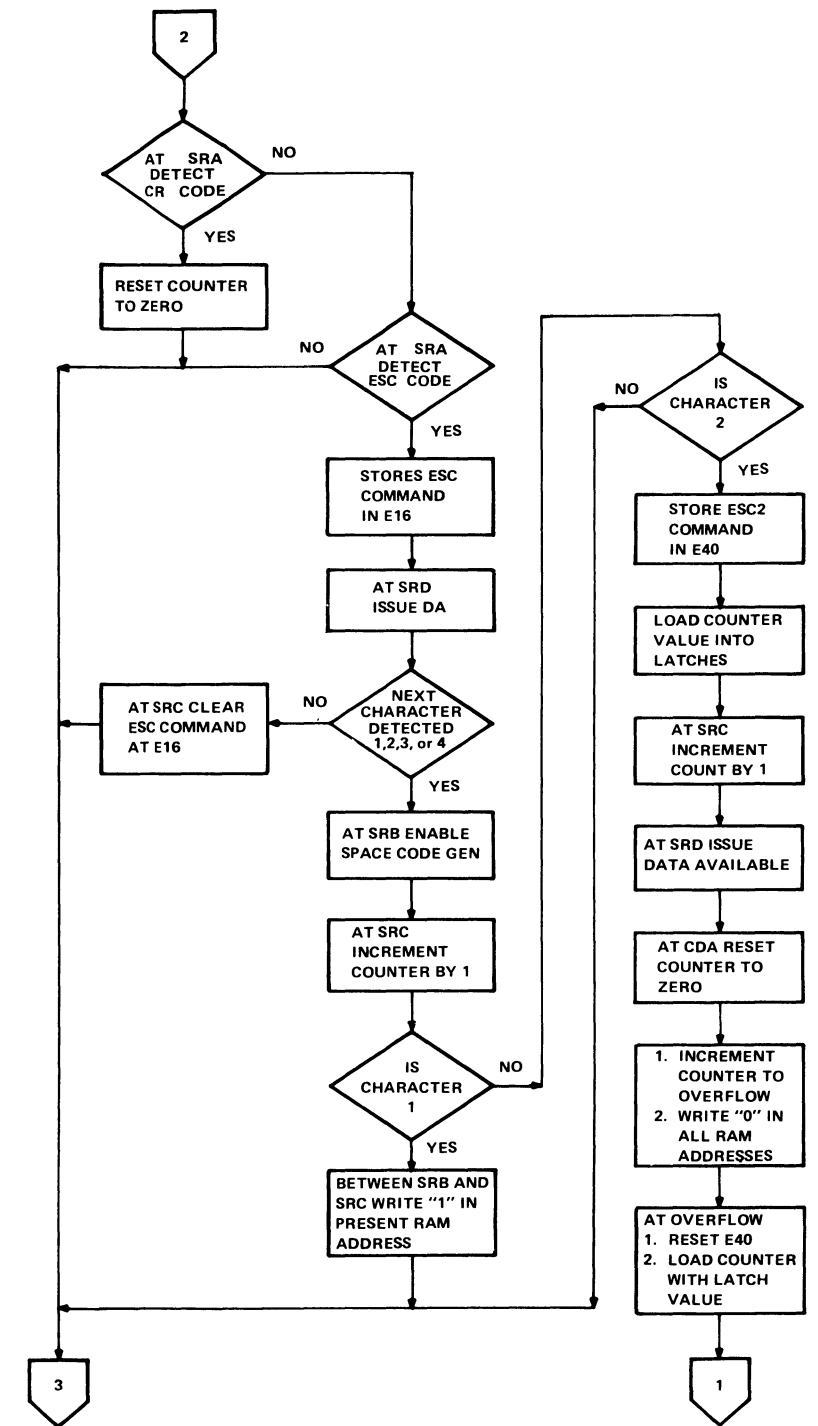


CP-2353

Figure 14-5 Horizontal Tabs Circuits
Basic Block Diagram



CP-2354A



CP-2354B

Figure 14-6 Horizontal Tabs Circuits Operational Sequence

The horizontal tabs circuits perform the following four functions:

1. Monitoring the horizontal position of the print head
2. Setting horizontal tab locations
3. Tabbing action
4. Clearing horizontal tab locations

14.4.3.1 Monitoring – Each time the decoding circuits detect a character or command that moves the print head, the Clock Counter pulse from E8 is applied to the forward or back space steering gates E22 and E23. If the motion is forward, the Horizontal Counter E32, E38 is incremented by one count; if back space, the Counter is decremented by one. As the Counter changes, the position value is present on the output lines that are hardwired to the input address lines of HT RAM E39. Therefore, the RAM's address is representative of the current print head position.

NOTE

These Counter values are not written into the RAM, just present at the address lines.

When a carriage return is performed, the Horizontal Counter resets to zero and the HT RAM is at address zero also.

14.4.3.2 Setup – The command that establishes a horizontal tab is ESC1. When this command is given it is detected by the decoding circuits and applied to pin 9 of E23. Between SRB and SRC time it enables the write input (pin 12) of the HT RAM. At this time there is a high level on the data input (pin 13) of the HT RAM and a 1 is written into the HT RAM location that is addressed by the Horizontal Counter output. As the print head is advanced to the right to another tab location, the Horizontal Counter output increments the HT RAM pointer to new addresses. During this incrementing the HT RAM is not storing new locations; only when the ESC1 command is received are 1s stored in the HT RAM.

NOTE

When the ESC1 command is typed the print head moves as the 1 is depressed but the horizontal tab location is set at the column location established when the ESC key was depressed.

14.4.3.3* Horizontal Tab Action – A Horizontal Tab command is decoded, then applied to the horizontal tabs circuits as the (HT) signal. This signal sets HT flip-flop E25, which remains set until the tab function is completed. Four events occur as a result of E25 storing the Horizontal Tab command:

1. UART is disabled.
2. Data Available signal path is blocked.
3. Horizontal Counter is ready to be incremented by one count.
4. Space Code Generator is enabled at SRB.

The $\overline{\text{HT}}$ signal from pin 6 of E25 is applied to the timing circuits where it blocks the Data Available signal path through E15 and disables the UART through E1. The $\overline{\text{HT}}$ signal level is also applied to E26 of the Decoder Circuits to clock the HT Counter by 1. This level on the $\overline{\text{data}}$ input (pin 2) of E8 is clocked through E8 at SRC time of each Timing Sequencer cycle. At SRB time the $\overline{\text{HT}}$ signal enables the Space Code Generator E1, E10 which places the ASCII code for a space on the bidirectional lines to the Character Buffer. At SRD time the

option-generated Data Available signal is produced and this space code is ready to be processed and move the print head one space to the right. As the Horizontal Tab command increments the Horizontal Counter, a new HT RAM address is accessed. If this new address contains a zero (indicating that a horizontal tab was set at this position), the MEM signal is present at pin 6 of the HT RAM. This MEM signal combines at E27 with the Clear Data Available (CDA) signal associated with the space code that just incremented the Horizontal Counter and resets the HT flip-flop E25. This resetting action enables the UART, clears the Data Available signal path, and removes the increment signal from the Horizontal Counter at E26 pin 1.

If the MEM signal is not present at the HT RAM, the horizontal tabs circuits increment the counter at SRC, issue a space code at SRD, and continue this spacing cycle until the next horizontal tab location is reached (MEM signal out of the HT RAM).

14.4.3.4 Clearing Horizontal Tabs – Horizontal tab locations are cleared (erased) by either of two events: receiving an ESC2 command or during a power-up sequence (wake-up routine).

The ESC2 command is detected by the decoding circuits and is applied as a clearing pulse to E14 in the horizontal tabs circuits. The leading edge of this clearing pulse enables the Storage Latches E33 and E37 which load and store the current value in the Horizontal Counter. The trailing edge of this pulse clocks JK flip-flop E40. The high level output of E40 (Q) resets the Horizontal Counter to zero for the duration of CDA. Then the Counter starts counting up from zero at the Option Clock rate. As the Horizontal Counter increments, the low level on the write input (pin 12) of the HT RAM writes 0s into each address location the Counter advances through. Zeros are written because pin 8 of E40 is low during a clearing function. When the Horizontal Counter overflows, the CARRY signal is applied through E14 to set E8. As E8 sets, the JK flip-flop (E40) is reset, removing the writing function from the HT RAM and reloading the Horizontal Counter with the print head value previously stored at the outset of the clearing action. Now the HT RAM is cleared of any tab settings and the Counter contains the value of the column in which the print head is positioned.

During a power-up sequence the Wake-Up command (WU) performs a function similar to the ESC2 command. All actions are the same except that the Horizontal Counter value stored in the latches at the beginning of the sequence is zero because the print head is always at column position 0 after a wake-up; therefore, the Counter value is zero also.

14.4.4 Top of Form (TOF) Circuits Basic Block Diagram

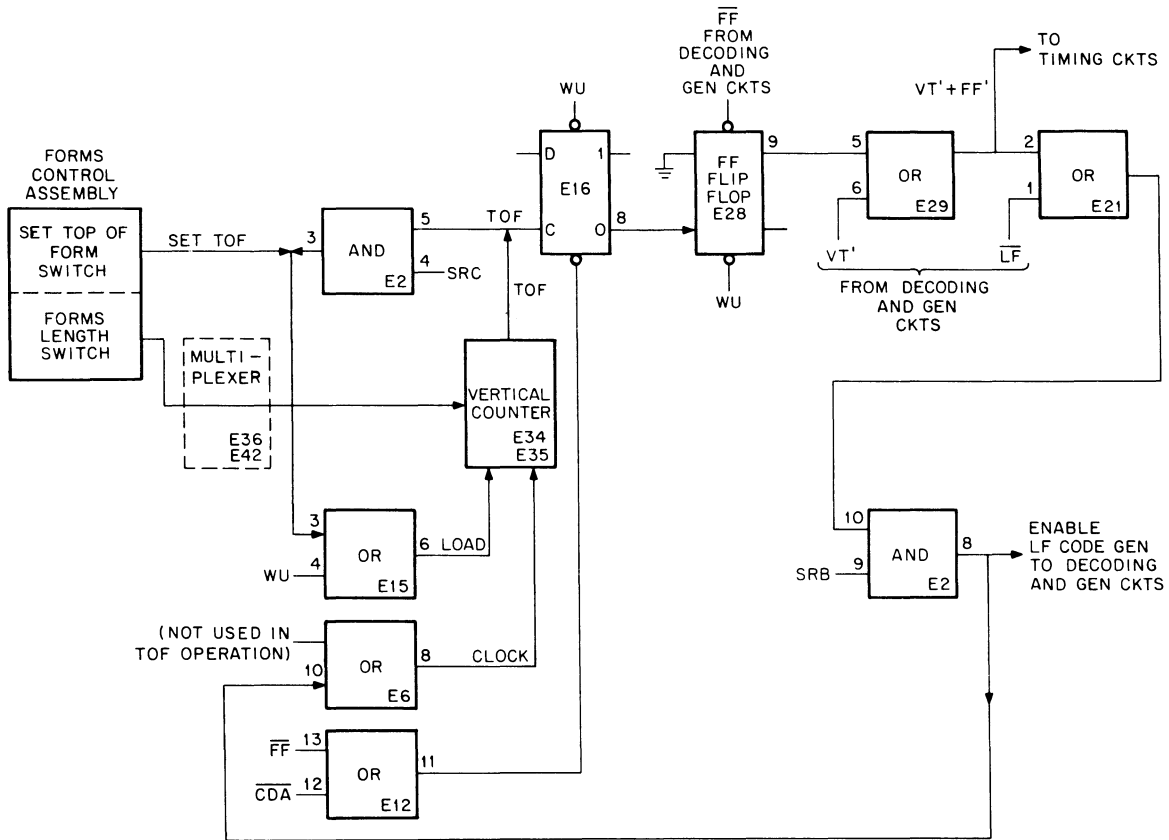
The basic block diagram for the TOF circuits is shown in Figure 14-7 and the operational sequence flow diagram is shown in Figure 14-8.

The TOF circuits perform three major functions:

1. Monitoring the vertical position of the print head
2. Form feeding
3. Setting form length values

14.4.4.1 Monitoring – This section of the option monitors the incoming data for codes that affect the vertical position of the print head. It responds to four codes:

1. Vertical tab stored – VT at pin 6 of E29
2. Line feed code – LF at pin 1 of E21
3. Form feed code – FF at pin 10 of E28
4. Set TOF command – TOF at pin 3 of E15



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Figure 14-7 Top of Form Circuits Basic Block Diagram

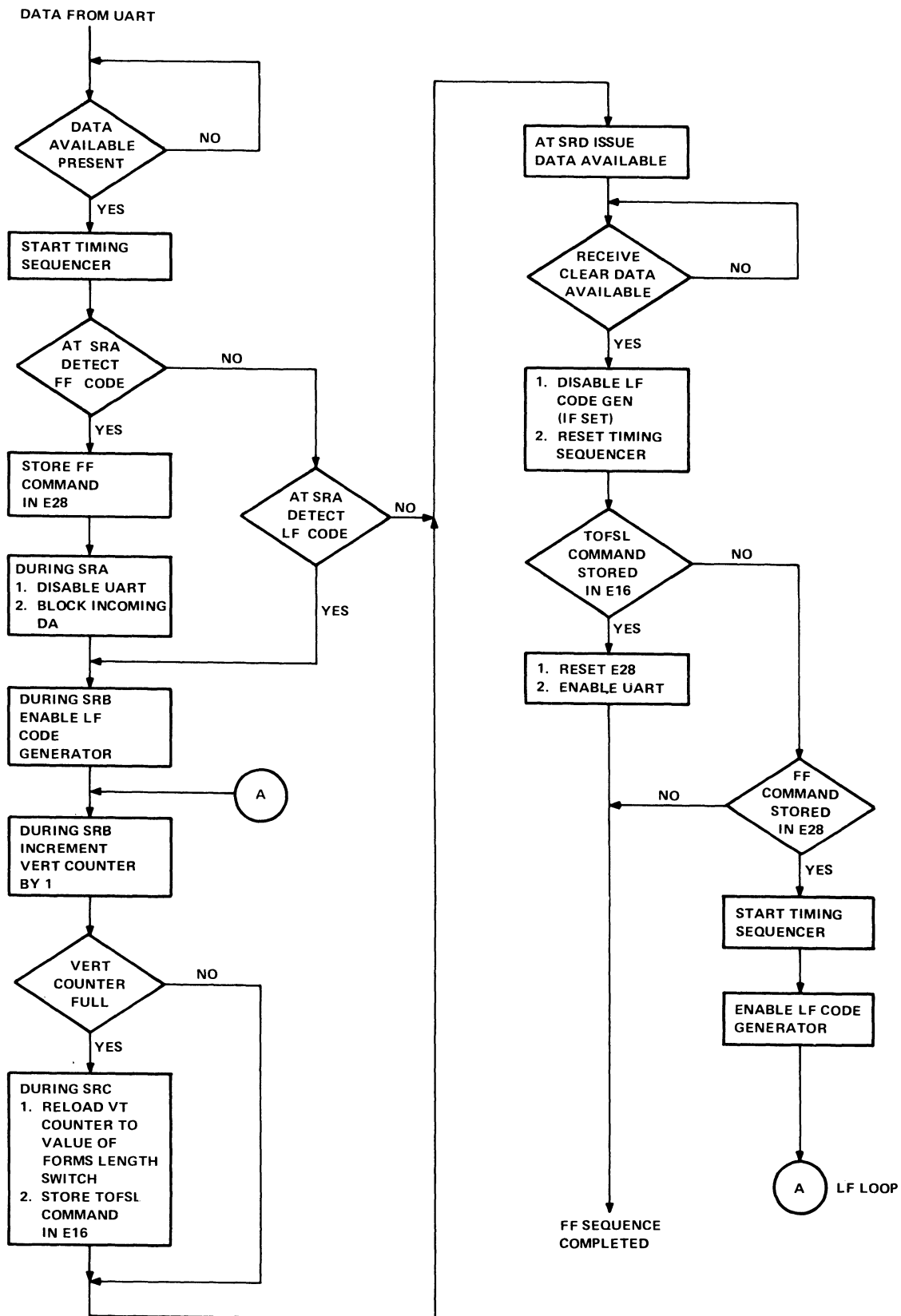
The VT and LF signals applied to E29 and E21 respectively enable the Line Feed Code Generator and increment the Vertical Counter E34, E35 at SRB time. The VT' signal is a low level that remains low as long as the option is performing a vertical tab, but the LF signal is a pulse that exists long enough to clock (increment) the Vertical Counter.

NOTE

The LF code also energizes the Line Feed Code Generator E1 and E10 through E2 which places an LF code on the bidirectional lines to the Character Buffer. This option-generated code is actually in parallel with the LF code generated by the UART. Both codes are available to the Character Buffer because the UART is not disabled by the Tabs Option when an LF code is detected. The VT' signal from pin 4 of E29 that is applied to the timing circuits does cause the UART to be disabled and, in this instance, the Character Buffer accepts the LF code generated by the Tabs Option.

14.4.4.2 Form Feeding – A Form Feed command detected by the decoding circuits sets Form Feed flip-flop E28. When E28 sets and stores the FF command, a high level from pin 9 initiates the following four actions:

1. UART is disabled.
2. Data Available signal path is blocked.
3. Vertical Counter is ready to be incremented by one count.
4. Line Feed Code Generator is enabled.



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Figure 14-8 Top of Form Circuits Operational Sequence

The FF' signal from pin 4 of E29 is applied to the timing circuits where it blocks the Data Available path through E15 and disables the UART through E1. The FF' high level at pin 10 of AND gate E2 is clocked through at SRB time to energize the LF Code Generator and increment the Vertical Counter by one count. If this increment overflows the Counter, the TOF signal is present at pin 12 of E34. This TOF signal is used to clock E16 pin 8 to a low level and to load the Vertical Counter through Multiplexer E36, E42 with the FORMS LENGTH switch value at SRC time. At SRD time the option-generated Data Available signal is issued and a line feed code is sent to the microprocessor. When the CDA signal is sent back to the option indicating that the line feed code was processed, the CDA signal resets E16 at pin 13. The TOFSL signal generated when E16 resets causes the FF flip-flop E28 to reset also.

If the Vertical Counter does not overflow after being incremented (no TOF signal), the FF flip-flop E28 remains set and holds the UART disabled. The CDA signal, returning after the first line feed code was processed, resets the Timing Sequencer. But, because the FF flip-flop is still set, the Form Feed Stored (FF') signal immediately restarts the Timing Sequencer again. At SRB time the Vertical Counter is incremented again and the LF Code Generator issues another line feed code. If this increment still does not overflow the Vertical Counter, the line feed code generation sequence is repeated again and again until the TOF signal is present at pin 12 of the Vertical Counter. When the CDA from the last LF returns, the Counter resets to the value of the FORMS LENGTH switch and the option removes the disable from the UART. The option has completed the top of form sequence and is now waiting for line feed or form feed codes before starting any action again.

14.4.4.3 Setup and Wake-Up – Initial setup of the TOF circuits is accomplished when the setting of the FORMS LENGTH switch is parallel loaded into the Vertical Counter as the SET TOP OF FORM pushbutton is depressed. This places a low level pulse on pin 1 of E34 and E35 (the load inputs) through E16 and E20. The Vertical Counter loads just as if a TOF occurred. The Wake-Up (WU) signal generated on the Logic Board during a power-up sequence performs the same parallel loading action and also ensures that the FF flip-flop E28 is cleared.

14.4.5 Vertical Tabs Circuits Basic Block Diagram

Figure 14-9 shows the basic block diagram for the vertical tabs circuit. The operational sequence for these circuits is shown in Figure 14-10.

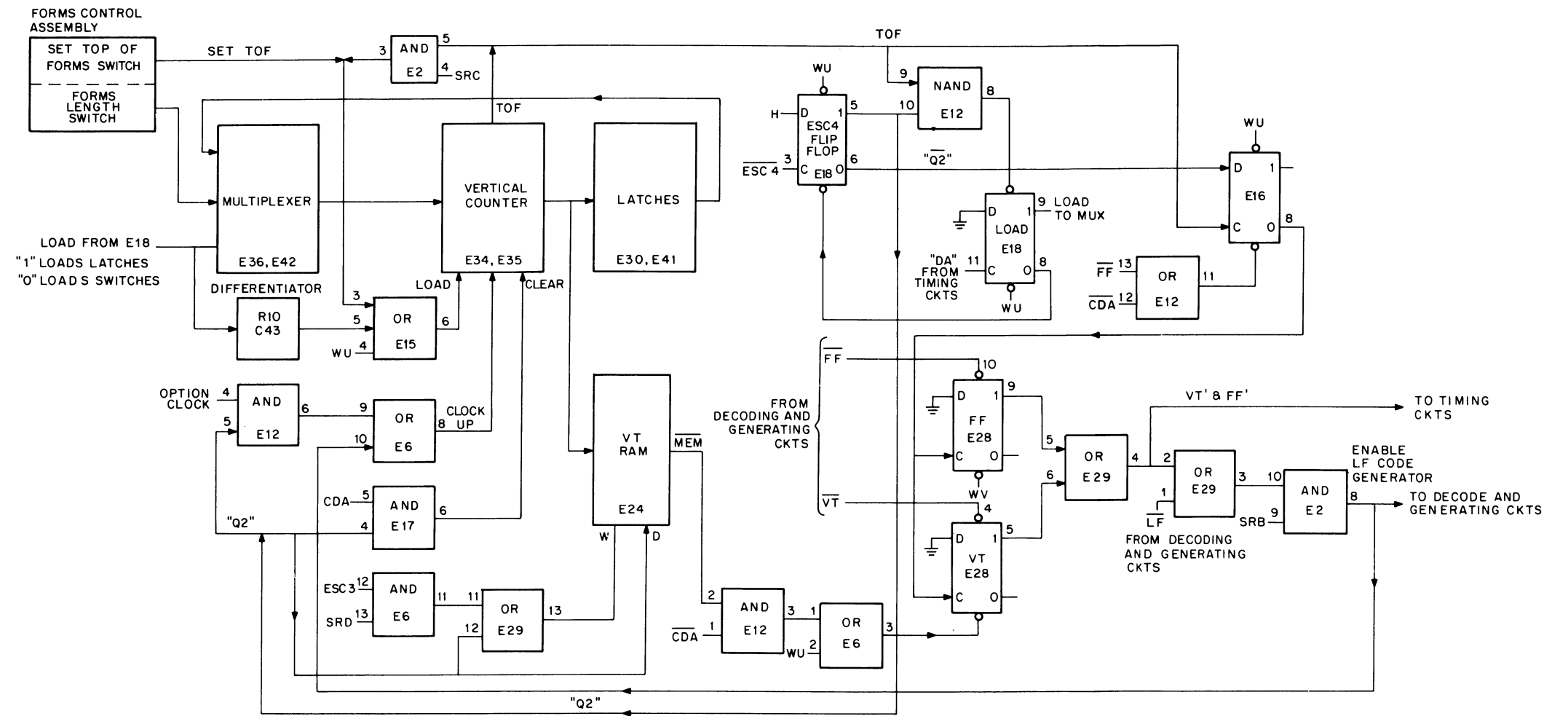
The vertical tabs circuits perform the following four major functions:

1. Monitoring the vertical position of the print head
2. Setting vertical tab locations
3. Tabbing action
4. Clearing vertical tab locations

As discussed earlier, vertical tab functions are very similar to top of form actions and in many instances both circuits share common components. This circuit sharing is shown graphically by the shaded components in Figure 4-11. As shown, most of the shaded components are relative to the major functions of monitoring, Counter incrementing, and Counter reloading. The unshaded components primarily process the unique commands associated with the vertical tabs circuits.

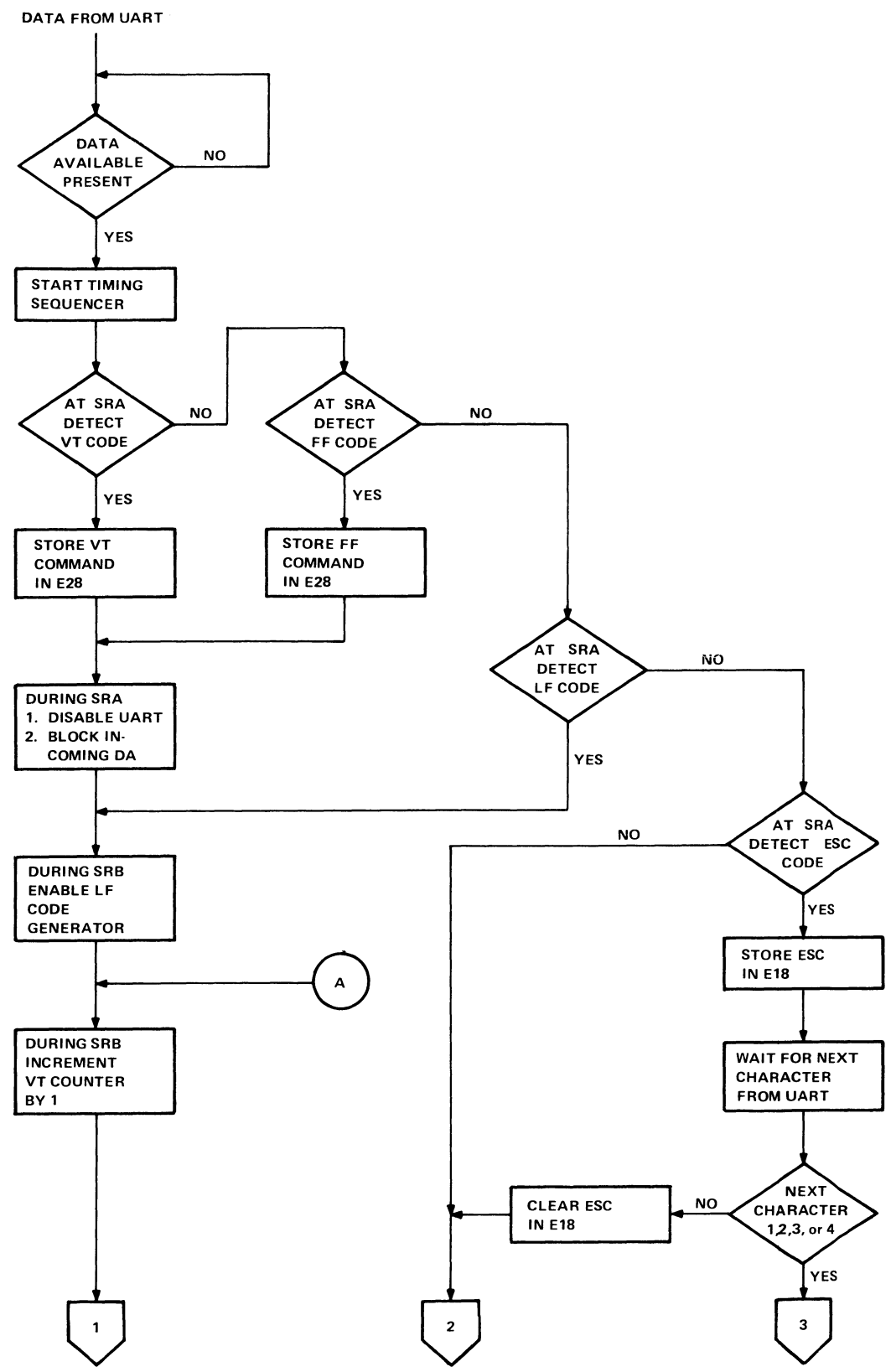
14.4.5.1 Monitoring – The following five incoming codes affect the function of the vertical tabs circuits:

1. Vertical Tab command – \overline{VT} at pin 4 of E28
2. Form Feed command – \overline{FF} at pin 10 of E28
3. Line Feed code – \overline{LF} at pin 1 of E21
4. Set HT command – ESC3 at pin 12 of E6
5. Clear HT command – ESC4 at pin 2 of E17 and at pin 3 of E18



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Figure 14-9 Vertical Tabs Circuits
Basic Block Diagram



CP-2358A

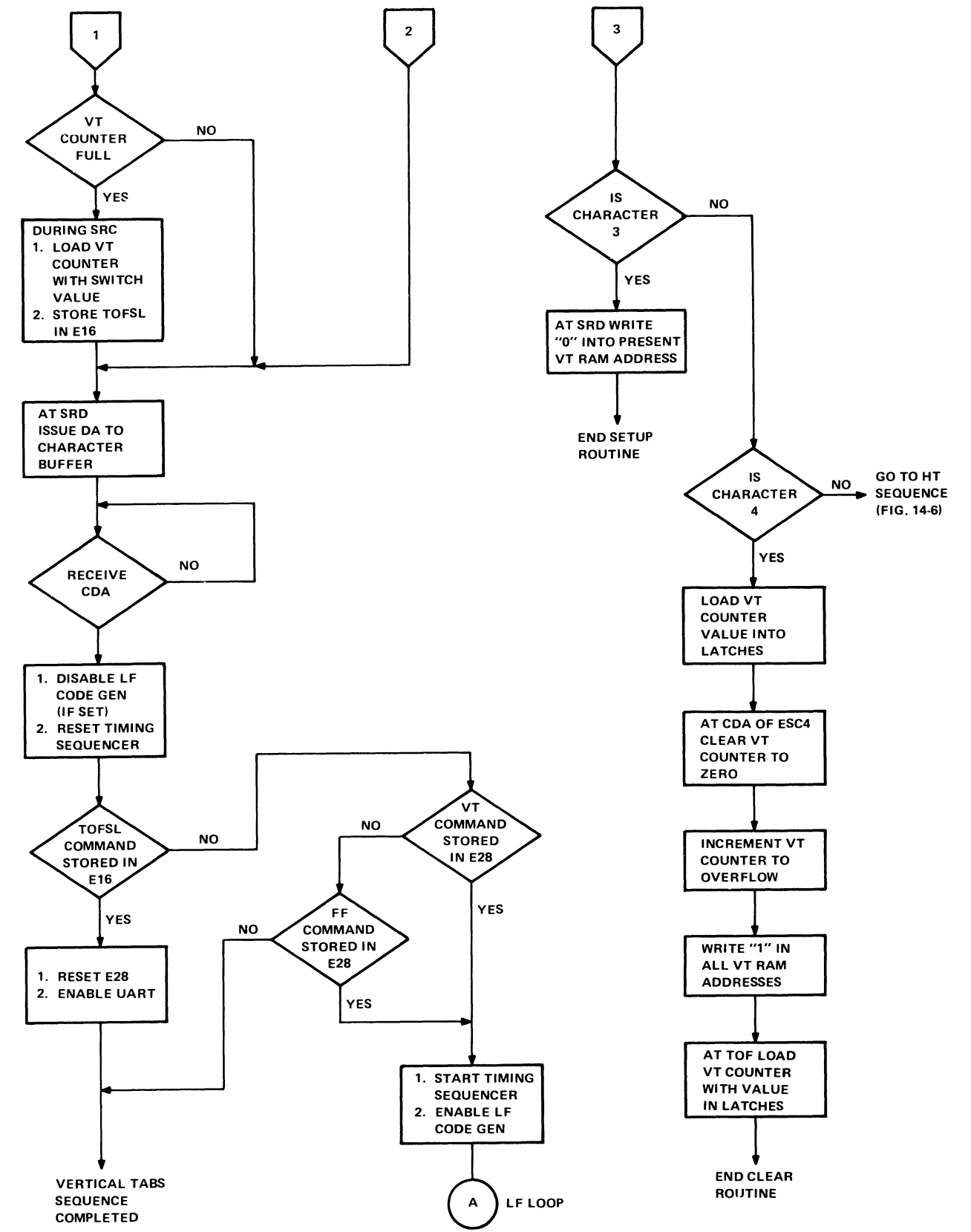
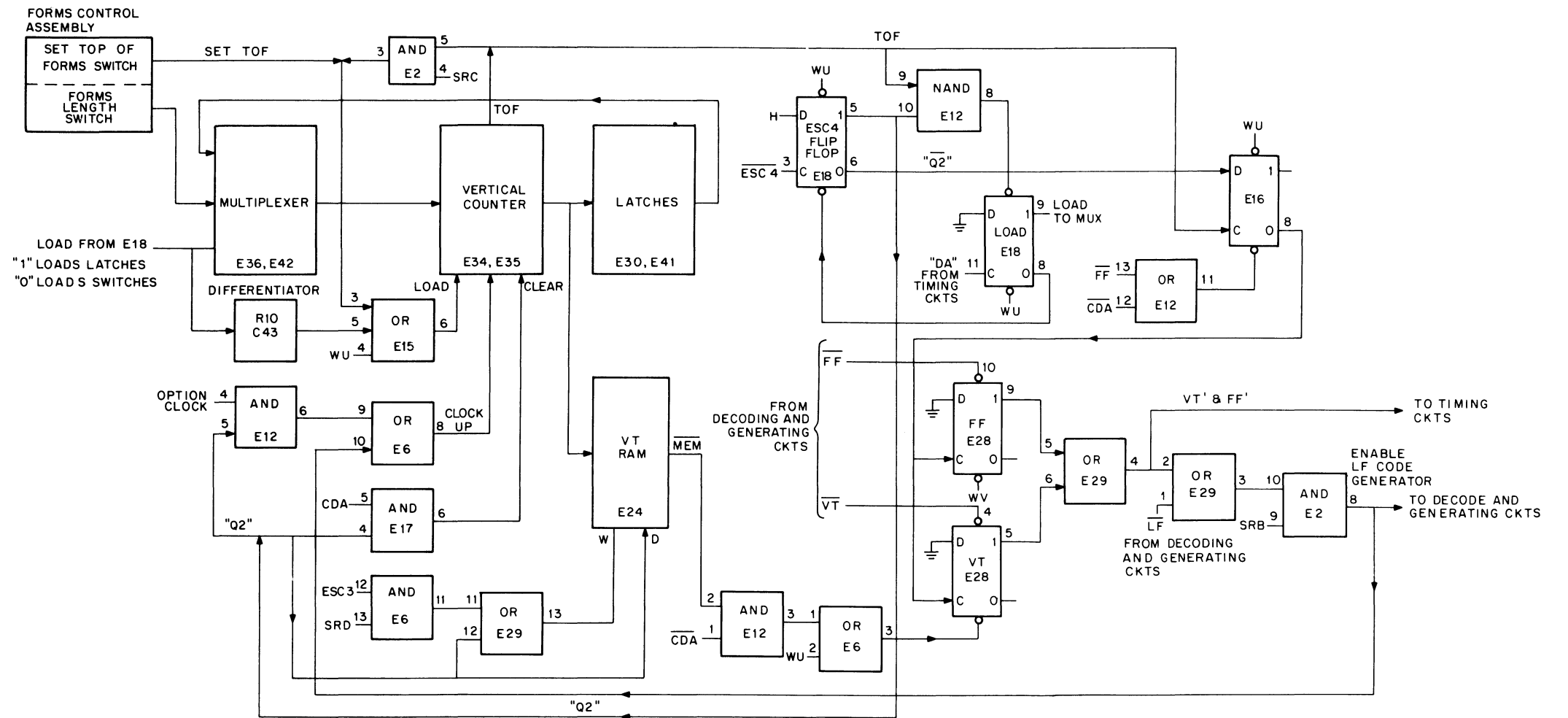


Figure 14-10 Vertical Tabs Circuits Operational Sequence

CP-2358B



NOTE
 Shaded components common to
 both TOF and Vertical Tabs Circuits.

CP - 2359

Figure 14-11 Common Components of
 Vertical Tabs and TOF Circuits

The line feed code at E21 pin 1 causes the Vertical Counter to increment by one count at SRB time.

NOTE

The only function of a received line feed code is to increment the Vertical Counter. As in the TOF circuits, at SRB the Line Feed Code Generator is enabled and the UART is not disabled. Thus, the parallel LF code generation occurs at the input to the Character Buffer again.

14.4.5.2 Vertical Tab Setup – The ESC3 command establishes a vertical tab at the line location of the print head when the command is given. At SRD the ESC3 command enables the write input (pin 12) of the VT RAM. At this time there is a low level on the data input (pin 13) of the VT RAM and a 0 is written into the VT RAM location that is addressed by the Vertical Counter output. Whenever the ESC3 command is detected, a 0 is written into the VT RAM location corresponding to the print head position. A vertical tab can be set on any or all printable lines of a form.

14.4.5.3 Vertical Tab Action – A Vertical Tab command detected by the decoding circuits sets VT flip-flop E28. When E28 sets it causes the same action through E29 pin 5 as when the FF flip-flop sets. These actions are the same as in the TOF circuits.

1. UART is disabled through E1.
2. Data Available signal path is blocked through E15.
3. Vertical Counter is incremented by one count at SRB time.
4. Line Feed Code Generator E1, E10 is enabled at SRB time.

As the Vertical Counter increments, a new VT RAM address is accessed. If this new address contains a 1 (indicating that a vertical tab was set at this position), the MEM signal is present at pin 6 of the VT RAM. This MEM signal combines with the CDA signal associated with the line feed code that just incremented the Counter and resets VT flip-flop E28. Again, this resetting action enables the UART, clears the Data Available signal path, and removes the increment signal from the Vertical Counter.

If the MEM signal is not present at the VT RAM, the vertical tabs circuits increment the Counter at SRB, issue an LF code at SRD, and continue this paper advancing cycle until the next vertical tab position is reached (MEM signal out of VT RAM) or the top of form is reached (TOF signal out of Vertical Counter). If a TOF occurs during a vertical tab operation the same loading and resetting events take place as in a normal TOF function. These actions are:

1. The TOF signal out of Vertical Counter:
 - a. Clocks a high through E16 to clear E28 at CDA time.
 - b. Is not passed through NAND gate E12 pin 9 (the reset for LOAD flip-flop) because pin 10 is held low.
 - c. Loads the Vertical Counter with value of FORMS LENGTH switch at SRC time.
2. The switch setting is selected (not the latches) because the steering Multiplexer E36, E42 has a 0 on pin 1.

14.4.5.4 Clearing Vertical Tabs – Vertical tab locations are cleared (erased) by either of two events: receiving an ESC4 command or during-a power-up sequence (wake-up routine).

The negative-going ESC4 pulse generated by the decoding circuits is applied to E17 pin 2 and E18 pin 3. The leading edge through E17 enables the Latches E30, E41 and the current print head position value of the Vertical Counter is transferred into these latches. At the trailing edge of the ESC4 pulse E18 clocks a high level out on pin 5 (the Q2 signal). This Q2 signal initiates the following actions:

1. Vertical Counter clears to zero count at CDA (of the 4 in the ESC4 command) through E17 pin 6.
2. Vertical Counter increments up from zero at the rate of the Option Clock through E12 pin 6.
3. All VT RAM addresses written with 1s through E29 pin 13.

As E18 sets, the high level load signal on pin 9 is applied to the Multiplexer E36, E42. This load signal conditions the multiplexer to pass the data stored in the latches and load the Vertical Counter with this data.

NOTE

The value in the latches is the vertical position of the print head at the time the ESC4 command was given. Thus, this position is not lost as the counter is incremented to erase the VT RAM.

The low level on pin 8 of E18 is used to reset the ESC4 flip-flop E18. The DA signal associated with the next character received resets E18 at pin 11 to complete the vertical tab erasing action.

The clearing sequence performed when a wake-up occurs is somewhat similar to an ESC4 command and is as follows:

1. ESC4 flip-flop E18 sets and forces Q2 to a high level at the leading edge of the wake-up pulse.
2. At this time the load signal at E18 pin 9 is 0 and the Wake-Up signal transfers the FORMS LENGTH switch value through the multiplexer to load the Vertical Counter (WU at E15 pin 4) and then enables the latches (WU at E17 pin 1) to store this switch setting.
3. During this time the Option Clock cannot increment the Vertical Counter because the loading action overrides the clocking function.
4. At the trailing edge of the wake-up pulse the Vertical Counter starts incrementing through E12 at the Option Clock rate.
5. Each VT RAM address is written with a 1 because Q2 signal is still high on pin 13 of the VT RAM.
6. At TOF (Counter overflow) E18 sets, making the Load signal high and resetting the ESC4 flip-flop (Q2 is now low).
7. The high level Load signal causes the multiplexer to select the value stored in the latches and E15 pin 5 loads this value into the Vertical Counter.
8. DA signal from the next character received resets E18 and the wake-up clearing routine is completed.

After wake-up the vertical tabs circuits are cleared and are set with the value of the new form and consider the print head to be positioned at the top of this new form.

14.5 TROUBLESHOOTING

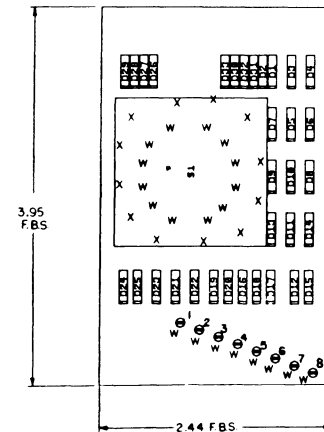
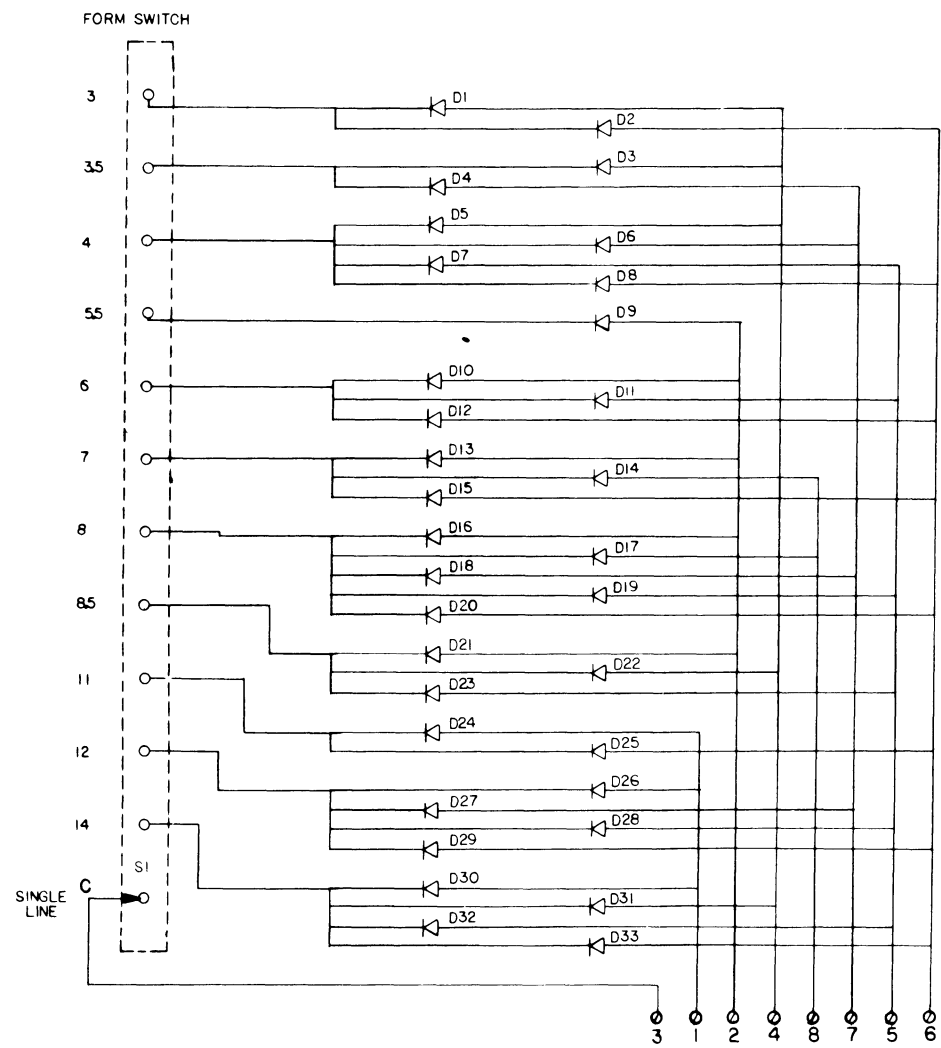
The troubleshooting chart in Table 14-4 lists the common trouble symptoms that could be observed during installation checkout or normal operation.

14.6 LAXX-KY PRINT SET

Figure 14-12 is the supporting diode matrix for the LAXX-KY print set. The print set is shown at the end of this chapter.

Table 14-4
Troubleshooting for VT, HT, and TOF Option (LAXX-KY)

Symptom	Problem Area	Probable Cause	Action	Reference
1. After installation, improper operation or no operation of terminal	Cabling	Wrong cabling connections	Check all cabling between M7728 Logic Board, Expander Board, and TOF Assembly beneath top cover	Figure 9-4
	Option location	Option inserted in wrong location on Expander Board	Install Tabs Option in locations A and B	
	Data Available signal distribution	Signal path interrupted	Check for Data Available signal in at E15 pin 13 and out at E19 pin 12	
2. Performs HT operations but VT and TOF operations not correct	LF Code Generator	LF code not being generated	Check E1 and E10 for LF code	D-CS-M7736-0-1, Sheet 3
	Vertical Counter	Vertical Counter not loading proper value	Check E34 and E35 for proper operation during load	D-CS-M7736-0-1, Sheet 2
	Set TOF assembly	Incorrect value being loaded	Check operation of SET TOP OF FORM switch and FORMS LENGTH switch	
3. Performs TOF and VT operations but not HT operations	Space code	Space code not being generated	Check E1 and E10 for the space code	D-CS-M7736-0-1, Sheet 3
	Horizontal Counter	Horizontal Counters not loading proper value	Check E32 and E38 for proper operation during load	D-CS-M7736-0-1, Sheet 5
4. Performs HT and TOF operations but not VT operations	LF code	LF Code Generator not energized	Check E28 pin 5 for a high level on VT command	D-CS-M7736-0-1, Sheet 2
	Vertical tabs circuits	VT tabs not being cleared by ESC 4	Check E18 pin 5 high at ESC 4	D-CS-M7736-0-1, Sheet 2
	Vertical tabs circuits		Check all circuitry not common with TOF circuits	Figure 14-11



Forms Control Board Pin Numbers

3	1	2	4	8	7	5	6
---	---	---	---	---	---	---	---

Single Line •	0	1	1	1	1	1	1	1
3.0 •	0	1	1	0	1	1	1	0
3.5 •	0	1	1	0	1	0	1	1
4.0 •	0	1	1	0	1	0	0	0
5.5 •	0	1	0	1	1	1	1	1
6.0 •	0	1	0	1	1	1	0	0
7.0 •	0	1	0	1	0	1	1	0
8.0 •	0	1	0	1	0	0	0	0
8.5 •	0	1	0	0	1	1	0	1
11.0 •	0	0	1	1	1	1	1	0
12.0 •	0	0	1	1	1	0	0	0
14.0 •	0	0	1	0	1	1	0	0

MSB	8	7	6	5	4	3	2	1	LSB
-----	---	---	---	---	---	---	---	---	-----

J1 M7735
Sheet 3 of 3

J1 M7736
Sheet 2 of 5

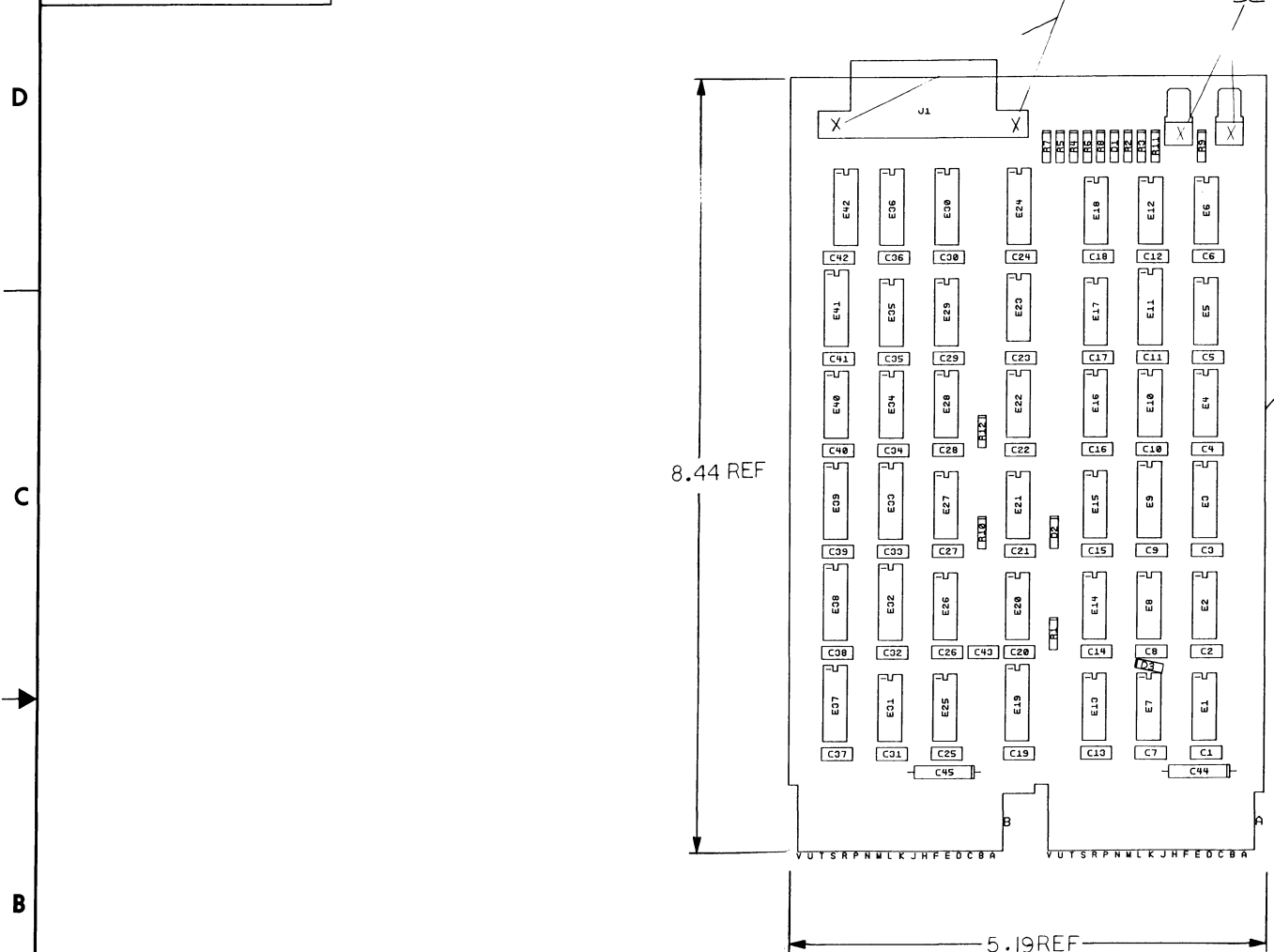
BINARY PATTERN/FORMS LENGTH SELECTED

Figure 14-12 LAXX-KY Diode Matrix

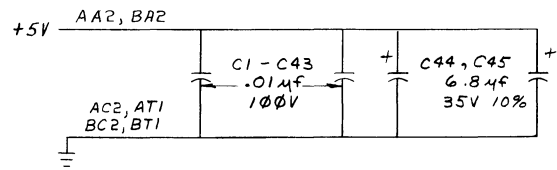
8 7 6 5 4 3 2 1

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NOTES:



IC TYPE	QTY	REF. DESIGNATION
3106	8	16
74157	8	16
7442	8	16
74193	8	16
8271	8	16
7475	12	5
7473	11	4
GND		+5V



REF	DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
		ASSY/DRILLING HOLE LAYOUT	D-AH-M7736-0-5	1
		MODULE ECO HISTORY	B-MH-M7736-0-6	2
1		ETCHED CIRCUIT BOARD	5011716	3
43	C1 - C43	CAP .01µF 100V DISC	1001610-01	4
2	C44, C45	CAP 6.8µF 35V 10%	1005306-00	5
3	D1, D2, D3	DIODE D664	1100114-00	6
3	R1 - R8, R11	RES. 3K 1/4W 5% CC	1300432-00	7
2	R9, R12	RES. 1K 1/4W 5% CC	1300365-00	8
1	R10	RES. 270 1/4W 5% CC	1301972-00	9
1	J1	CONN. MATE'N LOK 8PIN	1209340-00	10
8		PINS MATE'N LOK	1209456-01	11
2	J2, J3	FASTON TAB	9007112-00	12
1	E1	IC 7405	1909930-00	13
5	E2, E12, E17, E21, E22	IC 7400	1905575-00	14
2	E3, E9	IC 7442	1910046-00	15
3	E4, E14, E27	IC 7432	1911521-00	16
3	E5, E13, E20	IC 7404	1909686-00	17
3	E6, E23, E31	IC 7408	1910155-00	18
1	E7	IC 7430	1905578-00	19
5	E8, E16, E18, E25, E28	IC 7474	1905547-00	20
1	E10	IC 8003	1910837-00	21
2	E11, E19	IC 8071	1909615-00	22
1	E15	IC 7427	1910878-00	23
2	E24, E39	IC 3106	1910818-02	24
1	E26	IC 7410	1905576-00	25
1	E29	IC 7402	1909004-00	26
4	E30, E33, E37, E41	IC 7475	1909050-00	27
2	E32, E38	IC 74193	1910018-00	28
2	E34, E35	IC 74197	1910035-00	29
2	E36, E42	IC 74157	1910655-00	30
1	E40	IC 7473	1905587-00	31
2		EYELET	9009000-00	32
2		EYELET	9006732-00	33
2		WASHER FIBER FLAT 3/8 O.D.	9006693-00	34

DEC FORM NO. 190 130-A

SEMICONDUCTOR CONVERSION CHART

DEC. NO.	EIA NO.	DEC. NO.	EIA NO.

REVISIONS

CHK	CHANGE NO.	REV.

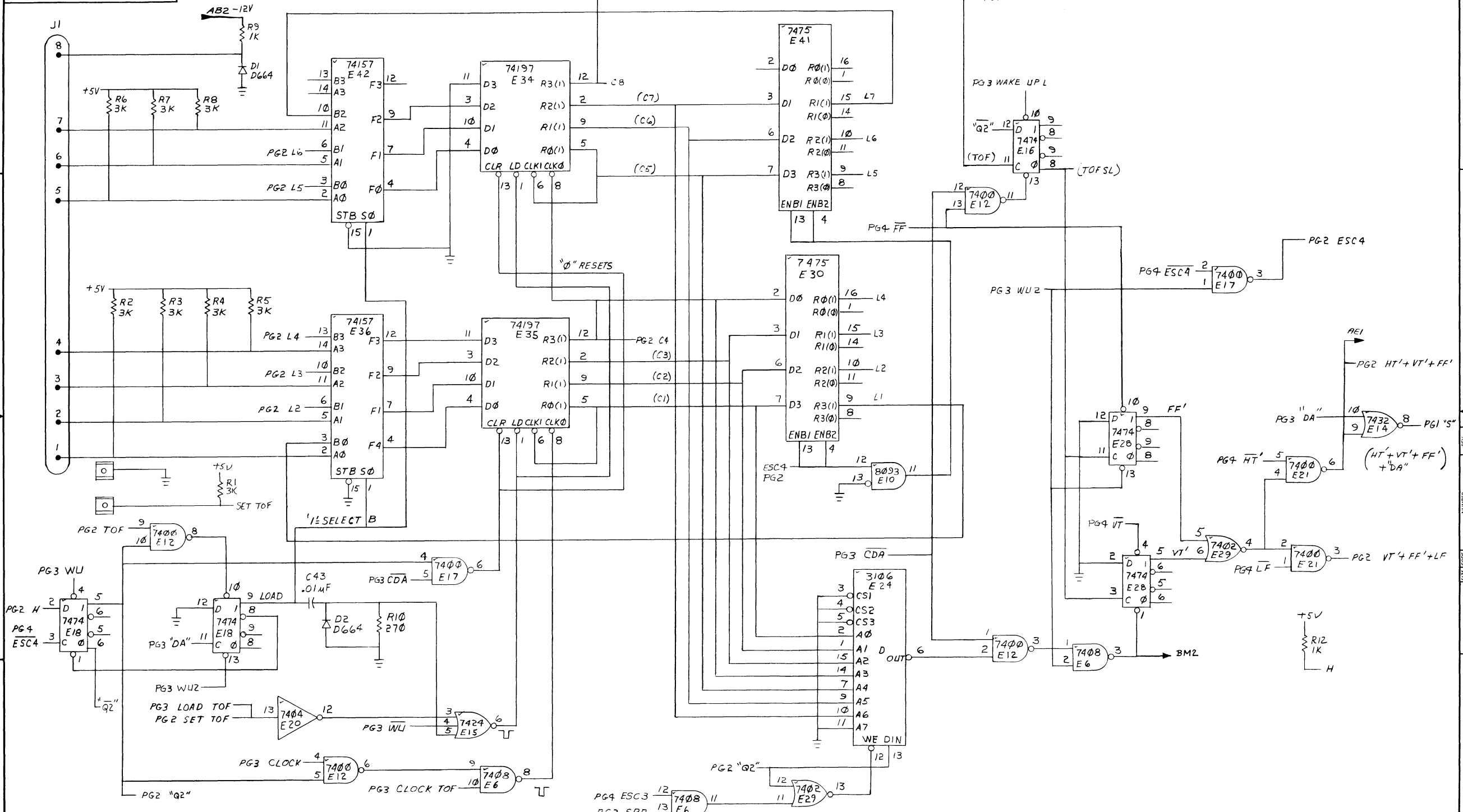
DRN. Silvia DATE 7-8-75
 CHK'D. DATE 7-16-75
 ENGR. DATE 8-25-75
 PROJ. ENGR. DATE 8-18-75
 PROD. DATE 8-23-75

digital
 HT VT TOF OPTION

SCALE: 1 OF 5 SHEET

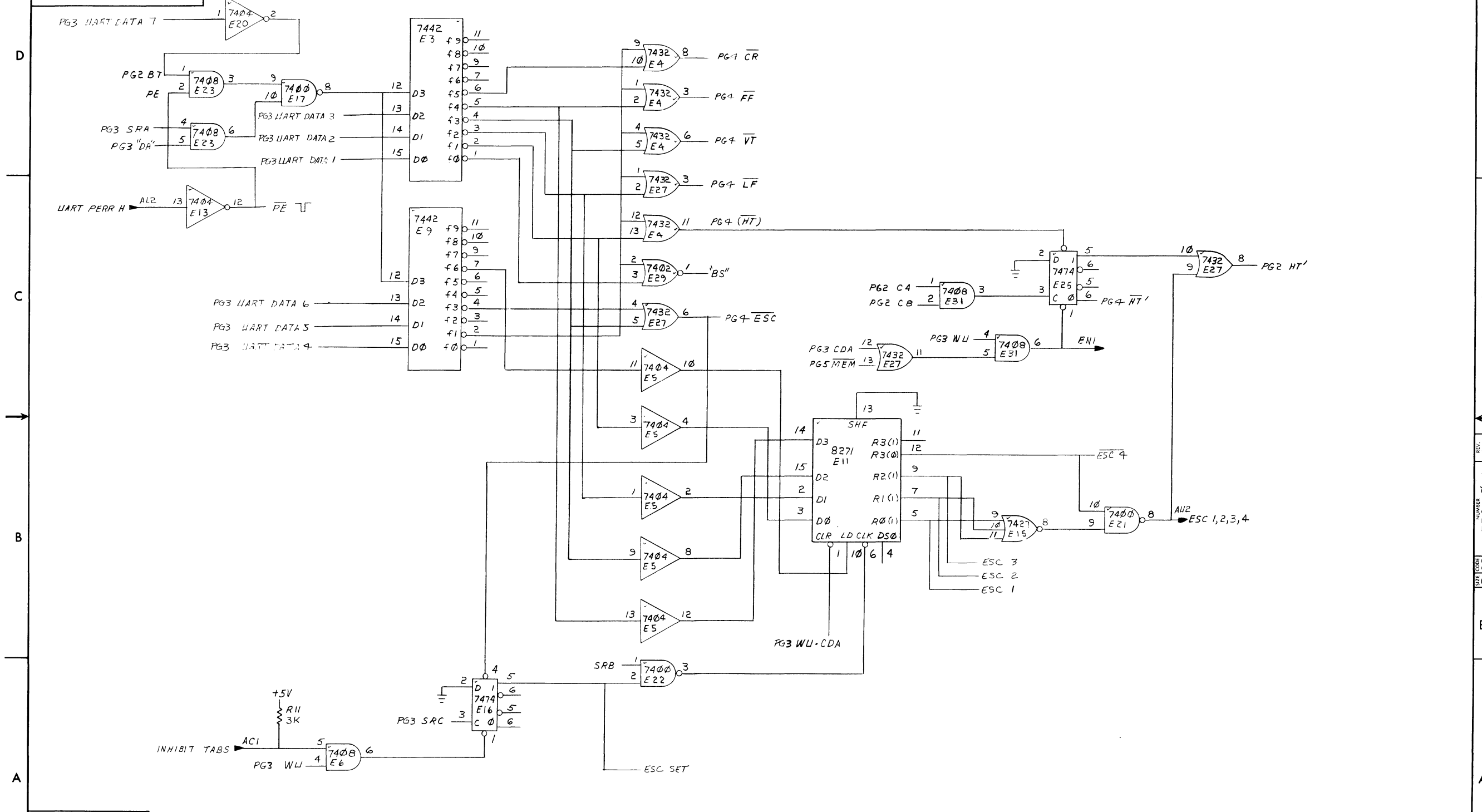
SIZE CODE: DCSM7736-0-1 NUMBER: B

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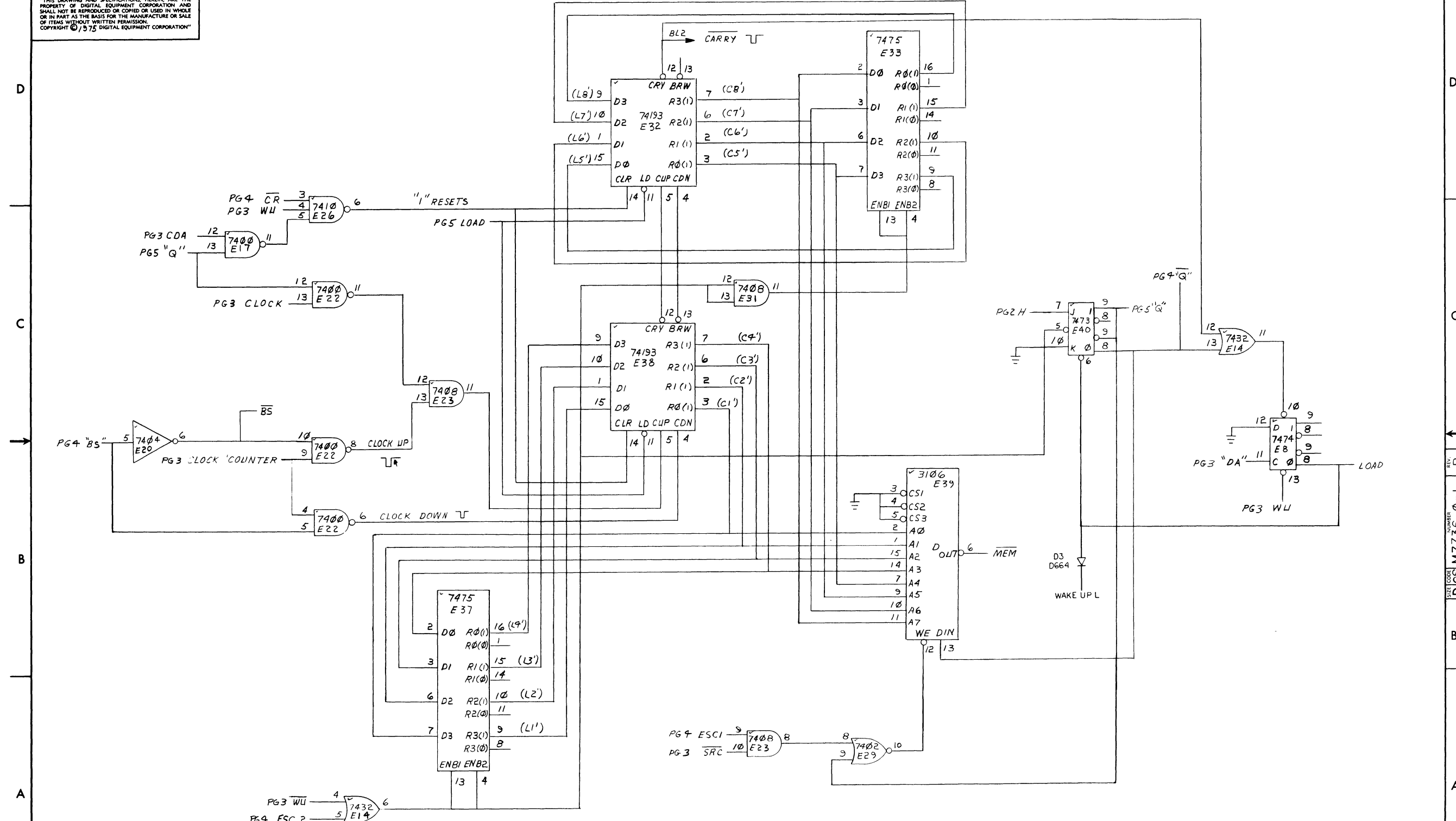
REVISIONS		
CHK	CHANGE NO.	REV.

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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	HT-VT-TOF OPTION	SIZE CODE	D CS	NUMBER	M7736-0-1	REV.	B
SCALE	+-	SHEET	5 OF 5	DIST.			

CHAPTER 15

AUTOMATIC LINE FEED OPTION (LAXX-LA)

15.1 AUTOMATIC LINE FEED INTRODUCTION

The function of the Automatic Line Feed Option is to insert a line feed code after receiving or transmitting a Carriage Return command.

In the transmit mode of operation, this feature eliminates having to type the keyboard LINE FEED key after each Carriage Return command at the end of each line. With this option installed and the front panel AUTO LF switch depressed, typing the CARRIAGE RETURN key causes a line feed code to be transmitted after the carriage return code.

In the receive mode of operation, an incoming carriage return code is detected by this option and it automatically inserts a line feed code after the carriage return code. This is a convenience feature for existing programs that do not normally follow a carriage return code with a line feed code. A wire jumper (W1) located on the automatic line feed option circuit board permits the automatic insertion of a line feed code after a received carriage return code. Removing this jumper disables the automatic insertion of line feed codes when operating in the receive mode but does not affect the transmit mode, which is controlled by the AUTO LF switch.

15.2 AUTOMATIC LINE FEED FUNCTIONAL BLOCK DIAGRAM

Figure 15-1 shows the functional block diagram of the Automatic Line Feed Option in a typical installation. Incoming data (SI) is processed by the UART on the M7728 Logic Board then routed through the Expander Option Mounting Board to the Receiver Section of the Automatic Line Feed Option Board. This section of the option monitors each incoming character and, after receiving a carriage return code, generates a line feed code. This line feed code is inserted right after the carriage return code and is sent back to the Character Buffer on the bidirectional line. The Character Buffer accepts both the carriage return and the line feed codes as if they were sent into the terminal from an external source. The printer mechanism reacts to this internally generated Line Feed command in a normal manner.

In the transmit mode of operation, characters typed at the keyboard pass through J3 on the Expander Option Mounting Board to the Transmit Section of the option. When the CARRIAGE RETURN key is depressed, the option detects the carriage return code and inserts an option-generated line feed code after the carriage return code. The carriage return from the keyboard and the line feed from the option are routed to the UART on the M7728 Logic Board. The UART processes and transmits these two codes just as if both were originally generated by two separate keys.

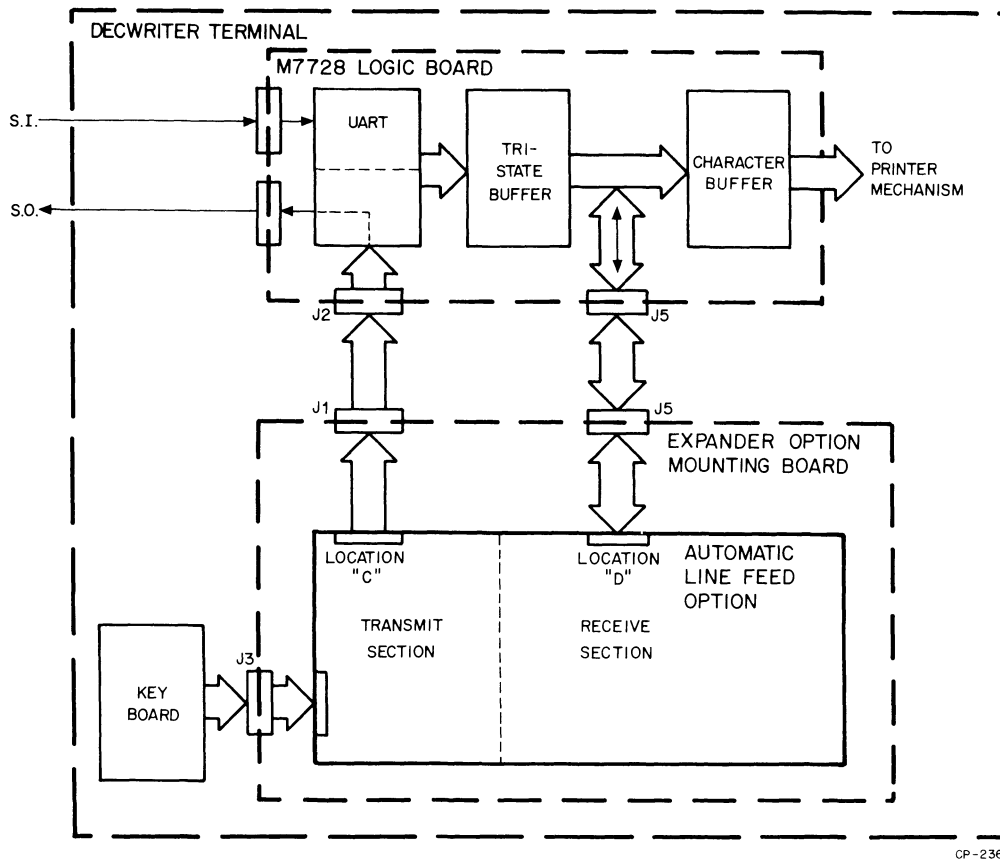


Figure 15-1 Automatic Line Feed Functional Diagram

If the terminal is operated in the local mode, with the front panel AUTO LF switch depressed and Jumper W1 inserted on the option circuit board, a carriage return code from the keyboard causes a carriage return and two line feed increments at the printer mechanism. This action occurs because the Transmit Section of the option adds a line feed code after the carriage return from the keyboard then the Receive Section of the option inserts another line feed code as the carriage return code leaves the UART for the Character Buffer. Thus, two line feed codes are acted on by the printer mechanism.

NOTE

When the terminal is on-line and transmitting in an echo mode and if the AUTO LF switch is in the down position, the option generates a line feed code after each carriage return. In this operational configuration, the printer mechanism advances two lines for each carriage return, even though only one line feed code is being transmitted out from the terminal. The second line feed occurring at the terminal is generated by the returning (echoing) carriage return as it is processed by the Receiver Section of the option.

15.3 AUTOMATIC LINE FEED BASIC BLOCK DIAGRAM

The basic block diagram for the Automatic Line Feed Option is shown in Figure 15-2. This diagram is a simplified representation of the automatic line feed circuit schematic (D-CS-M7738-0-1). Circuit designations and pin numbers indicated on Figure 15-2 correlate with corresponding components on the schematic. Buffers, inverters, and other components that do not have major operational functions are omitted from the block diagram.

The Automatic Line Feed Option can be divided into two functional areas: Transmit Section and Receive Section.

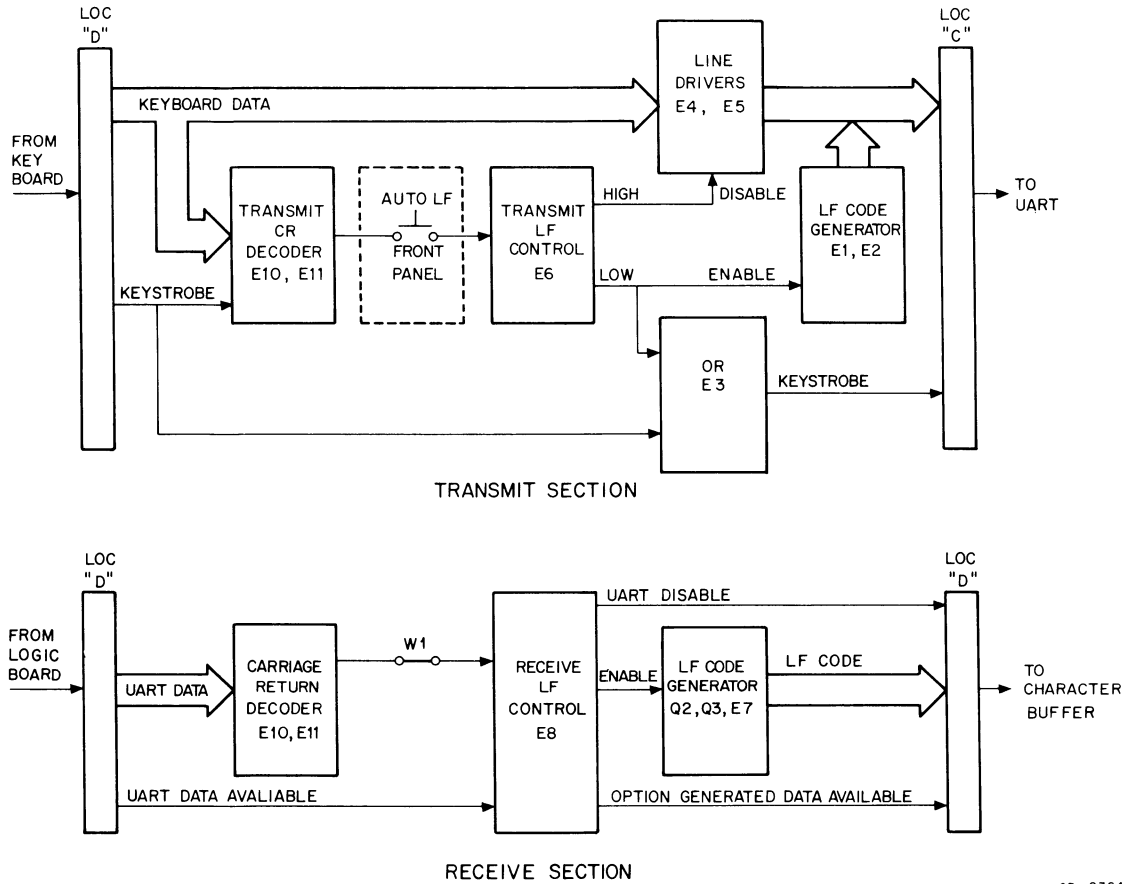
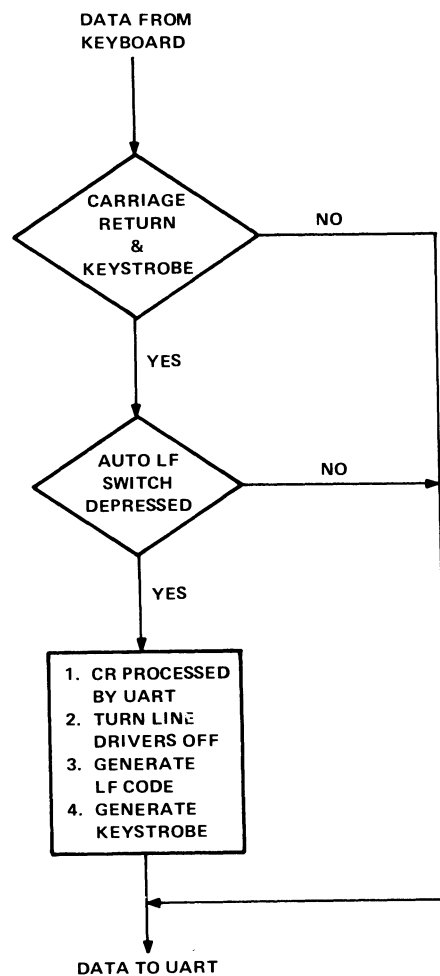


Figure 15-2 Automatic Line Feed Block Diagram

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15.3.1 Transmit Section

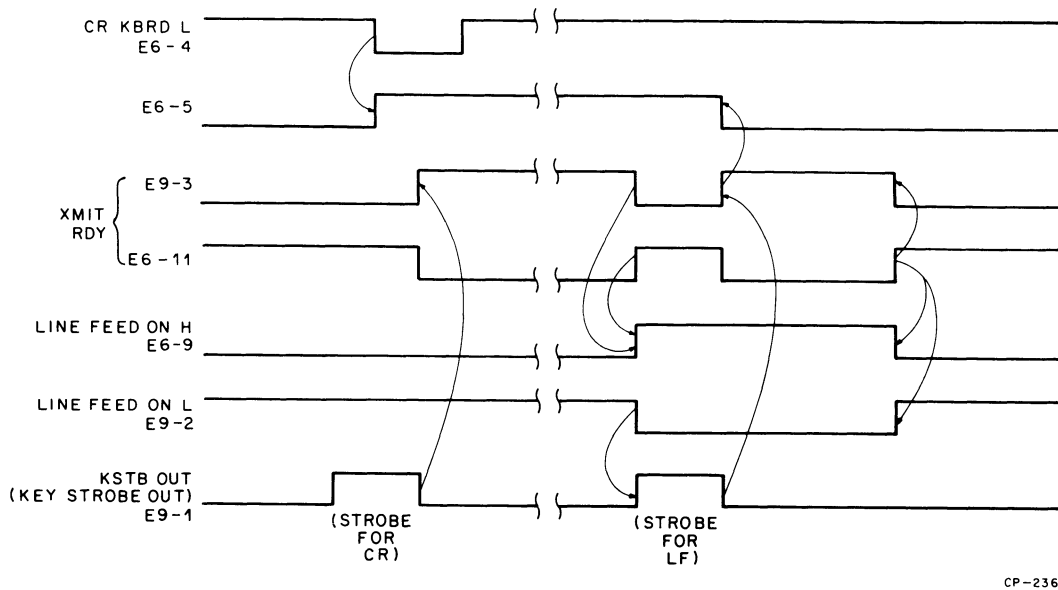
Figure 15-3 shows the operational sequence of the Transmit Section. The Transmit Section accepts keyboard characters and their associated keystrokes from the Expander Option Mounting Board through an edge connector at location D. If the front panel AUTO LF switch is not depressed, each keyboard character is passed through Line Drivers E4 and E5 then out through location C to the UART on the M7728 Logic Board. The corresponding keystroke for each character is also passed through without any action being taken by the option. Transmit Carriage Return Decoders E10 and E11 monitors these characters from the keyboard and when a carriage return is detected and the front panel AUTO LF switch is depressed, the CR KBRD L signal is generated. This signal is applied to Transmit LF Control E6 where it initiates the line feed code insertion sequence after the carriage return code is sent out. First the Line Drivers E4 and E5 are disabled (preventing data from the keyboard from being passed to the UART), then the LF Code Generator E1 and E2 is allowed to place a line feed code on the outgoing line to the UART. At the same time the Transmit LF Control generates the KSTB OUT signal which is interpreted by the UART as a valid keystroke command. After the UART accepts the line feed code, the XMIT RDY L signal resets the Transmit LF Control which removes the disable condition from the Line Drivers and allows keyboard data to pass through the option again.



CP-2365

Figure 15-3 Operational Sequence for Automatic Line Feed Transmit Section

The timing sequence for the Transmit LF Control E6 is shown in Figure 15-4. When a carriage return code from the keyboard is detected, the CR KBRD L signal at E6-4 sets the first flip-flop and causes E6-5 to go high. During this time the carriage return code is passed through the option to the UART. The XMIT RDY L signal at E12-1 is held high by the UART, indicating that the carriage return is being processed and that the UART is not ready to accept another character. When the UART is ready for another character, the XMIT RDY L signal at E12-1 goes low indicating that the UART has accepted the CR. This low level is inverted by E12 and then applied to the clock input of E6-11. When clocked, a high level (LINE FEED ON H) is present at E6-9 and a low level (LINE FEED ON L) is present at E6-8. The low level performs two functions: (1) enables the LF Code Generator E1 and E2 which places a line feed code on the output lines to the UART, and (2) combines at E9 with the XMIT RDY L signal to produce the KSTB OUT pulse and simultaneously resets E6 at pin 3. The high level at E6-9 disables the Line Drivers E4 and E5 which prevents data from the keyboard from passing through the option. As the option-generated line feed code and keystrobe are processed by the UART, the XMIT RDY L signal clears flip-flop E6 (pin 11) in the LF Transmit Control. Thus, the LF Code Generator is disabled and the Line Drivers are enabled again, allowing keyboard data to pass through the option.



CP-2366

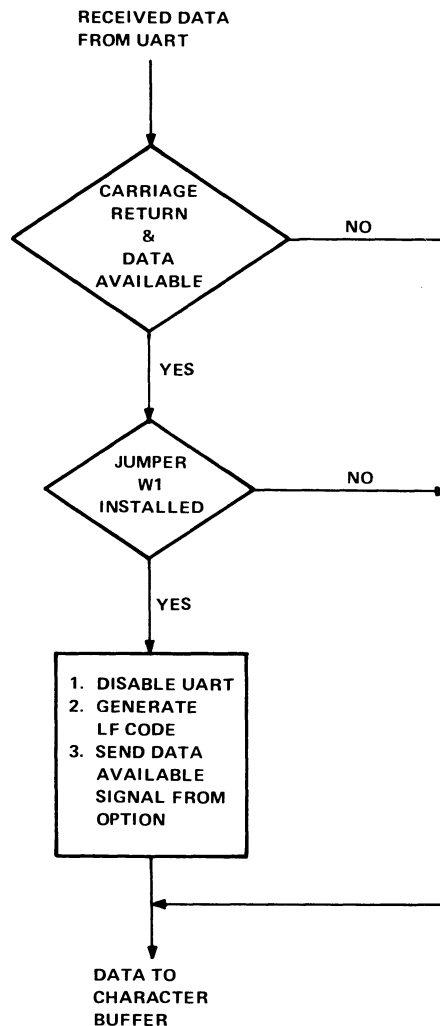
Figure 15-4 Transmit Line Feed Control Timing Sequence

15.3.2 Receive Section

Figure 15-5 shows the operational sequence for the Receive Section of the Automatic Line Feed Option. The Receive Section monitors the received data at a point that is between the output of the UART and the input to the Character Buffer. This data is present at the option on the bidirectional line through the edge connector at location D. Receiving both a carriage return code and the signal UART DA L (Data Available signal from the UART) at the Receive Carriage Return Detector E10 and E11 produces an output signal that is applied to the Receive LF Control E8, if Jumper W1 is installed. The Receive LF Control initiates three actions:

1. Disables the UART
2. Enables the LF Code Generator Q2, Q3, and E7
3. Issues an option-generated data available signal

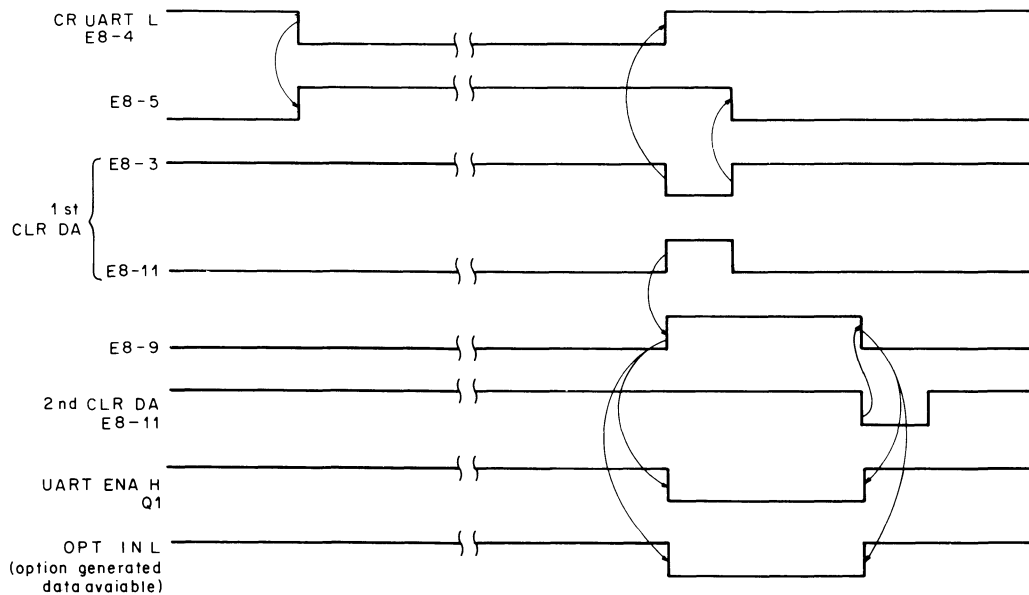
Disabling the UART prevents it from sending data to the Character Buffer while the option is issuing a line feed code. The LF Code Generator places a line feed code on the bidirectional line to the Character Buffer. The option-generated Data Available signal is interpreted just the same as a UART-generated data available and the Character Buffer accepts the option-generated line feed code as if it was received by the terminal. After the line feed code is processed, the CLR DA signal from the microprocessor in the terminal returns the option to the monitoring condition and it waits for another carriage return code.



CP-2367

Figure 15-5 Operational Sequence for Automatic Line Feed Receive Section

The timing sequence for the Receive LF Control E8 is shown in Figure 15-6. A decoded carriage return generates the CR UART L signal which is passed through Jumper W1 to E8-4. This signal sets E8, placing a high level on both E8-5 and E8-12. After the carriage return code is processed by the terminal, the microprocessor sends the CLR DA L signal back to the option at inverter E12-9. The leading edge of this signal clocks the high level on E8-12 through to E8-9 and forces E8-8 to a low level. The trailing edge resets E8 at pin 3. The high on the base of Q1 forces the signal UART ENA H to disable the UART. The high/low outputs of E8 that are applied to the LF Code Generator Q2, Q3, and E7 produce a line feed code. The option-generated data available signal is represented by the low level of the OPT IN L signal. (The steering gates on the Expander Option Mounting Board convert this OPT IN L signal to a signal that has the same affect as the Option Data Available signal.) After the microprocessor accepts the option-generated line feed code and data available, it sends a second CLR DA L signal back to the option. This resets flip-flop E8 at pin 11 which, then allows the UART to pass received data to the Character Buffer in a normal manner.



CP-2368

Figure 15-6 Receive Line Feed Control Timing Sequence

15.4 TROUBLESHOOTING

The troubleshooting chart in Table 15-1 lists the common trouble symptoms that could be observed during installation checkout or normal operation.

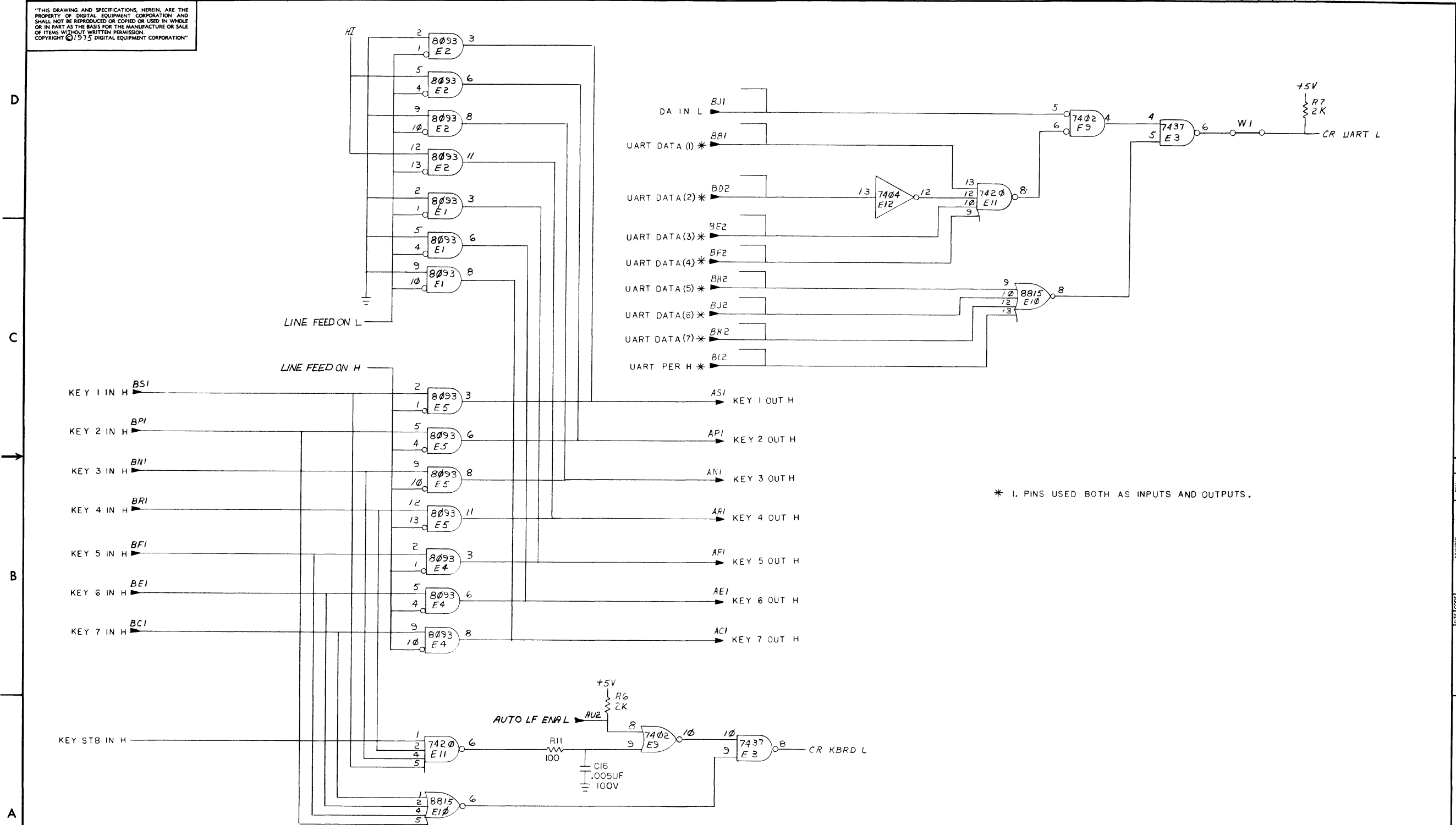
15.5 LAXX-LA PRINT SET

The figures at the end of this chapter are the LAXX-LA print set.

Table 15-1
Troubleshooting for Automatic Line Feed Option (LAXX-LA)

Symptom	Problem Area	Probable Cause	Action	Reference
1. After installation, characters typed on keyboard not transmitted	Cabling	Wrong cabling connections	Check all cabling between M7728 Logic Board and Expander Board	Figure 9-4
	Option location	Option inserted in wrong location on Expander Board	Install Line Feed Option in locations C and D	
	Keystrobe signal distribution	Signal path interrupted	Check for Keystrobe signal into Option Board at E12 pin 11 and out of board at E3 pin 3	D-CS-M7738-0-1, Sheet 3
	Line Drivers	Line Drivers on option not enabled	Check E6 pin 9 for low level	D-CS-M7738-0-1, Sheet 3
2. After installation, received characters not printing	Data Available signal distribution	Signal path interrupted	Check for Data Available signal at E9 pin 5	D-CS-M7738-0-1, Sheet 2
	Tri-State Buffer on M7728 Logic Board	Tri-State Buffer held disabled by option	Check collector of Q1 for high level	D-CS-M7738-0-1, Sheet 3
3. Line feed code not inserted after carriage return typed	AUTO LF switch	AUTO LF switch not depressed	Depress switch – if depressed and still no LF code, replace switch	
	Keystrobe signal	Signal not being generated by option	Check E3 pin 3 for Keystrobe signal associated with line feed code	D-CS-M7738-0-1, Sheet 3
	Line Feed Code Generator	Line feed code not being generated	Check for line feed code at E1, E2	D-CS-M7738-0-1, Sheet 2
4. Line feed code not inserted after received carriage return	Jumper W1	W1 not installed	Connect W1	D-CS-M7738-0-1, Sheet 2
	Data Available signal	Option not generating Data Available signal	Check for pulse at E8 pin 8	D-CS-M7738-0-1, Sheet 3
	Line Feed Code Generator	Line feed code not being generated	Check for line feed code at E7	D-CS-M7732-0-1, Sheet 3

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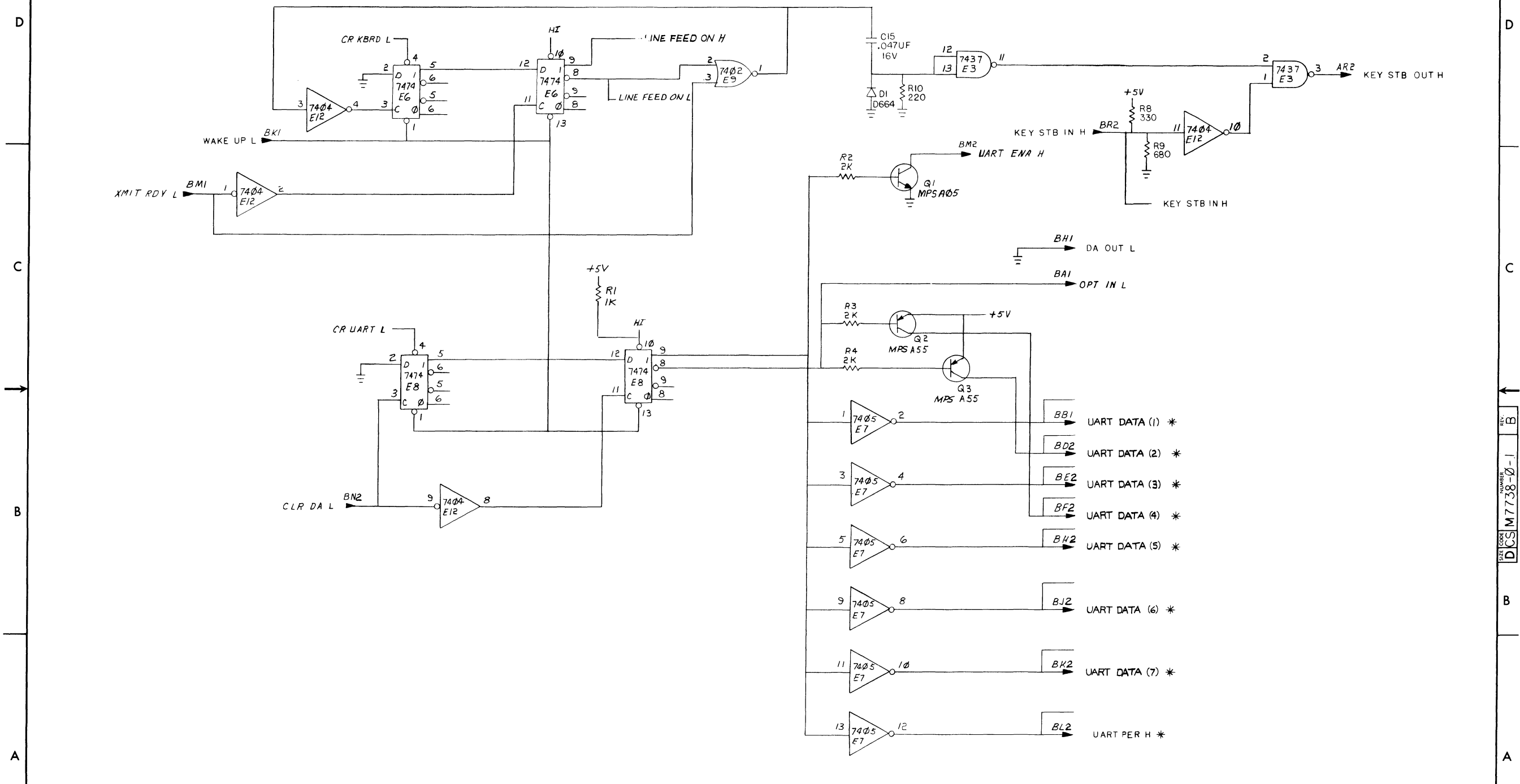


* 1. PINS USED BOTH AS INPUTS AND OUTPUTS.

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	AUTO LINEFEED OPTION FOR LA36	SIZE CODE	D CS	NUMBER	M7738-0-1	REV.	B
SCALE	---	SHEET	2	OF	3	DIST.	

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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE AUTOC LINEFEED OPTION FOR LA36
 SCALE 1:1 SHEET 3 OF 3
 SIZE CODE DCS NUMBER M7738-0-1 REV. B

CHAPTER 16

EXPANDER OPTION MOUNTING KIT (LAXX-LB)

16.1 EXPANDER OPTION MOUNTING KIT INTRODUCTION

The Expander Option Mounting Kit provides an interface between an upgradable DECwriter and various options that enhance the printer's operation. The Expander Option is a printed circuit board that functions as a motherboard for the following options:

1. APL/ASCII Dual Character Set LAXX-PK
2. Selective Addressing LAXX-KW
3. Automatic Answerback LAXX-KX
4. Automatic Line Feed LAXX-LA
5. Forms Control LAXX-KV
6. VT, HT, and TOF LAXX-KY

These options install on top of the Expander Board and connect to the Expander through type H851 Edge Connectors. There are six locations on the Expander Board for edge connectors.

NOTE

Even though there are six locations and six options, it is not physically possible to have all options installed at any one time. This is because some options are double width and occupy two locations. In addition, options are assigned to unique locations on the Expander Board and cannot be installed in any other location. The Answerback and Line Feed Options are assigned to the same locations (C and D) while the Forms Control and VT, HT, and TOF Options occupy locations A and B.

The Expander Board mounts on hinged rails above the M7728 Logic Board and can be lifted to provide access to the Logic Board. The options installed do not have to be removed when the Expander Board is raised.

16.2 EXPANDER BOARD DATA DISTRIBUTION

ASCII-coded characters and option commands are applied to and from the Logic Board through ribbon cables that connect to the connectors on the Expander Board. Figure 16-1 shows the data distribution paths on the Expander Board. Received serial data into the terminal is converted to parallel data by the UART, routed onto the Expander Board through J5, and applied simultaneously to locations A, B, D, and E. The parallel data applied back to the UART from the options is also routed through J5. The path between J5 and locations A, B, D, and E is bidirectional, while there are separate paths to and from J5 and location F. The bidirectional line through J5 intersects the data path between the Tri-State Buffer and the Character Buffer on the Logic Board. This allows the options to sample the incoming characters before they are processed by the terminal. Separate data paths are connected to location F. The input to location F is from the output of the Character Buffer and the output from F is applied back through J5 to the Print Head Drivers. This routing permits an optional character set option installed in location F to substitute incoming characters with characters from the alternate set.

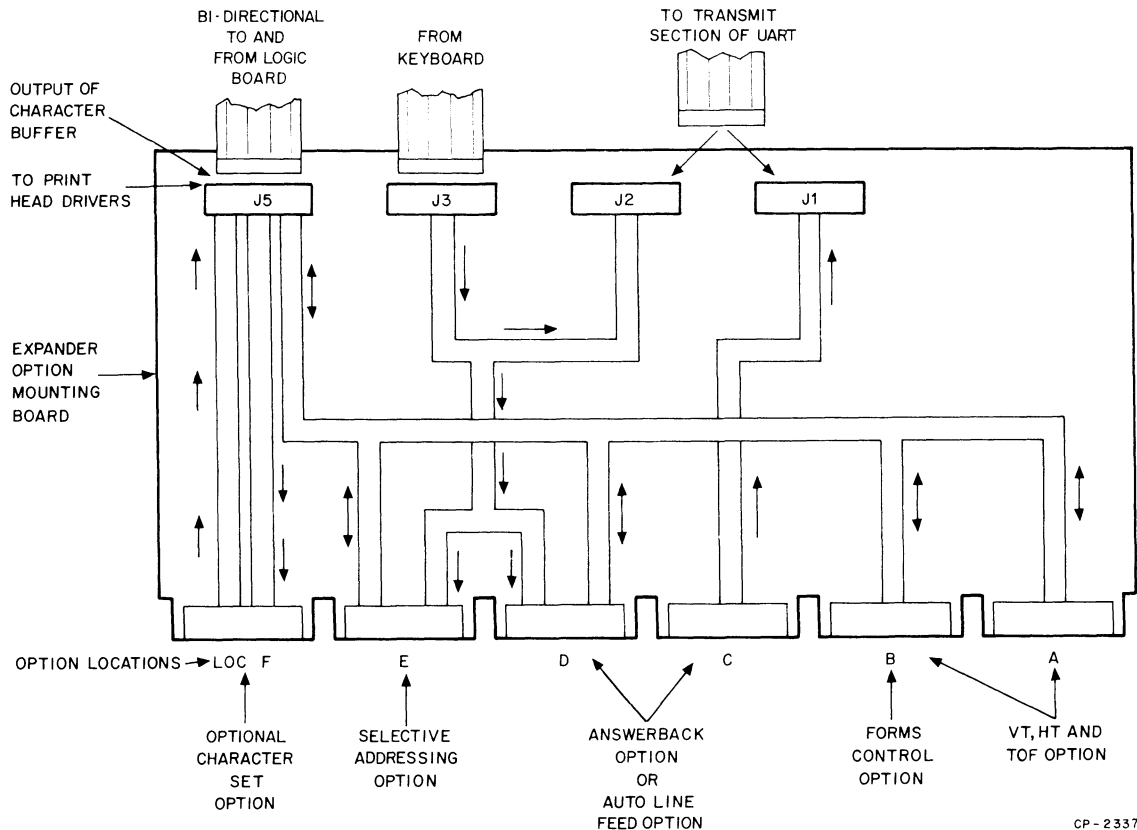


Figure 16-1 ASCII Data Distribution on Expander Board

Transmitted characters from the keyboard are connected to the Expander Board at J3 and are routed directly across the board to exit out J2. All typed characters are presented at location E for monitoring by the option. If either the Answerback or Line Feed Options are installed, no cable is connected to J2. Therefore, the data path is now: in through J3, through location D into the option, out of the option through location C, and out to the Logic Board through J1. This routing places either of the two options in series with the keyboard characters and allows them to insert data (answerback messages or carriage return codes) into the transmitted output.

16.3 EXPANDER BOARD CONTROL SIGNAL DISTRIBUTION

In addition to distributing ASCII data, the Expander also routes the control signals to the options. The two control signals are the Data Available signal associated with each received character and the Keystroke signal sent with each typed character.

16.3.1 Routing of DATA AVAILABLE Signal

The Data Available signal is issued by the Receive Section of the UART after a serial character is converted to parallel and is ready to be transferred to the Character Buffer. This character is applied to all options in parallel (Figure 16-1) but the Data Available signal for the character is applied to the options sequentially. This method of distribution is commonly called a daisy chain. The Data Available signal distribution is shown in Figure 16-2.

The Data Available signal enters the Expander Board through J5 and is routed, in order, to locations E, D, A, and B. If there is an option installed at a location, the Steering Gates for that location diverts the Data Available signal into the option. If no option, these gates direct the signal on to the next location.

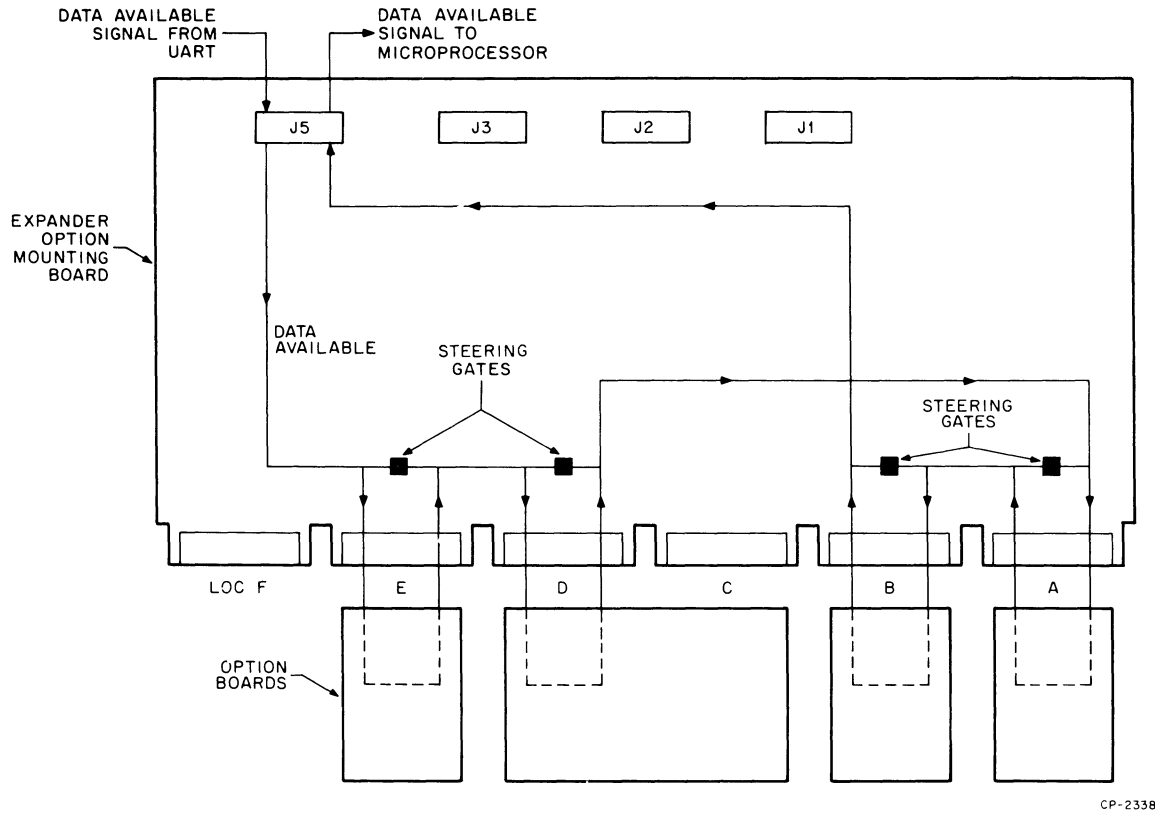
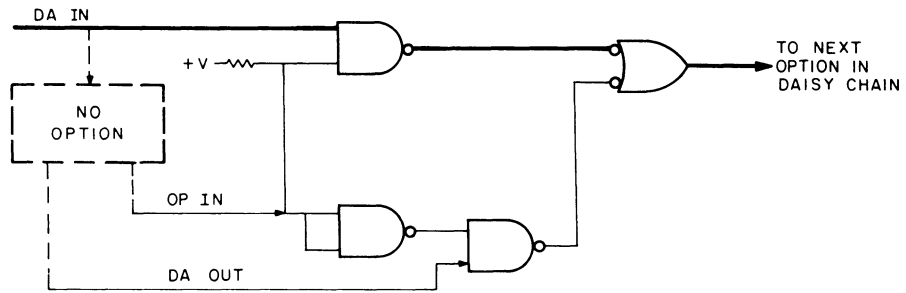


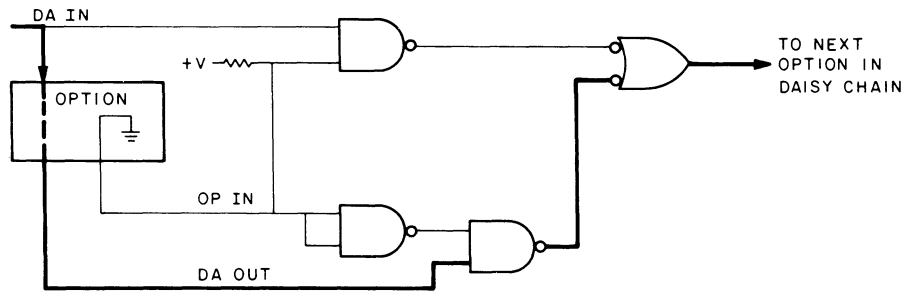
Figure 16-2 Data Available Signal Distribution on Expander Board

There are two methods employed by these Steering Gates to divert the Data Available signal. These methods are shown in Figure 16-3. Method No. 1 is used at locations A and E and utilizes the OP IN signal as the control signal. With no option installed, the Data Available signal is coupled right past this location to the next location in the daisy chain. Installing an option grounds the OP IN signal causes the Data Available signal to be diverted into the option. The option delays the Data Available signal long enough to establish whether the ASCII code contains a command recognizable for that particular option. The Data Available signal exits from the option on the DA OUT line and is applied to the next option in the chain.

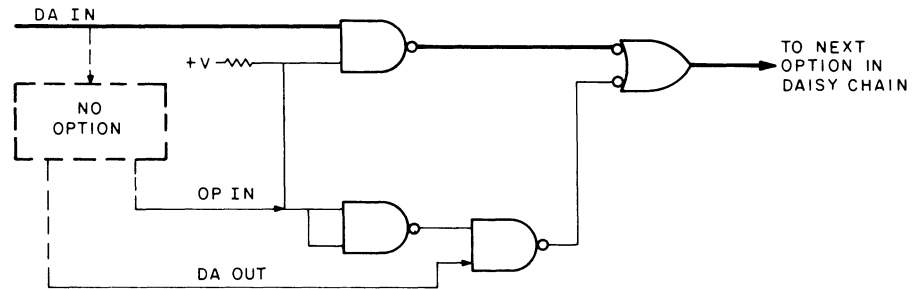
In Method No. 2 (used at location B), the Data Available signal passes right through the Steering Gates when no options are installed. Installing an option in either of these locations grounds the DA OUT line (rather than the OP IN line as in Method No. 1). The OP IN line of Method No. 2 is held high until the option has generated the ASCII character it is inserting into the transmit data, then the OP IN line pulses low. This pulse is the option-generated Data Available signal that is applied to the next option in the chain.



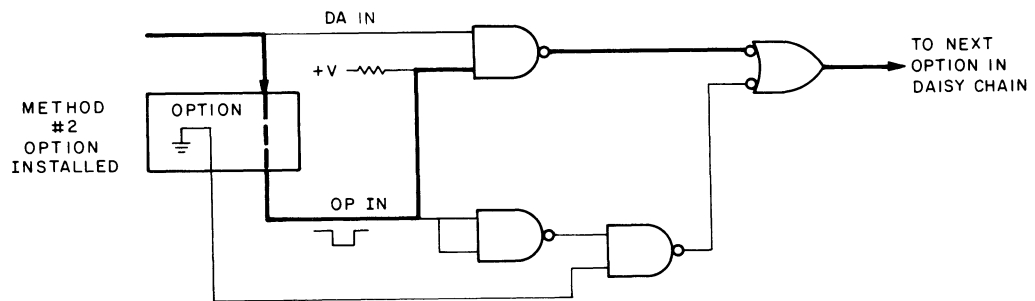
A. Method No. 1 - Option Not Installed



B. Method No. 1 - Option Installed



C. Method No. 2 - Option Not Installed



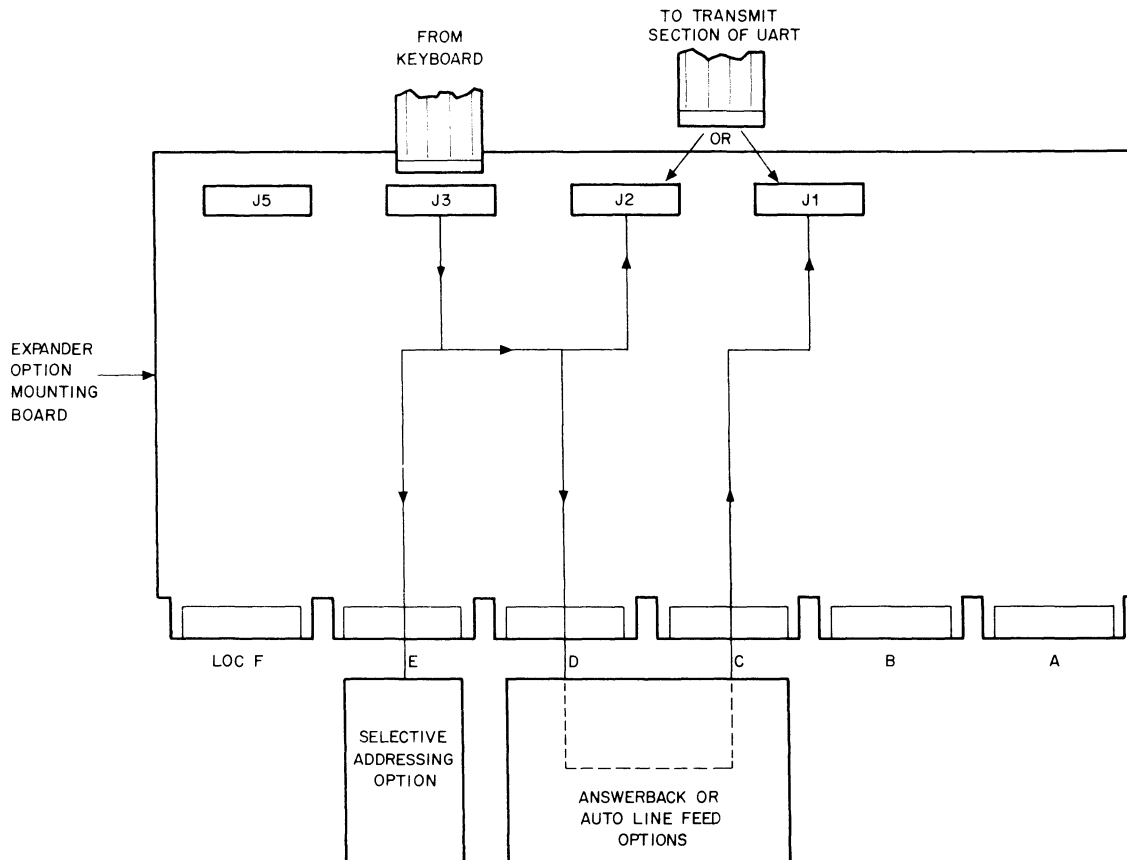
D. Method No. 2 - Option Installed

CP-2339

Figure 16-3 Methods of Switching Data Available Signal into Options

16.3.2 Routing of KEYSTROBE Signal

Distribution of the Keystrobe signal on the Expander Board is shown on Figure 16-4. As each character is typed, its ASCII code and associated Keystrobe signal are applied through J3 and routed out J2 (if the Answerback or Line Feed Options are not installed). The Selective Addressing Option at location F monitors all typed characters but is not in series with the data path as are either the Answerback or Line Feed Options which are installed at locations C and D. These options can break and insert characters and keystrokes into the transmit data line to the UART.



CP-2340

Figure 16-4 Keystrobe Distribution on Expander Board

16.4 TROUBLESHOOTING

The troubleshooting chart in Table 16-1 lists the common trouble symptoms that could be observed during installation checkout or normal operation.

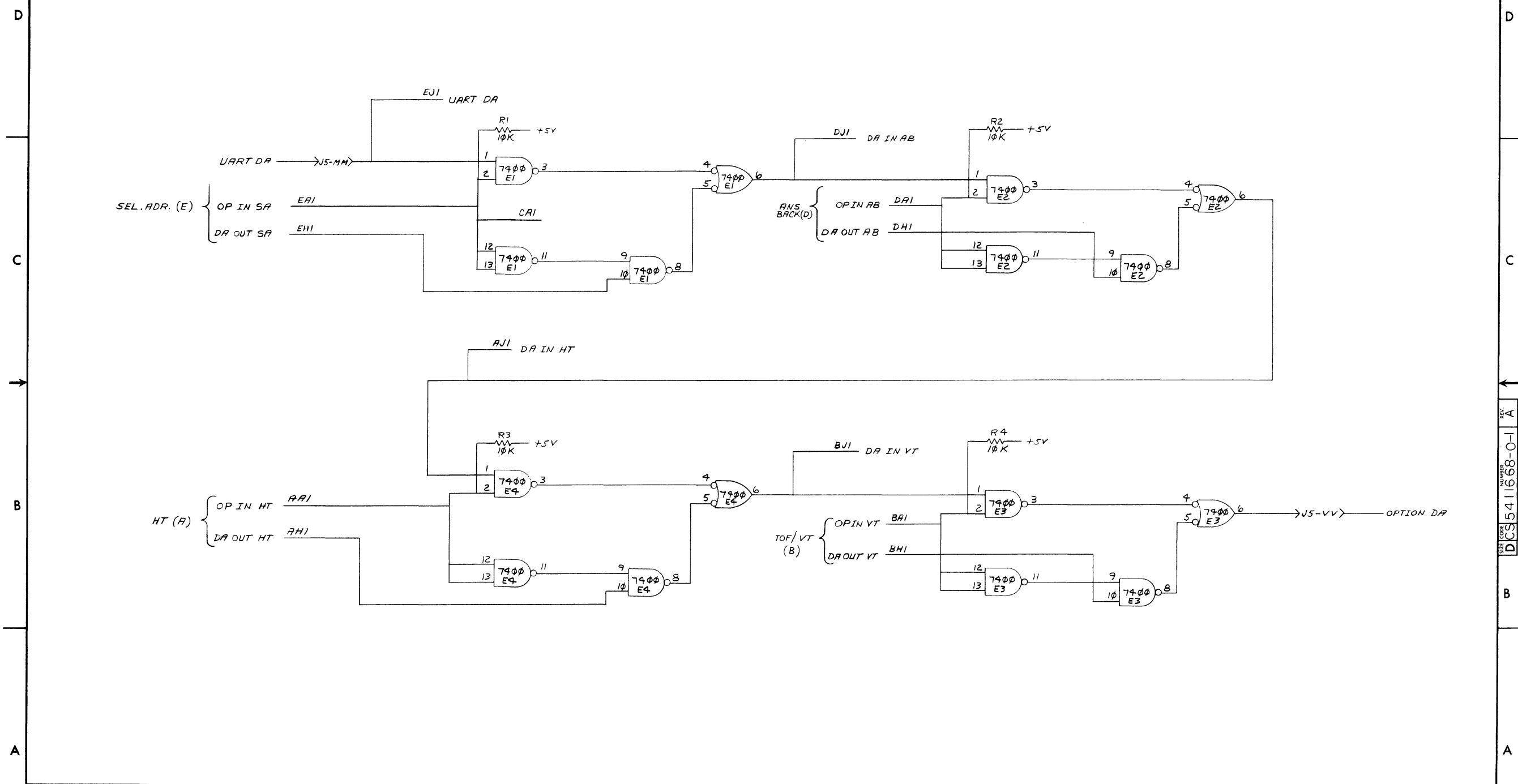
16.5 LAXX-LB PRINT SET

The figures at the end of this chapter are the LAXX-LB print set.

**Table 16-1
Troubleshooting for Expander Option Mounting Kit (LAXX-LB)**

Symptom	Problem Area	Probable Cause	Action	Reference
1. With no options installed on board, cannot receive	Cabling	Wrong polarity of bidirectional cabling	Check polarity between J5 of Expander Board and J5 of Logic Board	
2. With no options installed on board, cannot transmit from keyboard	Cabling	Wrong cabling connections	Check all cabling between M7728 Logic Board and Expander Board	Figure 9-4
	Circuit board etch	Open circuit	Check continuity between J2 and J3 on Expander Board	D-CS-5411668-0-1, Sheet 3
3. With no options installed on board, not able to transmit or receive	Signal distribution problem	Short or open in etch or cabling – or possibly a fault on Logic Board	<p>To isolate between Logic Board and Expander Board, perform the following:</p> <ol style="list-style-type: none"> 1. Remove cable from J5 on Expander Board 2. Remove keyboard cable from J3 on Expander Board and plug into J2 on Logic Board <p>If still not able to transmit or receive, troubleshoot Logic Board. If able to transmit and receive, check continuity of all cables and etch on Expander Board.</p>	

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CHAPTER 17

EIA INTERFACE OPTION KIT (LAXX-LG)

17.1 EIA INTERFACE INTRODUCTION

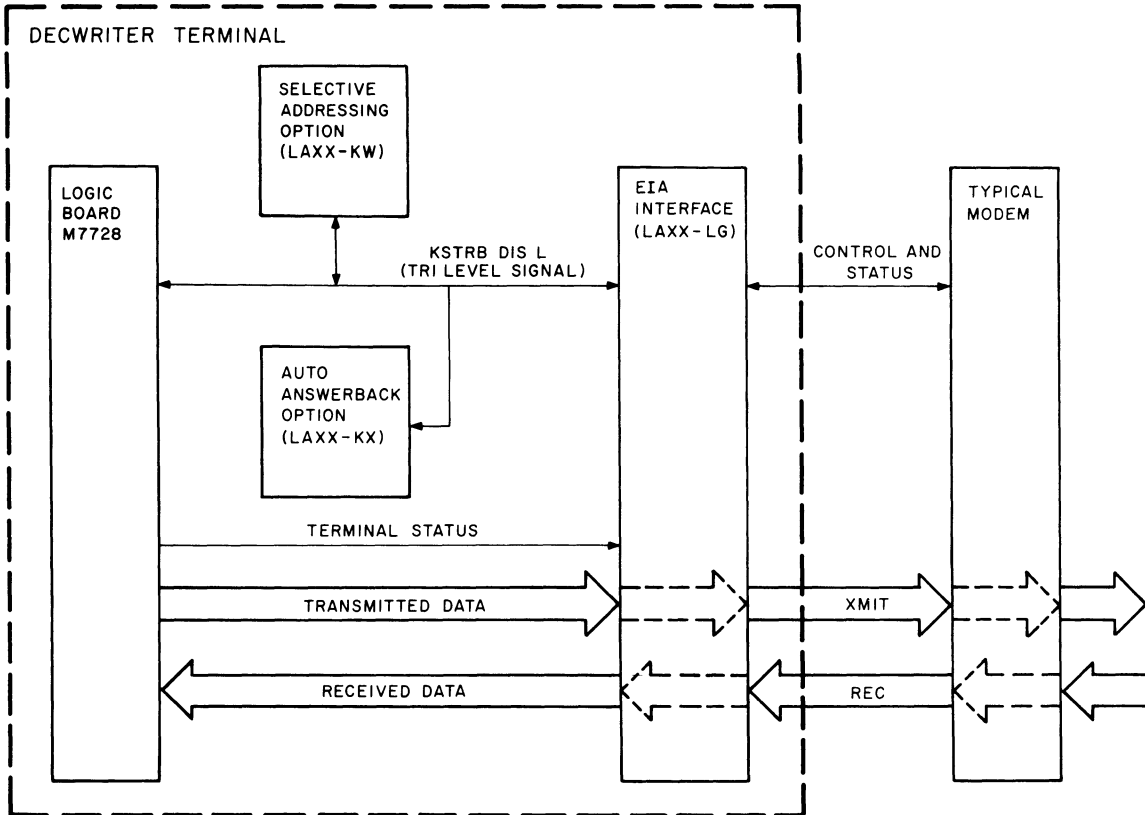
The EIA Interface Option provides a signal interface between a DECwriter and most modems, acoustical couplers, or other interfacing devices that use EIA levels. The EIA interface converts the level of the transmitting and received data from TTL to EIA bipolar (when the DECwriter is transmitting) or from EIA bipolar to TTL (when the DECwriter is receiving).

The EIA interface circuits provide the connect and disconnect control signals required in a communications-switched network environment and the carrier frequency selection command required in a multipoint network.

The EIA interface also monitors the operational status of both the terminal and the modem and, if either changes to a non-operational condition, the other is notified by the EIA.

17.2 EIA INTERFACE FUNCTIONAL BLOCK DIAGRAM

Figure 17-1 shows the EIA interface in a typical installation. Transmitted and received data signals are converted from one voltage level to another (TTL to EIA or EIA to TTL) as they pass through the EIA board. Status and control lines are monitored by the EIA circuits and, in the event of either a not ready or disconnect condition, appropriate commands are generated by the EIA.



CP-2341

Figure 17-1 EIA Interface Functional Diagram

The major command from the EIA to the terminal is the KSTRB DIS L signal. This command connects directly to the Logic Board in the terminal and also, if they are installed, to the Selective Addressing Option (LAXX-KW) and Answerback Option (LAXX-KX) as shown in Figure 17-1. The KSTRB DIS L command is a trilevel signal capable of attaining three distinct voltage levels: 0, M, or H. (0 = 0 V to 0.4 V; M = 2.0 V to 3.0 V; H = 4 V to 5 V. Voltage values are approximate and vary with the number of options on the trilevel line.) Each level is the result of a specific operational status and effects certain functions in the terminal and in the options connected to the line. Figure 17-1 shows this trilevel line as an input-only to both the Logic Board and the Answerback Option, and both an input and output from the Selective Addressing and EIA Options. Table 17-1 contains the various levels of this trilevel line and the effects on the overall system at each level.

Table 17-1
Effect of Tri-State Line Levels

Tri-State Signal Level	Generated by Option	When	Effect on Other Options			
			Selective Addressing	Auto Answerback	EIA Interface	Logic Board
O	Selective Addressing	Terminal is not the master and not able to transmit as a slave (transmit disable)	Prevents DEVICE SELECT light from illuminating	All requests for the answerback message are disregarded	Prevents Request to Send signal from being sent to modem	Inhibits transmitting from keyboard
M	EIA interface	Modem is not properly set up to pass data from terminal (Clear to Send signal not present at EIA)	Prevents DEVICE SELECT light from illuminating	Stores any received request for answerback message then transmits message after Clear to Send signal is received by EIA (The Tri-State signal is H).	Permits a Request to Send signal to be sent to modem	No effect – Able to transmit from keyboard
H	EIA interface	Modem is able to pass data from terminal (Clear to Send signal has been received by EIA)	Allows the DEVICE SELECT light to be turned on	Answerback message can be transmitted when request is received	Permits a Request to Send signal to be sent to modem	No effect – Able to transmit from keyboard

The EIA can only generate an M or H level but not a 0 level. The Selective Addressing Option only generates a 0 level and only responds to an H level. Also, the Selective Addressing Option has overriding control on the trilevel line in all cases of dispute. For example: if the EIA is generating an H (when modem is ready to accept transmit data) and at the same time the Selective Addressing Option is generating a 0 (when terminal not selected as a master or transmit enabled slave), the 0 level takes precedence and the terminal is transmit disabled.

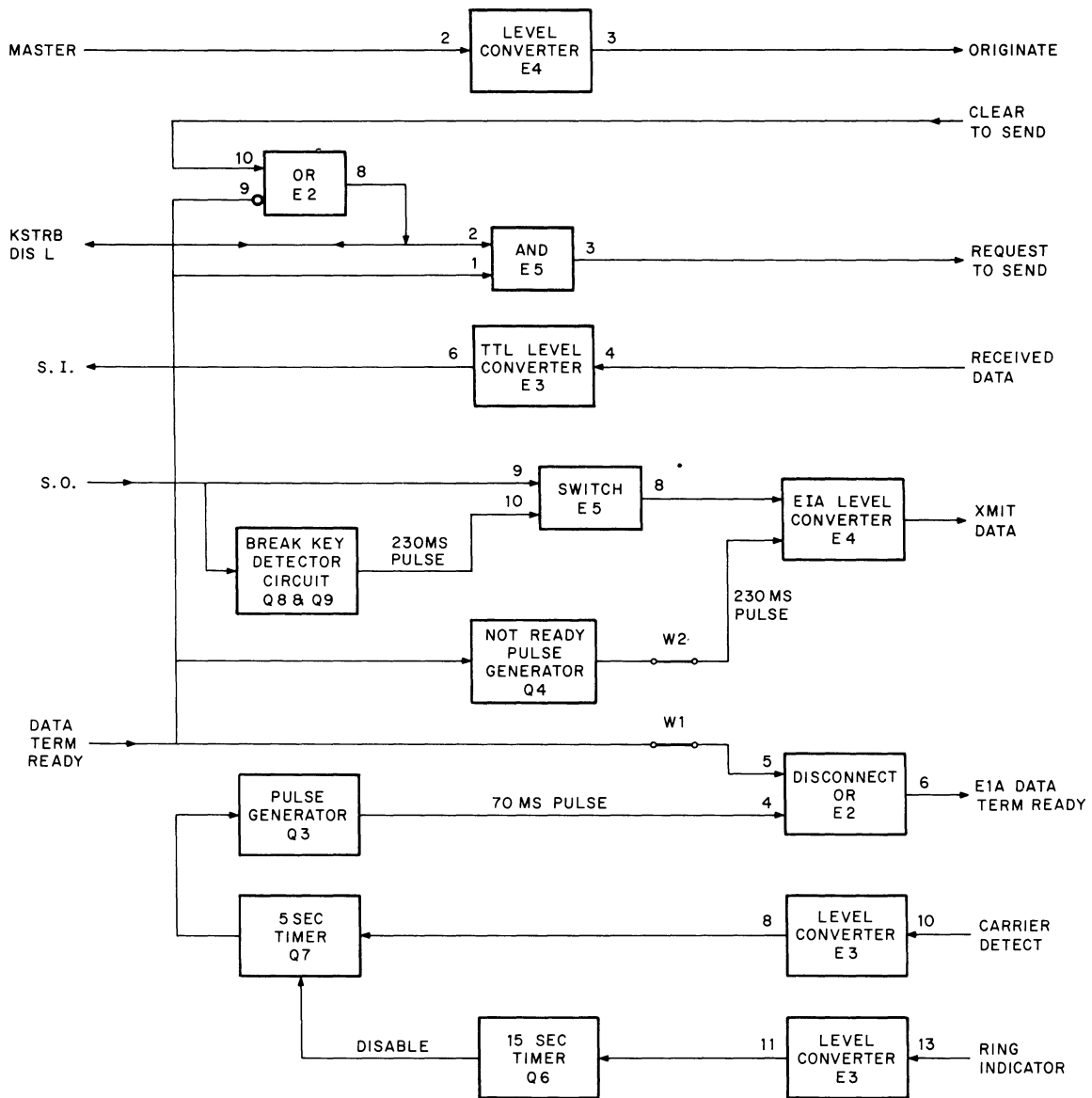
In installations where the Selective Addressing Option is not included, the trilevel line has only two states, M or H. The absence of the Answerback Option has no effect on the trilevel line because this option only uses the line as an input not as an output.

When the EIA is configured in a switched network environment (where calls are either automatically or manually established), disconnect signals are sent to the modem by the EIA when the terminal is not in the normal operating mode or the data carrier is not present at the modem.

17.3 EIA INTERFACE BASIC BLOCK DIAGRAM

The basic block diagram for the EIA Interface Option is shown in Figure 17-2. This diagram is a simplified representation of the EIA interface circuit schematic (D-CS-5411771-0-1). Circuit designations and pin numbers indicated on Figure 17-2 correlate with corresponding components on the schematic. Buffers, inverters, and other components that do not have major operational functions are omitted from the block diagram.

The EIA interface can be divided into the following three functional areas: data path, connection protocol, and disconnect functions.



CP-2342

Figure 17-2 EIA Interface Block Diagram

17.3.1 Data Path

Received EIA-level data is converted to TTL levels by E3 and then applied to the terminal as the SI signal. TTL output data (SO) from the terminal is generated at the keyboard and converted to EIA levels by E4. Two additional circuits can produce an effect on this output data signal: Break Key Detector Circuit and Not Ready Pulse Generator.

The Break Key Detector Circuit formed by Q8 and Q9 monitors the data out of the terminal and when a high level signal from the keyboard BREAK key appears, this circuit truncates this signal after 233 ms. This action ensures that if the BREAK key is depressed for a relatively long period of time (approximately 1 second) the receiving unit does not interpret this time break as a terminal disconnect signal and terminate the communications operation. This feature is desirable in environments where the Carrier Detect signal from the modem is not used to initiate terminal disconnects. The Break Key Detector Circuit generates a 233-ms time break pulse that is inserted on the Xmit Data line which overrides the actual pulse width caused by the BREAK key.

The other circuit that effects the Xmit Data line is the Not Ready Pulse Generator circuit formed by Q4. This circuit monitors the operational status of the terminal (DATA TERM READY) and, if the terminal changes to a not ready status, generates a 233-ms-wide pulse on the Xmit Data line. Anyone of the following four terminal actions can cause this pulse:

1. Paper out
2. Line/Local switch in LOC
3. Terminal power OFF
4. Power-up sequence not completed.

NOTE

Terminal actions that cause DATA TERM READY pulses of less than 233 ms wide are not extended but pulses wider than 233 ms are truncated to 233 ms.

When jumper W2 is installed, this pulse is applied on the Xmit Data line and is interpreted by the receiving unit as a Break command.

17.3.2 Connection Protocol

Five signals are used in conjunction with the Selective Addressing Option (LAXX-KW) and interfacing modems to establish data connections in typical multipoint networks. These signals are:

1. Data Term Ready (from terminal)
2. Request to Send (to modem)
3. Clear to Send (from modem)
4. KSTRB DIS L (bidirectional, to and from EIA interface)
5. Originate (to modem)

A terminal with EIA and Selective Addressing Options installed becomes the master terminal in the network by typing CTRL D. This causes two actions on the Selective Addressing circuit board. First the Master signal is sent through the EIA to the modem as the Originate signal. This signal causes the modem to switch to a transmitting carrier (frequency) so that the master terminal can transmit on the frequency that all the other terminals (slaves)

are receiving on. The Selective Addressing Option also removes the 0 level signal on the trilevel line (KSTRB DIS L at E5 pin 2 of the EIA switches to the M level). If the terminal is ready for normal operation (power ON, paper installed, on-line, and wake-up completed), the Data Term Ready signal and the M level signal at E5 generate the Request to Send signal. After the modem has switched to the transmitting frequency and established the channel, it sends the Clear to Send signal back to the EIA. The Clear to Send signal through OR E2 forces the KSTRB DIS L signal to the H level and the terminal front panel DEVICE SELECT light illuminates. The terminal has established a proper connection and can transmit data out the SO line.

The other input signal at E2 (pin 9) is the DATA TERM READY from the DECwriter terminal. This signal is used to monitor the local/line condition of the terminal. When in the local mode of operation and the EIA interface is not installed, the KSTRB DIS L signal connecting the Answerback and Selective Addressing Options is normally at the H level. This allows the answerback message to print locally and the Selective Addressing Option to control the front panel DEVICE SELECT and SELECT AVAIL lights. To prevent the installation of the EIA from inhibiting these functions, the local indication on the DATA TERM READY line is applied through OR gate E9 to hold the KSTRB DIS L signal at an H level even though the CLEAR TO SEND signal may not present from the modem. (In local mode, status of modem is not considered for normal operation.)

At the end of the transmission, typing CTRL D removes the Originate signal (terminal no longer is the master), causing the modem to switch the carriers back to the answer mode.

17.3.3 Disconnect Functions

When the EIA interface is used in a switched network environment the interconnect signals typically used are:

1. Data Term Ready (from terminal)
2. EIA Data Term Ready (to modem)
3. Carrier Detect (from modem)
4. Ring Indicator (from modem)

The EIA Data Term Ready signal is the primary interface between the EIA and modem. It functions as both the terminal status monitor and as the Disconnect signal. With Jumper W1 installed, EIA Data Term Ready signal reflects the operational condition of the terminal (paper out, local mode, etc.) and remains low as long as the improper terminal condition occurs. The disconnect action of the EIA Data Term Ready signal is indicated by a 70-ms pulse out of E2. This disconnect occurs when the carrier of the telephone connected to the modem is removed. In automatic answer applications (where calls are automatically answered), the Ring Indicator signal from the modem starts the 15-second timer circuit Q6. If at the end of 15 seconds, the Carrier Detect signal is not asserted high (indicating that a carrier is present at the modem), Pulse Generator Q3 applies a 70-ms disconnect pulse on the EIA Data Ready line. During normal operation (after communications have been established) if the carrier is removed or disconnected, the 5-second timer Q7 starts. At the completion of its count, a 70-ms disconnect pulse is applied on the EIA Data Term Ready line. This automatic disconnect feature prevents incorrectly terminated calls from tying up the communications line.

17.4 TROUBLESHOOTING

The troubleshooting chart in Table 17-3 lists the common trouble symptoms that could be observed during installation checkout or normal operation.

17.5 LAXX-LG PRINT SET

The figures at the end of this chapter are the LAXX-LG print set.

Table 17-2
Standard EIA Modem – Terminal Interface Connections

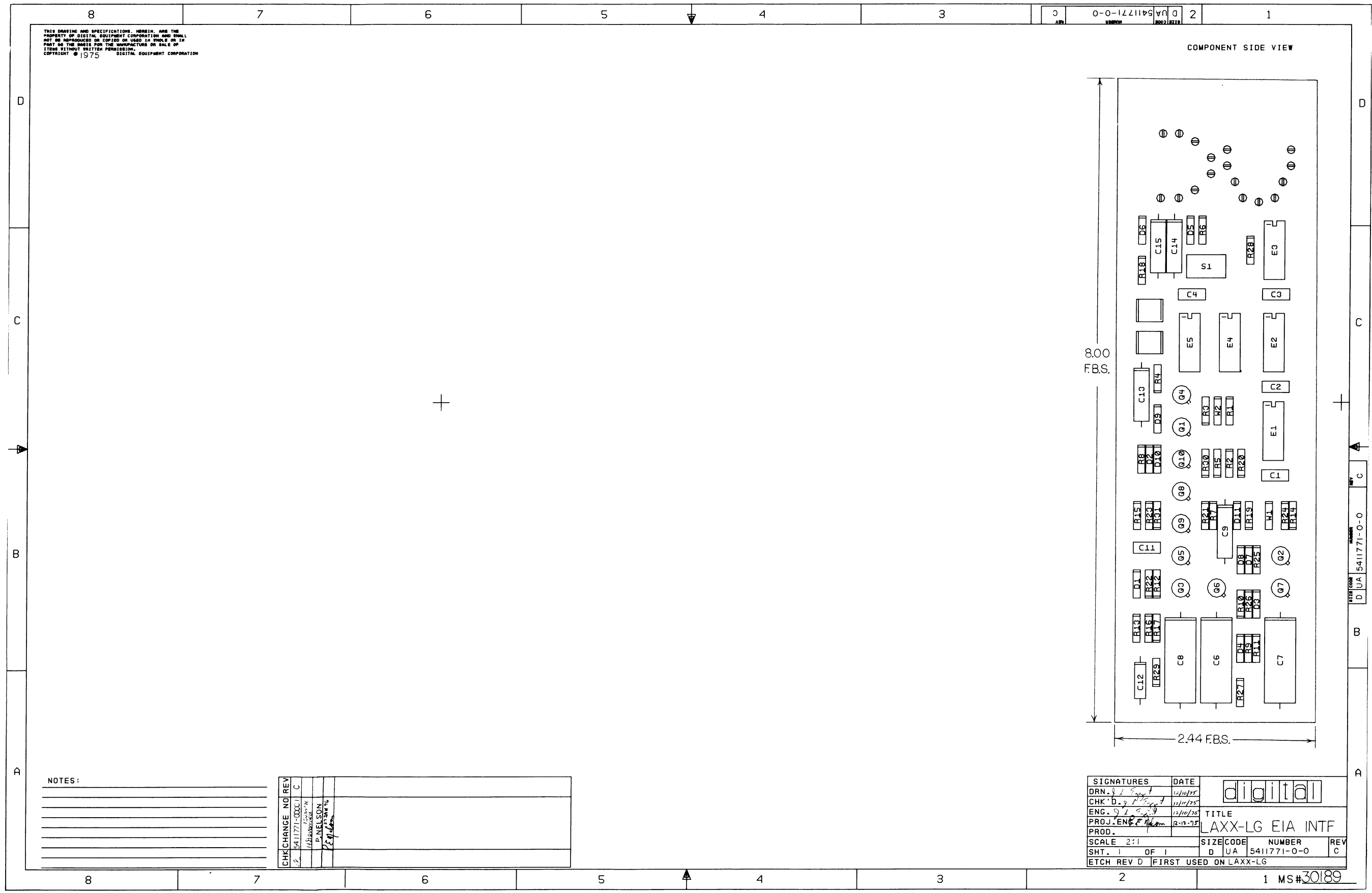
Pin	Name	Function	EIA Circuit Designation	Sent To	
				Data Terminal Equipment	Data Communications Equipment
1	FG	Frame Ground	AA		
2	TD	Transmitted Data	BA		X
3	RD	Received Data	BB	X	
4	RTS	Request To Send	CA		X
7	SG	Signal Ground	AB		
8	DCD	Data Carrier Detect	CF	X	
11	None	Unassigned	None		
20	DTR	Data Terminal Ready	CD		X
22	RI	Ring Indicator	CE	X	

Notes:

1. Positive voltage equals binary zero, space, on
2. Negative voltage equals binary one, mark, off

Table 17-3
Troubleshooting for EIA Interface Option (LAXX-LG)

Symptom	Problem Area	Probable Cause	Action	Reference
1. No operation of terminal on-line	Connections	EIA connector in wrong location	Plug EIA connector into J4 of Logic Board	
2. Not receiving incoming data	Level conversion	EIA to TTL converter defective	Replace E3	D-CS-5411771-0-1
3. Not transmitting typed data	Level conversion	TTL to EIA converter defective	Replace E4	D-CS-5411771-0-1
4. With no other options installed not able to type from keyboard when on-line	Keystrobe disable	Keyboard inhibited by KSTRB DIS L signal from EIA	Check E2 pin 10 for Clear to Send signal from modem	D-CS-5411771-0-1



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COMPONENT SIDE VIEW

8.00 FBS.

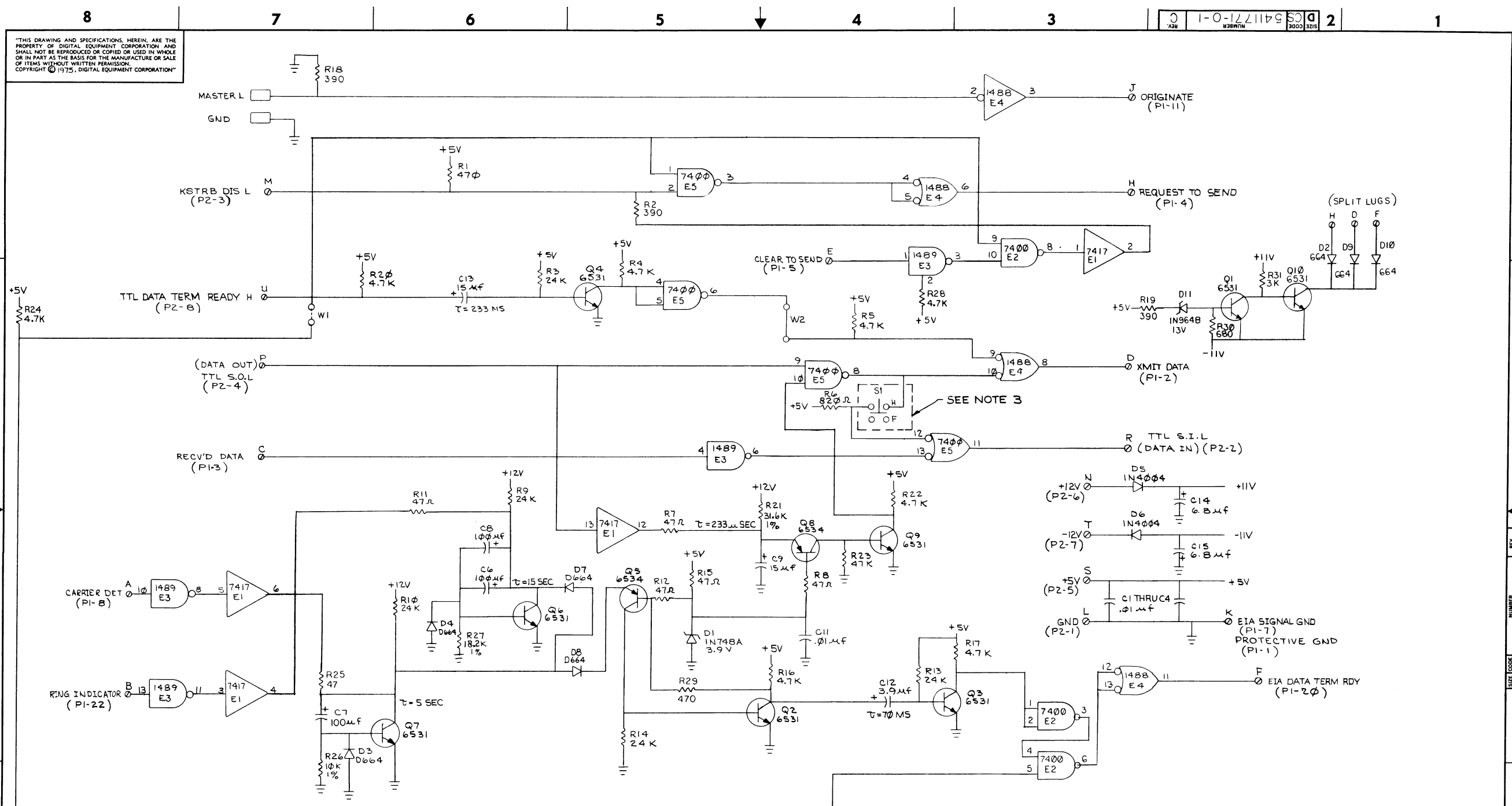
2.44 FBS.

NOTES:

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2	5411771-000	1	C		
				P. NELSON	

SIGNATURES	DATE	TITLE
DRN. J. L. [Signature]	12/10/75	
CHK. D. [Signature]	11/10/75	
ENG. S. [Signature]	12/10/75	
PROJ. ENG. [Signature]	12-13-75	
PROD.		
SCALE 2:1	SIZE CODE	NUMBER
SHT. 1 OF 1	D UA 5411771-0-0	REV C
ETCH REV D	FIRST USED ON LAXX-LG	

1 MS#30189



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REV. C
D CS 5411771-0-1
D CS 5411771-0-1

- NOTES:
1. SPLIT LUGS A-K (P1) IS THE EIA INTERFACE.
 2. SPLIT LUGS L-U (P2) IS THE DATA TERMINAL INTERFACE.
 3. SWITCH S1 ONLY INSTALLED IN FIELD USE AS REQUIRED BY SPECIFIC CUSTOMER APPLICATIONS.

REV. C	REV. C
CHANGE NO. 15411771-00001	CHANGE NO. 15411771-00001
DATE 14 JAN 76	DATE 14 JAN 76
BY P. NELSON	BY P. NELSON
27 JAN 76	27 JAN 76

DRN: T. Quinn	10/02/75	FIRST USED ON	LA36	digital
CHK'D: W. Jones	10/02/75	TITLE	LAXX-LG EIA INTERFACE	
ENGR: E. Melan	10 NOV 75	PROJ. ENGR: E. Melan	10 NOV 75	
PROD. ENGR: E. Melan	11/10/75	NEXT HIGHER ASSY.		
D-UA-5411771-0-0	SIZE CODE	NUMBER	D CS 5411771-0-1	REV. C
SCALE	DIST.	SHEET 1	OF 1	

CHAPTER 18

20 mA INTERFACE CABLE OPTION KITS (LAXX-LK DEC 10 AND LAXX-LH STANDARD)

18.1 20 mA INTERFACE CABLE INTRODUCTION

The only difference between these two cable options is the termination connectors at the cable ends.

The LAXX-LK Option has a Mate-N-Lok connector at one end and a 283B connector (for interfacing to a DEC 10) at the other end as shown in Figure 18-1.

From		To	
283B Connector Pin No.	Wire Color	Description	Mate-N-Lok Connector Pin No.
P1-R	Red	Negative side of Transmit Line	P2-2
P1-Y	White	Negative side of Receive Line	P2-3
P1-GN	Green	Positive side of Transmit Line	P2-5
P1-BK	Black	Positive side of Receive Line	P2-7

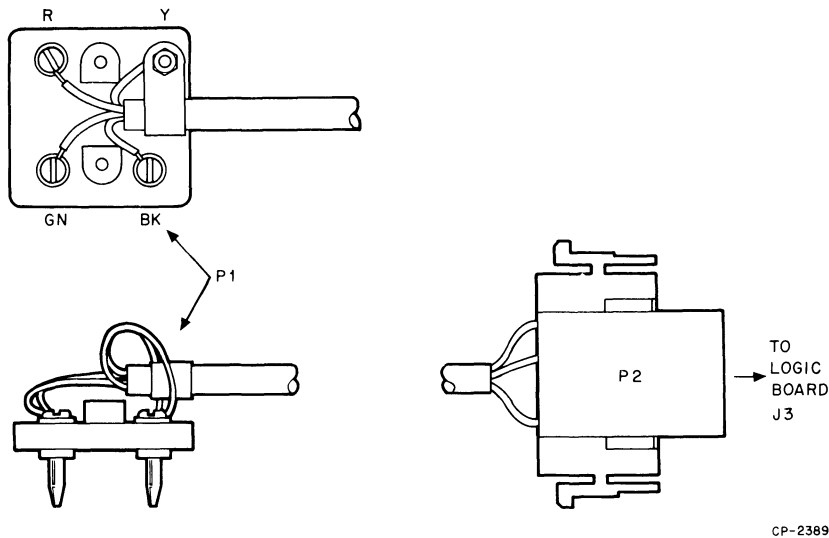


Figure 18-1 20 mA Interface Cable Option (LAXX-LK) Pin Assignments

The LAXX-LH Option has a Mate-N-Lok connector at each cable end. Refer to Figure 18-2.

From			To
Logic Board J3 Pin No.	Wire Color	Description	Computer Pin No.
P1-2	Black	Negative side of Transmit Line	P2-3
P1-3	Red	Negative side of Receive Line	P2-2
P1-5	White	Positive side of Transmit Line	P2-7
P1-7	Green	Positive side of Receive Line	P2-5

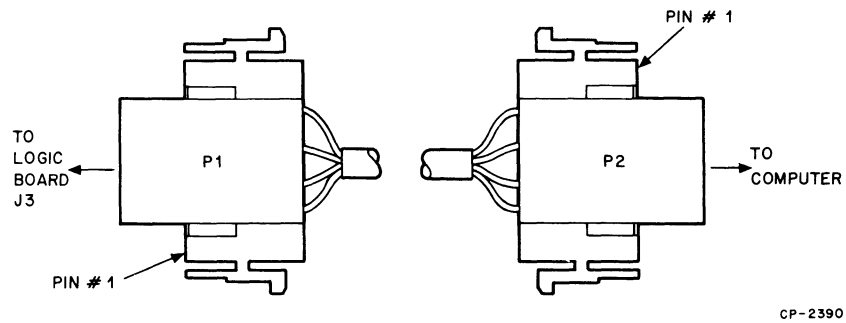


Figure 18-2 20 mA Interface Cable Option (LAXX-LH) Pin Assignments

CHAPTER 19

ACOUSTIC COUPLER OPTION KIT (LAXX-LM)

19.1 INTRODUCTION TO THE ACOUSTIC COUPLER

The Acoustic Coupler provides an interface between telephone data and the DECwriter. The coupler is a bidirectional device that converts incoming data into serial pulses acceptable to the terminal and converts data transmitted by the terminal into a data format compatible with standard phone requirements. The Acoustic Coupler assembly is incorporated in a special cover that replaces the standard cover supplied with each terminal. The coupler consists of a Muff assembly that accepts the telephone handset and a circuit board that contains the transmit and receive circuits. The coupler interfaces with the Logic Board through J4, the EIA connector.

NOTE

The Acoustic Coupler Option (LAXX-LM) is compatible with LA35 and LA36 terminals with either the M7722, M7723, or M7728 Logic Boards installed. The coupler does not require that the Expander Option Mounting Kit be installed for proper operation.

19.2 TYPICAL ACOUSTIC COUPLER OPERATION

The telephone system is a single wire system; therefore, to simultaneously transmit and receive over this wire, two distinct frequencies are used by Acoustic Couplers. By utilizing receivers with high selectivity, both frequencies can be present on the wire at the same time without noticeable interference.

Figure 19-1 shows a typical telephone data communications configuration between a DECwriter terminal and a computer installation. The Acoustic Coupler Option is always configured in the originate mode of operation (transmitting on 1 kHz and receiving on 2 kHz). The computer, or any other device or terminal communicating with the Acoustic Coupler Option, therefore, must be configured in the answer mode (transmitting on 2 kHz and receiving on 1 kHz).

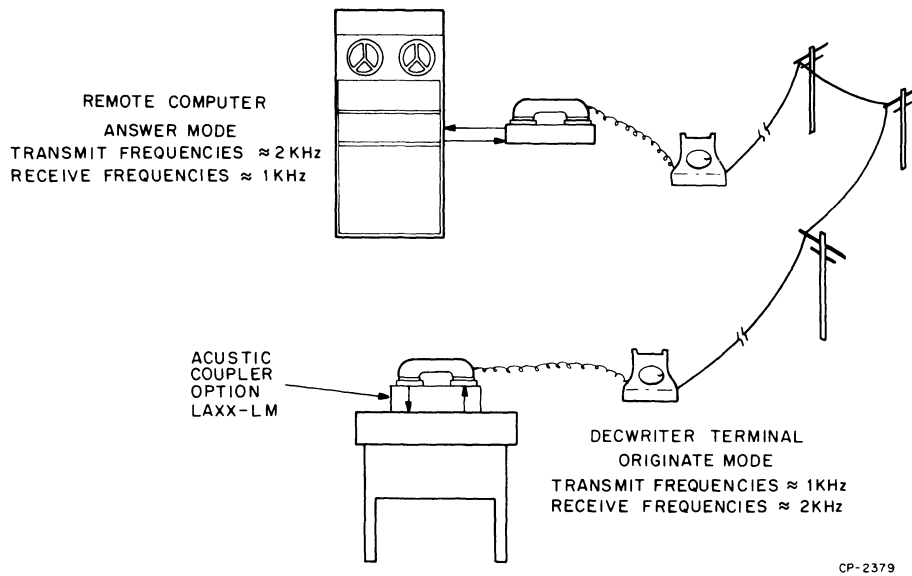


Figure 19-1 Typical Telephone Communication Configuration

Frequency Shift Keying (FSK) is used to modulate the transmitting frequencies as follows:

Originate Mode

1070 ± 10 Hz = High = Space = Binary Zero
 1280 ± 10 Hz = Low = Mark = Binary One

Answer Mode

2025 ± 10 Hz = High = Space = Binary Zero
 2225 ± 10 Hz = Low = Mark = Binary One

19.3 ACOUSTIC COUPLER FUNCTIONAL BLOCK DIAGRAM

The functional block diagram for the Acoustic Coupler is shown in Figure 19-2. Output data from the keyboard is converted to serial out (SO) by the UART and applied to the Transmit Section of the coupler. The Transmit Section applies the 1 kHz carrier and FSK information to the speaker in the Muff assembly. The telephone handset has a microphone in the mouthpiece which receives the data from the Muff's speaker. This data is transmitted out over the telephone line to the other device.

Received data is coupled through the speaker in the earpiece of the telephone to the microphone in the Muff. The Receiver Section of the coupler converts the received 2 kHz signal into serial in (SI) pulses and applies them to the UART on the Logic Board. The UART handles the received data in a normal manner and applies it to any installed options.

19.4 ACOUSTIC COUPLER BASIC BLOCK DIAGRAM

The basic block diagram for the Acoustic Coupler Option is shown in Figures 19-3 and 19-4. These diagrams are simplified representations of the Acoustic Coupler circuit schematic (D-AD-7012356-0-0). Circuit designations and pin numbers indicated on these figures correlate with corresponding components on the schematic. Buffers, inverters, and other components that do not have major operational functions are omitted from the block diagrams.

The Acoustic Coupler can be divided into two functional areas:

1. Transmit Section
2. Receive Section

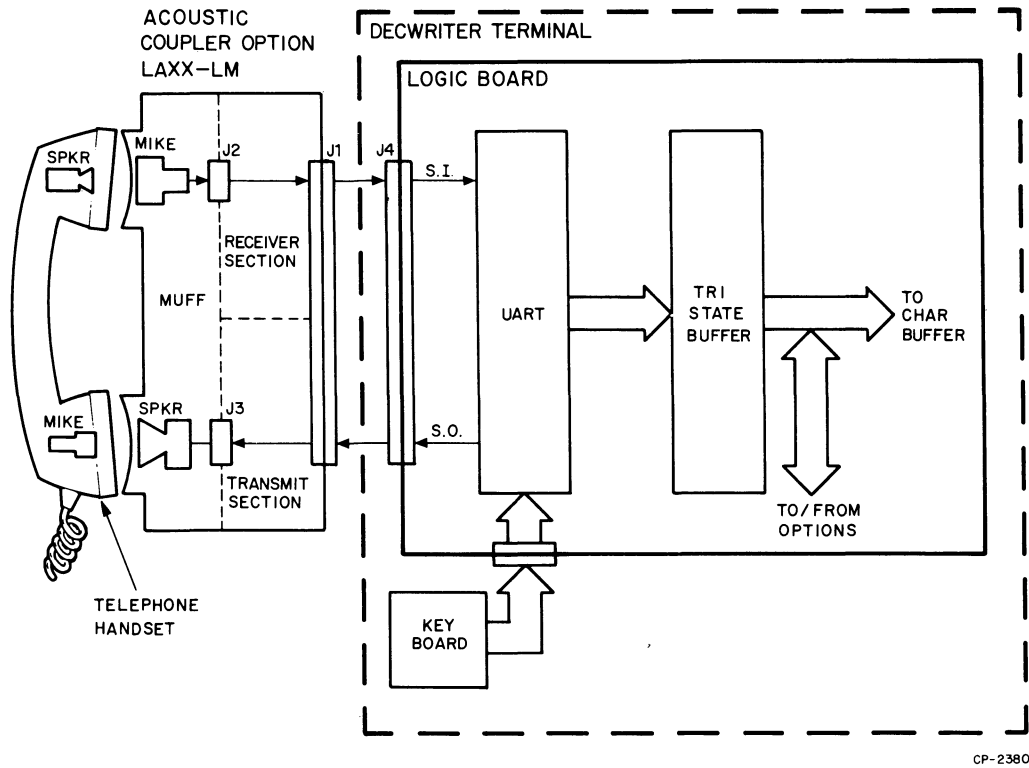


Figure 19-2 Acoustic Coupler Functional Block Diagram

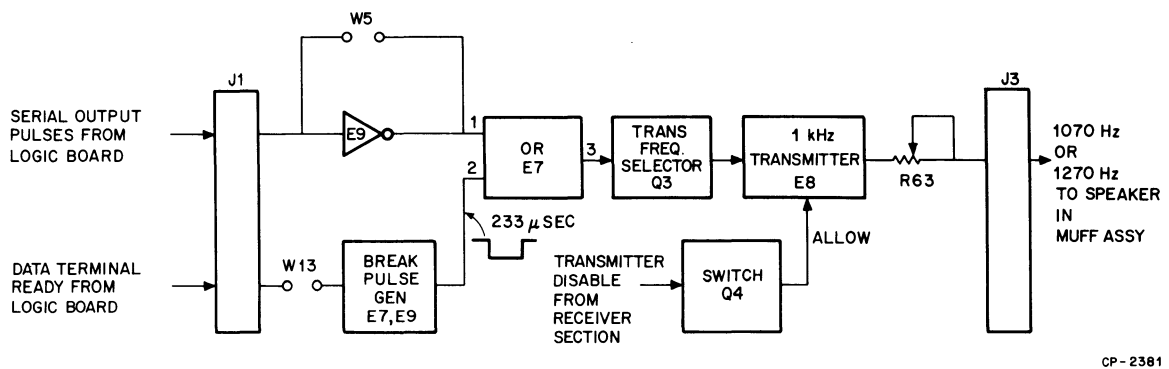


Figure 19-3 Acoustic Coupler Transmit Section Basic Block Diagram

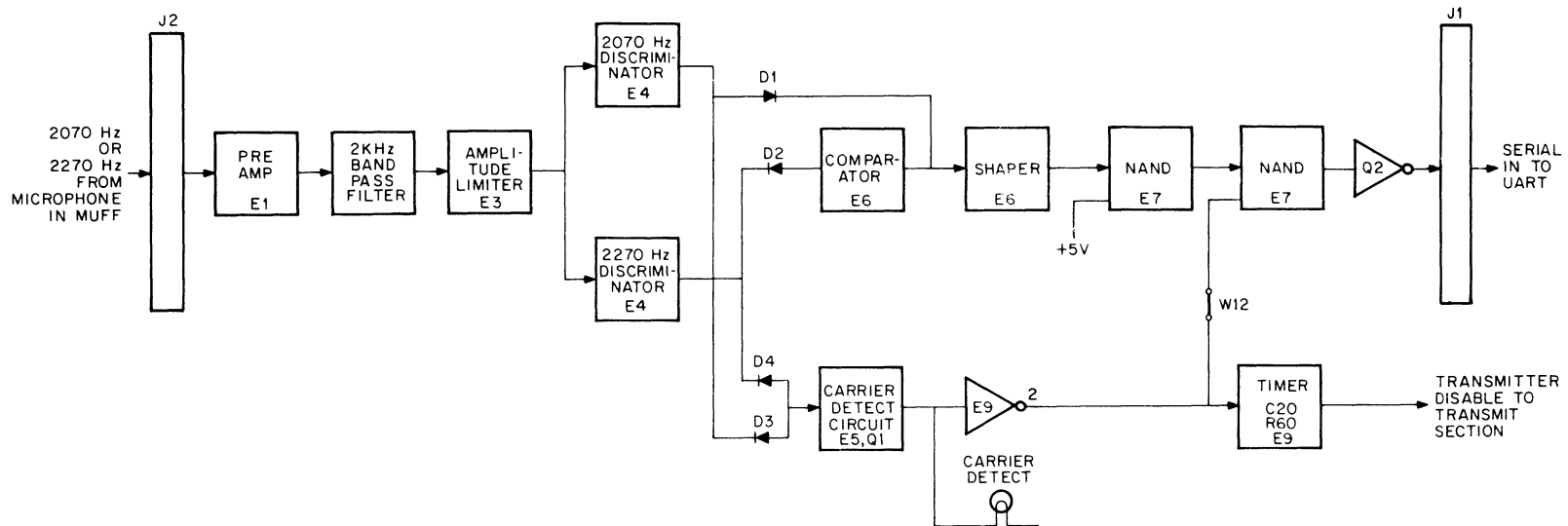


Figure 19-4 Acoustic Coupler Receive Section Basic Block Diagram

19.5 TRANSMIT SECTION

The basic block diagram for the Transmit Section of the Acoustic Coupler is shown in Figure 19-3. Keyboard ASCII characters are applied through Inverter E9 (W5 is normally removed), then through OR gate E7 to the Transmitter Frequency Selector Q3. A binary zero in the ASCII code selects the 1070 Hz output frequency and a binary one selects the 1270 Hz frequency. Resistor R63 permits adjustment of the output level that is applied to the speaker in the Muff assembly. This adjustment matches the circuit board to the Muff.

The Data Terminal Ready (DTR) signal from the Logic Board when the terminal goes not ready only (which is available from the M7728 board, not from the M7722 or M7723 boards) is coupled through W13 to enable the Break Pulse Generator E7, E9. This pulse generator produces a negative-going, 233 ms wide pulse. It extends DTR pulses shorter than 233 ms and truncates DTR pulses that are longer than 233 ms.

The transmitter is not permitted to output the 1 kHz carrier signal until the Receiver Section of the Acoustic Coupler has detected a valid carrier on the incoming receiver line. This action ensures that a proper communications channel has been established.

19.6 RECEIVE SECTION

The basic block diagram for the Receive Section is shown in Figure 19-4. Incoming data from the microphone in the Muff is applied through J2 to the Preamplifier E1. The Band Pass Filter, consisting of E2, E3, and the associated tuned circuits, passes only 2 kHz signals and rejects all others. Limiter E3 removes all noise-induced amplitude modulation on the 2 kHz signal. Each section of E4 forms a discriminator that detects the presence of 2025 Hz and 2225 Hz. The output of each discriminator is a wave whose amplitude is proportional to whether the incoming signal is a one or zero. The discriminator outputs are applied through positive rectifier D1 and negative rectifier D2 then compared at E6. As the amplitude out of one section of E4 becomes greater than the other section, the signal produced at E6 pin 7 approximates a square wave. This signal is passed through Shaper E6 to make the square wave more precise, then applied to NAND gate E7 which acts like a diode and only passes one-half of the square wave, producing a series of pulses at pin 10 of NAND E7. The other input to E7 (pin 9) is connected to the carrier detect circuitry of the Receiver Section. When a valid carrier is present for the required period of time, pin 9 becomes high and allows the series of data pulses to pass through E7 to Q2. The output of Q2 is applied through J1 to the receiver half of the UART on the Logic Board.

The carrier detect circuit (composed of E5 and Q1) also monitors the output of the two E4 discriminators. This detector circuit does not care whether the discriminator output is positive or negative, just that there is an output. This output is rectified by D3, D4 and applied to E5 pin 6. A negative output signal is present at E5 pin 1 when a valid carrier is detected. This negative voltage causes the carrier detect light on the cover assembly to illuminate. The negative voltage becomes a high level through Inverter E9 and enables the receiver at E7. This high level, which enables the receiver, is also applied through a timer circuit that is composed of E9, R60, and C20. This circuit controls whether the transmitter in the acoustical coupler is able to transmit.

When the output of E9 pin 6 is at a high level, the transmitter is enabled because Q4 is conducting. When E9 pin 6 is low Q4 conducts removing +12 V from E8 pin 5 and the transmitter is disabled. The carrier monitoring circuits are the controlling circuits for both the Transmit and Receive Sections of the coupler. After detecting a valid carrier for approximately 5 seconds, the Receiver Section is enabled and incoming data is passed onto the UART. If, while receiving data, the carrier is lost, the Receive Section is disabled 0.5 second after the carrier disconnects. The Transmit Section of the coupler is enabled after the 5 seconds that valid carrier is detected and remains enabled for about 4 seconds after the carrier is lost during transmission.

This non-symmetrical timing for connecting and disconnecting ensures that the coupler is properly configured before data is either transmitted or received. It also permits a fast disconnect for the Receiver Section so that spurious noise cannot enter into the receiver if the carrier is lost. The slower disconnect on the Transmit Section (if the received carrier is lost) permits momentary lost of input carrier without a break in the output data.

19.7 TROUBLESHOOTING

The troubleshooting chart in Table 19-1 lists the common trouble symptoms that could be observed during installation checkout or normal operation.

19.8 LAXX-LM PRINT SET

The figures at the end of this chapter are the LAXX-LM print set.

Table 19-1
Troubleshooting for Acoustic Coupler Option (LAXX-LM)

Symptom	Problem Area	Probable Cause	Action	Reference
1. After installation, does not receive or transmit	Set up configuration	Wrong baud rate	Match baud rates between sending and receiving units	
		Terminal not on-line Incorrect cabling	Place terminal on-line Connect Acoustic Coupler Cable to J4 on the Logic Board	
		Telephone not inserted in Muff correctly	Cord end of handset inserted in Muff with "dot" and/or word "CORD" next to it	
		No carrier being sent to Acoustic Coupler	Listen for carrier in handset	
2. Random errors appear in printing or transmission	Signal level or noise interference	Poor telephone connection	Hang up and try connection again	
		Mechanical noise	Check for printer cover rubbing on tractor shaft	
		Loose equipment	Check tightness of Paper Advance knob	
		High ambient noise level	Refer to Acoustic Coupler Specification for acceptable sound levels	

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D
C
B
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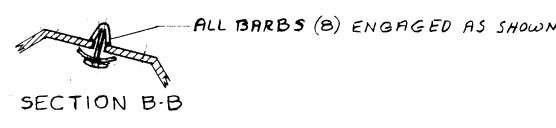
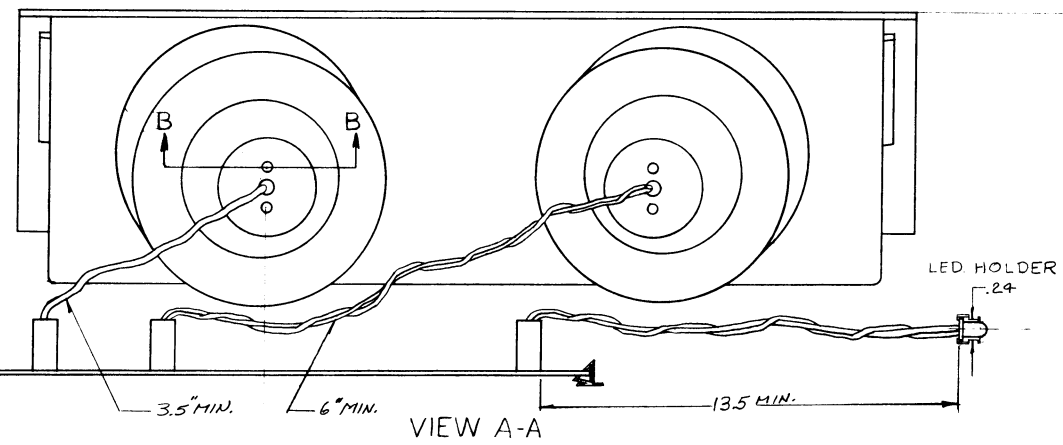
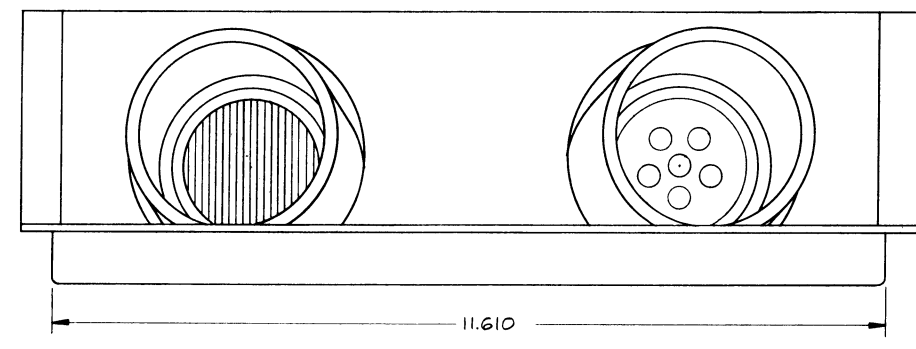
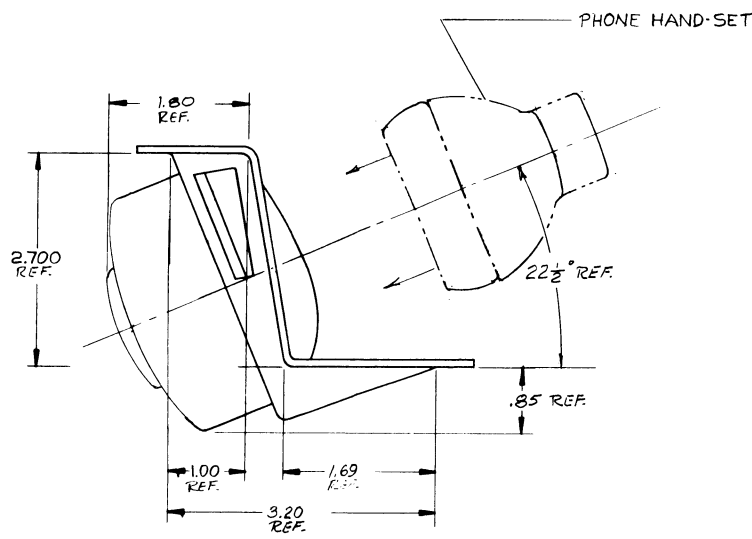
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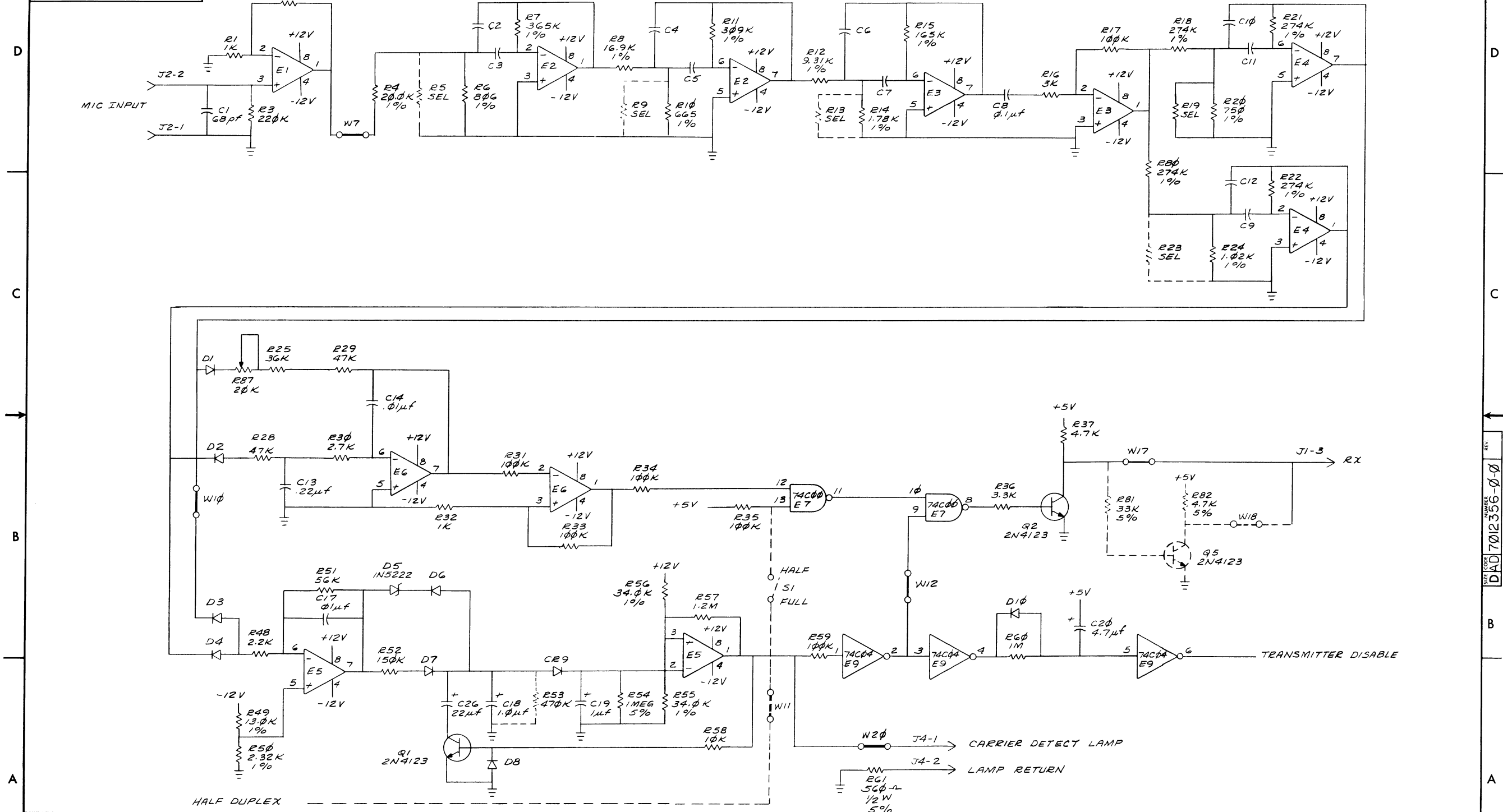
8 7 6 5 4 3



REF. SPEC. DEC. PROD. TEST. PROCEDURE	A-SP-LAXX-LM-3
REF. SPEC. DEC. ENG.	A-SP-LAXX-LM-1
REF. INCOMING INSPECTION PROCEDURE	A-II-7012356-0-1
DESCRIPTION	DWG./PART NO. ITEM NO.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	
ANGLES ±0° 30'	CLASS OF ACCURACY
SURFACE QUALITY IN	(CHECK ONE)
MICROINCHES	PREFERRED
QUANTITY & VARIATION	
THIRD ANGLE PROJECTION	
REMOVE BURRS AND BREAK SHARP CORNERS	
DO NOT SCALE DWG	
MATERIAL NOVATION PART NO. 490-770	
FINISH	
DRN. D. S. 11-3-75	FIRST USED ON
CHK'D. B. 12-31-75	LA36 digital
ENG. W. Benson 1-28-76	TITLE
PROJ. ENG. E. M. 12-21-76	ACOUSTIC COUPLER ASSY
PROD. J. P. 1/30/76	
NEXT HIGHER ASSY.	
D-AD-7012144-0-0	SIZE CODE
SCALE 1/1	D AD
SHEET 1 OF 4	DIST.
	NUMBER
	7012356-0-0
	REV.

REV. 0-0-0 7012356-0-0 D AD

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REVISIONS		
CHK	CHANGE NO.	REV.

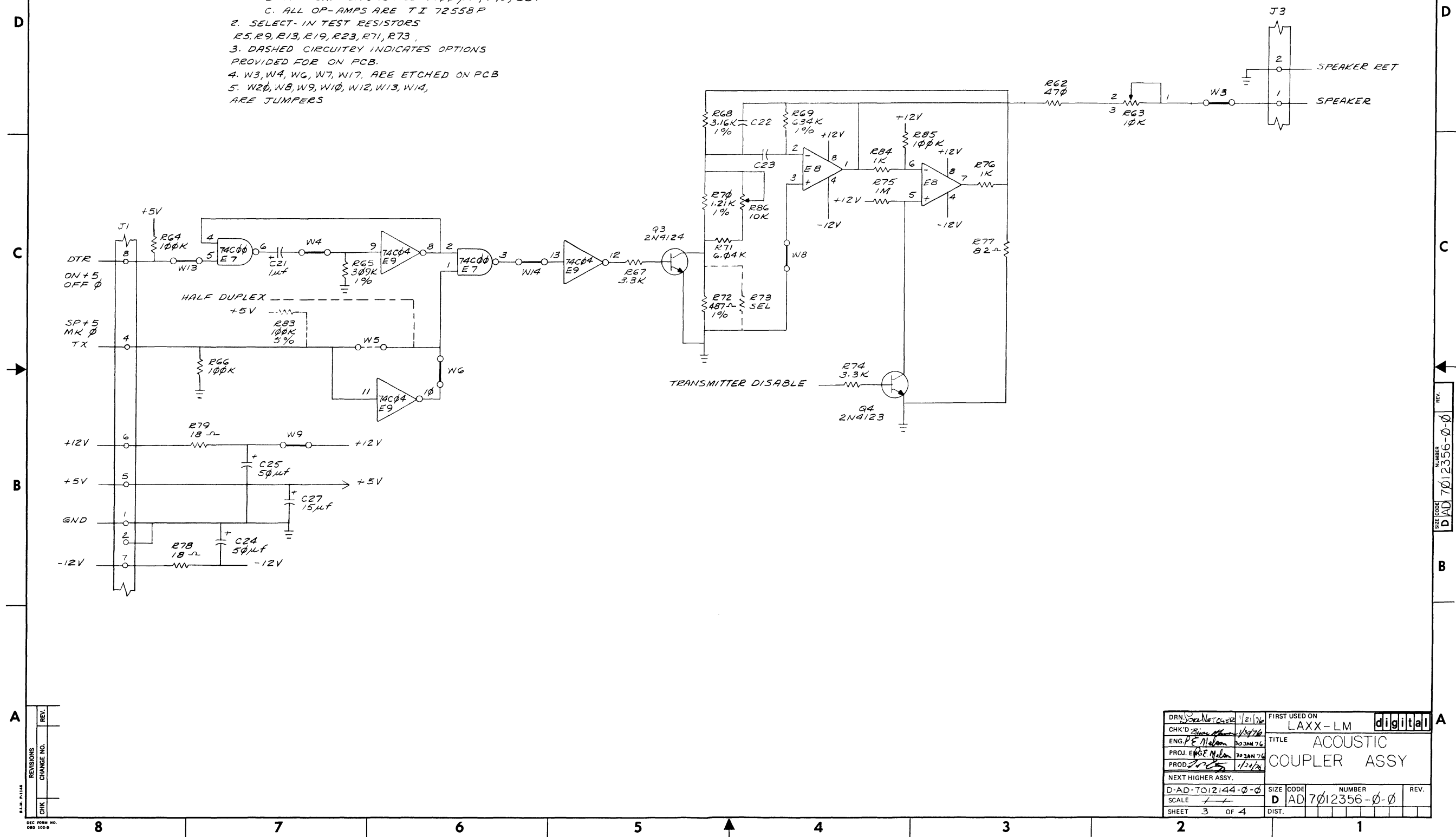
8	7	6	5	4	3	2	1		
TITLE ACOUSTIC COUPLER ASSY							SIZE CODE DAD 7012356-0-0	NUMBER	REV.
SCALE							SHEET 2 OF 4	DIST.	

REV. NUMBER DAD 7012356-0-0

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NOTES:

1. UNLESS OTHERWISE SPECIFIED
 - A. ALL DIODES ARE 1N4148
 - B. ALL CAPACITORS ARE 4700 pF, 1%, 33V
 - C. ALL OP-AMPS ARE TI 72558P
2. SELECT-IN TEST RESISTORS
R5, R9, R13, R19, R23, R71, R73
3. DASHED CIRCUITRY INDICATES OPTIONS PROVIDED FOR ON PCB.
4. W3, W4, W6, W7, W17, ARE ETCHED ON PCB
5. W2, W8, W9, W10, W12, W13, W14, ARE JUMPERS



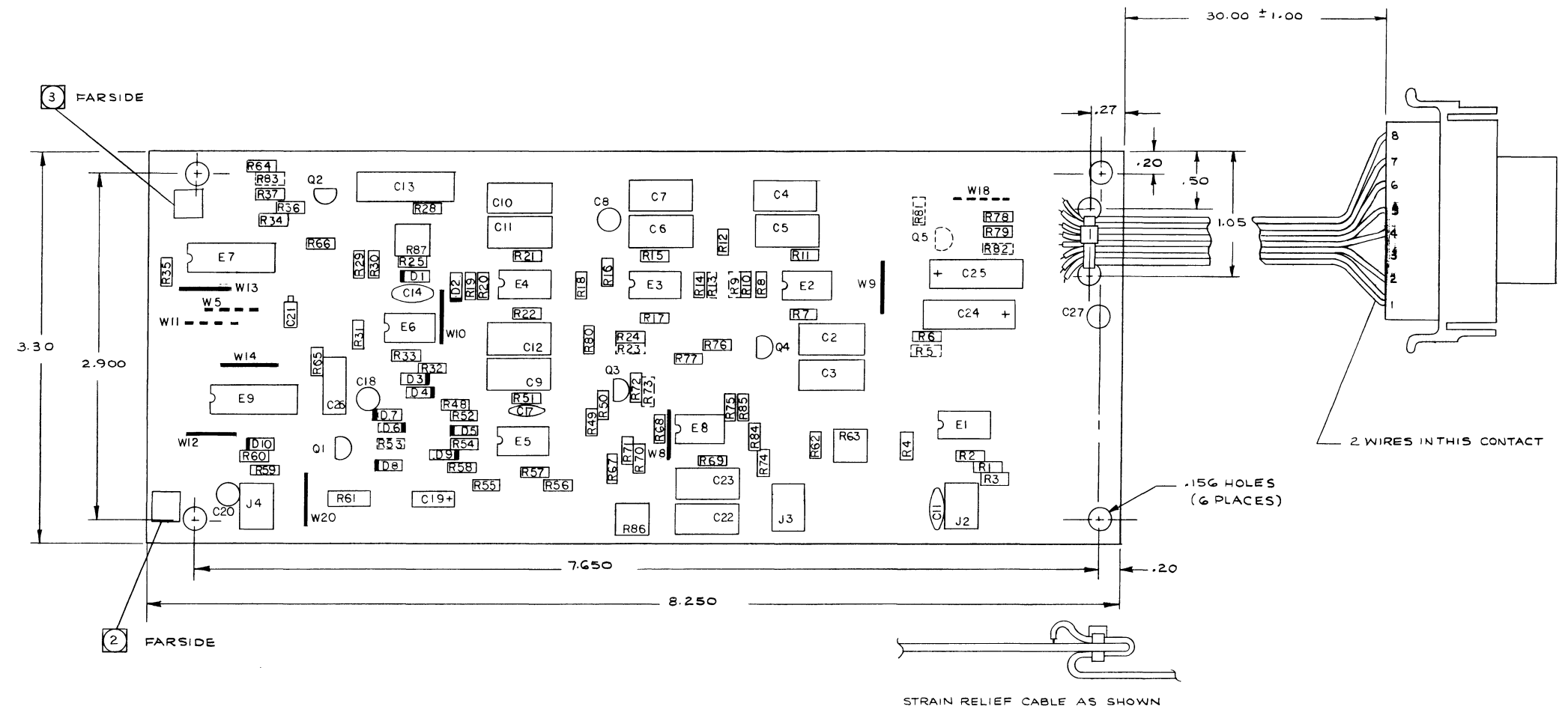
DRN: [Signature]	DATE: 1/21/76	FIRST USED ON: LAXX-LM	digital
CHK'D: [Signature]	DATE: 1/24/76	TITLE: ACOUSTIC COUPLER ASSY	
ENG: PE Nelson	DATE: 30 JAN 76		
PROD: [Signature]	DATE: 1/24/76		
NEXT HIGHER ASSY:			
D-AD-7012144-0-0		SIZE CODE: D AD 7012356-0-0	NUMBER: [Blank]
SCALE: 1:1			REV.:
SHEET: 3 OF 4			

REV.:	
CHANGE NO.:	
CHK:	

DEC FORM NO. 080 102-D

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- NOTES:
1. SELECT-IN-TEST RESISTORS ARE: R5, R9, R13, R19, R23, R26, R27, R71, R73
 2. MARK APPLICABLE DASH NO. IN THESE LOCATIONS
-1 DAA
-2 ACOUSTIC ONLY USED ON 490770
 3. MARK LATEST REV LETTER IN THIS LOCATION
 4. ——— INDICATES JUMPER, USE ITEM 2; (W1-W4, W6, W7, W17)



REV.	
CHG	
REVISIONS	CHANGE NO.

DRN: <i>John W. ...</i>	FIRST USED ON	LAXX - LM	digital
CHK: <i>...</i>	TITLE	ACOUSTIC COUPLER ASSY	
ENG: <i>E. M. ...</i>	PROJ. ENG: <i>E. M. ...</i>	NEXT HIGHER ASSY.	
PROD: <i>...</i>	SCALE	SIZE CODE	NUMBER
	SHEET 4 OF 4	D AD	7012356-0-0
		DIST.	REV.

REV. 1
D AD 7012356-0-0

CHAPTER 20

APL OPTION KIT (LAXX-PK)

20.1 APL INTRODUCTION

The APL Option is a distinct character set, which is one in a series of optional character sets that can be installed in a DECwriter. The APL Option provides a DECwriter with the ability to produce the 95 printing or spacing characters in the APL set. This feature adds a complete character set to the existing character set in a standard terminal. The two sets are: the standard ASCII set and the APL set.

The APL Option contains special characters and symbols not found in a standard set. In addition, the APL also contains the standard numerals (0 through 9) and a complete alphabet in small capital letters. (Print is 5 dots high and 7 dots wide rather than 7×7 dots as in a standard sized capital letter.)

Normal timing, print head configuration, and mechanical operation of the DECwriter is unaffected by the installation of an Optional Character Set (OCS) such as the APL. The option simply substitutes the incoming ASCII character with a print head pattern that causes a different character or symbol to print.

There are two methods of changing from one character set to the other: by local control using front panel switches or by remote control utilizing codes in the incoming data. Local character set selection always takes precedence and overrides all selection codes on the incoming data.

The optional character set circuit board has provisions for installing either of two character memory configurations. One configuration uses two ROMs, while the other uses three PROMs. Generally the ROMs are more costly than the PROMs (because the storage of the character pattern is actually a physical characteristic of the chip) and only become cost effective when many sets of the same character style are to be programmed. PROMs are less expensive (because they have a programmable memory) and are usually only used when a small number of terminals are having a distinctive character set installed. This is because the programming cost of each PROM is relatively high and is not justifiable for large numbers of PROMs.

The APL Option (LAXX-PK) is always installed in the ROM configuration.

20.2 APL FUNCTIONAL BLOCK DIAGRAM

Figure 20-1 shows the functional block diagram of the Optional Character Set (specifically, the APL Option) in a typical installation. The major difference between this installation and installations for the other DECwriter options is the point at which the Optional Character Set samples the data on the M7728 Logic Board. Most other options utilize a bidirectional line that monitors the incoming character data on the lines between the UART and the Character Buffer. These options also utilize the Data Available signal as a strobe to transfer either incoming characters out of the UART or option-generated characters into the Character Buffer. Figure 20-1 shows the Optional Character Set monitoring the data *after* the Character Buffer. Therefore, all other options have performed their functions (inserting messages or codes for carriage returns, spacing, or line feeds) *before* the data is available to the OCS option. This incoming data, whether serial in (SI) from an external source or local keyboard data, is cabled from the Logic Board to the Expander Option Mounting Board and is present at the input of the Optional Character Set at location F. This data also contains the column count codes from the Column Increment Counter on the Logic Board. These three lines represent 8 of the 10 possible positions of the print head in each character cell and are used by the option to synchronize the 7-column dot output for each character with the print head's actual physical position. The APL ROM (or OCS PROM) converts the 7-bit ASCII data into the print head dot pattern for APL characters. The ASCII-to-APL conversion is shown in Figure 20-2.

The output of the ROMs is applied to Line Drivers where the Remote Control Circuit samples the lines and decodes remote commands that switch from one character set to the other. The code SO (017₈) switches to APL and the code SI (016₈) switches to standard ASCII.

The Local Control Circuit monitors the positions of the front panel CHAR SET LOCK switch and the ALT CHAR SET switch. These switches provide operator control over the selection of which character set will print and override all set selection codes on the incoming data line. When the CHAR SET LOCK switch is in the up position, the incoming data can control set selection irrespective of the position of the ALT CHAR SET switch. Depressing the CHAR SET LOCK switch establishes local control and locks the option into the set established by the position of the ALT CHAR SET switch. If the ALT CHAR SET switch is up, the standard ASCII set is selected; when down, the APL (or OCS) set is selected.

The Character Set Control Logic determines which set the terminal will print and, if the APL is selected, disables the Line Drivers on the M7728 Logic Board and enables the Line Drivers on the option. Conversely, if the standard ASCII set is selected, the option Line Drivers are disabled and the Logic Board Line Drivers are enabled.

The character set selected (whether by local or remote control) is indicated by the illumination of either the front panel STD or ALT lights.

20.3 APL BASIC BLOCK DIAGRAM

The basic block diagram for the Optional Character Set (APL Option) is shown in Figure 20-3. This diagram is a simplified representation of the optional character set circuit schematic (D-CS-M7732-0-1). Circuit designations and pin numbers indicated on Figure 20-3 correlate with corresponding components on the schematic. Buffers, inverters, and other components that do not have major operational functions are omitted from the block diagram. The discussion of this option is divided into two major sections: character storage and character set selection.

20.4 CHARACTER STORAGE

One of two character storage memory configurations can be installed on the OCS board. In the APL Option, ROMs in sockets E10 and E11 store the dot pattern for each character in the APL set. For any other set, three PROMs can be programmed for a unique set and installed in sockets E4, E7, and E12. The installation of E15 is also required when using PROMs. Only one configuration is installed at a time.

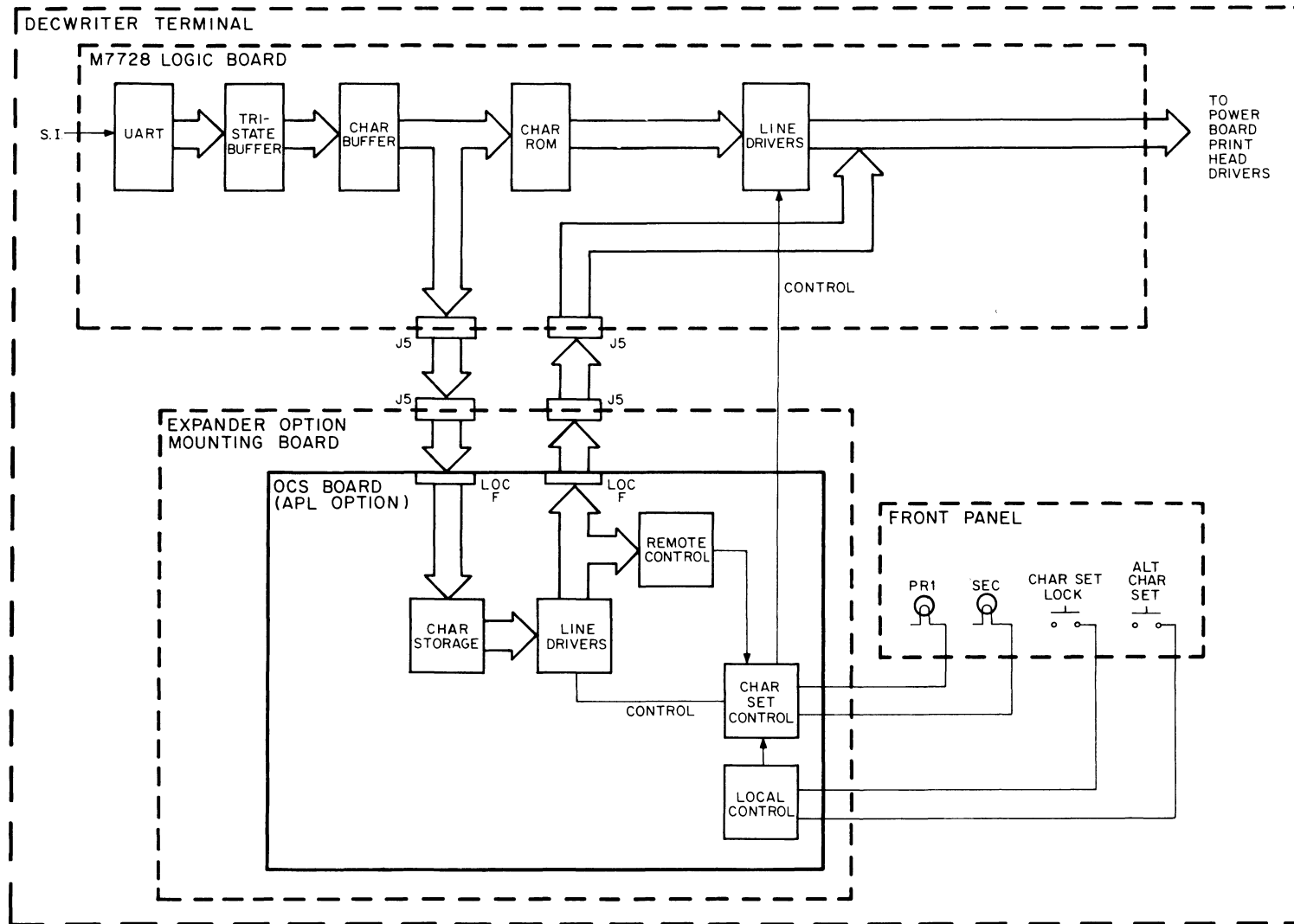


Figure 20-1 APL Character Set Functional Block Diagram

Bits				0	0	0	0	1	1	1	1
b ₇				0	0	1	1	0	0	1	1
b ₆				0	0	1	1	0	0	1	1
b ₅				0	1	0	1	0	1	0	1
b ₄	b ₃	b ₂	b ₁	Control Codes		Figures and Numbers		Upper Case		Lower Case	
0	0	0	0	NUL	DLE	SP	0	—	*	◇	Ⓢ
0	0	0	1	SOH	DC1	~	1	α	?	Α	Ⓠ
0	0	1	0	STX	DC2)	2	⊥	ƒ	Β	Ⓡ
0	0	1	1	ETX	DC3	<	3	η	Γ	ϒ	Ⓢ
0	1	0	0	EOT	DC4	⊥	4	⊥	~	Ⓡ	Ⓢ
0	1	0	1	ENQ	NAK	≡	5	ε	↓	Ⓡ	Ⓢ
0	1	1	0	ACK	SYN	>	6	—	u	Ⓢ	Ⓢ
0	1	1	1	BEL	ETB	⊥	7	∇	ω	Ⓢ	Ⓢ
1	0	0	0	BS	CAN	∇	8	Δ	⊃	Ⓢ	Ⓢ
1	0	0	1	HT	EM	^	9	ι	↑	Ⓢ	Ⓢ
1	0	1	0	LF	SUB	≠	(◊	c	Ⓢ	Ⓢ
1	0	1	1	VT	ESC	÷	⊥	'	←	Ⓢ	Ⓢ
1	1	0	0	FF	FS	∇	‡	□	⊥	Ⓢ	Ⓢ
1	1	0	1	CR	GS	+	x	⊥	→	Ⓢ	Ⓢ
1	1	1	0	SO	RS	◊	‡	Ⓢ	⊥	Ⓢ	Ⓢ
1	1	1	1	SI	US	/	\	Ⓢ	—	Ⓢ	DEL

A. Alternate (APL) Character Set

Bits				0	0	0	0	1	1	1	1
b ₇				0	0	1	1	0	0	1	1
b ₆				0	0	1	1	0	0	1	1
b ₅				0	1	0	1	0	1	0	1
b ₄	b ₃	b ₂	b ₁	Control Codes		Figures and Numbers		Upper Case		Lower Case	
0	0	0	0	NUL	DLE	SP	0	Ⓢ	Ⓢ	~	Ⓢ
0	0	0	1	SOH	DC1	!	1	Α	Ⓡ	α	Ⓡ
0	0	1	0	STX	DC2	"	2	Β	Ⓡ	β	Ⓡ
0	0	1	1	ETX	DC3	#	3	Ⓡ	Ⓢ	c	Ⓢ
0	1	0	0	EOT	DC4	\$	4	Ⓡ	Ⓢ	d	Ⓢ
0	1	0	1	ENQ	NAK	%	5	Ⓡ	Ⓢ	e	Ⓢ
0	1	1	0	ACK	SYN	&	6	Ⓢ	Ⓢ	f	Ⓢ
0	1	1	1	BEL	ETB	/'	7	Ⓢ	Ⓢ	s	Ⓢ
1	0	0	0	BS	CAN	(8	Ⓢ	Ⓢ	h	Ⓢ
1	0	0	1	HT	EM)	9	Ⓢ	Ⓢ	i	Ⓢ
1	0	1	0	LF	SUB	*	;	Ⓢ	Ⓢ	j	Ⓢ
1	0	1	1	VT	ESC	+	;	Ⓢ	Ⓢ	k	Ⓢ
1	1	0	0	FF	FS	∇	<	Ⓢ	Ⓢ	l	Ⓢ
1	1	0	1	CR	GS	—	=	Ⓢ	Ⓢ	m	Ⓢ
1	1	1	0	SO	RS	◊	>	Ⓢ	Ⓢ	n	Ⓢ
1	1	1	1	SI	US	/	?	Ⓢ	Ⓢ	o	DEL

B. Standard (ASCII) Character Set

CP-2384

Figure 20-2 Bit Assignments for ASCII and APL Character Sets

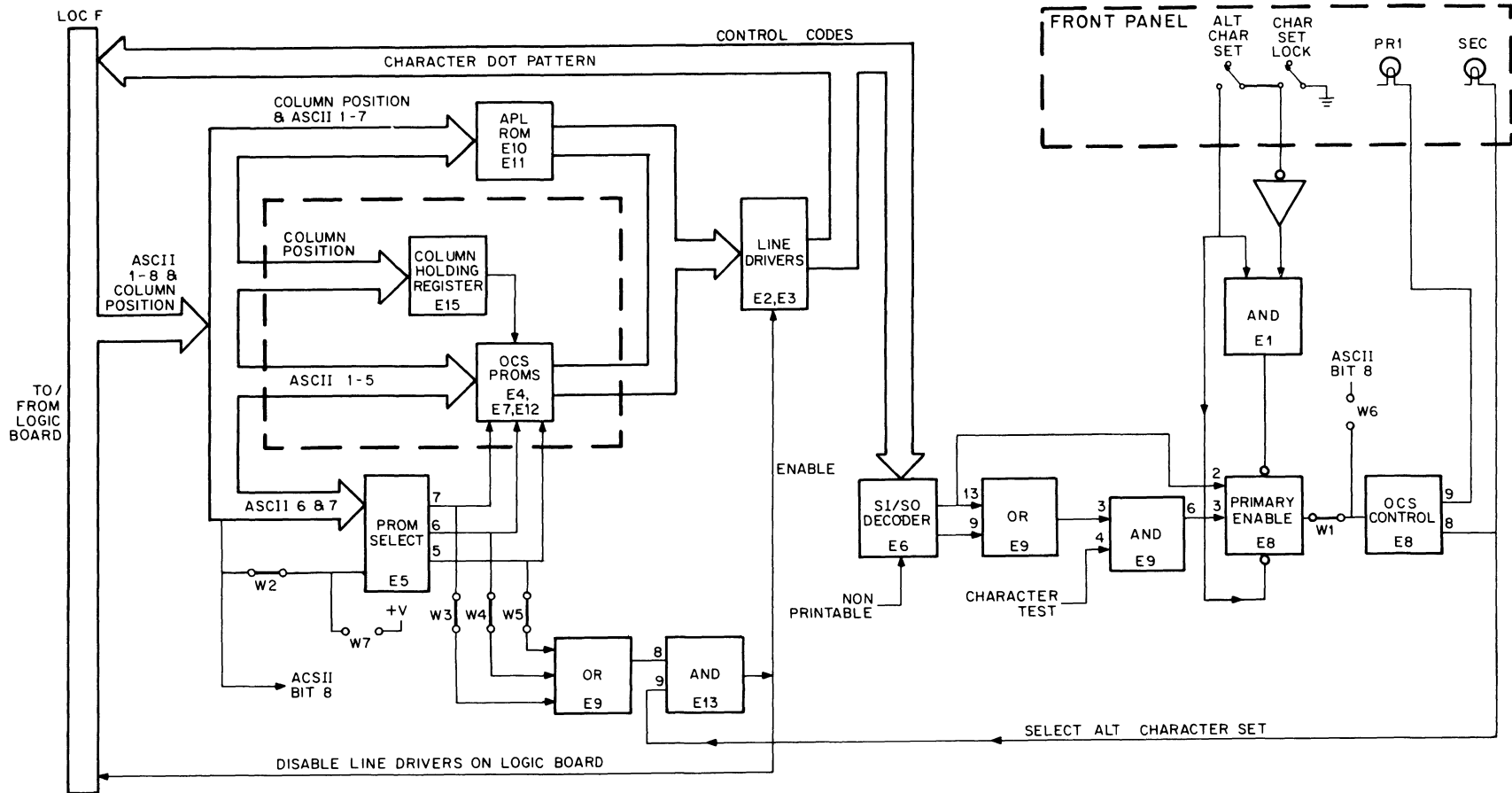


Figure 20-3 APL Option Basic Block Diagram

In the APL Option, 7-bit ASCII character codes and 3-bit column position data is applied to the APL ROMs E10, E11. The dot pattern for each ASCII character is substituted with the dot pattern for the APL character by the ROMs. (E10 stores upper and lower case letters and E11 stores the figures and numbers.) Figure 20-4 shows the print head dot pattern for the ASCII character "H" and its corresponding APL symbol delta (Δ).

Below each character are the ROM data words that are required to print each character. The information in rows 1-7 define a row of the character and the information in row 8 determines whether the character is printable or non-printable (such as a control character). As the print head moves across the 10 column increments that make up each character, the Column Increment Counter on the Logic Board outputs positioning data for each of the seven possible printing locations. Because columns 8 and 9 are always blank, only three binary-coded lines are required for proper spacing between characters to define the remaining eight column increments. The three column position lines plus the ASCII lines are applied either directly to the ROMs or through storage Latch E15 to the three PROMs, if they are used. The eight possible codes are used by the ROMs as addresses to access the proper dot pattern for the coinciding head position. For example: if an ASCII "H" is typed and the APL Option is installed, the ASCII "H" code accesses the " Δ " location in the APL ROM and the head position addresses the column increments starting with column 0 and continuing to column 7. At column 2 the dot pattern code accessed is 000 000 which causes the solenoids in the print head to produce the dot display as shown in column 2. After the head reaches column 10 (which is actually column 0 of the next character), another ASCII character is ready to be converted to APL and the Column Increment Counter is back at zero, ready to start addressing the increments in the new character. Data stored in the eight row of each character determines whether the character is a printable character (i.e., any character or command that causes the print head to move). All non-printable control commands are detected in the character ROMs on the Logic Board. Character set switching commands pertaining to the option (SO or SI) are also detected by these ROMs and the dot information is applied to the option on the bidirectional SEL lines that are connected to the option at the output of the Line Drivers E2, E3.

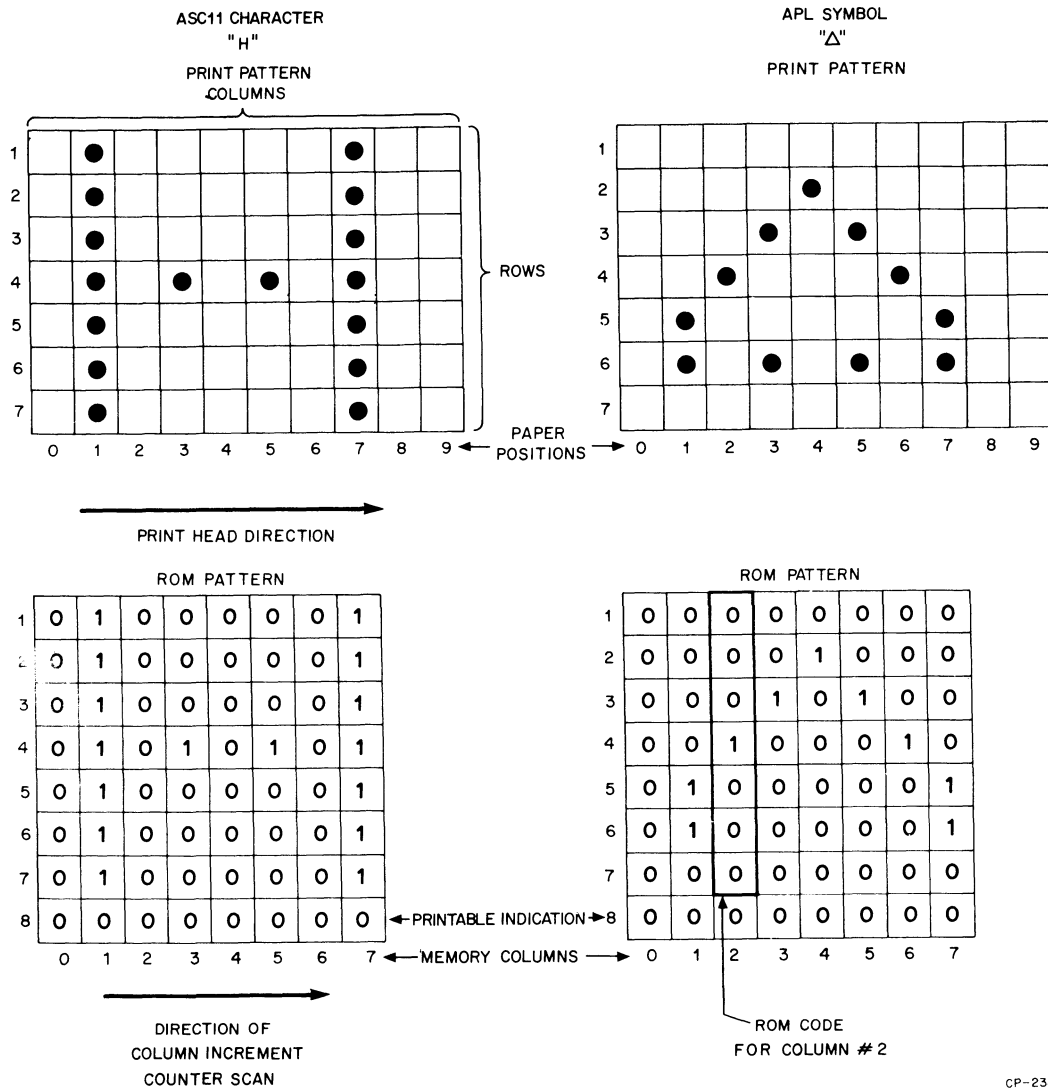
Jumpers W3, W4, and W5 (which are normally installed) can be used to selectively override the character substitution from either the ROMs or the PROMs. Normally, with the OCS set selected, an ASCII character is automatically substituted with a character from the optional storage location. But by utilizing these jumpers, selective parts of the optional character storage can be removed from this automatic substitution. When a certain portion of the OCS set is prevented from being accessed, the characters are then taken from the standard character set stored in the ROMs on the Logic Board.

Table 20-1 lists various jumper configurations for both ROM and PROM configurations. As shown by this table, with Jumper W3 installed and W4 and W5 cut out, the selection of either the upper or lower case characters stored in the option's ROMs or PROMs is prevented. This means that even if the OCS set is selected, the print head pattern for these upper and lower case characters are always taken from the standard character set and only the figures and numbers of the OCS set will print.

Even though Jumpers W3, W4, or W5 can be cut and eliminate part of the OCS from being selected, when the OCS is selected the front panel ALT CHARACTER SET light still illuminates as if no jumper were cut.

20.5 CHARACTER SET SELECTION

The selection of either of the character sets installed in a DECwriter can be controlled locally or remotely. Local switching is controlled by the positions of the front panel CHAR SET LOCK and ALT CHAR SET switches. The output of these switches connects to the set and reset pins of Primary Enable flip-flop E8. Remote switching control is connected to the clock and data pins of E8. The set and reset signals take control over the signals on the clock and data input pins of E8. When the CHAR SET LOCK switch is depressed and the ALT CHAR SET switch is up, E8 is set by the low signal on pin 4. This action places a high level on pin 12 of the OCS Control flip-flop E8. The OP CLK signal on pin 11 of E8 clocks this high out on pin 9 of E8. As the high level on pin 9 is applied through E13 to illuminate the front panel STD CHARACTER SET light, a low level from pin 8 is applied to pin 9 of AND gate E13. This low level produces a high on pin 10 of E13 which holds the Line Drivers (E2 and E3) on the OCS board disabled and enables the Line Drivers on the Logic Board to pass the dot pattern of the standard character set to the print head drivers.



CP-2386

Figure 20-4 Typical ASCII/APL ROM Mapping and Print Pattern

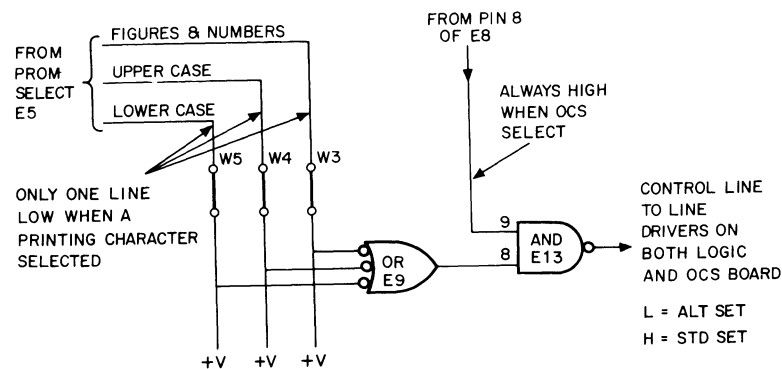
Table 20-1
OCS Jumper Configurations

Specified Secondary Group Selected	Storage Device Installed			Jumper Status		
	ROMs	OR	PROMs	W3	W4	W5
Figures and Numbers	E10		E4	IN	OUT	OUT
Upper Case	E11		E7	OUT	IN	OUT
Lower Case	E11		E12	OUT	OUT	IN

Note: Normal configuration has W3, W4, W5 installed; selecting all secondary groups.

If the ALT CHAR SET switch is depressed (while the CHAR SET LOCK switch is in the down position), a reset signal is applied to E8 pin 1 and the next pulse from the Option Clock transfers a low level through E8 onto pin 9. In this instance the low on pin 9 extinguishes the STD CHARACTER SET while the high level on pin 8 causes the ALT CHARACTER SET light to illuminate. This high level is also applied to pin 9 of AND gate E13 where it combines with a high level generated by the PROM Select E5 to produce the control signal that disables the Line Drivers on the Logic Board and enables the Line Drivers on the Option Board. Thus, the dot pattern for an optional character is sent to the head drivers to be printed.

Figure 20-5 shows why Jumpers W3, W4, and W5 have such an overriding effect on the selection of the OCS set. When the OCS is selected (whether by local or remote command), the input to E13 on pin 9 is always a high level. Another high level is required on pin 8 to force the desired low level on the output of E8 that causes the OCS Line Drivers to energize and supply the optional character. If pin 8 of E13 is held low through E9, the OCS can never be selected because the output of E13 is always forced to a high level which enables the Line Drivers on the Logic Board. The level on pin 8 is established by Prom Select E5 and the W3, W4, and W5 jumper configuration. The Prom Select E5 places a low level on one of the three output lines for each printable character. The low level passes through one of the jumpers to OR gate E9 where it is inverted and applied as a high level to E13. Cutting out the jumper in this signal path prevents the Prom Select output from qualifying AND gate E13. Therefore, anytime a jumper is cut, all characters from the section of the PROM the jumper is in series with do not print because the low out of Prom Select for the section chosen never forces E13 high.



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Figure 20-5 Jumper Control over Character Set Selection

Remote character set selection, when the CHAR SET LOCK switch is up, is accomplished either by inserting command codes in the incoming data or by utilizing the eighth level bit in each ASCII character code.

Depending upon the configuration on the Logic Board, the eighth level bit is used either as a switching command or for parity error detection. The LAXX-PK is shipped ready for installation into a system that utilizes the eighth bit as a parity error bit. Should parity error occur when the OCS set is selected, the option's substitution is inhibited and the logic board controls the insertion of the parity error printout indication.

The two command codes used to change character sets are: Shift In (SI - 017₈), shift into standard character set from alternate (APL or OCS) character set and shift out (SO - 016₈) shift out of standard character set into alternate. These two commands are decoded by the character ROMs on the Logic Board and are sent to the OCS board via the interconnecting bidirectional lines (sections 1, 2, 3, 6, and PRINTABLE). These lines are decoded by E6 and, depending on the command, a low level signal is applied to OR gate E9. If an SO command is detected, a low is applied to the data input of E8 (pin 2) and the CHAR TEST signal from the Logic Board is used to clock this low through to pin 12 of OCS Control flip-flop E8. The OP CLK signal clocks this low through E8, forcing pin 9 low and pin 8 high. The option switches out of the standard character set and into the alternate set. When the SI code is received, the action is similar; pin 2 of E8 is now high and is clocked through both flip-flop sections to cause the option to switch back into the standard character set.

NOTE

If the eighth bit method of control is used, provisions for monitoring parity errors are eliminated.

When the eighth level code is used to switch character sets, Jumpers W1 and W2 must be cut and Jumpers W6 and W7 must be installed. This action removes the effect of *all* other switching controls (even front panel switches have no effect now). With W6 installed, the level of bit 8 is applied directly to the data input (pin 12) of OCS Control E8. This level is clocked through E8 by the OP CLK signal and effects the option just like any other switching command: bit 8 high, switch into standard set; bit 8 low, switch out of standard set. Note that Jumpers W3, W4, and W5 still have the final control irrespective of the method of character set selection.

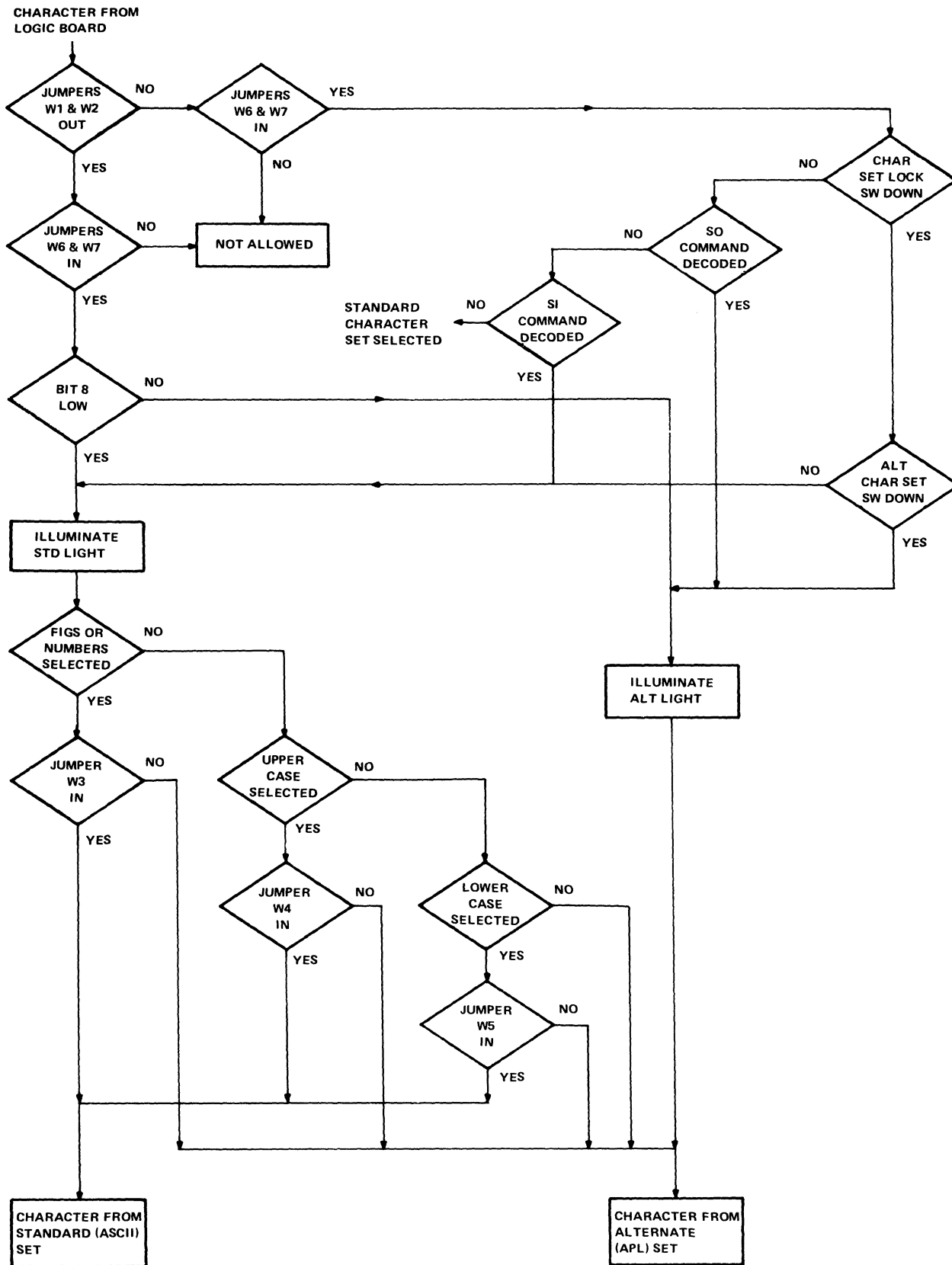
Figure 20-6 shows the complete operational sequence for the OCS set character selection.

20.6 TROUBLESHOOTING

The troubleshooting chart in Table 20-2 lists the common trouble symptoms that could be observed during installation checkout or normal operation.

20.7 LAXX-PK PRINT SET

The figures at the end of this chapter are the LAXX-PK print set.



CP-2388

Figure 20-6 Operational Sequence for OCS Set

Table 20-2
Troubleshooting for APL Option Kit (LAXX-PK)

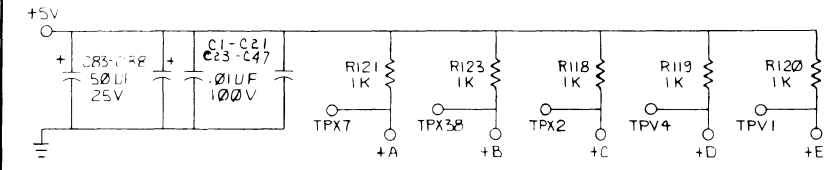
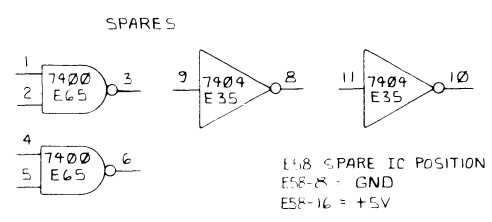
Symptom	Problem Area	Probable Cause	Action	Reference
1. After installation, improper operation or no operation of terminal	Cabling	Wrong cabling connections	Check all cabling between M7728 Logic Board, Expander Board, and Front Panel Control Board	Figure 9-4
	Option location	Option inserted in wrong location on Expander Board	Install APL Option in location F	
	ROMs	Improper insertion	Check insertion of ROMs for proper fit	
2. With ALT CHAR SET and CHAR SET LOCK switches down and terminal printing in APL, the PRI light remains illuminated	Control Board	Jumper W1 not cut out	Remove W1	
3. Able to switch between character sets using switches but not with CNTL N or CNTL O codes when CHAR SET LOCK switch is in up position	Function Decoder E6	Not decoding commands	Check E6 for SI at pin 7 and SO at pin 6	D-CS-M7732-0-1, Sheet 2
	Timing between Logic Board and Option Board	CHAR TEST pulse not being received	Check E14 pin 11 for the 50-ns CHAR TEST pulse	D-CS-M7732-0-1, Sheet 2
4. Able to switch between character sets using control codes but not using switches	Cabling	Cable between Expander Board and Front Panel Control Board defective or inserted incorrectly	Check for continuity between ends	

CHAPTER 21
M7728 PRINT SET

CHAPTER 21
M7728 PRINT SET

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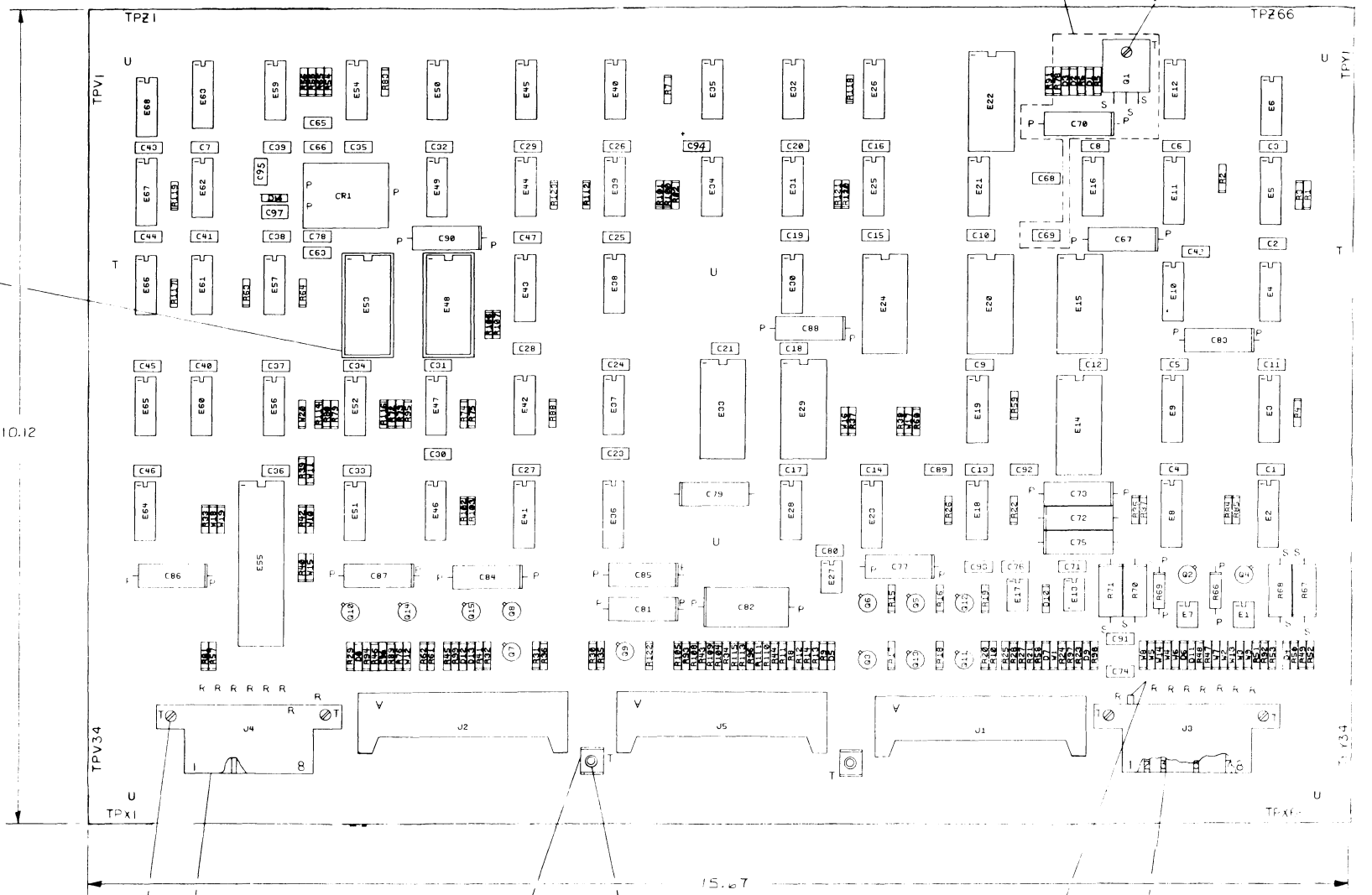
- NOTES:**
- CONNECTORS:
 J1 → J1 POWER BOARD
 J2 → KEYBOARD
 J3 → 20MA SERIAL LINE
 J4 → OPTIONAL INTERFACE PORT
 J5 → J5 EXPANDER OPTION MOUNTING BOARD
 - COMPONENTS WITHIN OUTLINE NOT INSERTED IN PREFERRED CONFIGURATION
 - REF DES NOT USED ARE:
 C60, C61, C62, C64, C98-C58
 - MAXIMUM REF DES USED ARE:
 W20, R123, E66, C97, D14, J5, CR1, Q15



8640	1	8
LM301A	—	—
1702A	—	16
7413	8	16
74150	12	24
74154	12	24
74161	8	16
74175	8	16
74190	8	16
74193	8	16
7442	8	16
7439	8	16
7493	10	5
MK2600P	12	24
UART	3	1
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS



SIZE CODE NUMBER
 DCS M7728-0-1 REV C

92 93
 19 23 (QTY 8)

94 96

25 19
 23 (QTY 4) LOCATIONS 3,5,7 ONLY

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
FIRST USED ON OPTION MODEL				
LA36				
ETCH BOARD REV. B				
PARTS LIST				
DRY		DATE		
CHK'D.		DATE		
ENG.		DATE		
PROJ. ENG.		DATE		
PROD.		DATE		
NEXT HIGHER ASSY				
DEC NO.		EIA NO.	DEC NO.	EIA NO.
SEMICONDUCTOR CONVERSION CHART				
SCALE		SHEET		OF 9
SIZE CODE		NUMBER		REV.
DCS		M7728-0-1		C

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1-0-8222W DCS 2

D
C
B
A

D
C
B
A

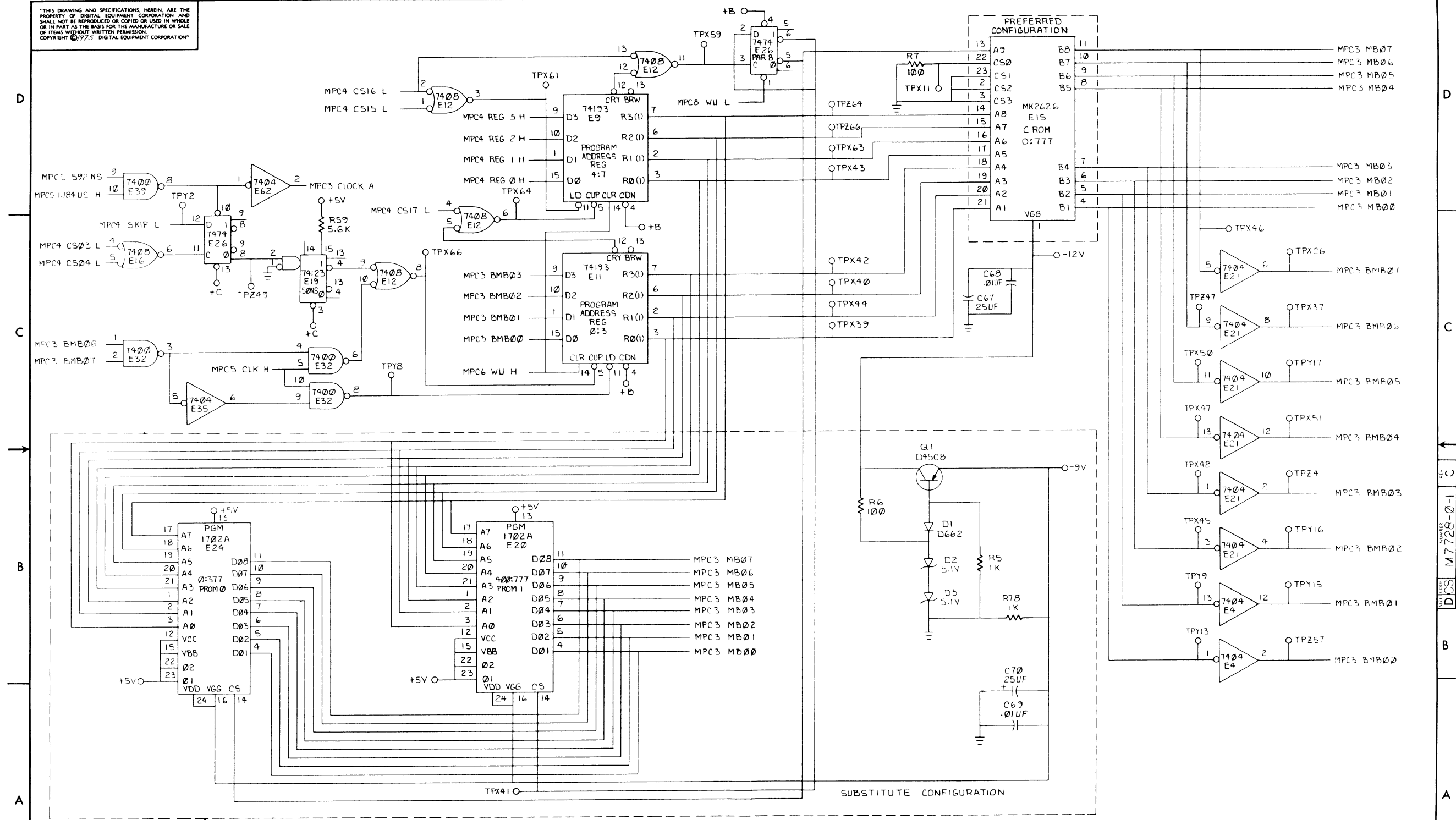
QTY/VAR		REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
REFERRED	SUBSTITUTE				
REF	REF		ASSY/DRILLING HOLE LAYOUT	AH-M7728-B-5	1
REF	REF		MODULE ECO HISTORY	B-MH-M7728-B-6	2
1	1		ETCHED CIRCUIT BOARD	5011682	3
4	4	C71, C76, C80, C97	CAP39 PF 100V 5% DIPPED MICA	1000010	4
1	1	C91	CAP 470PF 100V 5% DIPPED MICA	1000024	5
1	1	C82	CAP 22UF 100V 10% NYLAR	1000037	6
3	3	C72, C75, C79	CAP 047UF 100V 10% NYLAR	1000051	7
5	6	C67, C73, C77, C81, C90	CAP 25UF 25V AL EL	1000075	8
53	54	C1-C21, C63, C68, C74, C78, C89, C92-C98	CAP .01UF 100V DISC	1001610-01	9
3	3	C85, C86, C96	CAP .005UF 100V DISC	1001765	10
6	6	C83-C88	CAP 50UF 25V AL EL	1001796	11
0	1		DIODE D662	1100113	12
6	5	D5, D7, D8, D12, D14	DIODE D664	1100114	13
2	2	D9, D10	DIODE IN748A 3.9V 5% ZENER	1100122	14
1	1	D4	DIODE IN748A 3.3V 5% ZENER	1104860	15
1	1	D11	DIODE MCL1301	1105610	16
1	1	D6	DIODE IN4004	1105796	17
1	3	D13	DIODE 4M5JAZ1 5.1V 1% ZENER	1105873	18
2	2	J3, J4	CONN 8 PIN MATE-N-LOCK (HOUSING)	1209340-00	19
3	3	J1, J2, J5	CONN 40 PIN BERG	1209941-02	20
3	3	J1, J2, J5	LATCH LEFT FOR BERG	1209941-03	21
3	3	J1, J2, J5	LATCH RIGHT FOR BERG	1209941-04	22
12	12		SOCKET MATE-N-LOCK 61320-3	1209456-01	23
2	4	E48, E53	SOCKET 1C 24 PIN	1210693	24
1	1	J3	KEYING PLUG MATE-N-LOCK	1211595	25
1	1	R50	RES 47 1/2W 5% CC	1300202	26
5	6	R7, R33, R58, R91, R46	RES 100 1/2W 5% CC	1300229	27
1	1	R47	RES 150 1/2W 5% CC	1300250	28
2	2	R66, R69	RES 180 1/2W 5% CC	1300260	29
2	2	R49, R89	RES 220 1/2W 5% CC	1300271	30
1	1	R30	RES 330 1/2W 5% CC	1300295	31
3	3	R29, R34, R88	RES 470 1/2W 5% CC	1300316	32
25	27	R1, R4, R32, R35, R45, R52, R55, R61, R65, R76, R94, R99, R112, R118 - R123, R44	RES 1K 1/2W 5% CC	1300365	33
4	4	R67, R88, R70, R71	RES 1K 1W 5% CC	1300368	34
1	1	R31	RES 1.5K 1/2W 5% CC	1300391	35
26	26	R37, R48, R53, R63, R66, R102, R109, R110, R111, R113, R117, R100	RES 10K 1/2W 5% CC	1300479	36
1	1	R16	RES 59.0K 1/2W 1% 100PPM MF RN65D-F	1300525	37
2	2	R97, R98	RES 10 1/2W 5% CC	1301317	38
3	3	R13, R22, R26	RES 180 1/2W 5% CC	1301322	39
1	1	R48	RES 68K 1/2W 5% CC	1301327	40
2	2	R11, R92	RES 820 1/2W 5% CC	1301775	41
6	6	R36, R54, R56, R57, R59, R60	RES 5.6K 1/2W 5% CC	1301874	42
8	8	R72, R75, R79, R81, R85	RES 47K 1/2W 5% CC	1302177	43
6	6	R82, R87	RES 2K 1/2W 5% CC	1302388	44
1	1	R51	RES 470K 1/2W 5% CC	1302398	45
2	2	R27, R23	RES 511 1/2W 1% 100PPM MF RN65 D-F	1302411	46
1	1	R8	RES 100K 1/2W 5% CC	1302488	47
1	1	R18	RES 14.7K 1/2W 1% 100PPM MF RN65 D-F	1302941	48
2	2	R12, R14	RES 1.00K 1/2W 1% 100PPM MF RN65 D-F	1303114	49
2	2	R24, R28	RES 5.11K 1/2W 1% 100PPM MF RN65 D-F	1304854	50
1	1	R19	RES 3.48K 1/2W 1% 100PPM MF RN65 D-F	1305114	51

QTY/VAR		REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
REFERRED	SUBSTITUTE				
1	1	R15	RES 121K 1/2W 1% MF	1305255	52
2	2	R9, R10	RES 232K 1/2W 1% MF	1305424	53
2	2	R21, R25	RES 1M 1/2W 5% CC	1309595	54
1	1	R17	RES 30.1K 1/2W 1% MF	1311594	55
1	1	R20	RES 2.15K 1/2W 1% MF	1311853	56
0	1		TRANSISTOR D45C8	1510598	57
10	10	Q2-Q6, Q10-Q14	TRANSISTOR MPSA05	1510705	58
3	3	Q7, Q8, Q15	TRANSISTOR MPSA55	1510706	59
1	1	Q9	TRANSISTOR DEC6531B	1509338	60
1	1	CR1	CRYSTAL 1 6896 MHZ (WIRE LEADS)	1811689	61
11	11	E25, E26, E30, E31, E34, E37, E40, E44, E45, E50, E54	I C 7474	1905547	62
6	6	E32, E38, E39, E49, E60, E65	I C 7400	1905575	63
4	4	E10, E47, E52, E57	I C 7401	1905590	64
2	2	E66, E68	I C 7493A	1909054	65
6	6	E4, E21, E28, E35, E56, E62	I C 7404	1909686	66
2	2	E22, E33	I C 74154	1909701	67
1	1	E18	I C 7413	1909989	68
3	3	E5, E9, E11	I C 74193	1910018	70
1	1	E23	I C 7442	1910046	71
1	1	E61	I C 7437	1910091	72
1	1	E43	I C 74190	1910095	73
2	2	E14, E29	I C 74150	1910153	74
5	5	E6, E12, E16, E42, E64	I C 7408	1910155	75
3	3	E13, E17, E27	I C LM301AN DIP	1910282	76
3	3	E3, E36, E41	I C 7489	1910396	77
1	1	E19	I C 74123	1910436	78
1	1	E55	I C UART	1910459	79
2	2	E63, E67	I C 74161	1910650	80
2	2	E2, E8	I C 74175	1910651	81
2	2	E46, E51	I C 8093	1910837	82
1	1	E59	I C 8640	1911469	83
2	2	E1, E7	I C SOC75, 4N26	1911998	84
0	1		PROM 1702A PROGRAMMED PROMB	2308244	85
0	1		PROM 1702A PROGRAMMED PROMI	2308344	86
1	1	E53	ROM MK2627 (ALPHA SET ASCII)	2307046	87
1	1	E48	ROM MK2626 (NO SET ASCII)	2307146	88
1	0	E15	ROM MK2628 (CONTROL PROGRAM)	2308246	89
0	1		SCREW SLOTTED BIND HD 4 40 x5/16	9006010-4	90
0	1		NUT KEP 4 40	9006557	91
4	4		WASHER FLAT NYLON #6	9006707	92
4	4		EYELET (MATE-N-LOCK MOUNTING)	9006732	93
2	2		FASTON TERMINAL	9007113	94
0	A/R		THERMAL COMPOUND	9008268	95
2	2		EYELET (FASTEN MOUNTING)	9009000	96
7	7	W1-W5, W18, W20	WIRE, INSULATED JUMPER	9009185	97
1	1	C95	CAP .1UF 100V 20% DISC	0000330	98
1	1	R101	RES 270 1/4W 5% CC	1301972	99
1	1	C94	CAP 39UF 10V 10% STANT	1000076	00
A/R	A/R		WIRE, INSULATED JUMPER 30AWG	9105740	01
A/R	A/R		CEMENT, PERMA BOND #102	9009157	102

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE LA36 MPC SIZE CODE DCS NUMBER M7728-0-1 REV. C
SCALE / / SHEET 2 OF 9

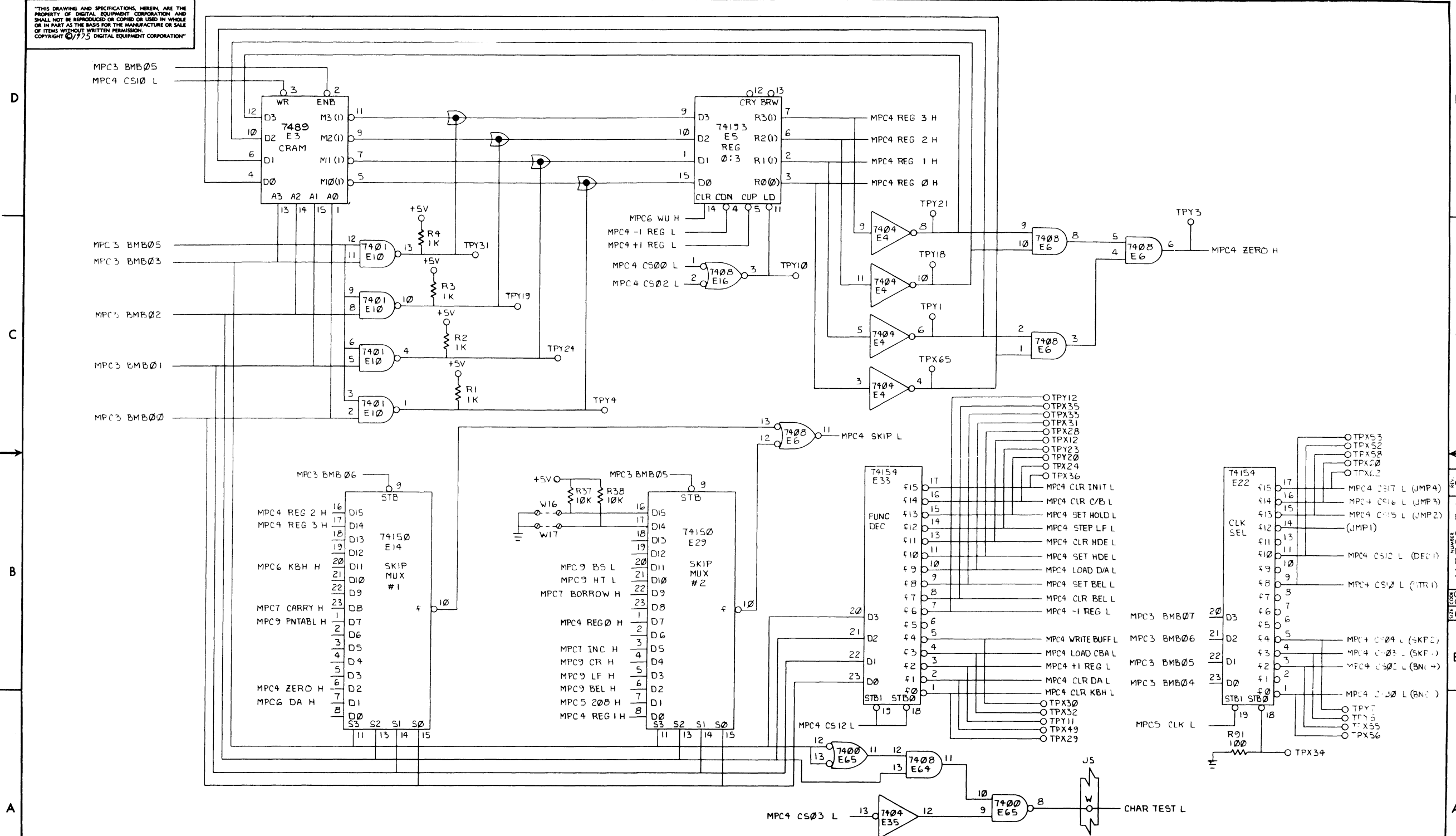
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REVISIONS		
CHK	CHANGE NO.	REV.

8	7	6	5	4	3	2	1	
TITLE LA36 MPC						SIZE CODE DCS	NUMBER M7728-0-1	REV. C
SCALE / /						SHEET 3 OF 9	DIST.	

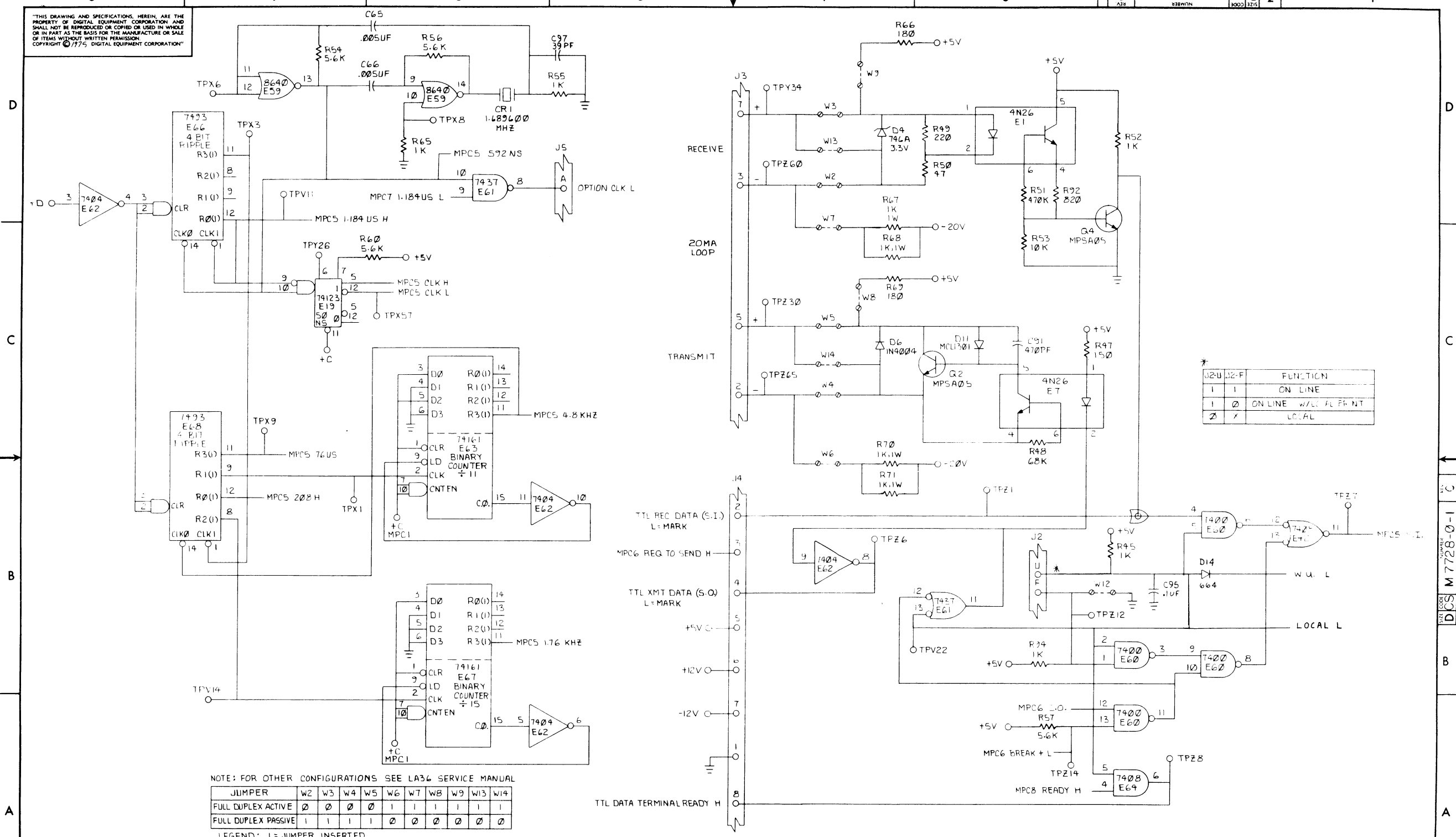
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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	LA36 MPC	SIZE CODE	DCS	NUMBER	M7728-0-1	REV.	C
SCALE	1:1	SHEET	4	OF	9	DIST.	

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J2-U	J2-F	FUNCTION
1	1	ON LINE
1	0	ON LINE WALL PL. FRONT
2	7	LOCAL

NOTE: FOR OTHER CONFIGURATIONS SEE LA36 SERVICE MANUAL

JUMPER	W2	W3	W4	W5	W6	W7	W8	W9	W13	W14
FULL DUPLEX ACTIVE	0	0	0	0	1	1	1	1	1	1
FULL DUPLEX PASSIVE	1	1	1	1	0	0	0	0	0	0

LEGEND: 1 = JUMPER INSERTED
0 = JUMPER NOT INSERTED

REVISIONS		
CHK	CHANGE NO.	REV.

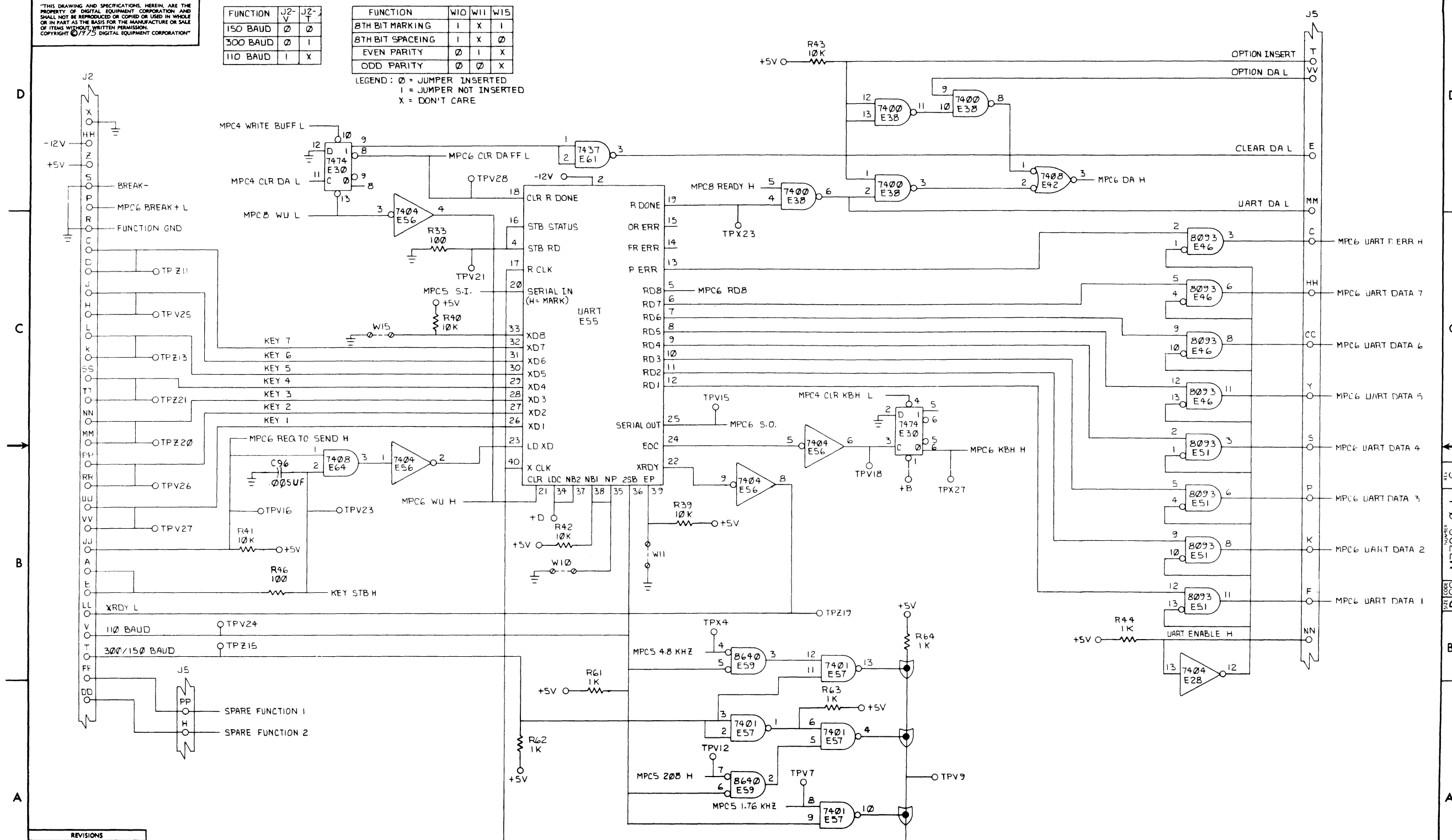
TITLE	LA36 MPC	SIZE	CODE	NUMBER	REV.
SCALE		SHEET	5	OF	9
DIST.		DCS		M7728-0-1	C

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FUNCTION	J2-V	J2-T
150 BAUD	Ø	Ø
300 BAUD	Ø	1
110 BAUD	1	X

FUNCTION	W10	W11	W15
8TH BIT MARKING	1	X	1
8TH BIT SPACING	1	X	Ø
EVEN PARITY	Ø	1	X
ODD PARITY	Ø	Ø	X

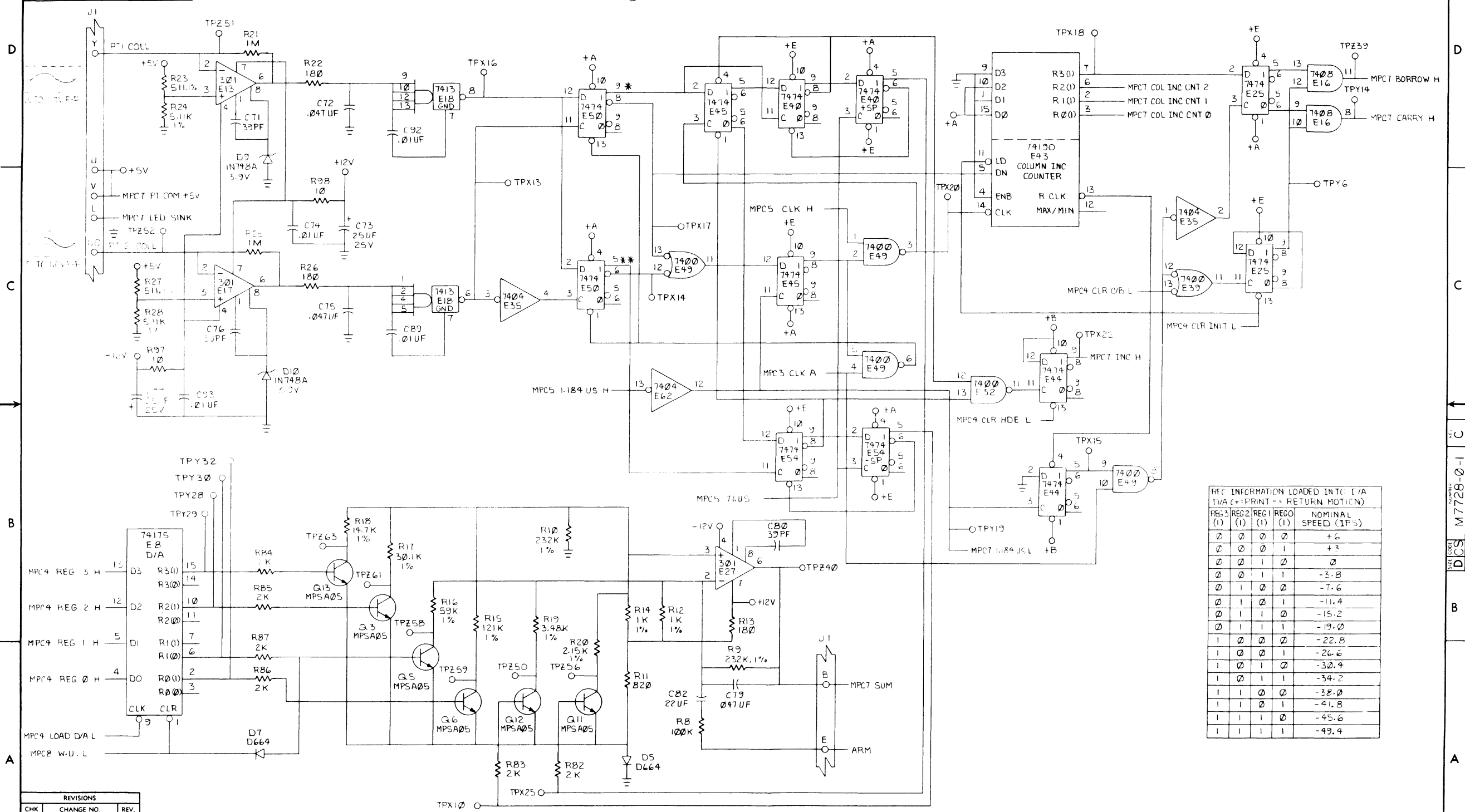
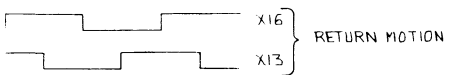
LEGEND: Ø = JUMPER INSERTED
 1 = JUMPER NOT INSERTED
 X = DON'T CARE



REVISIONS		
CHK	CHANGE NO.	REV.

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* PRINT MOTION (010*)
 ** RETURN MOTION (010*)

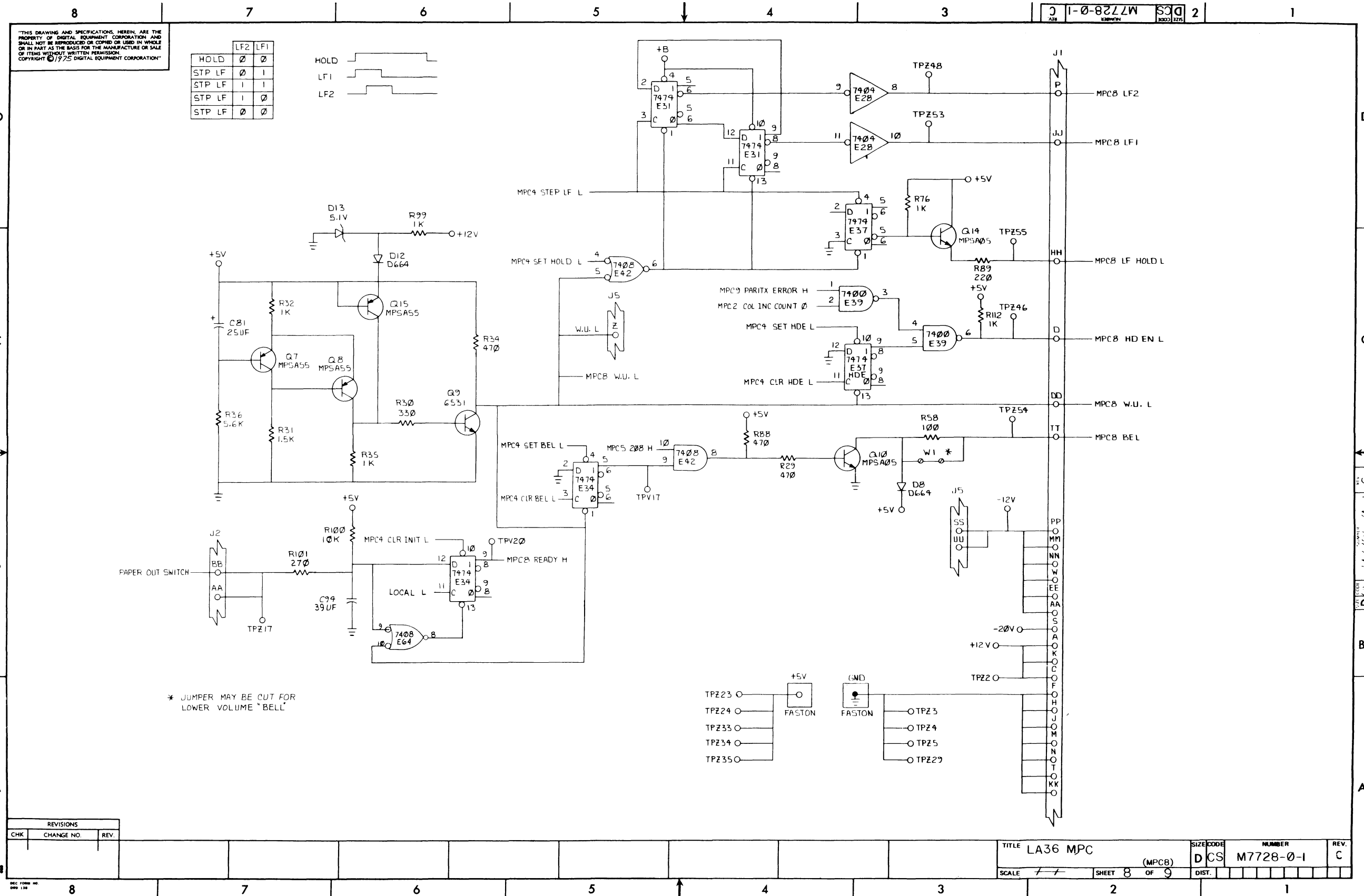


REG INFORMATION LOADED INTO E/A
 (1/A (+PRINT - RETURN MOTION))

REG3	REG2	REG1	REG0	NOMINAL SPEED (IPs)
0	0	0	0	+6
0	0	0	1	+3
0	0	1	0	0
0	1	0	0	-3.8
0	1	0	1	-7.6
0	1	1	0	-11.4
0	1	1	1	-15.2
1	0	0	0	-19.0
1	0	0	1	-22.8
1	0	1	0	-26.6
1	0	1	1	-30.4
1	1	0	0	-34.2
1	1	0	1	-38.0
1	1	1	0	-41.8
1	1	1	1	-45.6
1	1	1	1	-49.4

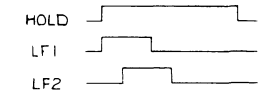
REVISIONS		
CHK	CHANGE NO.	REV.

TITLE LA36 MPC (MPC7) SIZE CODE DCS NUMBER M7728-0-1 REV. C



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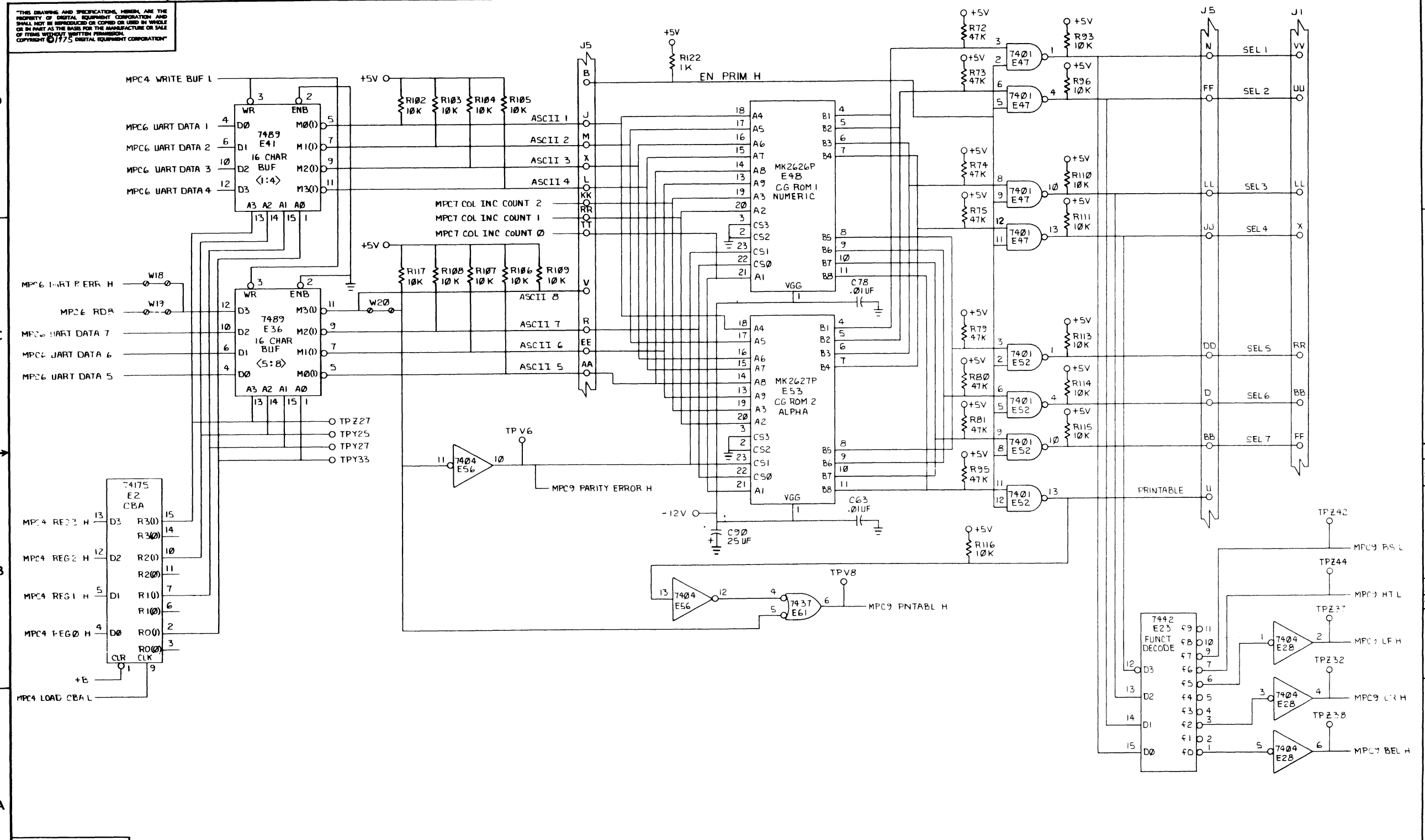
	LFI	LFP
HOLD	0	0
STP LF	0	1
STP LF	1	1
STP LF	1	0
STP LF	0	0



* JUMPER MAY BE CUT FOR LOWER VOLUME "BELL"

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	LA36 MPC	SIZE CODE	D CS	NUMBER	M7728-0-1	REV.	C
SCALE	1/1	SHEET	8	OF	9	DIST.	



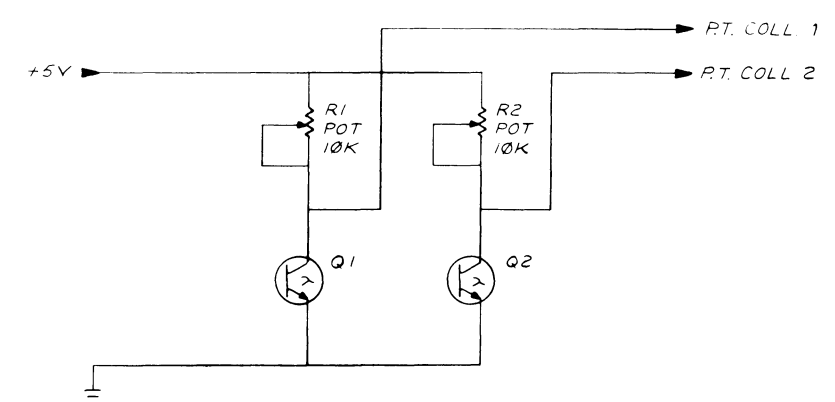
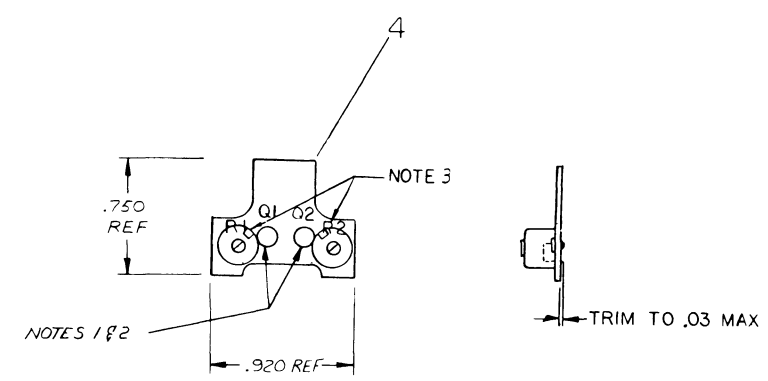
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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	LA36 MPC	SIZE CODE	D CS	NUMBER	M7728-0-1	REV.	C
SCALE	1:1	SHEET	9	OF	9	DIST.	

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- NOTES:**
1. HEAT APPLIED TO Q1 AND Q2 DURING SOLDERING SHALL NOT EXCEED 285° C FOR A PERIOD OF 15 SECONDS.
 2. FINISHED HOLE SIZE FOR MOUNTING Q1 AND Q2 SHALL BE .078 MIN., .083 MAX.
 3. R1 AND R2 MUST BE ORIENTED AS SHOWN, WITH NOTCH TOWARD CENTER OF BOARD.



REF	DESCRIPTION	QTY	PART NO	ITEM NO
	X-Y COORDINATE HOLE LOCATION		K-CO-5411049-0-1	1
	ASSY/DRILLING HOLE LAYOUT		D-AH-5411049-0-5	2
	MODULE ECO HISTORY		B-MH-5411049-0-6	3
	ETCHED CIRCUIT BOARD		D-IA-5010730-0-0	4
2	R1, R2		POTENTIOMETER 10K 1309150-12	5
2	Q1, Q2		PHOTOTRANSISTOR 1511906	6

QTY	REF DESIGNATION	DESCRIPTION	PART NO	ITEM NO
PARTS LIST				
	ETCH BOARD REV	B		

DRN	DATE	 EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
CHK'D	DATE	
ENG	DATE	
PROB. ENG	DATE	
PROD.	DATE	
NEXT HIGHER ASSY		
TITLE		LA36
ENCODER PC BOARD		
PHOTOTRANSISTOR		
SIZE CODE	NUMBER	REV.
DCS	5411049-0-1	3
SCALE		
SHEET 1 OF 1		

REV	DESCRIPTION
1	INITIAL
2	1/6/75
3	5411049-00002
4	C. B. MOFF
5	5411049-00001
6	CHANGE NO.
7	REV

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

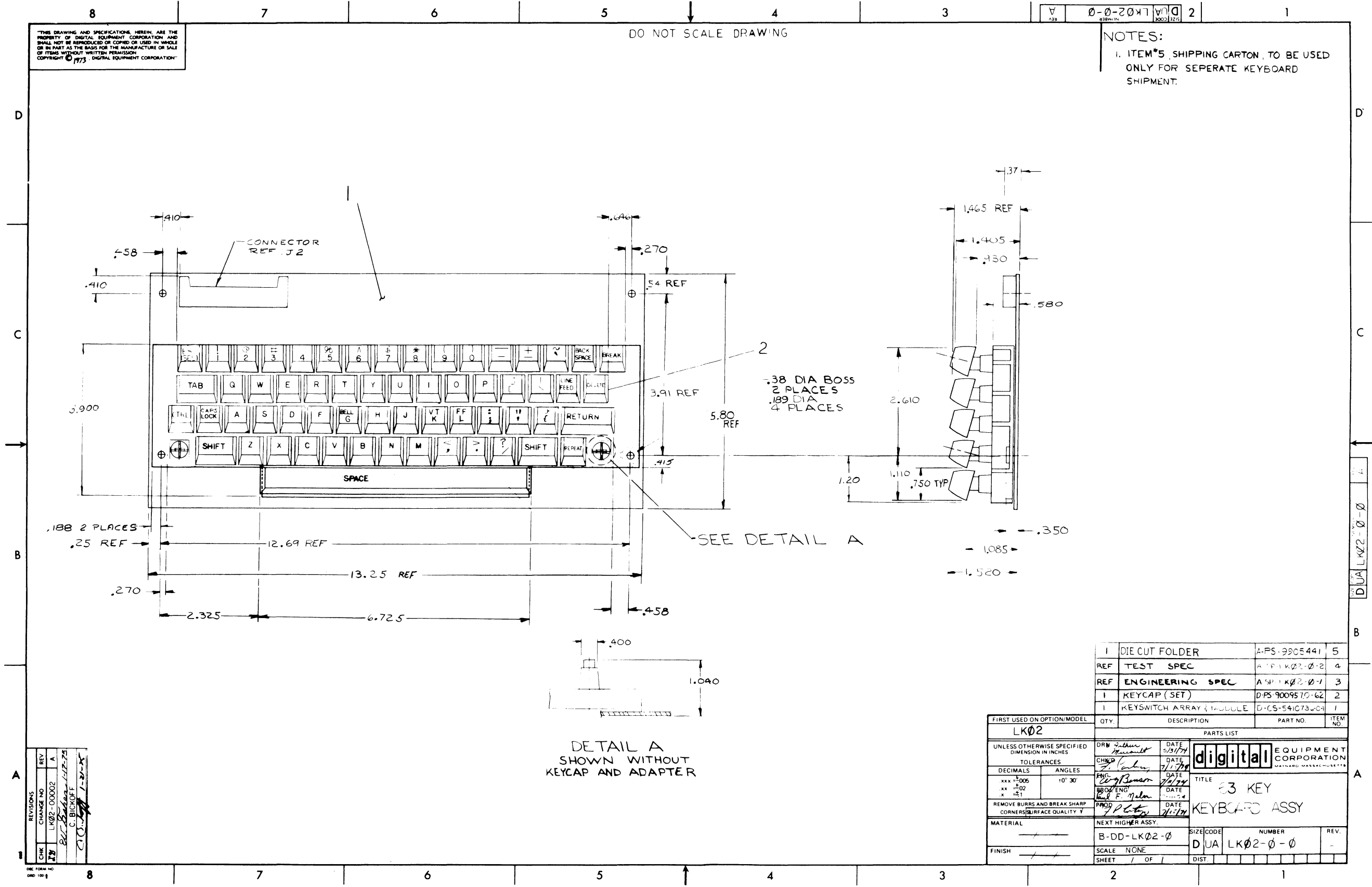
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DO NOT SCALE DRAWING

NOTES:

- ITEM #5, SHIPPING CARTON, TO BE USED ONLY FOR SEPERATE KEYBOARD SHIPMENT.



DETAIL A
SHOWN WITHOUT
KEYCAP AND ADAPTER

1	DIE CUT FOLDER	A-PS-9905441	5
REF	TEST SPEC	A-PS-LK02-0-2	4
REF	ENGINEERING SPEC	A-PS-LK02-0-1	3
1	KEYCAP (SET)	D-PS-9009570-62	2
1	KEYSWITCH ARRAY & MODULE	D-CS-541073-001	1

FIRST USED ON OPTION/MODEL		PARTS LIST																					
LK02		QTY.	DESCRIPTION																				
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES		<table border="1"> <tr> <td>DRW</td> <td><i>William</i></td> <td>DATE</td> <td>5/31/74</td> </tr> <tr> <td>CHKD</td> <td><i>William</i></td> <td>DATE</td> <td>7/1/74</td> </tr> <tr> <td>ENG.</td> <td><i>Benjamin</i></td> <td>DATE</td> <td>7/1/74</td> </tr> <tr> <td>BRD/ENG</td> <td><i>Paul F. Nelson</i></td> <td>DATE</td> <td>7/1/74</td> </tr> <tr> <td>PROD</td> <td><i>Paul F. Nelson</i></td> <td>DATE</td> <td>7/1/74</td> </tr> </table>		DRW	<i>William</i>	DATE	5/31/74	CHKD	<i>William</i>	DATE	7/1/74	ENG.	<i>Benjamin</i>	DATE	7/1/74	BRD/ENG	<i>Paul F. Nelson</i>	DATE	7/1/74	PROD	<i>Paul F. Nelson</i>	DATE	7/1/74
DRW	<i>William</i>	DATE	5/31/74																				
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BRD/ENG	<i>Paul F. Nelson</i>	DATE	7/1/74																				
PROD	<i>Paul F. Nelson</i>	DATE	7/1/74																				
TOLERANCES		<table border="1"> <tr> <td>DECIMALS</td> <td>ANGLES</td> </tr> <tr> <td>xxx = .005</td> <td>+0° 30'</td> </tr> <tr> <td>xx = .02</td> <td></td> </tr> <tr> <td>x = .01</td> <td></td> </tr> </table>		DECIMALS	ANGLES	xxx = .005	+0° 30'	xx = .02		x = .01													
DECIMALS	ANGLES																						
xxx = .005	+0° 30'																						
xx = .02																							
x = .01																							
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY 'Y'		<table border="1"> <tr> <td colspan="2">digital EQUIPMENT CORPORATION</td> </tr> <tr> <td colspan="2">TITLE</td> </tr> <tr> <td colspan="2">63 KEY KEYBOARD ASSY</td> </tr> </table>		digital EQUIPMENT CORPORATION		TITLE		63 KEY KEYBOARD ASSY															
digital EQUIPMENT CORPORATION																							
TITLE																							
63 KEY KEYBOARD ASSY																							
MATERIAL	NEXT HIGHER ASSY.	SIZE CODE	NUMBER																				
	B-DD-LK02-0	DUA	LK02-0-0																				
FINISH	SCALE NONE	SHEET	1 OF 1																				

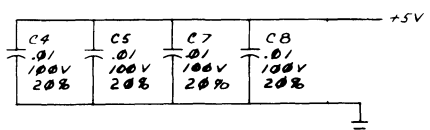
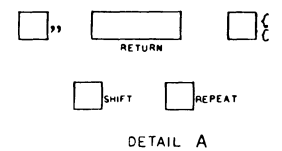
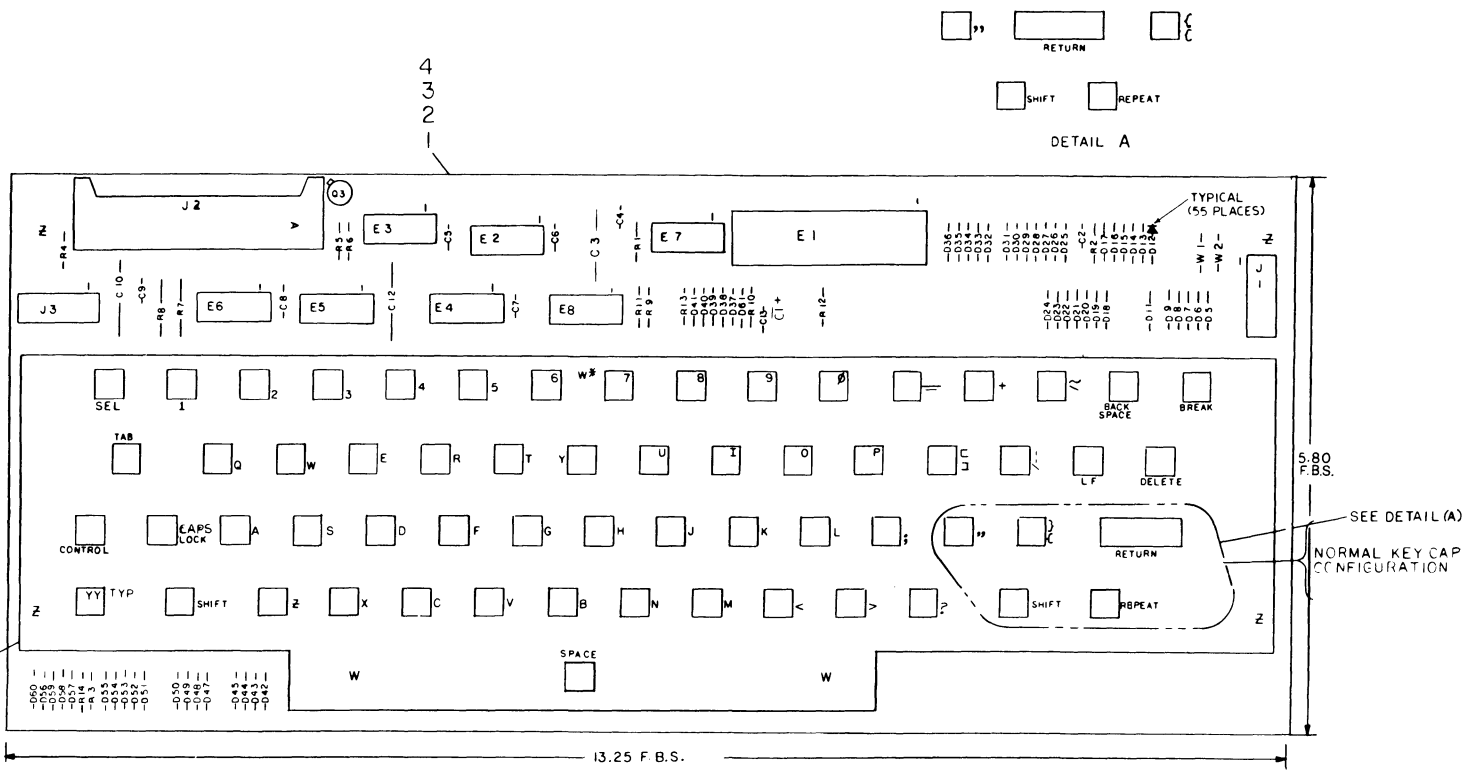
REV	CHANGE NO	DATE
A	LK02-00002	

C. BICKOFF
 1-20-X

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NOTES: TWO VARIATIONS OF THIS BOARD SHALL BE AVAILABLE:
 1. 5410736-0-0 NORMAL = NORMAL KEY CAP CONFIGURATION; W1, IN; W2, OUT
 2. 5410736-YA-0 YA = OPTIONAL KEY CAP CONFIGURATION; W2, IN; W1, OUT

DRAWING 40-107 11944



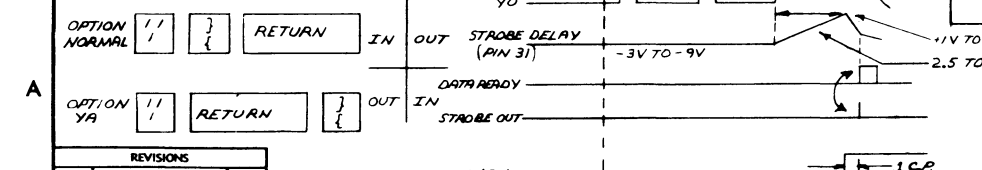
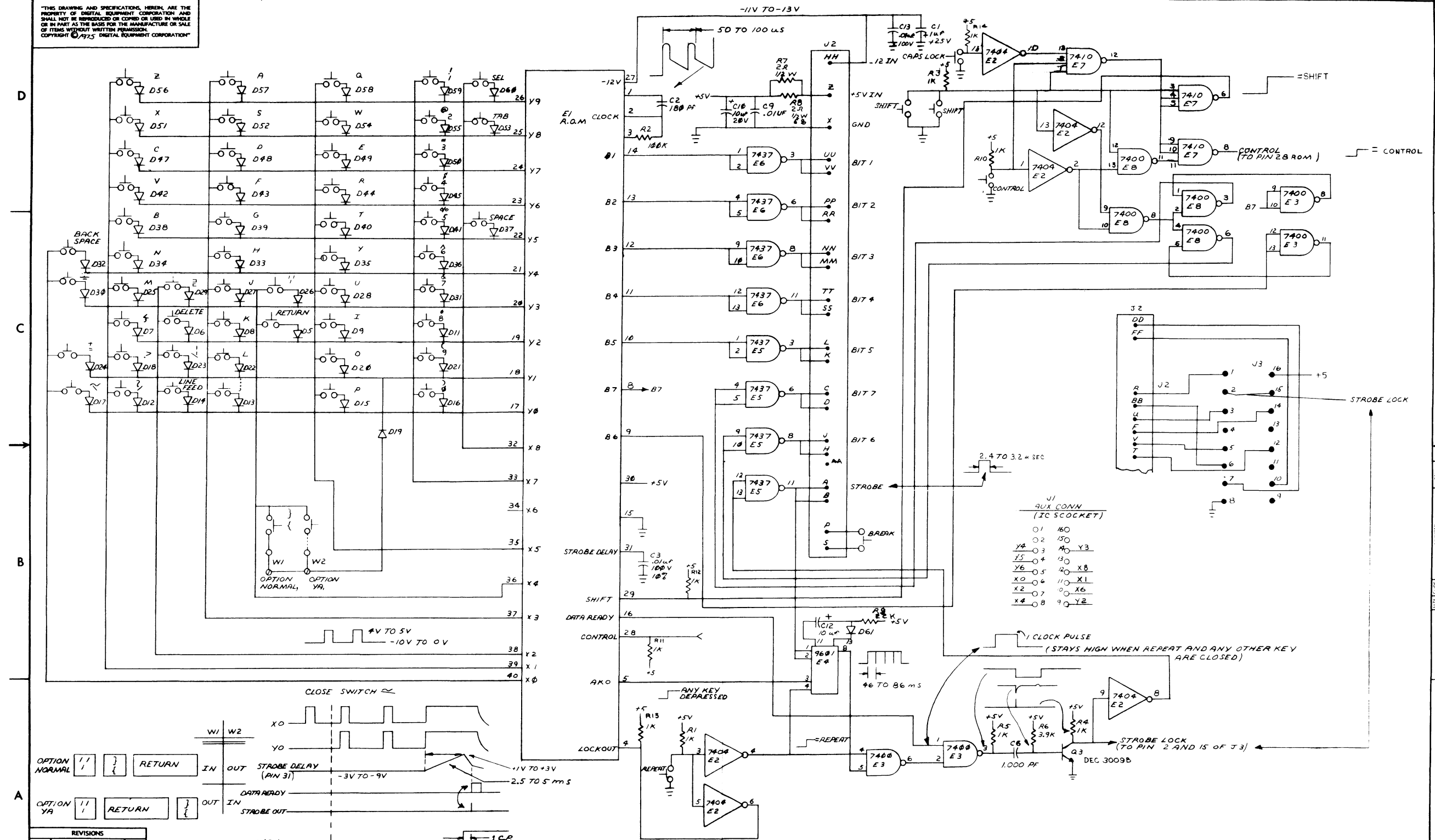
REF	REF	X-Y COORDINATE HOLE LOCATION	K-CD-5410736-0-4	1
REF	REF	ASSY/DRILLING HOLE LAYOUT	D-AH-5410736-0-5	2
REF	REF	MODULE ECO HISTORY	B-MH-5410736-0-6	3
1	1	ETCHED CIRCUIT BOARD	5010735	4
1	1	C3	CAP, .01UF, 100V 10% MYLAR	1005784
6	6	C4, C5, C7, C8, C9, C13	CAP, .01UF, 100V 20% DISC	1001610-01
1	1	C1	CAP, 1UF, 25V TANT	1010866-01
1	1	C2	CAP, 180PF, 100V 5% MICH	1000020-00
2	2	C10, C12	CAP, 10UF, 20V 10% TANT	1004813
55	55	D5-D9, D11-D15, D17-D18	DIODE, D664	1100114-00
1	1	Q3	TRANSISTOR DEC 3009B	1503100-00
2	2	J1, J3	SOCKET (16 PINS)	1211813
1	1	J2	CONNECTOR, RIGHT ANGLE HEADER	1209941-02
1	1	XE1	SOCKET ROM	1212385-00
1	1	E2	I.C. 7404	1909686
2	2	E3, E8	I.C. 7400	1905575
2	2	E5, E6	I.C. 7437	1910091
1	1	E4	I.C. 9601	1909373
1	1	E1	I.C. ROM	2300201
0	1	W1	JUMPER (INSULATED .4)	9009185
1	1		63 KEYSWITCH ARRAY	D-AD-7009892-0-0
9	9	R1, R3, R4, R5, R10-R14	RES 1K 1/4W 5%	1300365-00
1	1	R6	RES 3.9K 1/4W 5%	1300444-00
1	1	R9	RES 22K 1/4W 5%	1301808-00
1	1	R2	RES 100K 1/4W 5%	1302466-00
2	2	R7, R8	RES 2 OHM 1/2W 5%	1309421-00
1	1	E7	I.C. 7410	1905576
1	0	W2	JUMPER (INSULATED .4)	9009185
1	1	C6	CAP 1000PF 100V 5% MICH	1000042-00

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST				
	ETCH BOARD REV	F		

03 Feb 74 J. BITTO 7. Symonova 1-2-74 ER 5410736-00005 F P. E. Nelson 10-1-75 P. NELSON 5-12-75 PAUL E. NELSON 1/14/75 REVISED & REDRAWN 5410736-00003 E 5410736-00002 D 5410736-00002 D CHG CHANGE NO. REV	DRN POIRIER DATE 1-25-74 CHK'D DATE 3-2-75 ENG P. NELSON DATE 2-2-74 PROJ. ENG P. NELSON DATE 2-4-74 PROD. DATE	digital EQUIPMENT CORPORATION MATTAPOISETT, MASSACHUSETTS TITLE LK02 KEYBOARD NEXT HIGHER ASSY D-UA-LK02-0-0 SCALE SHEET 1 OF 2	SIZE CODE DCS 5410736-0-1 NUMBER REV. E
--	---	---	--

SEMICONDUCTOR CONVERSION CHART

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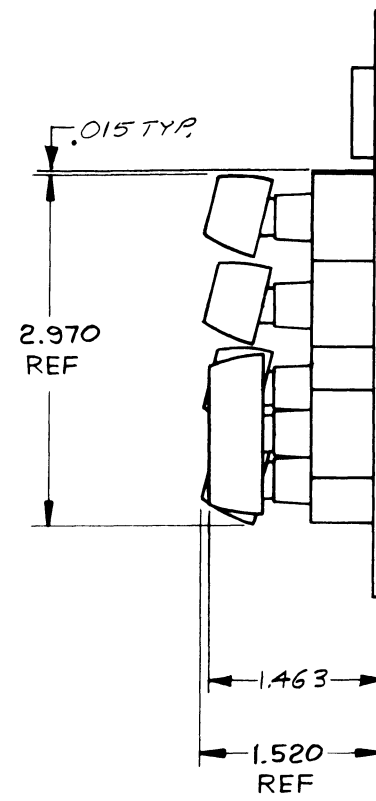
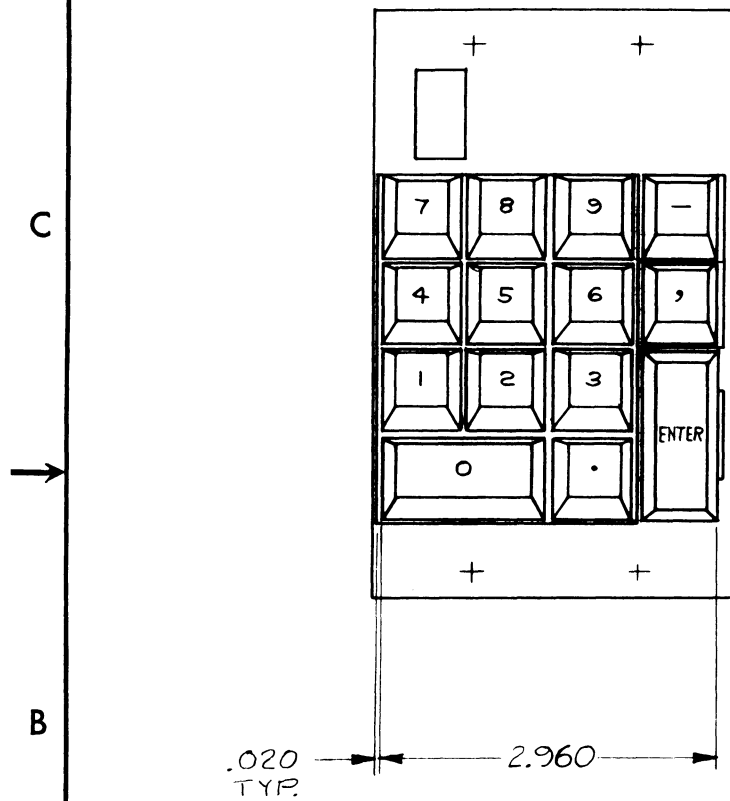


J1 AUX CONN (IC SOCKET)

01	40
02	40
03	40
04	40
05	40
06	40
07	40
08	40
09	40
10	40
11	40
12	40
13	40
14	40
15	40
16	40
17	40
18	40
19	40
20	40
21	40
22	40
23	40
24	40
25	40
26	40
27	40
28	40
29	40
30	40
31	40
32	40
33	40
34	40
35	40
36	40
37	40
38	40
39	40
40	40

REVISIONS			TITLE		SIZE CODE		NUMBER		REV.
CHK	CHANGE NO.	REV.	LK02 KEYBOARD		D CS		5410736-01		F
			SCALE		SHEET	2	OF	2	DIST.

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REV. NO.	REV.
CHANGE NO.	
CHK	

FIRST USED ON OPTION/MODEL		LK03-A	
DIMENSIONAL TOLERANCE		PARTS LIST	
DIMENSIONS ARE MILLIMETERS INCHES UNLESS OTHERWISE SPECIFIED		DRN. <i>B. Silby</i> DATE 4-17-75	
MILLIMETERS INCHES ANGLES		CHK'D <i>W. Benson</i> DATE 7/24/75	
X,XX ± 0.10 X,X ± 0.5 X ± 2	.XXX ± .005 .XX ± .02 .X ± .1	ENG. <i>W. Benson</i> DATE 7/24/75	
THIRD ANGLE PROJECTION	REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓	PROD. ENG. <i>P. E. Nelson</i> DATE 7-28-75	
MATERIAL SEE PARTS LIST		PROD. <i>M. C. G. J.</i> DATE 7-28-75	TITLE 14 KEY KEYBOARD ASSY
FINISH		E-AD-7009750-0-0	SIZE CODE C UA
SCALE 1/1		NUMBER LK03-A-Ø	REV.
SHEET OF 1		DIST.	

REF	TEST SPEC	A-SP-LK02-Ø-2	4
REF	ENGINEERING SPEC	A-SP-LK02-Ø-1	3
1	KEYCAP SET	D-PS-1212287-74	2
1	14 KEYSWITCH ARRAY MOD.	D-CS-5411635-Ø-1	1

REV. NUMBER LK03-A-Ø

APPENDIX A

REFERENCE DATA

A.1 ABBREVIATIONS

The abbreviations used in this manual are listed in Table A-1.

A.2 SIGNAL GLOSSARY

The signal names used in this manual are listed in Table A-2.

A.3 IC PIN LOCATION DRAWINGS

The pin locations of the Integrated Circuits used in the LA36 are illustrated in Figures A-1 through A-29.

Table A-1
Glossary of Abbreviations

2SB	Two Stop Bits
AKO	Any Key On
AMP	Amplifier
AR	Address Register
BCD	Binary Coded Decimal
BEL	Bell
BS	Backspace
BUF	Buffer
BUFF	Buffer
C/B	Carry/Borrow
CB RAM	Character Buffer Read Access Memory
CBA	Character Buffer Address
CG ROM	Character Generator Read Only Memory
CHAR	Character
CLK	Clock
CLR	Clear
CM	Centimeter
CNTR	Counter
COL	Column
COL HI	Column High
COL LO	Column Low
CONTROL RAM	Control Read Access Memory
CRAM	Control Read Access Memory
CTRL	Control
D/A	Digital to Analog
DAC	Digital to Analog
DEC	Decoder
DIR	Direction
DM	Down
DRVR	Driver
ENB	Enable
ER	Error
F/F	Flip Flop
FIFO	First In/First Out
H	High
HDE	Head Drive Enable
INC	Increment
INIT	Initialize
IPS	Inches Per Second

Table A-1 (Cont)
Glossary of Abbreviations

KBD	Keyboard
KBH	Keyboard Hold
kHz	Kilohertz
L	Low
LCV	Last Character Visibility
LF	Line Feed
LSB	Least Significant Bit
M	Meter
MHz	Megahertz
mm	Millimeter
MPC	Microprogrammed Controller
μ s	Microseconds
ms	Milliseconds
MSB	Most Significant Bit
MUX	Multiplexer
NB	Number Of Bits
ns	Nanoseconds
POS HI	Position High
POS LO	Position Low
POS MD	Position Middle
POS	Position
POSIT	Position
PT	PRINT Timer
R	Read or Register
RAM	Read Access Memory
RCV	Receive
RCVR	Receiver
RD ADR	Read Address
RD	Read or Register
RD	Receive Data
REG	Register
ROM	Read Only Memory
ST	Status
SYNC	Synchronize
TACH	Tachometer
TTL	Transistor To Transistor Logic
UART	Universal Asynchronous Receiver Transmitter
VREF	Voltage Reference

Table A-1 (Cont)
Glossary of Abbreviations

WC	Word Count
WD CNT	Word Count
WT ADR	Write Address
XD	Read Access Memory Transmit Data
XMIT	Transmit

**Table A-2
Signal Glossary**

Mnemonic	Definition	Source	Destination
BELL SINK	Bell Return	J5-2	Speaker
BELL SOURCE	+5 V to Bell	R118	J5-1, Speaker
COMMON	From LF Motor	J5-4	LF Motor
PHASE 1	To LF Motor	J5-7	LF Motor
PHASE 2	To LF Motor	J5-6	LF Motor
SOL 1:7	Solenoid Driver Outputs to Head Solenoids		
MPC3 BMB00	Buffered Memory Bit 0	E58-4 or E61-4	E49-9, E21-2 E31-15, E15-15
MPC3 BMB01	Buffered Memory Bit 1	E58-5 or E61-5	E49-5, E21-5 E31-14, E15-14
MPC3 BMB02	Buffered Memory Bit 2	E58-6 or E61-6	E49-3, E21-8 E31-13, E15-13
MPC3 BMB03	Buffered Memory Bit 3	E58-7 or E61-7	E49-1, E21-11 E31-11, E15-11
MPC3 BMB04	Buffered Memory Bit 4	E58-8 or E61-8	E54-13, E46-23 E50-15
MPC3 BMB05	Buffered Memory Bit 5	E58-9 or E61-9	E54-11, E46-22 E50-14
MPC3 BMB06	Buffered Memory Bit 6	E58-10 or E61-10	E54-9, E53-1 E46-21, E50-13
MPC3 BMB07	Buffered Memory Bit 7	E58-11 or E61-11	E54-5, E53-2 E46-20
MPC3 MB00	Memory Bit 00	E58-4 or E61-4	—
MPC3 MB01	Memory Bit 01	E58-5 or E61-5	—
MPC3 MB02	Memory Bit 02	E58-6 or E61-6	—
MPC3 MB03	Memory Bit 03	E58-7 or E61-7	—
MPC3 MB04	Memory Bit 04	E58-8 or E61-8	—
MPC3 MB05	Memory Bit 05	E58-9 or E61-9	—

Table A-2 (Cont)
Signal Glossary

Mnemonic	Definition	Source	Destination
MPC3 MB06	Memory Bit 06	E58-10 or E61-10	—
MPC3 MB07	Memory Bit 07	E58-11 or E61-11	—
MPC4 CLR BEL	Clear Bell	E44-9	E36-3
MPC4 CLR C/B	Clear Carries or Borrows	E44-16	E11-13
MPC4 CLR DA	Clear Data Available	E44-2	E60-11
MPC4 CLR HDE	Clear Head Drive Enable	E44-13	E39-11, E30-11
MPC4 CLR INIT	Clear Initialize	E44-17	E51-1
MPC4 CLR KBH	Clear Keyboard Hold	E44-1	E51-10
MPC4 CLR 568	Clear 568	E44-6	E15-23, E31-4 E30-4
MPC4 CS00	Clocked Selector 04	E46-1	E42-1
MPC4 CS01	Clocked Selector 04	E46-2	E42-2
MPC4 CS02	Clocked Selector 04	E46-3	E42-13
MPC4 CS03	Clocked Selector 04	E46-4	E37-4
MPC4 CS04	Clocked Selector 04	E46-5	E37-5
MPC4 CS10	Clocked Selector 04	E46-9	
MPC4 CS11	Clocked Selector 04	E46-10	E27-3
MPC4 CS12	Clocked Selector 04	E46-11	E44-18, 19
MPC4 CS13	Clocked Selector 04	E46-13	E44-18, 19
MPC4 CS14	Clocked Selector 04	E46-14	E42-5
MPC4 CS15	Clocked Selector 04	E46-15	E37-1, E42-3
MPC4 CS16	Clocked Selector 04	E46-16	E37-2, E37-13 E42-4
MPC4 CS17	Clocked Selector 04	E46-17	E53-4

Table A-2 (Cont)
Signal Glossary

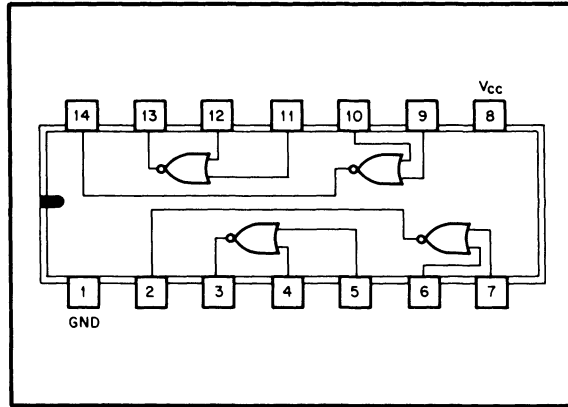
Mnemonic	Definition	Source	Destination
MPC4 LOAD CBA	Load Character Buffer Address	E44-4	E52-9
MPC4 LOAD D/A	Load Digital/Analog	E44-10	E14-9
MPC4 MAX	Maximum	E23-6	E31-5, E14-4, 5, 12, 13
MPC4 REG0:3	Register	E32-2, 3, 6, 7	E52-4, 5, 12, 13 E38-1, 5, 9, 10
MPC4 S000	Selector 0	E50-1	E22-2
MPC4 S001	Selector 1	E50-2	E27-2
MPC4 S002	Selector 2	E50-3	E21-3
MPC4 S003	Selector 3	E50-4	E31-9
MPC4 S004	Selector 4	E50-5	E15-9
MPC4 SET BEL	Set Bell	E44-9	E36-4
MPC4 SET HDE	Set Head Drive Enable	E44-11	E39-10
MPC4 SET HOLD	Set Hold	E44-15	E40-4
MPC4 STEP LF	Step Line Feed	E44-14	E24-3, 11, E29-5
MPC4 SKIP	Skip	E40-11	E60-2
MPC4 WRITE BUF	Write Buffer	E44-5	E60-10, E56-3
MPC4 ZERO	Zero	E23-8	E18-13, E31-3, 6
MPC4 -1 REG	Decrement Register	E44-7	E32-4
MPC4 +1 REG	Increment Register	E44-3	E32-5
MPC5 CLK	Clock	E64-5, 12	E46-18, 19, E29-10, E49-13
MPC5 S.I.	Serial In	E66-6	E55-20
MPC5 1.184 μ s	1.184 μ s	E13-12	E37-10, E13-1, E64-9, E7-13, E9-3, 11
MPC5 1.76 kHz	1.76 kHz	E68-11	E30-3, E59-3

Table A-2 (Cont)
Signal Glossary

Mnemonic	Definition	Source	Destination
MPC5 4.8 kHz	4.8 kHz	E63-11	E26-14, E17-4
MPC5 19	19	E26-9	E67-5, E31-21, 22
MPC5 76 μ s	76 μ s	E26-11	E3-3, E5-3
MPC5 208	208	E26-12	E40-10, E67-11, E17-7, E15-7, E31-19
MPC5 568	568	E30-5, 6	E64-10, E9-4, 10 E13-14, E37-9
MPC5 592 ns	592 ns	E17-13	E20-1
MPC6 BEL	Bell	E19-1	E15-6
MPC6 BS	Back Space	E19-9	E15-20
MPC6 CR	Carriage Return	E19-3	E25-13, E15-4
MPC6 DA	Data Available	E55-19	E31-7
MPC6 HS1:7	Head Select	E28-4 to 11 and E33-4 to 11	Head Solenoid Drivers
MPC6 HT	Horizontal Tab	E19-7	E15-21
MPC6 KBH	Keyboard Hold	E51-8	E31-20
MPC6 LF	Line Feed	E19-6	E25-1, E15-5
MPC6 PNTABL	Printable	E33-11	E25-11, E31-1
MPC6 S.O.	Serial Out	E55-25	E29-12
MPC7 BORROW	Borrow	E12-3	E12-1, E15-22 E31-18
MPC7 CARRY	Carry	E7-6	E31-23
MPC7 COL INC COUNT 0:2	Column Increment Count	E16-2, 3, 6	E28-19 to 21, E33-19 to 21
MPC7 INC	Increment	E30-9	E15-3
MPC7 PT COM +5 V	Print Timer Common	J1-U, V	J1-13, 17 (R1, R2)

Table A-2 (Cont)
Signal Glossary

Mnemonic	Definition	Source	Destination
MPC7 SUM	Sum	E1-6 (J1-B)	
MPC8 BEL	Bell	R58	J1-TT, J1-38
MPC8 HDE (HDEM)	Head Drive Enable	E39-8	J5-2
MPC8 INIT	Initialize	E51-5, 6	E11-2, E31-8
MPC8 LF1	Line Feed 1	E24-9	J1-JJ
MPC8 LF2	Line Feed 2	E24-5	J1-P
MPC8 LF HOLD	Line Feed Hold	E29-6	J1-HH
MPC8 W.U.	Wake Up	Q9-C	E53-5, E10-12, E36-1, J1-DD, E14-1
P.T. COLL 1	Print Timer Collector 1	Q1-C (J1-21)	J1-Y (E34-2)
P.T. COLL 2	Print Timer Collector 2	Q2-C (J1-25)	J1-CC (E35-2)



IC-0013

Figure A-1 380 Quad 2-Input NOR Gate

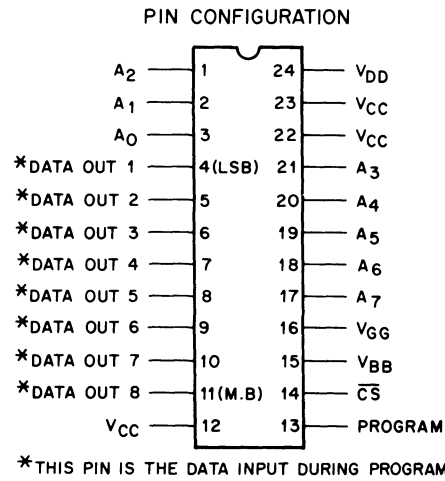
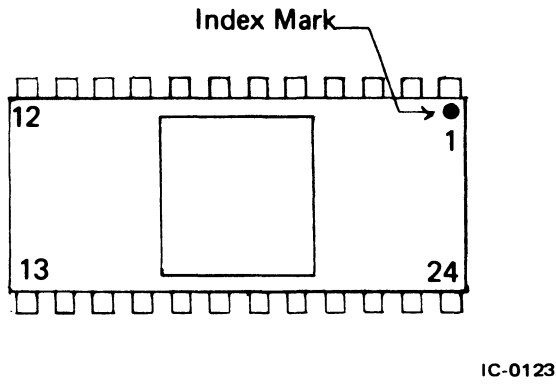


Figure A-2 1702A 8-Bit Reprogrammable ROM

PACKAGE "A" - BENT LEADS



PACKAGE "B" - BRAZED LEADS

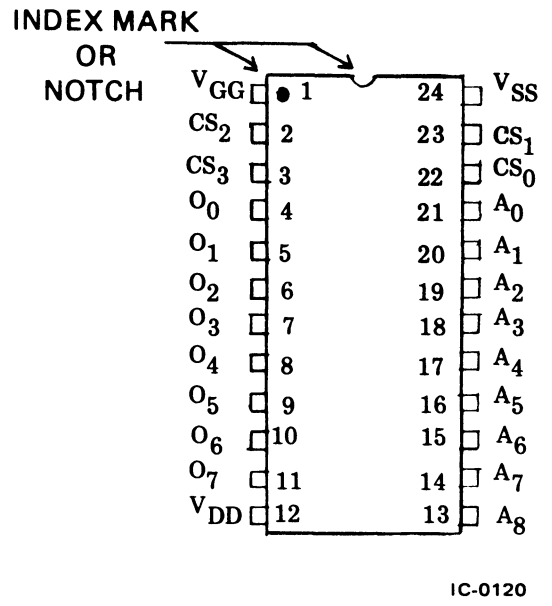
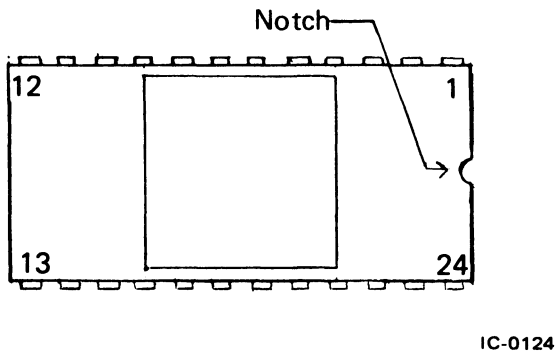
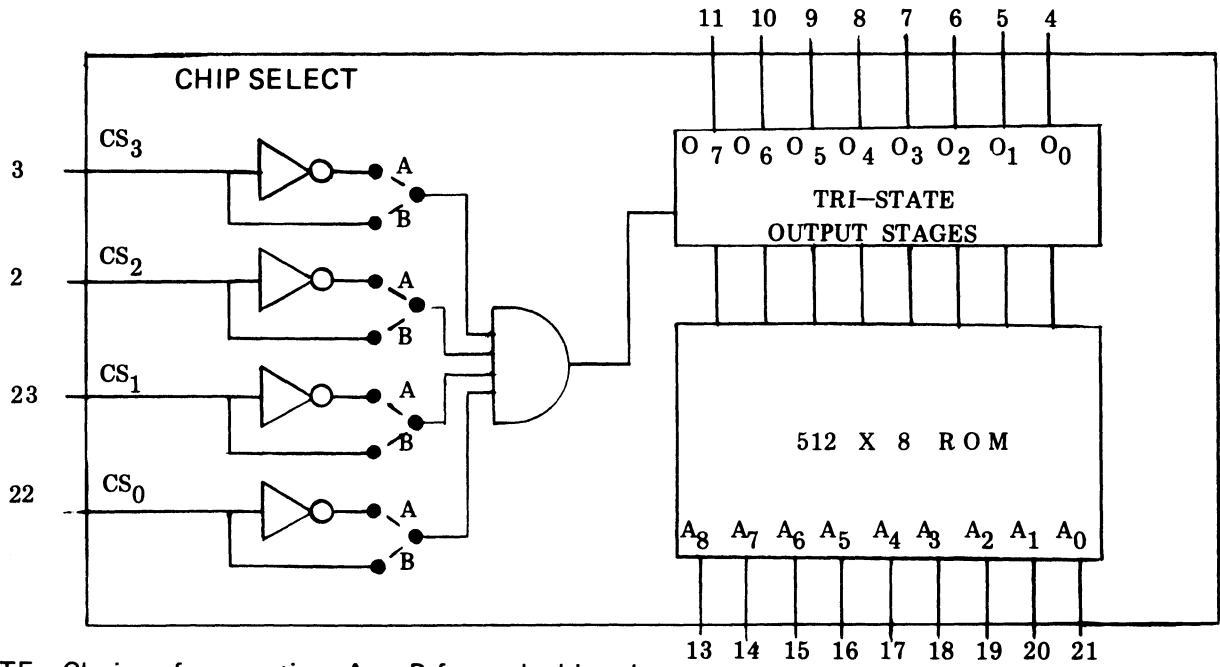


Figure A-3 2627P A6-01 Character Generator Alpha (Sheet 1 of 2)

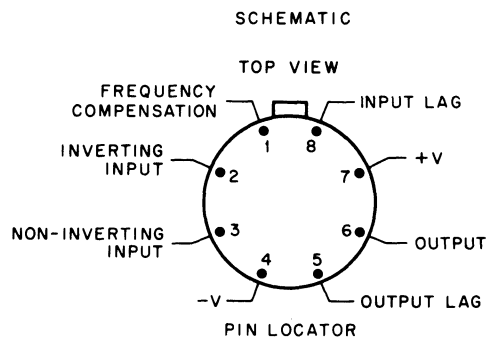
FUNCTIONAL BLOCK DIAGRAM



NOTE: Choice of connection A or B for each chip select is available as a mask option.

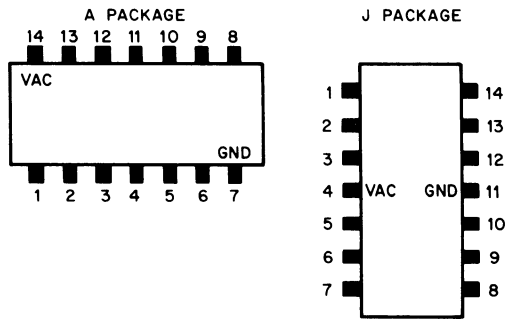
IC-0121

Figure A-3 2627P A6-01 Character Generator Alpha (Sheet 2 of 2)



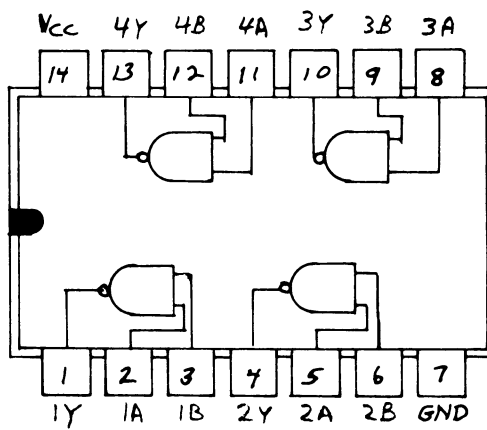
IC-0106

Figure A-4 3101 Random Access Memory



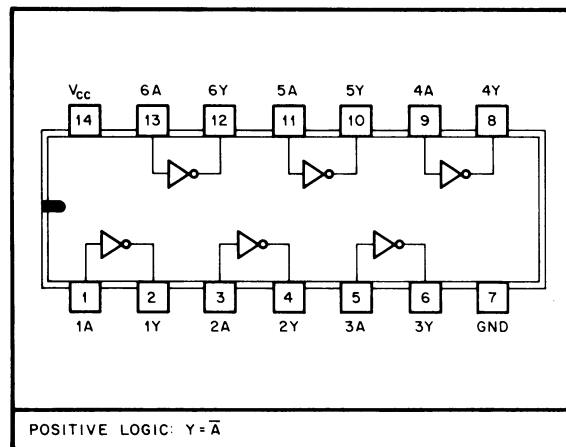
IC-0022

Figure A-5 7400 Quad 2-Input Positive NAND Gate



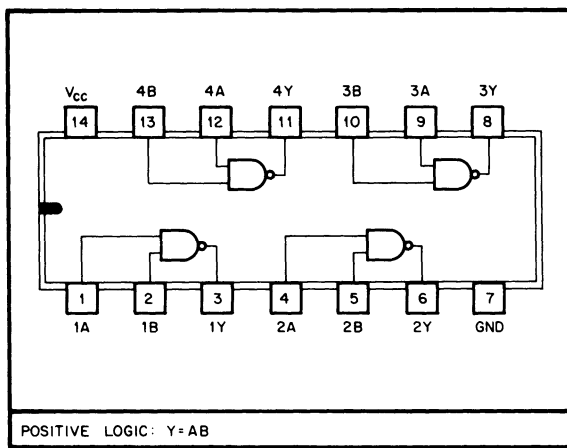
IC-0129

Figure A-6 7401 NAND Gate-Quad 2-Pin Open Collector



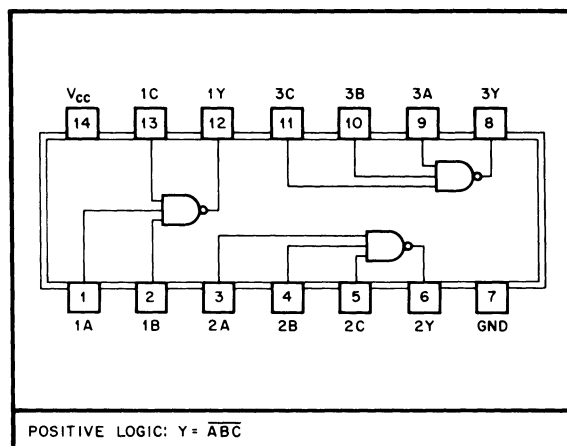
IC-0011

Figure A-7 7404 Hex Inverter



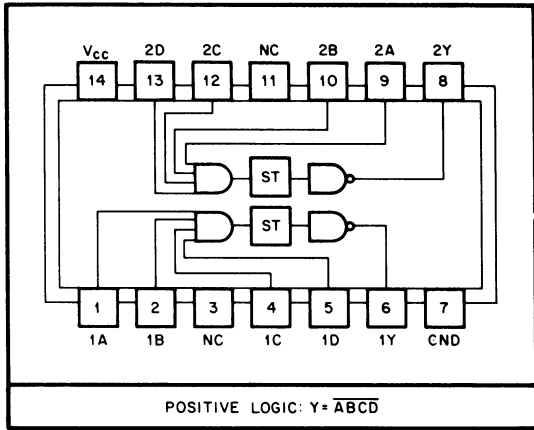
IC-0014

Figure A-8 7408 Quad 2-Input Positive AND Gate

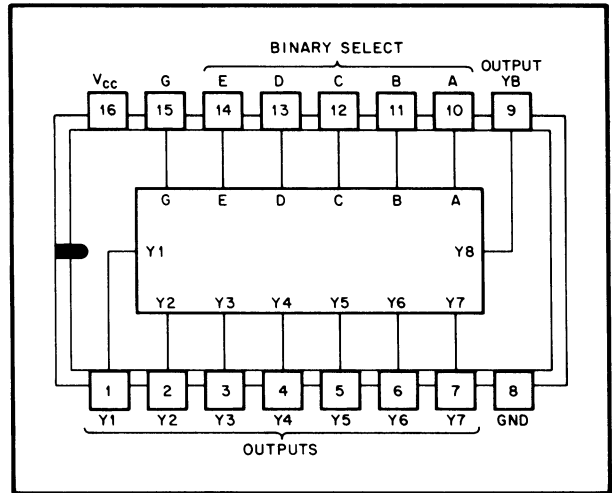


IC-0010

Figure A-9 7410 Triple 3-Input Positive NAND Gate

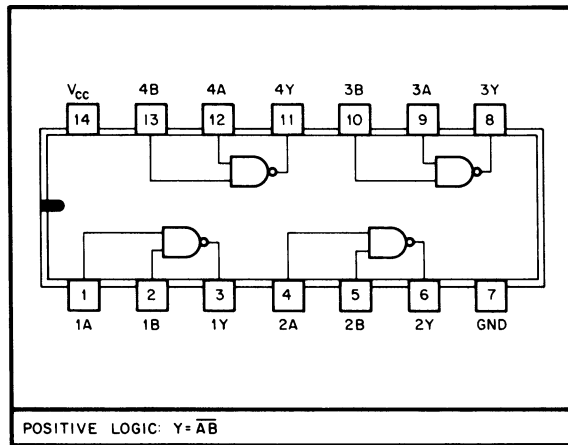


IC-0008



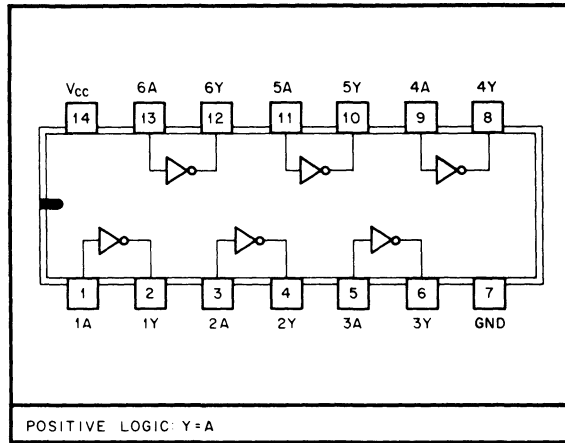
IC-0009

Figure A-10 7413 Schmitt Trigger

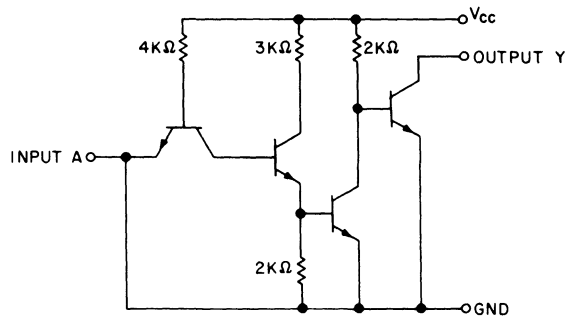


IC-0012

Figure A-11 7416 Hex Inverter Buffer/Driver



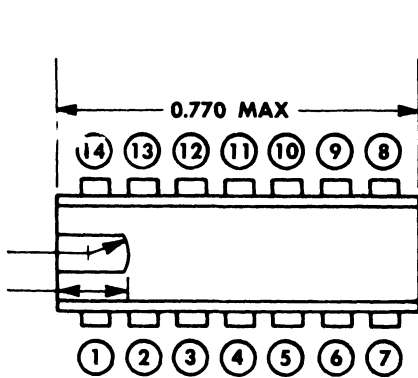
IC-0057



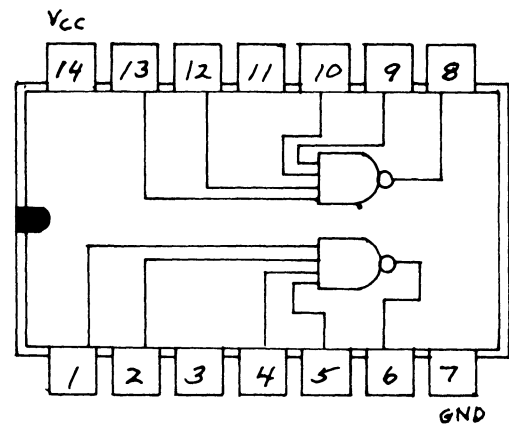
Component values shown are nominal.

IC-0056

Figure A-12 7417 Hex Buffers/Drivers



IC-0128

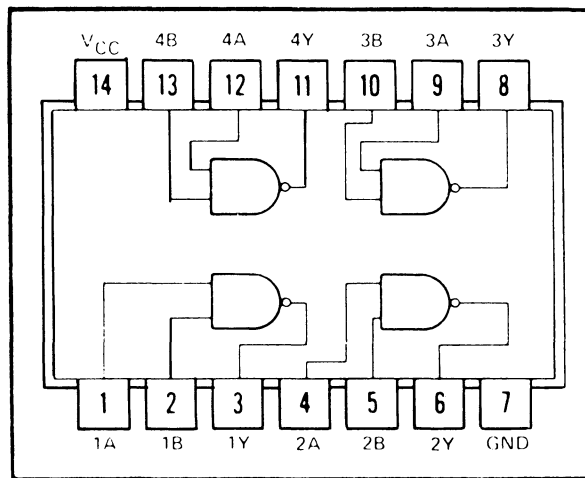


IC-0130

Figure A-13 7420 NAND Gate-Dual 4-Input

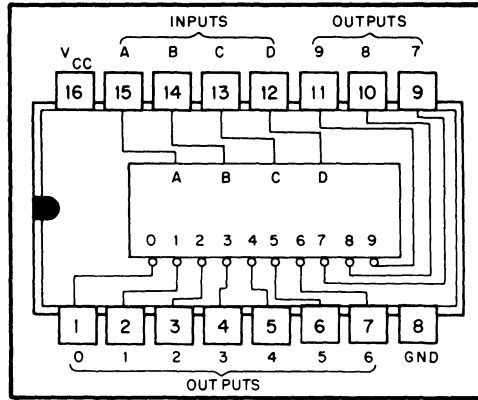
No Package Drawing Available

Figure A-14 7423

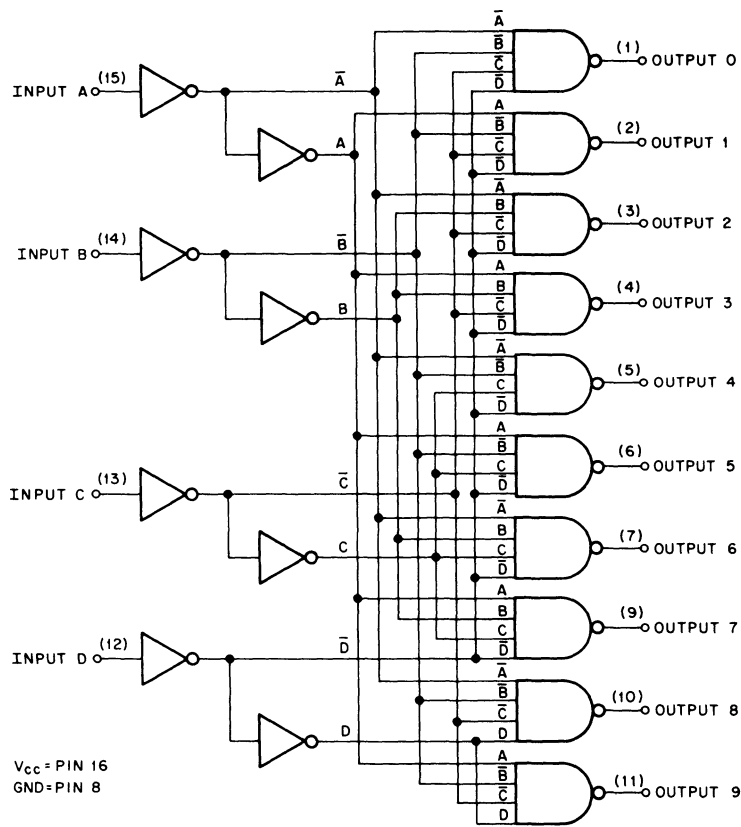


IC-0126

Figure A-15 7437 NAND Gate-Quad 2 In Buffer, 14 Pin

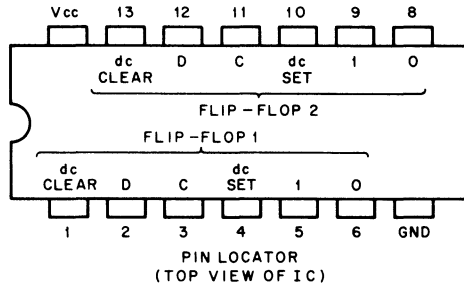


IC-0164



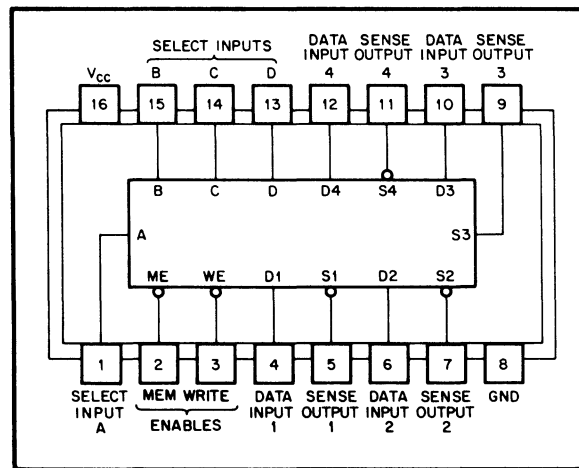
IC-0016

Figure A-16 7442 4-Line-to-10-Line Decoders



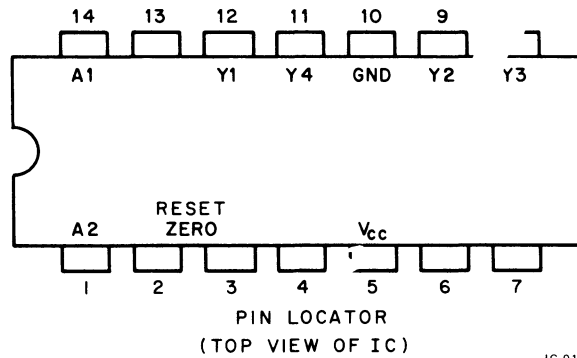
IC-0001

Figure A-17 7474 Dual D-Type Edge-Triggered Flip-Flop



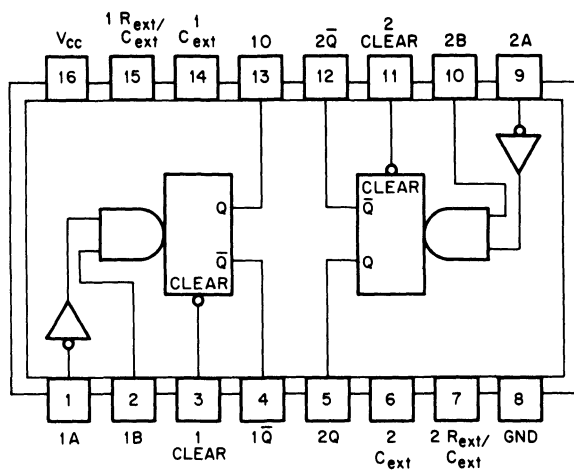
IC-0007

Figure A-18 7489 64-Bit Read/Write Memory



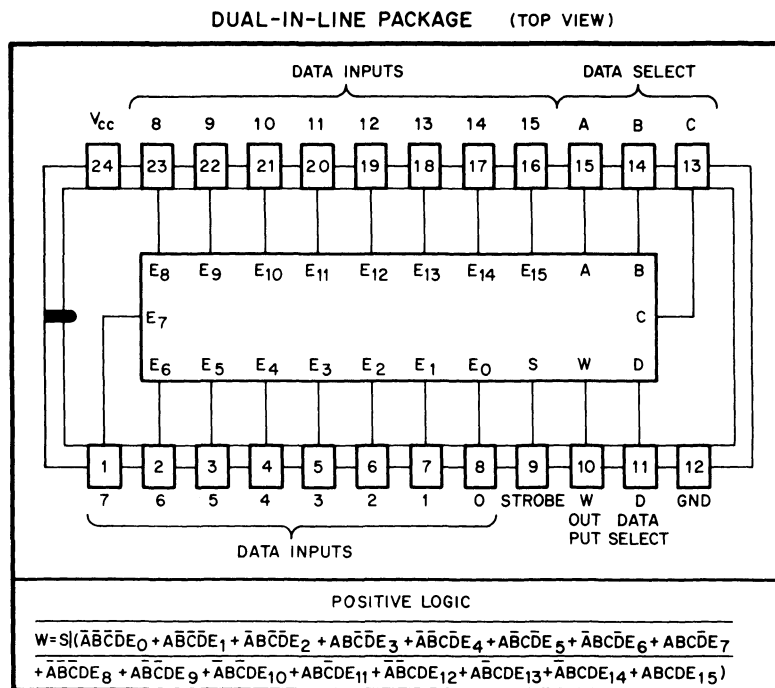
IC-0100

Figure A-19 7493A Counter Asynch Up, Binary



FUNCTIONAL LOGIC / PIN LOCATOR

Figure A-20 74123 Monostable Multivibrator



IC-0117

Figure A-21 74150 Data Selector/Multiplexer

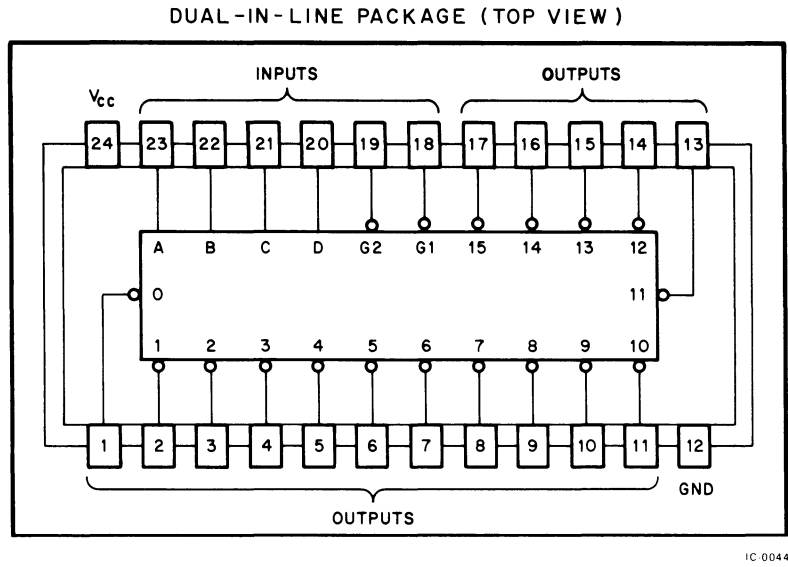


Figure A-22 74154 4-Line-to-26-Line Decoder/Demultiplexer

No Package Drawing Available

Figure A-23 74161 4-Bit Binary Counter

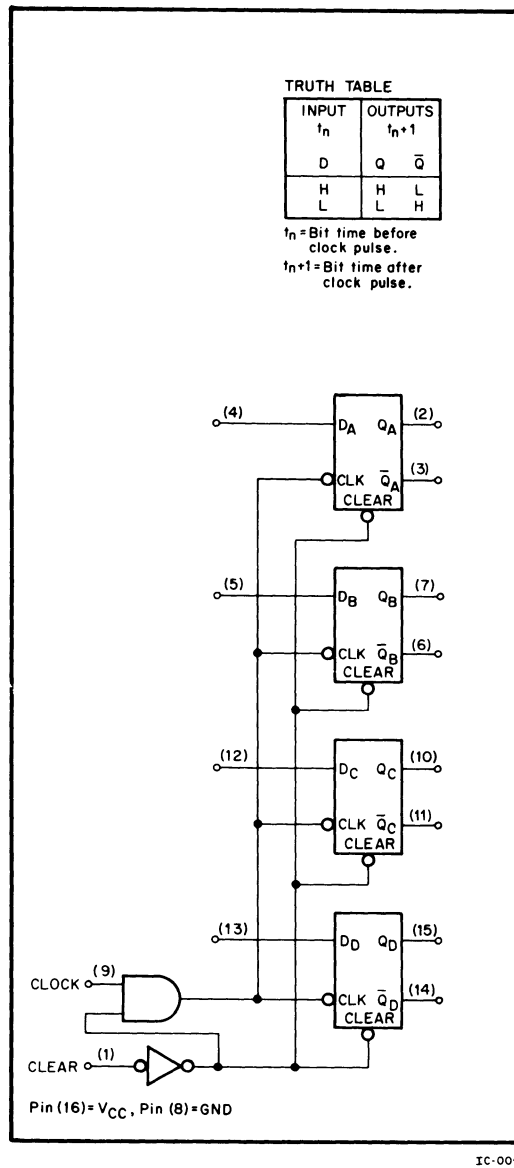
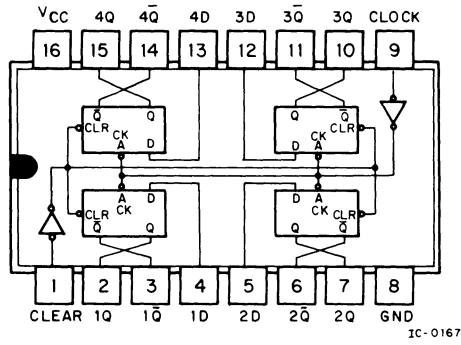
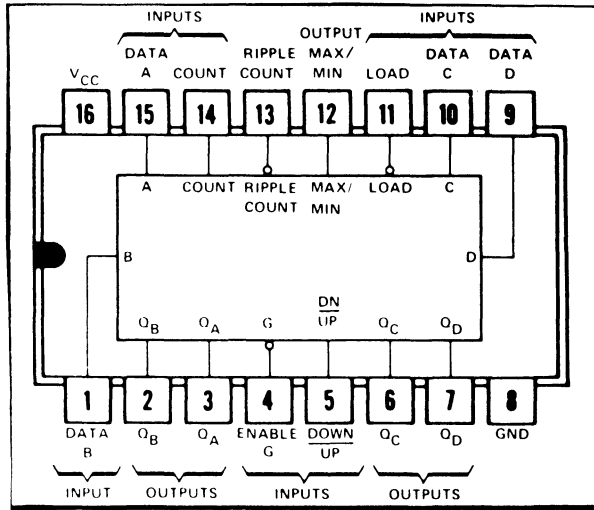
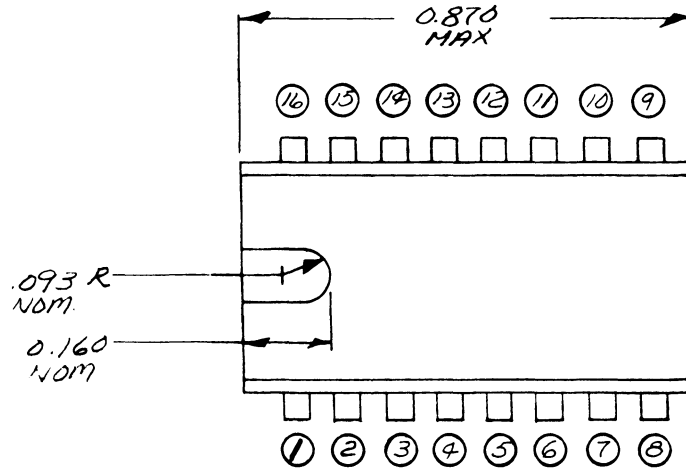


Figure A-24 74175 Quad D-Type Flip-Flop with Clear

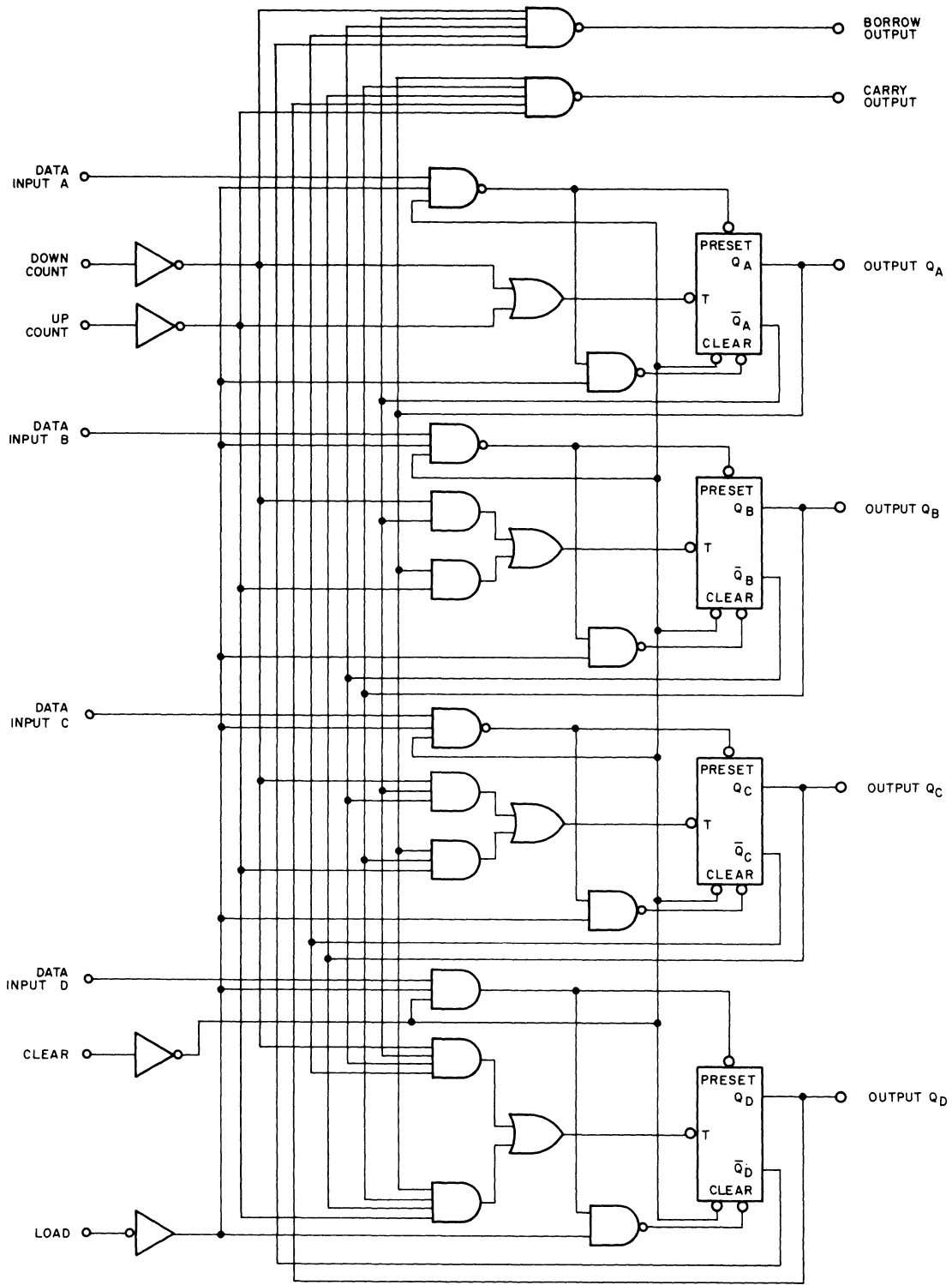


IC-0127



IC-0131

Figure A-25 74190 Counter, Synch Up/Down Decade, 16 Pin



IC-0002

Figure A-26 74193 Synchronous 4-Bit Up/Down Counter (Sheet 1 of 2)

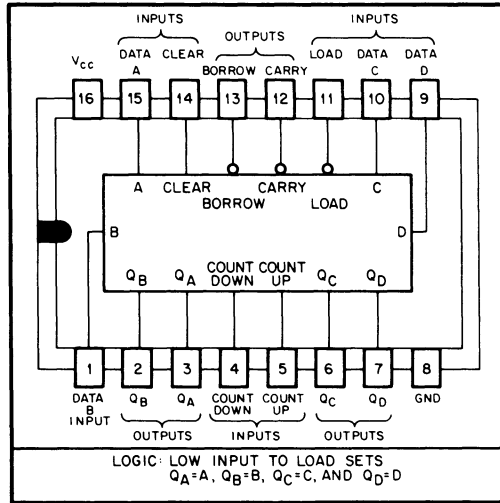


Figure A-26 74193 Synchronous 4-Bit Up/Down Counter (Sheet 2 of 2)

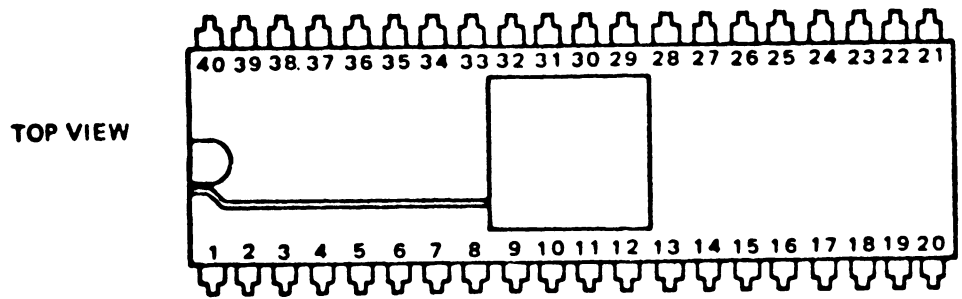


Figure A-27 Universal Asynchronous Receiver Transmitter

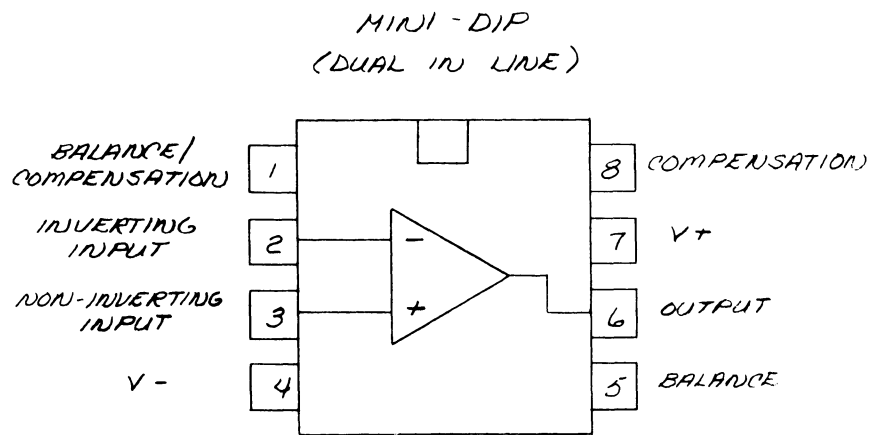
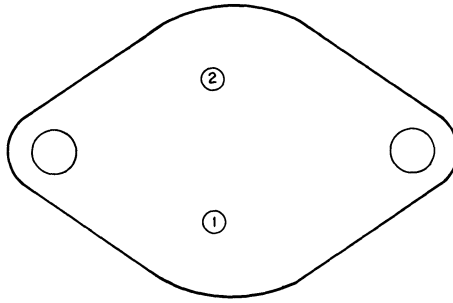


Figure A-28 301 AN DIP Operational Amplifier



TERMINAL CONNECTIONS
PIN 1 = INPUT
PIN 2 = OUTPUT
CASE = GROUND

IC-0168

Figure A-29 309 K Regulator

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What features are most useful? _____

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